UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	: 8,611,404 B2
APPLICATION NO.	: 13/887889
DATED	: December 17, 2013
INVENTOR(S)	: John A. Greszczuk et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS:

At Column 11, Claim 16, line 19, after "receiving," insert -- by a transceiver --

Signed and Sealed this
Tenth Day of March, 2015

Michelle K. Lee

Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: John A. Greszczuk	Application No.: 13/887,889
Patent No.: 8,611,404	Filed: May 6, 2013
Issued: December 17, 2013	Examiner: TRAN, Khai
Confirmation No.: 8684	Art Unit: 2632
Atty. File No.: 6936-28-CON-7	

For: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR APPLICANT'S MISTAKE (37 C.F.R §1.323)

Attn: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a request for a Certificate of Correction under 37 C.F.R. 1.323 for the above-identified patent. Attached is form PTO/SB/44. Applicants have determined that there was an error in claim 16 which was the mistake of the Applicant. The correction does not introduce new matter, do not require re-examination, and do not materially affect the scope or meaning of the patent.

- At Column 11, Claim 16, line 19, after "receiving," insert -- by a transceiver --

Payment in the amount of $100.00, as required by 37 C.F.R. § 1.20(a) is being submitted herewith. Although no additional fees are believed due in connection with the filing of this paper, please charge any additional fees deemed necessary or credit any overpayment to Deposit Account No. 19-1970.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 7 Dec 04

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

PTO/SB/44 (09-07)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,611,404

APPLICATION NO.: 13/887,889

ISSUE DATE : December 17, 2013

INVENTOR(S) : John A. Greszczuk et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At Column 11, Claim 16, line 19, after "receiving," insert -- by a transceiver --

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Jason H. Vick c/o Sheridan Ross, PC
1560 Broadyway, Suite 1200
Denver, CO 80202

Electronic Patent Application Fee Transmittal

Application Number:	13887889
Filing Date:	06-May-2013
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Filer:	Jason Vick/Joanne Vos
Attorney Docket Number:	6936-28-CON-7

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of Correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**100**

Electronic Acknowledgement Receipt

EFS ID:	20872121
Application Number:	13887889
International Application Number:	
Confirmation Number:	8684
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-28-CON-7
Receipt Date:	04-DEC-2014
Filing Date:	06-MAY-2013
Time Stamp:	18:46:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$100
RAM confirmation Number	5288
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)	
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)	
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	Request_for_COC.pdf	284773 c64e04c1d1a6e60d90a7cd7ae2fd0fabd2cb09cc	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30308 fdf357c93ccf33ff69003899d58bcbc9f7b0b4c5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	315081		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	7/18/2014	District of Delaware

PLAINTIFF	DEFENDANT
TQ Delta, LLC	ADTRAN, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	See Attached		
2	32 Pats		
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 8,090,008 B2	1/3/2012	TQ Delta, LLC
2	US 8,073,041 B1	12/6/2011	TQ Delta, LLC
3	US 7,292,627 B2	11/6/2007	TQ Delta, LLC
4	US 7,471,721 B2	12/30/2008	TQ Delta, LLC
5	US 8,218,610 B2	7/10/2012	TQ Delta, LLC
6	US 8,355,427 B2	1/15/2013	TQ Delta, LLC
7	US 7,453,881 B2	11/18/2008	TQ Delta, LLC
8	US 7,809,028 B2	10/5/2010	TQ Delta, LLC
9	US 7,978,706 B2	7/12/2011	TQ Delta, LLC
10	US 8,422,511 B2	4/16/2013	TQ Delta, LLC
11	US 7,889,784 B2	2/15/2011	TQ Delta, LLC
12	US 7,835,430 B2	11/16/2010	TQ Delta, LLC
13	US 7,570,686 B2	8/4/2009	TQ Delta, LLC
14	US 8,238,412 B2	8/7/2012	TQ Delta, LLC
15	US 8,432,956 B2	4/30/2013	TQ Delta, LLC
16	US 7,451,379 B2	11/11/2008	TQ Delta, LLC
17	US 8,516,337 B2	8/20/2013	TQ Delta, LLC
18	US 7,979,778 B2	7/12/2011	TQ Delta, LLC
19	US 7,925,958 B2	4/12/2011	TQ Delta, LLC
20	US 8,462,835 B2	6/11/2013	TQ Delta, LLC
21	US 8,594,162 B2	11/26/2013	TQ Delta, LLC
22	US 7,978,753 B2	7/12/2011	TQ Delta, LLC
23	US 6,445,730 B1	9/3/2002	TQ Delta, LLC
24	US 8,611,404 B2	12/17/2013	TQ Delta, LLC
25	US 8,437,382 B2	5/7/2013	TQ Delta, LLC
26	US 7,836,381 B1	11/16/2010	TQ Delta, LLC
27	US 7,844,882 B2	11/30/2010	TQ Delta, LLC
28	US 8,276,048 B2	9/25/2012	TQ Delta, LLC
29	US 8,495,473 B2	7/23/2013	TQ Delta, LLC
30	US 8,607,126 B1	12/10/2013	TQ Delta, LLC
31	US 7,831,890 B2	11/9/2010	TQ Delta, LLC
32	US 8,625,660 B2	1/7/2014	TQ Delta, LLC

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/887,889	12/17/2013	8611404	6936-28-CON-7	8684

62574 7590 11/26/2013

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

John A. Greszczuk, Stow, MA;
Richard W. Gross, Acton, MA;
Halil Padir, N. Andover, MA;
Michael A. Tzannes, Lexington, MA;
TQ DELTA, LLC, Austin, TX

OK to entered.
10/29/2013
KT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: John A. Greszczuk	Group Art Unit: 2632
Application No.: 13/887,889	Examiner: TRAN, Khai
Filed: May 6, 2013	Confirmation No.: 8684
Atty. File No.: 6936-28-CON-7	

For: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

Applicants submit this Amendment After Allowance pursuant to 37 C.F.R. 1.312 in response to the Notice of Allowance having a mailing date of October 23, 2013. While Applicants believe that no fees are due with the filing of this response, the undersigned hereby authorizes the charge of any fees deemed necessary to Deposit Account No. 19-1970.

An amendment may be entered after the mailing of a Notice of Allowance but prior to payment of the issue fee upon recommendation of the primary Examiner. Therefore, it is respectfully requested that the above-referenced application be amended as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 6 of this paper.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/887,889	05/06/2013	John A. Greszczuk	6936-28-CON-7	8684

62574 7590 11/15/2013

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
TRAN, KHAI	
ART UNIT	PAPER NUMBER
2632	

NOTIFICATION DATE	DELIVERY MODE
11/15/2013	ELECTRONICELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jvick@sheridanross.com

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address : COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
13/887,889	06 May, 2013	GRESZCZUK ET AL.	6936-28-CON-7

		EXAMINER	
Jason H. Vick Sheridan Ross, PC Suite # 1200 1560 Broadway Denver, CO 80202		KHAI TRAN	
		ART UNIT	PAPER
		2632	20131107

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The amendment filed 10/29/2013 has been approved and entered.

/KHAI TRAN/
Primary Examiner, Art Unit 2632

PTO-90C (Rev.04-03)

Response to Rule 312 Communication	Application No.	Applicant(s)
	13/887,889	GRESZCZUK ET AL.
	Examiner	Art Unit
	KHAI TRAN	2632

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *29 October 2013* under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☒ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/KHAI TRAN/
Primary Examiner, Art Unit 2632

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

62574 7590 10/23/2013
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/887,889	05/06/2013	John A. Greszczuk	6936-28-CON-7	8684

TITLE OF INVENTION: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	01/23/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, KHAI	2632	375-219000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Jason H. Vick
2 Sheridan Ross, PC
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: TQ DELTA, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): AUSTIN, TEXAS

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☑ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-1970 (enclose an extra copy of this form).

PTOL-85 (Rev. 02/11)

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 29 Oct 13

Typed or printed name Jason H. Vick Registration No. 45,285

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: John A. Greszczuk	)	Group Art Unit: 2632
Application No.: 13/887,889	)	Examiner: TRAN, Khai
Filed: May 6, 2013	)	Confirmation No.: 8684
Atty. File No.: 6936-28-CON-7	)	

For: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Madam:

Applicant submits this Comments on Statement of Reasons for Allowance to address further the Notice of Allowability ("Notice") having a mailing date of October 23, 2013.

In the Notice, the Examiner's stated reasons for allowance were that:

> Claims 18-37 are allowed.
>
> The following is an examiner's statement of reasons for allowance: none of the prior art discloses or suggests that An apparatus and a method, comprising a transceiver operable to: comprises a plurality of data frames followed by a synchronization frame; transmit, in the full power mode, a synchronization signal; receive a message to enter into a low power mode; enter into the low power mode by reducing a power consumption of at least one portion of a transmitter; store, in the low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter; transmit, in the low power mode, a synchronization signal; and exit from the low power and re-enter into .restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

Based on the Notice, the patentability of all other independent and dependent claims is assumed to be based upon the elements as set forth in such claims and that such claims meet all criteria for patentability under §101, §102, §103 and §112.

As is clear from MPEP 1302.14,

> "The statement [of reasons for allowance] is not intended to necessarily state all the reasons for allowance or all the details why claims are allowed and should not be written to specifically or impliedly state that all the reasons for allowance are set forth."

While the stated Reasons for Allowance may be a stated reason for allowing some independent claims, Applicant submits that some independent claims have a different reason for allowance and that some independent claims have other reasons for allowance.

Specifically, the prior art fails to teach the specific combination of features as recited in the independent claims 18, 23, 28, and 33.

Although the Applicant believes that no fees are due for filing this Comments on Statement of Reasons for Allowance, please charge any fees deemed necessary to Deposit Account No. 19-1970.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 2 9 0 4 1 3

By: _____

Jason H. Vick,
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: John A. Greszczuk	)	Group Art Unit: 2632
Application No.: 13/887,889	)	Examiner: TRAN, Khai
Filed: May 6, 2013	)	Confirmation No.: 8684
Atty. File No.: 6936-28-CON-7	)	

For: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

Applicants submit this Amendment After Allowance pursuant to 37 C.F.R. 1.312 in response to the Notice of Allowance having a mailing date of October 23, 2013. While Applicants believe that no fees are due with the filing of this response, the undersigned hereby authorizes the charge of any fees deemed necessary to Deposit Account No. 19-1970.

An amendment may be entered after the mailing of a Notice of Allowance but prior to payment of the issue fee upon recommendation of the primary Examiner. Therefore, it is respectfully requested that the above-referenced application be amended as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-17. (Cancelled)

18. (Previously Presented) An apparatus comprising a transceiver operable to:

transmit, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by a synchronization frame;

transmit, in the full power mode, a synchronization signal;

receive a message to enter into a low power mode;

enter into the low power mode by reducing a power consumption of at least one portion of a transmitter;

store, in the low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

transmit, in the low power mode, a synchronization signal; and

exit from the low power and restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

19. (Previously Presented) The apparatus of claim 18, further operable to transmit at least one test signal prior to restoring the full power mode.

20. (Previously Presented) The apparatus of claim 18, further operable to continue to maintain a synchronized frame count with a second transceiver during the low power mode.

21. (Previously Presented) The apparatus of claim 18, wherein the apparatus is a CO device that is capable of transmitting internet and video data.

22. (Previously Presented) The apparatus of claim 18, wherein the apparatus is a customer premises equipment that is capable of transmitting internet and video data.

23. (Previously Presented) An apparatus comprising a transceiver operable to:

receive, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by a synchronization frame;

receive, in the full power mode, a synchronization signal;

transmit a message to enter into a low power mode;

store, in a low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

receive, in the low power mode, a synchronization signal; and

exit from the low power and restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

24. (Previously Presented) The apparatus of claim 23, further operable to receive at least one test signal prior to restoring the full power mode.

25. (Previously Presented) The apparatus of claim 23, further operable to continue to maintain a synchronized frame count with a second transceiver during the low power mode.

26. (Previously Presented) The apparatus of claim 23, wherein the apparatus is a CO device that is capable of transmitting internet and video data.

27. (Previously Presented) The apparatus of claim 23, wherein the apparatus is a customer premises equipment that is capable of transmitting internet and video data.

28. (Currently Amended) A method of multicarrier communications comprising:

transmitting, by a transceiver, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by a synchronization frame;

transmitting, in the full power mode, a synchronization signal;

receiving a message to enter into a low power mode;

entering into the low power mode by reducing a power consumption of at least one portion of a transmitter;

storing, in the low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

transmitting, in the low power mode, a synchronization signal; and

exiting from the low power and restoring~~restore~~ the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

29. (Previously Presented) The method of claim 28, further comprising transmitting at least one test signal prior to restoring the full power mode.

30. (Previously Presented) The method of claim 28, further comprising continuing to maintain a synchronized frame count with a second transceiver during the low power mode.

31. (Previously Presented) The method of claim 28, wherein the method is performed by a CO device that is transmitting internet and video data.

32. (Previously Presented) The method of claim 28, wherein the method is performed by a customer premises equipment that is transmitting internet and video data.

33. (Currently Amended) A method of multicarrier communications comprising:

receiving, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by a synchronization frame;

receiving, in the full power mode, a synchronization signal;

transmitting a message to enter into a low power mode;

storing, in a low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

receiving, in the low power mode, a synchronization signal; and

exiting from the low power and restoring~~restore~~ the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

34. (Previously Presented) The method of claim 33, further comprising receiving at least one test signal prior to restoring the full power mode.

35. (Previously Presented) The method of claim 33, further comprising continuing to maintain a synchronized frame count with a second transceiver during the low power mode.

36. (Previously Presented) The method of claim 33, wherein the method is performed by a CO device that is receiving internet and video data.

37. (Previously Presented) The method of claim 33, wherein the method is performed by a customer premises equipment that is receiving internet and video data.

REMARKS

By this amendment, claims 28 and 33 have been amended to correct a minor grammatical error. No new matter is believed to be introduced by this amendment.

The Commissioner is hereby authorized to charge to deposit account number 19-1970 any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 2 1 0 8 12

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

Electronic Patent Application Fee Transmittal

Application Number:	13887889
Filing Date:	06-May-2013
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Filer:	Jason Vick/Joanne Vos
Attorney Docket Number:	6936-28-CON-7

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2080**

Electronic Acknowledgement Receipt

EFS ID:	17256335
Application Number:	13887889
International Application Number:	
Confirmation Number:	8684
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-28-CON-7
Receipt Date:	29-OCT-2013
Filing Date:	06-MAY-2013
Time Stamp:	15:23:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2080
RAM confirmation Number	2170
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_Fee_Payment.pdf	190567 dabf9c665081a6580ec022f625b8480ef871852b	no	2
Warnings:					
Information:					
2	Post Allowance Communication - Incoming	Comments_on_Reason_for_Allowance.pdf	166194 51d233ade63ec78766f653dad7253f56fcc96f25	no	2
Warnings:					
Information:					
3		AMEND_312.pdf	442049 9493905bd90b79823d6c6a13f111a50a73500059	yes	6

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment after Notice of Allowance (Rule 312)	1	1
Claims	2	5
Applicant Arguments/Remarks Made in an Amendment	6	6

Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32415 a8816f8d1bb97909184d08a1f794aef500be1279	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	831225	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

62574 7590 10/23/2013

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER
TRAN, KHAI

ART UNIT	PAPER NUMBER
2632	

DATE MAILED: 10/23/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/887,889	05/06/2013	John A. Greszczuk	6936-28-CON-7	8684

TITLE OF INVENTION: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	01/23/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

62574 7590 10/23/2013
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/887,889	05/06/2013	John A. Greszczuk	6936-28-CON-7	8684

TITLE OF INVENTION: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	01/23/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, KHAI	2632	375-219000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

PTOL-85 (Rev. 02/11)

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/887,889	05/06/2013	John A. Greszczuk	6936-28-CON-7	8684

62574 7590 10/23/2013

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
TRAN, KHAI	

ART UNIT	PAPER NUMBER
2632	

DATE MAILED: 10/23/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notices of Allowance and Fee(s) Due mailed between October 1, 2013 and December 31, 2013

(Addendum to PTOL-85)

If the "Notice of Allowance and Fee(s) Due" has a mailing date on or after October 1, 2013 and before January 1, 2014, the following information is applicable to this application.

If the issue fee is being timely paid on or after January 1, 2014, the amount due is the issue fee and publication fee in effect January 1, 2014. On January 1, 2014, the issue fees set forth in 37 CFR 1.18 decrease significantly and the publication fee set forth in 37 CFR 1.18(d)(1) decreases to $0.

If an issue fee or publication fee has been previously paid in this application, applicant is not entitled to a refund of the difference between the amount paid and the amount in effect on January 1, 2014.

Notice of Allowability	Application No. 13/887,889	Applicant(s) GRESZCZUK ET AL.	
	Examiner KHAI TRAN	Art Unit 2632	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 09/12/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *18-37*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

REASONS FOR ALLOWANCE

1. The amendment filed 09/12/2013 has been entered. Claims 1-17 have been cancelled. Claims 18-37 are pending in this Office action.

Allowable Subject Matter

2. Claims 18-37 are allowed.

3. The following is an examiner's statement of reasons for allowance: none of the prior art discloses or suggests that An apparatus and a method, comprising a transceiver operable to: comprises a plurality of data frames followed by a synchronization frame; transmit, in the full power mode, a synchronization signal; receive a message to enter into a low power mode; enter into the low power mode by reducing a power consumption of at least one portion of a transmitter; store, in the low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter; transmit, in the low power mode, a synchronization signal; and exit from the low power and re-enter into .restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAI TRAN whose telephone number is (571)272-3019. The examiner can normally be reached on 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KHAI TRAN/
Primary Examiner, Art Unit 2632

KT
October 17, 2013

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13887889	GRESZCZUK ET AL.
	Examiner	**Art Unit**
	KHAI TRAN	2632

CPC		
Symbol	**Type**	**Version**

CPC Combination Sets				
Symbol	**Type**	**Set**	**Ranking**	**Version**

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/KHAI TRAN/ Primary Examiner.Art Unit 2632 (Primary Examiner)	10/17/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office — Part of Paper No. 20131017

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13887889	GRESZCZUK ET AL.
	Examiner	**Art Unit**
	KHAI TRAN	2632

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
375	219	H 0 4 L 5 / 16 (2006.01.01)	
CROSS REFERENCE(S)		H 0 4 L 27 / 28 (2006.01.01)	
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)		
375	260		

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/KHAI TRAN/ Primary Examiner.Art Unit 2632 (Primary Examiner)	10/17/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13887889	GRESZCZUK ET AL.
	Examiner	**Art Unit**
	KHAI TRAN	2632

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17	16	33										
	2	1	18	17	34										
	3	2	19	18	35										
	4	3	20	18	36										
	5	4	21	20	37										
	6	5	22												
	7	6	23												
	8	7	24												
	9	8	25												
	10	9	26												
	11	10	27												
	12	11	28												
	13	12	29												
	14	13	30												
	15	14	31												
	16	15	32												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/KHAI TRAN/ Primary Examiner.Art Unit 2632	10/17/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office Part of Paper No. 20131017

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13887889	GRESZCZUK ET AL.
	Examiner	Art Unit
	KHAI TRAN	2632

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2013	10/17/2013							
	1	-	-							
	2	-	-							
	3	-	-							
	4	-	-							
	5	-	-							
	6	-	-							
	7	-	-							
	8	-	-							
	9	-	-							
	10	-	-							
	11	-	-							
	12	-	-							
	13	-	-							
	14	-	-							
	15	-	-							
	16	-	-							
	17	-	-							
1	18	✓	=							
2	19	✓	=							
3	20	✓	=							
4	21	✓	=							
5	22	✓	=							
6	23	✓	=							
7	24	✓	=							
8	25	✓	=							
9	26	✓	=							
10	27	✓	=							
11	28	✓	=							
12	29	✓	=							
13	30	✓	=							
14	31	✓	=							
15	32	✓	=							
16	33	✓	=							
17	34	✓	=							
18	35	✓	=							
19	36	✓	=							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13887889	GRESZCZUK ET AL.
	Examiner	**Art Unit**
	KHAI TRAN	2632

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2013	10/17/2013							
20	37	✓	=							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13887889	GRESZCZUK ET AL.
	Examiner	Art Unit
	KHAI TRAN	2632

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
375	219,220,222,260,282,356,373,376	8/30/2013	KT
370	278,311,503	8/30/2013	KT
455	500,551,560,574	8/30/2013	KT
search updated		10/17/2013	KT

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	8/30/2013	KT
EAST updated	10/17/2013	KT

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
375	219,220,222,260,282,356,373,376	10/17/2013	KT
370	278,311,503	10/17/2013	KT
455	500,551,560,574	10/17/2013	KT

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/887,889	05/06/2013	John A. Greszczuk	6936-28-CON-7

CONFIRMATION NO. 8684

62574
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

PUBLICATION NOTICE

OC000000063886013

Title:MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

Publication No.US-2013-0243051-A1
Publication Date:09/19/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: John A. Greszczuk	Group Art Unit: 2632
Application No.: 13/887,889	Examiner: TRAN, Khai
Filed: May 6, 2013	Confirmation No.: 8684
Atty. File No.: 6936-28-CON-7	

For: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

AMENDMENT AND RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

Applicants submit this Amendment and Response to address the Office Action having a mailing date of September 6, 2013. Please credit any overpayment or charge any underpayment to Deposit Account No. 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Claims are shown in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-17. (Cancelled)

18. (Currently Amended) An apparatus comprising a transceiver operable to:

transmit, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by a synchronization frame;

transmit, in the full power mode, a synchronization signal;

receive a message to enter into a low power mode;

enter into the low power mode by reducing a power consumption of at least one portion of a transmitter;

store, in the low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

transmit, in the low power mode, a synchronization signal; and

exit from the low power and ~~re-enter into~~ restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

19. (Currently Amended) The apparatus of claim 18, further operable to transmit at least one test signal prior to ~~re-entering into~~ restoring the full power mode.

20. (Previously Presented) The apparatus of claim 18, further operable to continue to maintain a synchronized frame count with a second transceiver during the low power mode.

21. (Previously Presented) The apparatus of claim 18, wherein the apparatus is a CO device that is capable of transmitting internet and video data.

22. (Previously Presented) The apparatus of claim 18, wherein the apparatus is a customer premises equipment that is capable of transmitting internet and video data.

23. (Currently Amended) An apparatus comprising a transceiver operable to:

receive, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by a synchronization frame;

~~enter~~receive, in the full power mode, a synchronization signal;

transmit a message to enter into a low power mode;

store, in a low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

receive, in the low power mode, a synchronization signal; and

exit from the low power and ~~re-enter into~~ restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

24. (Currently Amended) The apparatus of claim 23, further operable to receive at least one test signal prior to ~~re-entering into~~ restoring the full power mode.

25. (Previously Presented) The apparatus of claim 23, further operable to continue to maintain a synchronized frame count with a second transceiver during the low power mode.

26. (Previously Presented) The apparatus of claim 23, wherein the apparatus is a CO device that is capable of transmitting internet and video data.

27. (Previously Presented) The apparatus of claim 23, wherein the apparatus is a customer premises equipment that is capable of transmitting internet and video data.

28. (Currently Amended) A method of multicarrier communications comprising:

transmitting, by a transceiver, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by a synchronization frame;

transmitting, in the full power mode, a synchronization signal;

receiving a message to enter into a low power mode;

~~enter~~entering into the low power mode by reducing a power consumption of at least one portion of a transmitter;

storing, in the low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

transmitting, in the low power mode, a synchronization signal; and

exiting from the low power and ~~re-entering into~~ restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

29. (Currently Amended) The method of claim 28, further comprising transmitting at least one test signal prior to ~~re-entering into~~ restoring the full power mode.

30. (Previously Presented) The method of claim 28, further comprising continuing to maintain a synchronized frame count with a second transceiver during the low power mode.

31. (Previously Presented) The method of claim 28, wherein the method is performed by a CO device that is transmitting internet and video data.

32. (Previously Presented) The method of claim 28, wherein the method is performed by a customer premises equipment that is transmitting internet and video data.

33. (Currently Amended) A method of multicarrier communications comprising:

receiving, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by a synchronization frame;

~~entering~~receiving, in the full power mode, a synchronization signal;

transmitting a message to enter into a low power mode;

storing, in a low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

receiving, in the low power mode, a synchronization signal; and

exiting from the low power and ~~re-enter into~~ restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

34. (Currently Amended) The method of claim 33, further comprising receiving at least one test signal prior to ~~re-entering into~~ restoring the full power mode.

35. (Previously Presented) The method of claim 33, further comprising continuing to maintain a synchronized frame count with a second transceiver during the low power mode.

36. (Previously Presented) The method of claim 33, wherein the method is performed by a CO device that is receiving internet and video data.

37. (Previously Presented) The method of claim 33, wherein the method is performed by a customer premises equipment that is receiving internet and video data.

REMARKS

Applicant respectfully requests reconsideration of this application as amended.

Applicant would like to thank the Examiner for the indication of allowable subject matter.

Regarding the outstanding 35 U.S.C. §112 rejection, Applicant believes the objected to term is fully supported by the specification and Figures. See, for example, Figure 2 and the corresponding description. Nevertheless, to advance prosecution, the objected to term has been amended to recite "restore." This term is also fully supported by Fig. 2, and the corresponding description and, at least, page 11, first full paragraph. (See substitute specification.)

With the rejection having been overcome, Applicant respectfully submits the application is in condition for allowance.

A prompt notice of allowance is respectfully solicited.

Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is encouraged to contact Applicants undersigned representative at the telephone number listed below.

The Commissioner is hereby authorized to charge to deposit account number 19-1970 any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby Petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 12 Sept 13

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

Electronic Acknowledgement Receipt

EFS ID:	16837980
Application Number:	13887889
International Application Number:	
Confirmation Number:	8684
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-28-CON-7
Receipt Date:	12-SEP-2013
Filing Date:	06-MAY-2013
Time Stamp:	15:40:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		AMEND_01.pdf	482763 fb5902a805fe0e71ec447b434018dcf0d3f51f8c	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	6
Warnings:			
Information:			
	Total Files Size (in bytes):	482763	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/887,889	Filing Date 05/06/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	09/12/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/CORALIA BETANCOURT/

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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/887,889	05/06/2013	John A. Greszczuk	6936-28-CON-7	8684

62574 7590 09/06/2013

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
TRAN, KHAI	
ART UNIT	**PAPER NUMBER**
2632	

NOTIFICATION DATE	DELIVERY MODE
09/06/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jvick@sheridanross.com

Office Action Summary	Application No. 13/887,889	Applicant(s) GRESZCZUK ET AL.	
	Examiner KHAI TRAN	Art Unit 2632	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *18-37* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *18-37* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/06/2013; 08/05/2013*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. The preliminary amendment field 08/21/2013 has been entered. Claims 1-17 have been cancelled. Claims 18037 are pending in this Office action.

Claim Rejections - 35 USC § 112

2. Claims 18-$$ are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 18, line 13, the phrase "exit from the low power mode and ***re-enter*** into the full power mode", the phrase "re-enter into the full power mode" is not disclosed in the specification and the phrase is not clear what is re-entered into the full power mode as set forth in claim 23, line 10, claim 28, line 12 and claim 33, line 10.

Claim 19-22, 24-27, 29-32 and 34-37 are rejected by virtue of their dependency.

Allowable Subject Matter

3. Claims 18, 23, 28 and 33 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), 2nd paragraph, set forth in this Office action.

4. Claims 19-22, 24-27, 29-32 and 34-37 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Garrett et al (U.S. Pat. 6,047,378) disclose wake multiple over LAN.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAI TRAN whose telephone number is (571)272-3019. The examiner can normally be reached on 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KHAI TRAN/
Primary Examiner, Art Unit 2632

KT
August 30, 2013

Notice of References Cited	Application/Control No. 13/887,889	Applicant(s)/Patent Under Reexamination GRESZCZUK ET AL.	
	Examiner KHAI TRAN	Art Unit 2632	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,047,378	04-2000	Garrett et al.	713/300
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BIB DATA SHEET

CONFIRMATION NO. 8684

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/887,889	05/06/2013 RULE	375	2632	6936-28-CON-7

APPLICANTS

John A. Greszczuk, Stow, MA;
Richard W. Gross, Acton, MA;
Halil Padir, N. Andover, MA;
Michael A. Tzannes, Lexington, MA;
TQ DELTA, LLC, Austin, TX

**** CONTINUING DATA ***************************

This application is a CON of 13/152,558 06/03/2011 PAT 8437382
which is a CON of 12/615,946 11/10/2009 PAT 7978753
which is a CON of 11/425,507 06/21/2006 PAT 7697598
which is a CON of 11/289,516 11/30/2005 ABN
which is a CON of 11/090,183 03/28/2005 ABN
which is a CON of 10/778,083 02/17/2004 ABN
which is a CON of 10/175,815 06/21/2002 ABN
which is a CON of 09/581,400 06/13/2000 PAT 6445730
which is a 371 of PCT/US99/01539 01/26/1999
which claims benefit of 60/072,447 01/26/1998

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
06/05/2013

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /KHAI TRAN/ Examiner's Signature	☑ Met after Allowance KT Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	4	9	1

ADDRESS

Jason H. Vick
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UNITED STATES

TITLE

MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

FILING FEE RECEIVED		
2160	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue)

BIB (Rev. 05/07).

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/887,889
				Filing Date	May 6, 2013
				First Named Inventor	John A. Greszczuk
				Art Unit	
				Examiner Name	Khai Tran
Sheet	1	of	6	Attorney Docket Number	6936-28-CON-7

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Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	2	5224152	06-29-1993	Harte	
	3	5428790	06-27-1995	Harper et al	
	4	5452288	09-19-1995	Rahuel et al.	
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Examiner Signature	/Khai Tran/	Date Considered	08/28/2013

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

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				Examiner Name	Khai Tran
Sheet	2	of	6	Attorney Docket Number	6936-28-CON-7

UNPUBLISHED U.S. PATENT DOCUMENTS					
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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
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Examiner Signature	/Khai Tran/	Date Considered	08/28/2013

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				Examiner Name	Khai Tran
Sheet	3	of	6	Attorney Docket Number	6936-28-CON-7

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				Examiner Name	Khai Tran
Sheet	4	of	6	Attorney Docket Number	6936-28-CON-7

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				Art Unit	
				Examiner Name	Khai Tran
Sheet	5	of	6	Attorney Docket Number	6936-28-CON-7

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Examiner Signature	/Khai Tran/	Date Considered	08/28/2013

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				Examiner Name	Khai Tran
Sheet	6	of	6	Attorney Docket Number	6936-28-CON-7

/K.T./	87	Notice of Allowance for U.S. Patent Application No. 11/425,507, mailed Sep. 22, 2009 (Attorney's Ref. No. 6936-28-CON-4)
	88	Official Action for U.S. Patent Application No. 12/615,946, mailed Aug. 06, 2010 (Attorney Ref. No. 6936-28-CON-5)
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Examiner Signature	/Khai Tran/	Date Considered	08/28/2013

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	2	13/152558	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:02
L3	11512	"re-entering"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:02
L4	0	2 and 3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:02
L5	16106	low adj1 power adj1 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:02
L6	1	2 and 5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:03
L7	1823	full adj1 power adj1 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:03
L8	2	2 and 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:03
L9	1062997	exit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:04
L10	2	2 and 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:04
L11	36941	"re-enter"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:04

L12	0	11 aND 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:04
L13	3360613	ENTER$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:05
L14	188399	9 with 13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:05
L15	0	2 and 14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:05
L16	298008	9 same 13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:06
L17	0	2 and 16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:06
L18	575779	9 and 13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:06
L19	2	2 and 18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:06
L20	883989	frames	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/08/30 10:34
L21	4755	synchronization adj1 frame	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:34
L22	0	21 same 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:35
L23	524	5 same 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:35

L24	9176	synchroniz$5 adj1 frame	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:35
L25	0	23 and 24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:35
L26	133882	synchroniz$5 adj1 signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:37
L27	1139798	message	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:37
L28	47793	transmi$5 near2 20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:41
L29	34964	full adj1 power	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:42
L30	369353	low adj1 power	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:42
L31	3229	29 same 30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:43
L32	177	28 and 31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:43
L33	3	32 and (@ad<="19980126")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 10:43
S1	0	13/887889	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:29
S2	12	"8437382".pn. "7978753".pn. "7697598".pn. 11/425507 11/289516 11/090183 10/778083 10/175815 "6445730".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:31

S3	34930	full adj1 power	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:37
S4	11	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:37
S5	1861	full adj1 power.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:37
S6	1861	S5 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:38
S7	4	S2 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:38
S8	7749	superframe	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:43
S9	6	S5 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:43
S10	10	S2 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:43
S11	1593	superframe.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:43
S12	10	S2 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:44
S13	0	S2 and S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/28 15:44

8/30/2013 11:17:25 AM
C:\Users\ktran1\Documents\EAST\Workspaces\13-887889-1st.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13887889	GRESZCZUK ET AL.
	Examiner	Art Unit
	KHAI TRAN	2632

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
375	219,220,222,260,282,356,373,376,	8/30/2013	KT
370	278,311,503	8/30/2013	KT
455	500,551,560,574	8/30/2013	KT

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	8/30/2013	KT

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13887889	GRESZCZUK ET AL.
	Examiner	Art Unit
	KHAI TRAN	2632

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2013								
	1	-								
	2	-								
	3	-								
	4	-								
	5	-								
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	30	✓								
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	32	✓								
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	34	✓								
	35	✓								
	36	✓								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13887889	GRESZCZUK ET AL.
	Examiner	**Art Unit**
	KHAI TRAN	2632

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2013								
	37	✓								

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/887,889
				Filing Date	May 6, 2013
				First Named Inventor	John A. Greszczuk
				Art Unit	2631
				Examiner Name	Khai Tran
Sheet	1	of	1	Attorney Docket Number	6936-28-CON-7

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

UNPUBLISHED U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] (if known)	Filing Date MM-DD-YYYY	Name of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No.[1]	
/K.T./	1	Official Action for European Patent Application No. 10011996.5, dated May 29, 2013 (Attorney Ref. No. 6936-28-PEP-3-DIV-1)
/K.T./	2	Communication under Rule 71(3) EPC, dated July 5, 2013 granting European Patent Application No. 10012013.8 (Attorney Ref. No. 6936-28-PEP-3-DIV-2)

Examiner Signature	/Khai Tran/	Date Considered	08/28/2013

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: John A. Greszczuk	Group Art Unit: 2632
Application No.: 13/887,889	Examiner: TRAN, Khai
Filed: May 6, 2013	Confirmation No.: 8684
Atty. File No.: 6936-28-CON-7	

For: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the initial review of the above-identified patent application by the Examiner, please enter the following Preliminary Amendment. Although Applicants do not believe that any fees are due based upon the filing of this Preliminary Amendment, please charge any such fees to Deposit Account 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Claims are shown in the listing of claims which begin on page 2 of this paper.

Remarks begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1.-17. (Cancelled)

18. (New) An apparatus comprising a transceiver operable to:

transmit, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by synchronization frame;

transmit, in the full power mode, a synchronization signal;

receive a message to enter into a low power mode;

enter into the low power mode by reducing a power consumption of at least one portion of a transmitter;

store, in the low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

transmit, in the low power mode, a synchronization signal; and

exit from the low power and re-enter into the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

19. (New) The apparatus of claim 18, further operable to transmit at least one test signal prior to re-entering into the full power mode.

20. (New) The apparatus of claim 18, further operable to continue to maintain a synchronized frame count with a second transceiver during the low power mode.

21. (New) The apparatus of claim 18, wherein the apparatus is a CO device that is capable of transmitting internet and video data.

22. (New) The apparatus of claim 18, wherein the apparatus is a customer premises equipment that is capable of transmitting internet and video data.

23. (New) An apparatus comprising a transceiver operable to:

receive, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by synchronization frame;

enter, in the full power mode, a synchronization signal;

transmit a message to enter into a low power mode;

store, in a low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

receive, in the low power mode, a synchronization signal; and

exit from the low power and re-enter into the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

24. (New) The apparatus of claim 23, further operable to receive at least one test signal prior to re-entering into the full power mode.

25. (New) The apparatus of claim 23, further operable to continue to maintain a synchronized frame count with a second transceiver during the low power mode.

26. (New) The apparatus of claim 23, wherein the apparatus is a CO device that is capable of transmitting internet and video data.

27. (New) The apparatus of claim 23, wherein the apparatus is a customer premises equipment that is capable of transmitting internet and video data.

28. (New) A method of multicarrier communications comprising:

transmitting, by a transceiver, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by synchronization frame;

transmitting, in the full power mode, a synchronization signal;

receiving a message to enter into a low power mode;

enter into the low power mode by reducing a power consumption of at least one portion of a transmitter;

storing, in the low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

transmitting, in the low power mode, a synchronization signal; and

exiting from the low power and re-entering into the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

29. (New) The method of claim 28, further comprising transmitting at least one test signal prior to re-entering into the full power mode.

30. (New) The method of claim 28, further comprising continuing to maintain a synchronized frame count with a second transceiver during the low power mode.

31. (New) The method of claim 28, wherein the method is performed by a CO device that is transmitting internet and video data.

32. (New) The method of claim 28, wherein the method is performed by a customer premises equipment that is transmitting internet and video data.

33. (New) A method of multicarrier communications comprising:

receiving, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by synchronization frame;

entering, in the full power mode, a synchronization signal;

transmitting a message to enter into a low power mode;

storing, in a low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;

receiving, in the low power mode, a synchronization signal; and

exiting from the low power and re-enter into the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

34. (New) The method of claim 33, further comprising receiving at least one test signal prior to re-entering into the full power mode.

35. (New) The method of claim 33, further comprising continuing to maintain a synchronized frame count with a second transceiver during the low power mode.

36. (New) The method of claim 33, wherein the method is performed by a CO device that is receiving internet and video data.

37. (New) The method of claim 33, wherein the method is performed by a customer premises equipment that is receiving internet and video data.

REMARKS/ARGUMENTS

By this amendment, claims 1-17 are canceled without prejudice or disclaimer and new claims 18-37 have been added.

Applicant requests examination on the merits.

Applicant believes that the pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

The Commissioner is hereby authorized to charge to Deposit Account No. 19-1970 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby Petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 2/4/13

Electronic Patent Application Fee Transmittal	
Application Number:	13887889
Filing Date:	06-May-2013
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Filer:	Jason Vick/Joanne Vos
Attorney Docket Number:	6936-28-CON-7
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Independent claims in excess of 3	1201	1	420	420
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**420**

Electronic Acknowledgement Receipt

EFS ID:	16645240
Application Number:	13887889
International Application Number:	
Confirmation Number:	8684
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-28-CON-7
Receipt Date:	21-AUG-2013
Filing Date:	06-MAY-2013
Time Stamp:	13:26:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$420
RAM confirmation Number	10625
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		AMEND_PRELIM_02.pdf	435489 14eb281fe96c218ab27ef3d67471959f76896c4b	yes	6

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Claims	2	5
Applicant Arguments/Remarks Made in an Amendment	6	6

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30797 872d1769f8a590e5f1c6a6b7aec9916dac570392	no	2

Warnings:

Information:

Total Files Size (in bytes):	466286

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/887,889	Filing Date 05/06/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	08/21/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X $420 =	420
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**420**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/TERRANCE LAWRENCE/

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/887,889
				Filing Date	May 6, 2013
				First Named Inventor	John A. Greszczuk
				Art Unit	2631
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	6936-28-CON-7

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

UNPUBLISHED U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] (if known)	Filing Date MM-DD-YYYY	Name of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No.[1]	
	1	Official Action for European Patent Application No. 10011996.5, dated May 29, 2013 (Attorney Ref. No. 6936-28-PEP-3-DIV-1)
	2	Communication under Rule 71(3) EPC, dated July 5, 2013 granting European Patent Application No. 10012013.8 (Attorney Ref. No. 6936-28-PEP-3-DIV-2)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt

EFS ID:	16504572
Application Number:	13887889
International Application Number:	
Confirmation Number:	8684
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-28-CON-7
Receipt Date:	05-AUG-2013
Filing Date:	06-MAY-2013
Time Stamp:	17:34:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_02.pdf	359449 b01c18f4f49c098351048d4c7bdc5e8992e9c9dc	yes	4

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Form (SB08)		4	4	
Warnings:					
Information:					
2	Non Patent Literature	6936-28-PEP-3-DIV-2_Intent_to_Grant_07-05-2013.pdf	488375 a5a91a03854e25adba1308b9999266d216f2ab4c	no	7
Warnings:					
Information:					
3	Non Patent Literature	6936-28-PEP-3-DIV-1_OA_05-29-2013.pdf	101892 05ba6189305ea6bff5bb5f8f78ca6e24efe717c8	no	4
Warnings:					
Information:					
		Total Files Size (in bytes):	949716		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2631
John A. Greszczuk	)	Confirmation No.: 8684
Serial No.: 13/887,889	)	Examiner:
Filed: May 6, 2013	)	
Atty. File No.: 6936-28-CON-7	)	SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
Entitled: "MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY"	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.

☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.

☐ Copies of the cited U.S. patents/unpublished patent applications/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).

☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.

☐ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English translation/abstracts and/or in the figures, although applicants do not necessarily vouch for the accuracy of the translation.

☐ Examiner's attention is drawn to the following related applications:

- Serial No. _____ filed _____(Attorney Ref. No. _____)

☐ Other:_____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the pertinence of any reference without the benefit of hindsight, nor should an inference be

drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☒	**37 CFR 1.97(b)**: No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry into the national stage of an international application as set forth in 37 CFR 1.491 or ☒ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☐	**37 CFR 1.97(c)**: The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of one of the following conditions: (1) a final action under 37 C.F.R. 1.113 or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☐ A Certification (below) as specified by 37 C.F.R. 1.97(e). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of $180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	**37 CFR 1.97(d)**: This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of $180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)

☐ The undersigned certifies that:

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).

☐ A copy of the communication from the foreign patent office is enclosed.

OR

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 5 May 12

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: John A. Greszczuk	Group Art Unit: 2631
Application No.: 13/887,889	Examiner:
Filed: May 6, 2013	Confirmation No.: 8684
Atty. File No.: 6936-28-CON-7	

For: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

SUBMISSION OF DECLARATION

Dear Madam:

The Informational Notice to Applicant dated June 13, 2013 required an executed Declaration to be submitted at any time before the issuance of the Notice of Allowance. In response to the Notice, submitted herewith is a fully executed Declaration.

Applicants believe no further fees or petitions are required. However, if any such petitions or fees are necessary, please consider this a request therefore and authorization to charge Deposit Account No. 19-1970 accordingly. Any deficiency or overpayment may also be applied to Deposit Account No. 19-1970.

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____
Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 15 Jul '13

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: John A. Greszczuk Date (Optional): May 10, 2013

Signature: John A Greszczuk

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

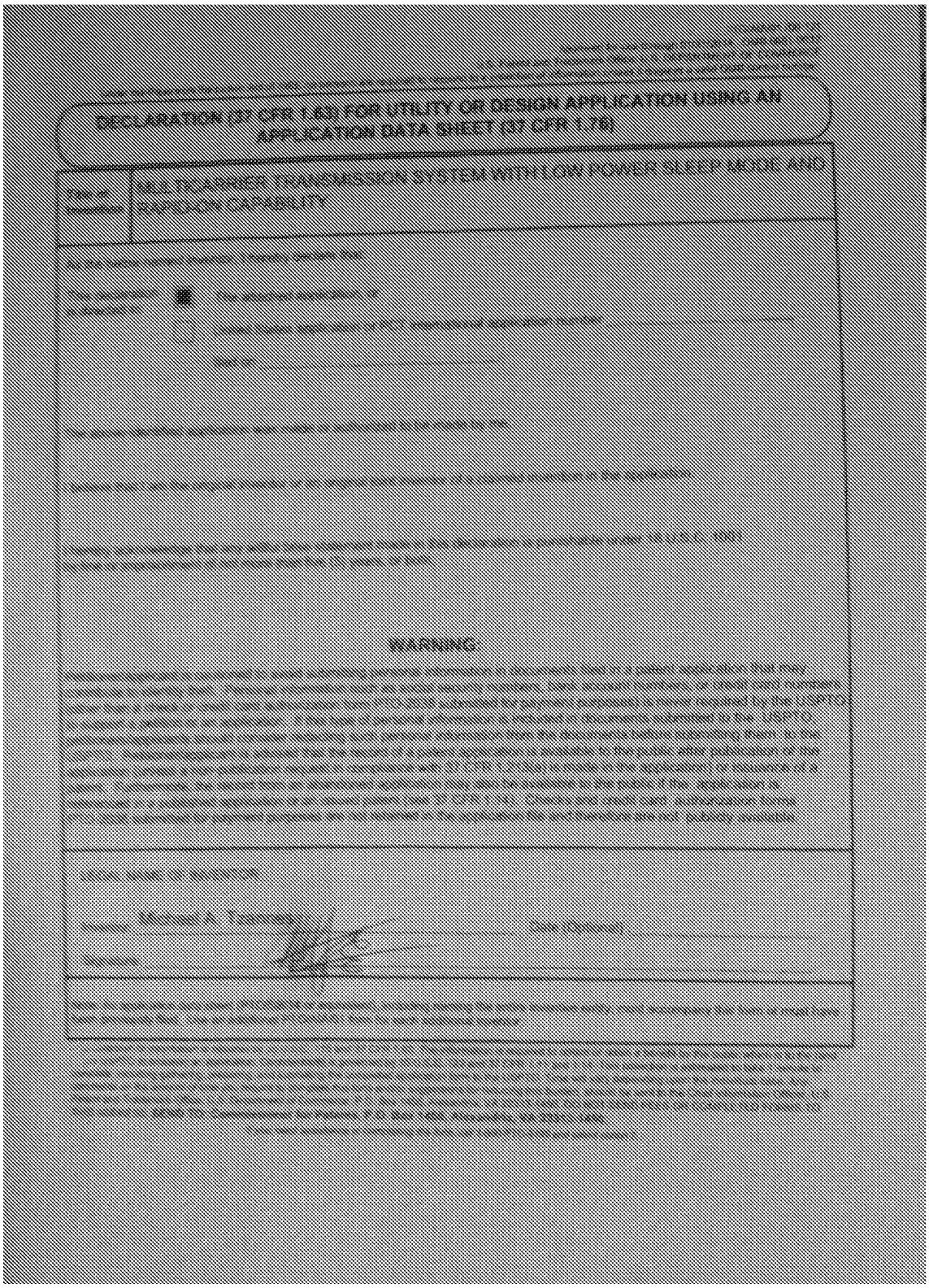
Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Richard W. Gross Date (Optional): 4/10/2013

Signature: Richard W. Gross

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.



DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

WARNING:

Doc code: Oath
Document Description: Oath or declaration filed

PTO/AIA/02 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

This statement is directed to:

☐ The attached application,

OR

☒ United States application or PCT international application number 13/887,889 filed on May 6, 2013.

LEGAL NAME of inventor to whom this substitute statement applies:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

Halil Padir

Residence (except for a deceased or legally incapacitated inventor):

City	State	Country
Lexington	MA	US

Mailing Address (except for a deceased or legally incapacitated inventor):

26B Parker Street

City	State	Zip	Country
Lexington	MA	02421	US

I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Relationship to the inventor to whom this substitute statement applies:

☐ Legal Representative (for deceased or legally incapacitated inventor only),

☒ Assignee,

☐ Person to whom the inventor is under an obligation to assign,

☐ Person who otherwise shows a sufficient proprietary interest in the matter (petition under 37 CFR 1.46 is required), or

☐ Joint Inventor.

PTO/SB/AIA02 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

SUBSTITUTE STATEMENT

Circumstances permitting execution of this substitute statement:

- ☐ Inventor is deceased,
- ☐ Inventor is under legal incapacity,
- ■ Inventor cannot be found or reached after diligent effort, or
- ☐ Inventor has refused to execute the oath or declaration under 37 CFR 1.63.

If there are joint inventors, please check the appropriate box below:

- ■ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

OR

- ☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Mark K. Roche, Managing Director of TQ Delta, LLC | Date (Optional):

Signature: Mark K Roche

Residence (unless provided in an application data sheet, PTO/AIA/14 or equivalent):

City Austin | State TX | Country US

Mailing Address (unless provided in an application data sheet, PTO/AIA/14 or equivalent)

805 Las Cimas Parkway, Suite 240

City Austin | State TX | Zip 78746 | Country US

Note: Use an additional PTO/AIA/02 form for each inventor who is deceased, legally incapacitated, cannot be found or reached after diligent effort, or has refused to execute the oath or declaration under 37 CFR 1.63.

Electronic Acknowledgement Receipt

EFS ID:	16319689
Application Number:	13887889
International Application Number:	
Confirmation Number:	8684
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-28-CON-7
Receipt Date:	15-JUL-2013
Filing Date:	06-MAY-2013
Time Stamp:	17:11:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	Submisison_of_Declaration.pdf	77288 bc15677e8bb2f30f8fedc01b88f25ceb73bddbe2	no	1

Warnings:

Information:

2	Oath or Declaration filed	Executed_AIA_Dec.pdf	1427118 b254377cc3c088a532dca99330cc0acf10dff2aa1	no	5

Warnings:	
Information:	
Total Files Size (in bytes):	1504406

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/887,889

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	9 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/887,889	05/06/2013	2631	1740	6936-28-CON-7	9	1

CONFIRMATION NO. 8684

62574
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

FILING RECEIPT

OC000000061731546

Date Mailed: 06/13/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

John A. Greszczuk, Stow, MA;
Richard W. Gross, Acton, MA;
Halil Padir, N. Andover, MA;
Michael A. Tzannes, Lexington, MA;

Applicant(s)

TQ DELTA, LLC, Austin, TX

Assignment For Published Patent Application

TQ DELTA, LLC, Austin, TX

Power of Attorney: The patent practitioners associated with Customer Number 62574

Domestic Priority data as claimed by applicant

This application is a CON of 13/152,558 06/03/2011 PAT 8437382
which is a CON of 12/615,946 11/10/2009 PAT 7978753
which is a CON of 11/425,507 06/21/2006 PAT 7697598
which is a CON of 11/289,516 11/30/2005 ABN
which is a CON of 11/090,183 03/28/2005 ABN
which is a CON of 10/778,083 02/17/2004 ABN
which is a CON of 10/175,815 06/21/2002 ABN
which is a CON of 09/581,400 06/13/2000 PAT 6445730
which is a 371 of PCT/US99/01539 01/26/1999
which claims benefit of 60/072,447 01/26/1998

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 06/05/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/887,889**

Projected Publication Date: 09/19/2013

Non-Publication Request: No

Early Publication Request: No

Title

MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

Preliminary Class

375

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/887,889	05/06/2013	John A. Greszczuk	6936-28-CON-7

CONFIRMATION NO. 8684

62574
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

NOTICE

OC000000061731547

Date Mailed: 06/13/2013

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  All
  Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

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CONFIRMATION NO. 8684

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POA ACCEPTANCE LETTER

OC000000061731597

Date Mailed: 06/13/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/06/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/agizaw/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: John A. Greszczuk	Group Art Unit:
Application No.: Not yet assigned	Examiner:
Filed: Herewith	Confirmation No.:
Atty. File No.: 6936-28-CON-7	

For: MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the initial review of the above-identified patent application by the Examiner, please enter the following Preliminary Amendment. Although Applicants do not believe that any fees are due based upon the filing of this Preliminary Amendment, please charge any such fees to Deposit Account 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are shown in the listing of claims which begin on page 3 of this paper.

Remarks begin on page 5 of this paper.

AMENDMENTS TO THE SPECIFICATION

Attached hereto is a substitute specification including a clean copy and a marked-up copy thereof. No new matter is believed to have been added therein.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A multicarrier transceiver having a sleep mode capability, comprising

A. means responsive to a sleep mode command for:

(1) storing selected state parameters characteristic of the communications channel over which the transceiver is operating; and

(2) reducing power to selected portions of transceiver circuitry; and

B. means responsive to a wake-up command for:

(1) restoring power to said transceiver;

(2) restoring the state of said transceiver from said sleep mode by means of said stored parameters; and

C. means for maintaining a common, synchronized data frame count between said transceiver and a remote transceiver with which it communicates, to thereby facilitate restoration of communication without reinitialization of said transceiver.

2. (Original) A multicarrier transceiver according to claim 1 in which said state parameters include one or more parameters selected from the group comprising frequency-domain equalizer coefficients, time-domain equalizer coefficients, echo canceller coefficients, bit allocations, coding parameters, fine gains, and subchannel gains.

3. (Original) A multicarrier transceiver according to claim 1 in which the means for maintaining said frame count comprises a signal defining a timing reference during at least the time when said first transceiver is in sleep mode.

4. (Original) A multicarrier transceiver according to claim 3 in which said signal comprises a pilot tone transmitted from one transceiver to another with which it is in communication.

5. (Original) A multicarrier transceiver according to claim 4 in which said pilot tone is transmitted between said transceivers during both normal operation and reduced power operation.

6. (Original) A multicarrier transceiver according to claim 1 in which maintaining synchronization includes maintaining synchronization of frame counters between said transceivers.

7. (Original) A multi carrier transceiver according to claim 6 in which maintaining synchronization further includes maintaining synchronization of the phase of a synchronizing signal transmitted between said transceivers.

8. (Original) A multicarrier transceiver according to claim 1 including means to transmit an idle symbol to said remote transceiver when said transceiver is in sleep mode.

9. (Original) A multicarrier transceiver according to claim 1 including means to transmit to said remote transceiver a short test signal on awaking from sleep mode in order to determine whether transmission conditions have changed sufficiently during sleep mode to require reinitialization of said transceiver on emerging from sleep mode.

10-17. (Cancelled)

REMARKS/ARGUMENTS

By this amendment, claims 10-17 are canceled without prejudice or disclaimer.

Applicant requests examination on the merits.

Applicant believes that the pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

The Commissioner is hereby authorized to charge to Deposit Account No. 19-1970 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby Petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

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Date: 6 Mar 12

MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

BACKGROUND OF THE INVENTION

The invention relates to multicarrier transmission systems, and comprises method and apparatus for establishing a power management sleep state in a multicarrier system.

SUMMARY OF THE INVENTION

This application is based on United States Provisional Application Sere No. ***, filed January 26, 1998 by John Greszczuck. Rick Gross and Halil Padir and claims the benefit thereof.

Multicarrier transmission systems provide high speed data links between communication points. Such systems have recently been introduced for communications over the local subscriber loop that connects a telephone service subscriber to a central telephone office; in this important application they are commonly referred to as "xDSL" systems, where the "x" specifies a particular variant of DSL (digital subscriber loop) communications, e.g., ADSL (asynchronous digital subscriber loop), HDSL (High-Speed Digital Subscriber Loop), etc. These will be referred to generically herein simply as "DSL" systems.

In such systems, a pair of transceivers communicate with other by dividing the overall bandwidth of the channel interconnecting the subscriber and the central office into a large number of separate subchannels, each of limited bandwidth, operating in parallel with each other. For example, one common system divides thee subscriber line channel into two hundred and fifty six subchannels, each of 4.3 kilohertz bandwidth. A first group of these (e.g., one hundred ninety six) is allocated to communications from the central office to the subscriber (this is known as the "downstream" direction); a second group (e.g., thirty-two) is allocated to communications from the subscriber to the central office (this is known as the "upstream" direction). The remaining subchannels are allocated to administrative, overhead and control (AOC) functions.

Data to be communicated over the link is divided into groups of bits, one group for each subchannel. The group of bits allocated to a given subchannel is modulated onto a carrier whose

frequency is specific to that channel. Typically, quadrature amplitude modulation (QAM) is used for this purpose, and the group of bits is mapped into a vector defined by one of the points of a "constellation" which specifies the allowable data points for transmission over that subchannel at a particular time. Each vector or data point thus comprises a unique symbol representing a specific bit configuration for transmission as a group over its associated subchannel. During the time period allocated for transmission of a symbol (commonly referred to as a "symbol period" or "frame"), each subchannel transmits its symbol in parallel with all other subchannels so that large amounts of data can be transmitted during each frame.

The number of bits carried by a symbol is dependent on the characteristics of the subchannel over which it is to be transmitted. This may vary from one subchannel to another. The principal determinant is the signal-to-noise ratio oft he subchannel. Accordingly, this parameter is measured from time to time in order to ascertain its value for each subchannel, and thus determine the number of bits to be transmitted on the particular subchannel at a given time.

The telephone channel is subject to a number of impairments which must be compensated for in order to ensure reliable transmission. Phase (delay) distortion of the transmitted signal is typically the most limiting of these impairments. This distortion is frequency-dependent, and thus components of a signal at different frequencies are shifted by varying amounts, thereby distorting the signal and increasing the likelihood of erroneous detection unless provision is made to combat it. To this end, frequency domain equalizers (FDQ) and time domain equalizers (TDQ) are commonly incorporated into the transmission channel in order to equalize the phase (time) delay across the channel frequency band. Other impairments also exist. For example, frequency-dependent signal attenuation adversely affects signal transmission on the telephone line. This is compensated by the use of gain equalizers on the line, while echo on the line is handled by the use of echo cancellers.

The problem of signal impairment is especially serious in those xDSL configurations which carry the DSL communications on a common line with ordinary voice communications but which omit the use of a "splitter" at either the subscriber premises the central office or both. A "splitter" is basically a filter which separates the low-frequency voice communications (e.g., from zero to four kilohertz) from the higher frequency data communications (which may extend up into the megahertz band) and provides a strong degree of isolation between the two. In the

absence of a splitter, unique provisions must be made to accommodate voice and data communications on the same line. For a more detailed description of the problem and its solution, see the co-pending application of Richard Gross et al. entitled "Splitterless Multicarrier Modem", Serial No. PCT/US98 21442, filed October 9, 1998, and assigned to the assignee of the present invention, the disclosure of which is incorporated herein by reference.

Because of their extensive use in Internet communications as well as in other applications, DSL transceivers are commonly maintained in the "on" state, ready to transmit or receive once they have been installed and initialized. Thus, such modems consume a significant amount of power, even when they are not actively transmitting or receiving data. It is generally desirable to limit this power consumption, both for environmental reasons as well as to prolong the life of the equipment. Further, such modems may be implemented or incorporated in part or in whole in computer equipment such as in personal computers for home and business use, and such computers increasingly incorporate power conservation procedures. See, for example, U.S. Patent No. 5,428,790, "Computer Power Management System", issued June 27, 1995 on the application of L. D. Harper. Thus, it is desirable to provide an ADSL modem which can accommodate power conservation procedures in equipment with which it is associated, as well as independently of such equipment as may be appropriate.

Because of the complexity of DSL transceivers, and the conditions under which they must operate, it is necessary to initialize them prior to the transmission and reception of data. This initialization includes, *inter alia,* channel corrections such as "training" the frequency-domain and time-domain equalizers and the echo cancellers; setting the channel gains; negotiating the transmission and reception data rates; adjusting the fine gains on the subchannels over which communication is to take place; setting the coding parameters; and the like. Additionally, it includes measuring the signal-to-noise ratio of each of the subchannels, calculating the bit-allocation tables characteristic of each under given conditions of transmission, and exchanging these tables with other modems with a given modem communicates. For more detailed discussion of these procedures, refer to the application of Richard Gross et al., cited above and incorporated herein by reference. These procedures can require from seconds to tens of seconds. In a new installation, the time required is inconsequential. However, in an already-operating installation, the time required to initialize or re-initialize the system after a suspension

of operation in connection with power conservation is generally unacceptable, since it is typically desired to have the modem respond to request for service nearly instantaneously.

Accordingly, it is an object of the invention to provide a multicarrier transmission system having a low power sleep mode and a rapid-on capability.

Further, it is an object of the invention to provide a multicarrier transmission system for use in digital subscriber line communications that can rapidly switch from a sleep mode to a full-on condition.

Still another object of the invention is to provide a DSL system that can readily be integrated into a computer having a low power sleep mode and which is capable of rapid return to full operation.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention description below refers to the accompanying drawings, of which:

Figure 1 is a block and line diagram of a multicarrier transmission system in accordance with a preferred embodiment of the present invention;

Figure 1A is a portion of an exemplary chart showing a possible bit distribution among subchannels;

Figure 1B illustrates a timing signal used in accordance with the invention;

Figure 2 is a flow diagram of the operation of the present invention; and

Figure 3 is a block and line diagram of still another aspect of the present invention.

DETAILED DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

For purposes of explanation, the present invention will be described in the context of an ADSL system having a first transceiver located at the site of a customer's premises (referred to hereinafter as the "CPE transceiver") and a second transceiver located at a local central telephone office (hereinafter referred to as the "CO transceiver"). The two are interconnected for communication by means of a common telephone line over which voice and data are to be transmitted, and the CO transceiver is commonly connected into a broader network such as the Internet to and from which data is to be communicated. The system will be described as using

Fourier transform technology for modulation and demodulation of the data to be transmitted. It will be understood, however, that the invention is not limited to this environment, and is applicable to point-to-point communications is other environments, and with other forms of modulation/demodulation. Further, since the CPE transceiver and CO transceiver are very similar, the invention will be explained in connection with a detailed illustration of the CPE transceiver only.

In Figure 1, a DSL transceiver 10 in accordance with the present invention has a transmitter section 12 for transmitting data over a digital subscriber line 14 and a receiver section 16 for receiving data from the line. The transmitter section 12 is formed from an input buffer and converter (IBC) 18 that receives a serial string of data (e.g., binary digits) b_i to be transmitted and converts the data into a plurality of pairs of complex-valued symbols X_i and their conjugates $X_{N-i} = X^*_i$, i = 0, 1, ...N. Typically, the buffer 18 holds at least a frame of data (a frame comprising the amount of data to be transmitted during one symbol period). The pairs of symbols X_i and X^*_i are applied to an Inverse Fast Fourier Transform (IFFT) 20 to provide real time output signals X_j, j = 0, 1, ...N/2 -1. The latter in turn are converted to serial form in a parallel-to-serial convener (PSC) 22 and then applied to a digital-to-analog converter (DAC) 24 for application to a line driver 26. The converter 24 may apply a cyclic prefix to the signals X_j to combat intersymbol interference caused by the transmission medium. The driver 26 may incorporate a gain control section (GC) 26a for controlling the signal amplitude (and thus power) as it is applied to a communication channel such as the digital subscriber line 14.

IFFT 20 may be viewed as a data modulator. The symbols X_i , and their conjugates $X_{N-i,}$ correspond to data points defining signal vectors in a quadrature amplitude modulation (QAM) constellation set. The converter 18 forms the respective symbols from the input data with the aid of a bit allocation table (BAT) 28 which specifies, for each subchannel, the number of bits to be carried by the symbol transmitted over that subchannel, and thus defines the data point to be associated with the symbol. This table is typically calculated at the transceiver and is transmitted to other transceivers with which the instant transceiver communicates, to thereby enable them to decode the symbols received by them from the instant transceiver.

The number of bits which each symbol carries is determined by the characteristics of the subchannel over which the symbol is to be transmitted, and particularly by the signal-to-noise

ratio of the subcbannel. Procedures for this calculation are known. Figure lA shows an example of such a table as formed and stored at transceiver 10. Thus, the symbol to be transmitted over subchannel 50 may be determined to have an allocation of six bits; that of subchannel 51, six bits; that of subchannel 52, seven bits, etc.

A Clock 30 controls the timing of the operation of the transmitter 12. It supplies input to a Controller 32 which controls the individual units of the transmitter. In the case of the CO transceiver, the clock 30 typically is a master clock to which a remote transceiver, such as at a subscriber premises, will be synchronized. In the case of a transceiver at the subscriber premises, such as is shown here for purposes of illustration, the clock is derived from the master clock at the central office as described more fully below in connection with the receiver portion of the transceiver.

A Frame Counter (FC) 24 connected to the controller 32 maintains a count of the number of frames of data transmitted from or received by the transceiver 10. The clock 30 maintains the count in counter 34 synchronous with that of a corresponding counter (not shown) in the CO transceiver. In DSL systems, typically, data is communicated in the form of a sequence of data frames (e.g., sixty-eight frames for ADSL as specified in ITU Document G.992.2), followed by a synchronization frame, each frame having a duration of one symbol period of approximately two hundred and fifty microseconds. Together, the sixty-nine frames comprise a "superframe". Thus, the counter 34 typically maintains a count modulo sixty-nine. Finally, a State Memory (SM) 36 connected to the controller 32 records the state of the transceiver for reasons discussed more fully below.

Turning now to the receiver section 16, it is formed from a line conditioner 50; an analog-to-digital converter (ADC) 52; a serial-to-parallel converter 54; a Fast Fourier Transform (FFT) section 56; a decoder 58; and a parallel-to-serial converter 60. The conditioner 50 compensates for transmission distortions introduced by the line 14, and commonly includes a frequency-domain equalizer (FDQ) 50a; a time-domain equalizer (TDQ) 50b; and an echo canceller (EC) 50c, among other elements. The ADC 52 converts the received signal to digital form and applies it to the serial-to-parallel converter 54. The converter 54 removes any cyclic prefix that may have been appended to the signal before it was transmitted, and applies the resultant signal to the FFT 56 which effectively "demodulates" the received signal. The output

of the FFT is applied to decoder 58 which, in conjunction with a bit-allocation-table 62, recovers the symbols X_i and X_i and the bits associated with them. The output of detector 58 is applied to the parallel-to-serial converter 60 which restores the data stream, b_i, that was originally applied to the transmitter. The controller 32 also controls the operation of the receiver portion 16 of the transceiver 10.

During normal (non-sleep mode) operation, a phase-lock loop (PLL) 62 receives from the FFT 56 a timing reference signal 62a (see Figure lA) via a line 62b. The timing reference signal 62a is transmitted from the transmitter with which the receiver 16 communicates (e.g., the CO transmitter). This signal is advantageously a pure tone of fixed frequency and phase which is synchronized with the Master Clock in the transmitter; its frequency defines the frame rate of the transceivers. Other forms of timing signal may, of course, be used, but use of a pure tone has the advantage of simplicity and reliability even when portions of the transceiver are powered down in accordance with the invention. The PLL 62 locks itself to this signal and drives clock 30 in synchronism with the Master Clock in the driving transmitter. This also synchronizes frame counter 34 of the CPE transceiver to the corresponding frame counter of the CO transceiver. Control of the receiver section is provided by the controller 32.

In the sleep mode, the FFT 56 is preferably dormant. Accordingly, the timing reference signal for PLL 62 is provided from the output of the analog to digital convener 52 via a detector 64 which extracts the timing signal from the signal appearing on line 14 during sleep mode, by calculating the DFT of the synchronizing pilot tone. Controller 32 controls the switching of the input to PLL 62 between these two sources so that the PLL remains locked to the CO transceiver timing reference.

As noted earlier, the transceiver of the present invention will commonly be incorporated in a computer such as a personal computer; indeed, it may be implemented as an integral part of such a computer, which may have a power conservation capability for activation when the computer is not in active operation. It is thus desirable that the transceiver be able to suspend operations and enter a "sleep" mode in which it consumes reduced power when it is not needed for data transmission or reception, but nonetheless be able to resume transmission or reception almost instantaneously, e.g., within a few frames.

Further, when the ADSL transceiver is implemented as an integral part of a computer, it may often be the case that the processing power of the computer is, at a given moment, devoted to another task such as graphics, word processing, and the like, and is thus unable to service the transceiver. In such circumstances, it is possible that a frame that is assembled for transmission to the CO transceiver, and thence to some network connected to it, is incomplete, and thus would generate errors if transmitted. Accordingly, the transceiver of the present invention is responsive to such conditions by entering an "idle" state in which it ceases active transmission of data while the computer is elsewhere occupied. This state is similar in many ways to the sleep mode state although, of course, its purpose is not power conservation, and thus in the idle state the power to selected portions of the transceiver may, but need not, be reduced. The idle state maintains synchronous signaling between the CPE and CO transceivers but no data is transmitted. On receipt of the idle indicator from the CPE, the CO transceiver transmits idle cells to the network to maintain connection with the network.

Referring now more particularly to Figure 2, the power down operation of the CPE transceiver begins on receipt of a power down indication (step 80) by the CPE transceiver controller 32. The power down indication may be applied to the controller 32 from an external source such as a personal computer in which the transceiver is included; it may be generated within the transceiver itself as a result of monitoring the input buffer 18 and determining that no data has been applied to it for a given time interval or that the buffer has not been filled despite passage of a symbol time; it may be responsive to a power down command from the CO transceiver; or it may be generated in response to other conditions.

Considering for the moment the first two cases, the CPE transceiver responds to the indication by transmitting to the CO transceiver an "Intend To Enter Sleep Mode" notification (step 82). This notification indicates that the transceiver is about to undergo a change of state, and may take any of a variety of forms; preferably it is a message, but may also comprise a tone, an inverted sync signal, a flag, or even the cessation of data transmission itself. The notification may advantageously be transmitted over one of the embedded operations channels of the system. It provides the CO transceiver an opportunity to prepare itself to enter sleep mode, and also to signal the CPE transceiver if entrance into sleep mode is not appropriate or desirable at the particular moment.

If entrance into sleep mode is permissible at this time; the CO transceiver responds to the power down or idle signal by transmitting an "Acknowledge Sleep Mode" notification (step 84) to the CPE transceiver. This and subsequent notifications described in connection with the sleep or idle mode may similarly take any of a variety of forms such as described above for the "Intend To Enter Sleep Mode" notification, but again preferably is in the form of a message transmitted over an embedded operations channel.

After it has received acknowledgment from the CO transceiver, the CPE transceiver transmits an "Entering Sleep Mode" notification (step 86) to the CO transceiver and ceases transmission, either immediately or after a given number of frames. The CO transceiver detects this notification; transmits its own "Entering Sleep Mode" notification (step 88); and enters sleep mode (step 90). In pursuance of this, the CO transceiver stores its state in its own state memory corresponding to the state memory 38 of CPE transceiver 10. The state of the CO or CPE transceivers preferably includes at least the frequency and time-domain equalizer coefficients (FDQ; TDQ) and the echo-canceller coefficients (ECC) of its receiver portion and the gain of its transmitter portion; the transmission and reception data rates; the transmission and reception coding parameters; the-transmission fine gains; and the Bit Allocation Tables. The CO transceiver continues to advance the frame count and superframe count during the period of power-down in order to ensure synchrony with the remote CPE transceiver when communications are resumed. In order to maintain synchronization during the power down or idle state, the CO transceiver continues to transmit to the CPE transceiver the synchronizing pilot tone 62a. It may, at this time, perform its own power reduction. In particular, it may reduce or cut off power to the digital modulator/demodulator portions of its transmitter and receiver sections (corresponding to the IFFT 20 and FFT 56 of the CPE transceiver, Fig. 1); this provides a significant power reduction. Further, it may reduce power to parts of the analog circuitry. Power will be maintained, of course, to at least that portion of the analog driver circuitry which transmits the pilot tone and other control signals to the CPE transceiver, and to line circuits required to monitor the line 14 for signals from the CPE transceiver.

In a central office, the rest of the equipment is still operating, and while the link between the CO transceiver and the CPE transceiver is in a sleep state, user data provided by the CO

transceiver will be benign idle data such as ATM Idle-Cells or HDLC Flag octets, and not generate false data errors to other equipment.

In response to the "Entering Sleep Mode" notification from the CO transceiver, the CPE transceiver enters the sleep mode (step 92). In particular, it stores its state (step 94) in state memory 38; as noted above in connection with the CO transceiver, this includes preferably at least the frequency and time-domain equalizer coefficients (FDQ; TDQ) and the echo-canceller coefficients (ECC) of its receiver and the gain of its transmitter; the transmission and reception data rates; the transmission and reception coding parameters; the transmission fine gains; and the Bit Allocation Tables. The phase and frequency offset of the phase-locked loop 62 is maintained by continued operation of the loop. The CPE transceiver 10 then reduces power to the digital modulator/demodulator circuitry comprising IFFT 20 and FFT 56, as well as to and transmitter data line drivers 26. However, it continues to advance the frame counter 34 in accordance with the received synchronizing signal 62a. However, the CPE controller 32 now causes this signal to be applied to the PLL 62 from the output of the ADC 52 (Fig. 1) via the detector 64, which implements the DFT of a single tone, instead of directly from the output of the FFT 56 as was previously the case. This enables the FFT 56 to be powered down. The CPE and CO transceivers then operate in sleep mode (steps 95 and 97, respectively) until they awaken.

During the sleep mode state, the CO transceiver continues to monitor (step 90) the data subscriber line 14 for an "Exiting Sleep Mode" signal from the CPE transceiver (step 96). The CPE transceiver transmits this signal when its controller receives an "Awaken" indication (step 98) from an external source such as a computer in which it is installed or from other sources, or when its controller detects the presence of new data in the input buffer 18. In response to the "Awaken" signal, the CPE transceiver retrieves its stored state from the state memory 38; restores full power to its circuitry; and restores the output of the FFT 56 to the input .of the PLL 62 (step 96). The CO transceiver, on detecting the "Exit Sleep Mode" notification from the CPE transceiver (step 99), thereupon exits sleep mode by restoring its state and restoring power. On waking up from sleep mode, the CPE transceiver can begin transmitting immediately or after only a few frames delay, since it need not repeat the initialization that was earlier required to establish the requisite parameters (e.g., frequency and time-domain equalizer coefficients (FDQ; TDQ, echo-canceller coefficients (ECC), transmitter gains; transmission and reception data rates;

transmission and reception coding parameters; transmission fine gains; and Bit Allocation Tables) required for reliable communications. The same is true for the CO transceiver.

The present invention enables rapid resumption of transmissions, whether recovering from a power down or from an enforced idle condition due to temporary unavailability of processor resources in the case of an embedded transceiver, i.e., a transceiver implemented largely software and sharing CPU processing power with the other applications which may from time to time divert CPU resources from the transceiver. In particular, the transceiver of the present invention is capable of recovering full data transmission capabilities within a period of a few frames.

On resuming communication, it may be desirable for the CPE transceiver to transmit several frames of test (known) data (step 100) before resuming transmission of user data. This enables the system to verify that system conditions have not changed so significantly as to require renewed initialization. If the CO transceiver receives these without error, it notifies the CPE transceiver (step 102) and the latter resumes full user data transmission (step 104 and 106). Otherwise, reinitialization must be performed (steps 104 and 108) before user data transmission occurs. A similar procedure may be employed for the transmission by the CO transceiver, and need not be described in further detail.

It will be understood that the order of certain of the steps described above may be changed, and that some steps may be omitted or added. For example, instead of initiating sleep mode at the CPE transceiver as shown in Figure 2, the CO transceiver may initiate sleep mode. In such a case, the flow of notifications will be as shown in Figure 2, but with the positions of CO and CPE transceivers reversed. Further, in some cases it may be desirable to omit the preparatory notifications of steps 82 and 84 and commence entrance into sleep mode as at steps 86 and 88. This will speed entrance into sleep mode, but is more prone to error.

It should also be understood that it is possible, and in various circumstances may be desirable, to operate in a "partial" sleep mode, in which only part of each transceiver is powered down. For example, where data transfer is one-way (when, for example, receiving video at the CPE transceiver from the CO transceiver without any upstream data being sent in return to the CO), the CO receiver and the CPE transmitter may operate in the sleep mode, while the CO transmitter and the CPE receiver are operating in full power mode.

As noted earlier, it is possible to implement major portions of the CPE and CO transceivers in software. In some applications, a dedicated CPU will be used for this purpose; in others, the CPU will be shared with other applications. Even when the sleep mode power conservation procedures described above are not necessary, when the transceivers are implemented in a shared-CPU environment, it may often be necessary to enter an idle mode that is similar to the sleep mode described above in order to maintain synchronization between the transceivers whenever the CPU is unable to service the transceivers. This is accomplished in accordance with the present invention by providing an Interface Transmission Unit (ITU) between the CPU and the data subscriber line which generates an idle indicator whenever the CPU is unavailable for servicing the transceiver which and transmits it to the remote transceiver to maintain the latter in synchronism with the former.

In particular, referring now to Figure 3, an Interface Transmission Unit (ITU) 200 in accordance with the present invention is interposed between a CPU 202 and the data subscriber line 14. nThe unit 200 includes a PCI bus interface 204, a data buffer 206, an analog-to-digital and digital-to-analog converter 208, a controller 210, an idle indicator generator 212, and an analog front end 214.

In normal operation, the CPU passes data and control signals to the ITU 200 via the bus interface unit 204. Data from the CPU that is to be transmitted over the line 14 is stored in the buffer 206 and passed through the digital-to-analog converter portion of unit 208 for application to the line 214 through the analog front end. Conversely, data that is received from the line 14 is passed through the digital-to-analog converter portion of unit 208 to the buffer 206 and thence to the CPU 202 via the interface 204. The CPU processes the data flowing in the different directions in the manner illustrated in connection with Figure 1, i.e., it performs the requisite IFFT and FFT transforms on the data as appropriate. The idle indicator generator may be inactive in this state.

When the CPU must divert its resources elsewhere for servicing applications having higher priority at the moment, the controller 210 activates the idle indicator generator 212 which generates a synchronous idle indicator symbol for transmission to the other transceiver with which the present transceiver is communicating. For example, the CPU may affirmatively notify the controller 210 that this is about to occur. Alternatively, the controller may monitor the buffer

206 and note its filling with data by the CPU has been interrupted for some time period. The idle indicator symbol is preferably of the same duration as a data frame, so that the remote transceiver can process it in the normal manner. However, it must be distinct from any valid data frame so that it can be detected and distinguished without ambiguity. It may comprise a tone, a collection of tones, a collection of tones modulated by bits, with similar of different phases, an inverted sync signal, or even the absence of signal. The CO transceiver responds to receipt of the idle symbol by itself transmitting idling data to the network or other devices with which it is connected so that erroneous data will not be transmitted. When the CPU returns to servicing its associated transceiver, the idle generator suspends operation, preferably on command of the controller 210.

Even when the transceiver is not implemented as part of the shared resources of a CPU, it may nonetheless be beneficial to transmit an idle signal as described above when the transceiver is in sleep mode. This minimizes the likelihood that erroneous data may be emitted, for example, to a network by a CO transceiver when a CPE transceiver with which it is communicating is in sleep mode.

From the foregoing, it 'will be seen that we have provided a multitone transceiver system that capable of operating wholly or partially in a sleep mode, both for purposes of power conservation as well as to accommodate itself to integration with, or incorporation into, computer systems having a power conservation mode. The transceiver system also is adapted to implementation in software under circumstances where the CPU on which the software runs is shared with other applications which may sometimes preempt resources needed for the transceiver.

WHAT IS CLAIMED IS:

1. A multicarrier transceiver having a sleep mode capability, comprising

A. means responsive to a sleep mode command for:

(1) storing selected state parameters characteristic of the communications channel over which the transceiver is operating; and

(2) reducing power to selected portions of transceiver circuitry; and

B. means responsive to a wake-up command for:

(1) restoring power to said transceiver;

(2) restoring the state of said transceiver from said sleep mode by means of said stored parameters; and

C. means for maintaining a common, synchronized data frame count between said transceiver and a remote transceiver with which it communicates, to thereby facilitate restoration of communication without reinitialization of said transceiver.

2. A multicarrier transceiver according to claim 1 in which said state parameters include one or more parameters selected from the group comprising frequency-domain equalizer coefficients, time-domain equalizer coefficients, echo canceller coefficients, bit allocations, coding parameters, fine gains, and subchannel gains.

3. A multicarrier transceiver according to claim 1 in which the means for maintaining said frame count comprises a signal defining a timing reference during at least the time when said first transceiver is in sleep mode.

4. A multicarrier transceiver according to claim 3 in which said signal comprises a pilot tone transmitted from one transceiver to another with which it is in communication.

5. A multicarrier transceiver according to claim 4 in which said pilot tone is transmitted between said transceivers during both normal operation and reduced power operation.

6. A multicarrier transceiver according to claim 1 in which maintaining synchronization includes maintaining synchronization of frame counters between said transceivers.

7. A multi carrier transceiver according to claim 6 in which maintaining synchronization further includes maintaining synchronization of the phase of a synchronizing signal transmitted between said transceivers.

8. A multicarrier transceiver according to claim 1 including means to transmit an idle symbol to said remote transceiver when said transceiver is in sleep mode.

9. A multicarrier transceiver according to claim 1 including means to transmit to said remote transceiver a short test signal on awaking from sleep mode in order to determine whether transmission conditions have changed sufficiently during sleep mode to require reinitialization of said transceiver on emerging from sleep mode.

10. A multicarrier transceiver including

A. mean for storing the state of said transceiver responsive to a state change indicator;

B. means for restoring said state from the stored state parameters to thereby obviate reinitialization of said transceiver on return from sleep mode;

C. means detecting the absence of valid frame information for generating said state change indicator.

11. A multi carrier transceiver including

A. means for storing the state of transceiver responsive to an interruption of valid data transmission;

B. means for entering a sleep mode during said interruption;

C. means for maintaining communication of a synchronizing signal between said transceiver and another transceiver during sleep mode.; and

D. means for restoring said state from the stored state parameters to thereby obviate reinitialization of said transceiver on return from sleep mode.

12. A multicarrier transceiver according to claim 11 in which communication is maintained by transmitting a synchronizing signal to said other transceiver.

13. A multicarrier transceiver according to claim 11 in which communication is maintained by receiving by receiving a synchronizing signal from said other transceiver.

14. A multiracial transceiver according to claim 11 in which said state includes on or more parameters selected from the set comprising frequency-domain equalizer coefficients, time-domain equalizer coefficients, echo cancelled coefficients, bit allocations, coding parameter, fine gains and subchannel gains.

15. A method of providing a sleep mode in a multicarrier transceiver characterized by a plurality of state parameters characteristic of the communications channel over which the transceiver is operating and requiring initialization of said parameters for normal communications, comprising the steps of:

A. storing selected ones of said state parameters in response to a sleep mode command;

B. reducing power to selected portions of the circuitry following said storing;

C. restoring power to said selected portions in response to an awaken signal; and

D. restoring the state of said transceiver from said stored parameters in response to said wakeup signal to thereby obviate reinitialization of said transceiver.

16. A method according to claim 15 in which said selected state-parameters comprise one or more parameters selected from the group comprising frequency-domain equalizer coefficients, time-domain equalizer coefficients, echo-canceller coefficients, bit allocations, coding parameters, fine gains, and subchannel gains.

17. A method according to claim 15 or 16 including the step of maintaining synchronization in said transceiver with a synchronization signal transmitted to said said transceiver during the time that said transceiver is in sleep mode.

ABSTRACT OF THE DISCLOSURE

A multicarrier transceiver is provided with a sleep mode in which it idles with reduced power consumption when it is not needed to transmit or receive data. The full transmission and reception capabilities of the transceiver are quickly restored when needed, without requiring the full (and time-consuming) initialization commonly needed to restore such transceivers to operation after inactivity.

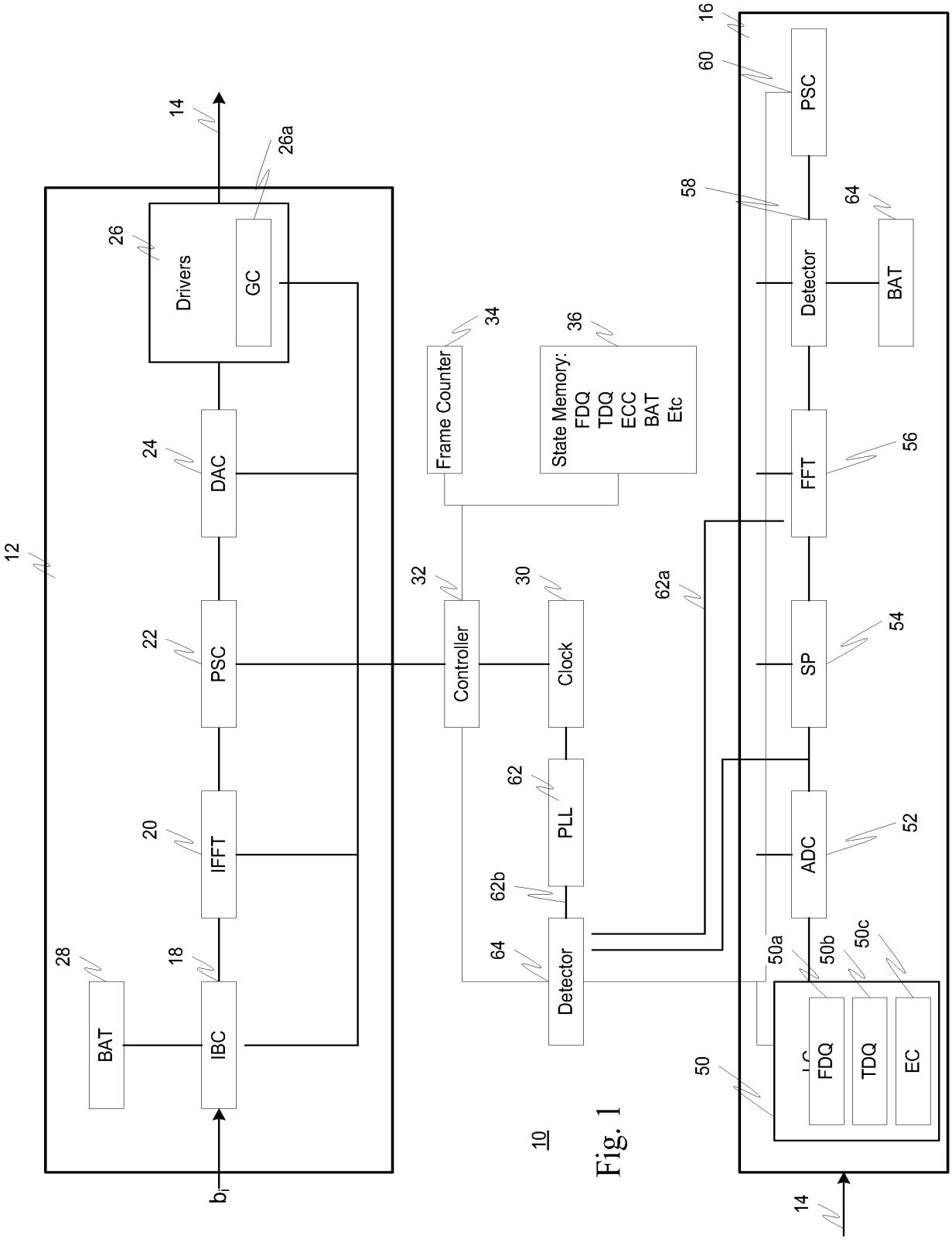
12
14
26a
26
Drivers
GC
24
DAC
22
PSC
20
IFFT
18
IBC
28
BAT
b_i
32
Controller
34
Frame Counter
36
State Memory:
FDQ
TDQ
ECC
BAT
Etc
30
Clock
62
PLL
62b
64
Detector
62a
16
60
PSC
58
Detector
64
BAT
56
FFT
54
SP
52
ADC
50a
50b
50c
50
I/O
FDQ
TDQ
EC
14
10

Fig. 1

Subchannel	Bits
.	.
.	.
50	6
51	6
52	7
.	.
.	.

Fig. 1A

Fig. 1B

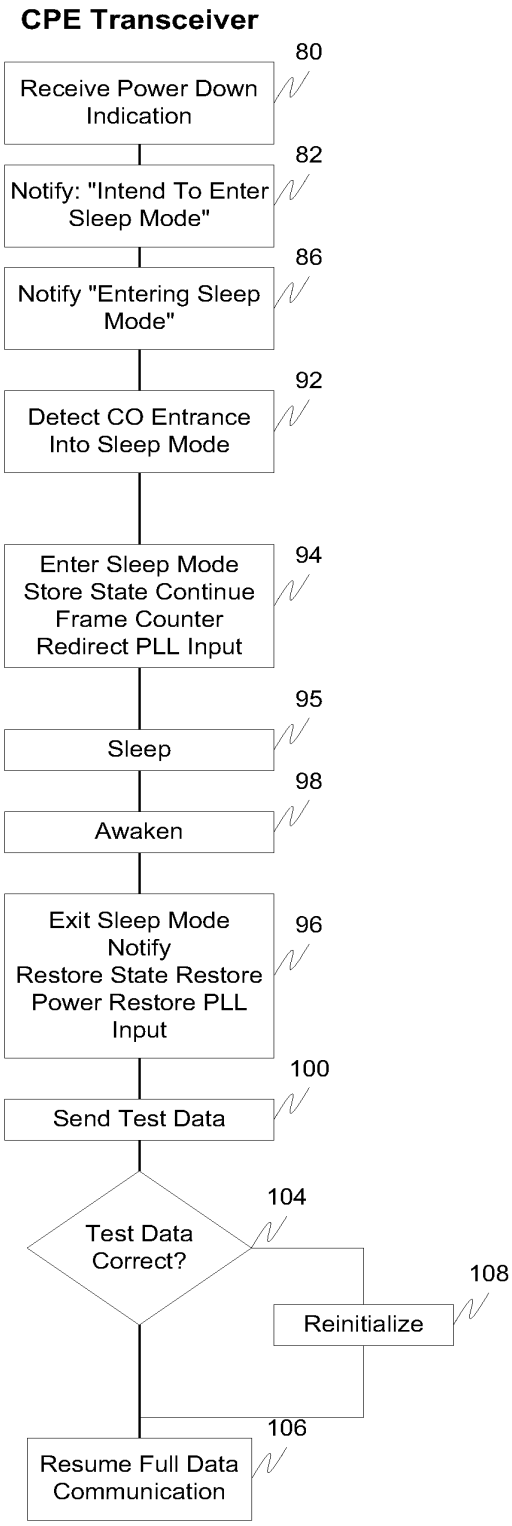
CPE Transceiver
80
Receive Power Down Indication
82
Notify: "Intend To Enter Sleep Mode"
86
Notify "Entering Sleep Mode"
92
Detect CO Entrance Into Sleep Mode
94
Enter Sleep Mode Store State Continue Frame Counter Redirect PLL Input
95
Sleep
98
Awaken
96
Exit Sleep Mode Notify Restore State Restore Power Restore PLL Input
100
Send Test Data
104
Test Data Correct?
108
Reinitialize
106
Resume Full Data Communication
CO Transceiver
84
Notify: Acknowledge Sleep Mode
88
Detect "Entering Sleep Mode" Notify: "Entering Sleep Mode"
90
Enter Sleep Mode Store State Continue Sync Monitor For Exit Reduce Power
97
Sleep
99
Dectect "Exiting Sleep Mode" Exit Sleep Mode Restore State Restore Power Resume Transmission
102
Verify Data
Full Data Communication

Fig. 2

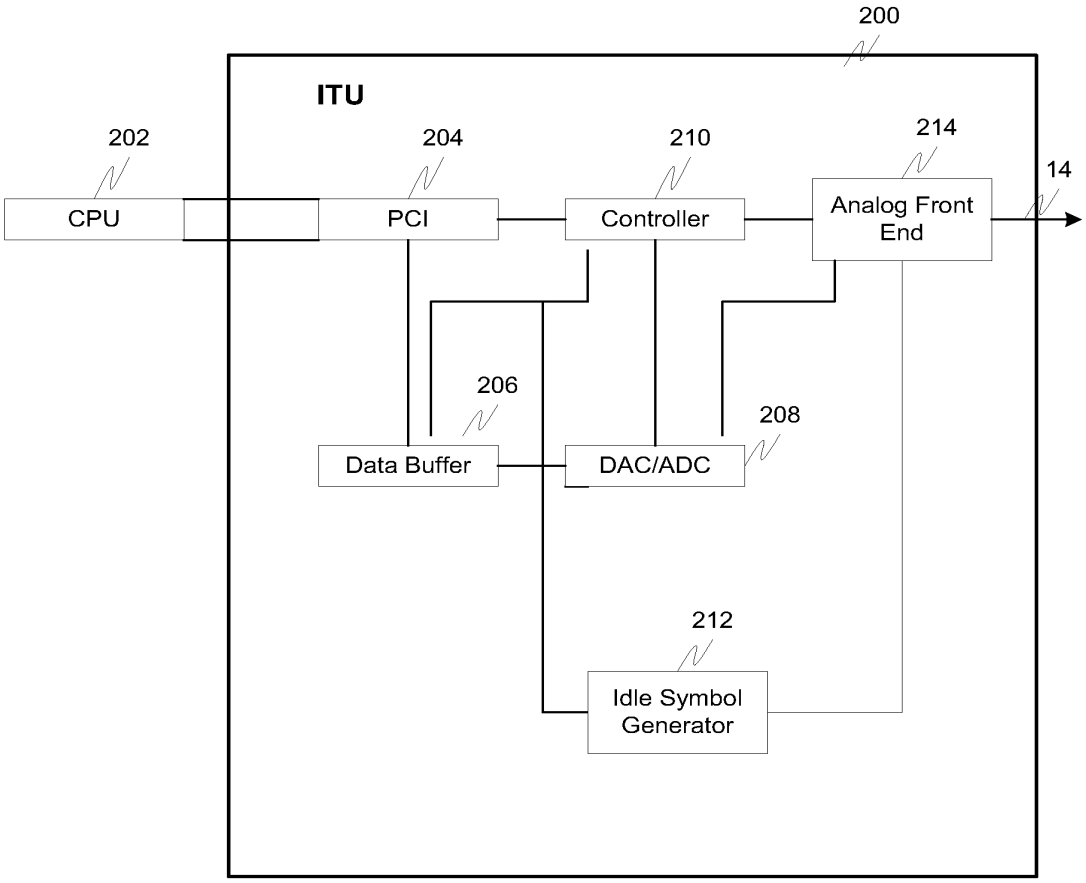
200
ITU
202
204
210
214
14
CPU
PCI
Controller
Analog Front End
206
208
Data Buffer
DAC/ADC
212
Idle Symbol Generator

Fig. 3

MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Application No. 13/152,558, filed June 3, 2011, now U.S. Patent No. 8,437,382, which is a continuation of U.S. Application No. 12/615,946, filed November 10, 2009, now U.S. Patent No. 7,978,753, which is a continuation of U.S. Application No. 11/425,507, filed June 21, 2006, now U.S. Patent No. 7,697,598, which is a continuation of U.S. Application No. 11/289,516, filed November 30, 2005, which is a continuation of U.S. Application No. 11/090,183, filed March 28, 2005, which is a continuation of U.S. Application No. 10/778,083, filed February 17, 2004, which is a continuation of U.S. Application No. 10/175,815, filed June 21, 2002, which is a continuation of U.S. Application No. 09/581,400, filed June 13, 2000, now U.S. Patent No. 6,445,730, which is a 371 of International Application No. PCT/US99/01539, filed January 26, 1999, which claims the benefit of and priority to U.S. Application No. 60/072,447, filed January 26, 1998 entitled "Multicarrier Transmission System with a Low Power Sleep Mode and with Instant-On Capability" each of which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

The invention relates to multicarrier transmission systems, and comprises method and apparatus for establishing a power management sleep state in a multicarrier system.

SUMMARY OF THE INVENTION

~~This application is based on United States Provisional Application Sere No. ***, filed January 26, 1998 by John Greszczuck, Rick Gross and Halil Padir and claims the benefit thereof.~~

Multicarrier transmission systems provide high speed data links between communication points. Such systems have recently been introduced for communications over the local subscriber loop that connects a telephone service subscriber to a central telephone office; in this important application they are commonly referred to as "xDSL" systems, where the "x" specifies a particular variant of DSL (digital subscriber loop) communications, e.g., ADSL (asynchronous digital subscriber loop), HDSL (High-Speed Digital Subscriber Loop), etc. These will be referred to generically herein simply as "DSL" systems.

In such systems, a pair of transceivers communicate with other by dividing the overall bandwidth of the channel interconnecting the subscriber and the central office into a large number of separate subchannels, each of limited bandwidth, operating in parallel with each other. For example, one common system divides thethee subscriber line channel into two hundred and fifty six subchannels, each of 4.3 kilohertz bandwidth. A first group of these (e.g., one hundred ninety six) is allocated to communications from the central office to the subscriber (this is known as the "downstream" direction); a second group (e.g., thirty-two) is allocated to communications from the subscriber to the central office (this is known as the "upstream" direction). The remaining subchannels are allocated to administrative, overhead and control (AOC) functions.

Data to be communicated over the link is divided into groups of bits, one group for each subchannel. The group of bits allocated to a given subchannel is modulated onto a carrier whose frequency is specific to that channel. Typically, quadrature amplitude modulation (QAM) is used for this purpose, and the group of bits is mapped into a vector defined by one of the points of a "constellation" which specifies the allowable data points for transmission over that subchannel at a particular time. Each vector or data point thus comprises a unique symbol representing a specific bit configuration for transmission as a group over its associated subchannel. During the time period allocated for transmission of a symbol (commonly referred to as a "symbol period" or "frame"), each subchannel transmits its symbol in parallel with all other subchannels so that large amounts of data can be transmitted during each frame.

The number of bits carried by a symbol is dependent on the characteristics of the subchannel over which it is to be transmitted. This may vary from one subchannel to another. The principal determinant is the signal-to-noise ratio of theoft-he subchannel. Accordingly, this

parameter is measured from time to time in order to ascertain its value for each subchannel, and thus determine the number of bits to be transmitted on the particular subchannel at a given time.

The telephone channel is subject to a number of impairments which must be compensated for in order to ensure reliable transmission. Phase (delay) distortion of the transmitted signal is typically the most limiting of these impairments. This distortion is frequency-dependent, and thus components of a signal at different frequencies are shifted by varying amounts, thereby distorting the signal and increasing the likelihood of erroneous detection unless provision is made to combat it. To this end, frequency domain equalizers (FDQ) and time domain equalizers (TDQ) are commonly incorporated into the transmission channel in order to equalize the phase (time) delay across the channel frequency band. Other impairments also exist. For example, frequency-dependent signal attenuation adversely affects signal transmission on the telephone line. This is compensated by the use of gain equalizers on the line, while echo on the line is handled by the use of echo cancellers.

The problem of signal impairment is especially serious in those xDSL configurations which carry the DSL communications on a common line with ordinary voice communications but which omit the use of a "splitter" at either the subscriber premises the central office or both. A "splitter" is basically a filter which separates the low-frequency voice communications (e.g., from zero to four kilohertz) from the higher frequency data communications (which may extend up into the megahertz band) and provides a strong degree of isolation between the two. In the absence of a splitter, unique provisions must be made to accommodate voice and data communications on the same line. For a more detailed description of the problem and its solution, see the co-pending application of Richard Gross et al. entitled "Splitterless Multicarrier Modem", Serial No. PCT/US98 21442, filed October 9, 1998, and assigned to the assignee of the present invention, the disclosure of which is incorporated herein by reference.

Because of their extensive use in Internet communications as well as in other applications, DSL transceivers are commonly maintained in the "on" state, ready to transmit or receive once they have been installed and initialized. Thus, such modems consume a significant amount of power, even when they are not actively transmitting or receiving data. It is generally desirable to limit this power consumption, both for environmental reasons as well as to prolong the life of the equipment. Further, such modems may be implemented or incorporated in part or

in whole in computer equipment such as in personal computers for home and business use, and such computers increasingly incorporate power conservation procedures. See, for example, U.S. Patent No. 5,428,790, "Computer Power Management System", issued June 27, 1995 on the application of L. D. Harper. Thus, it is desirable to provide an ADSL modem which can accommodate power conservation procedures in equipment with which it is associated, as well as independently of such equipment as may be appropriate.

Because of the complexity of DSL transceivers, and the conditions under which they must operate, it is necessary to initialize them prior to the transmission and reception of data. This initialization includes, *inter alia,* channel corrections such as "training" the frequency-domain and time-domain equalizers and the echo cancellers; setting the channel gains; negotiating the transmission and reception data rates; adjusting the fine gains on the subchannels over which communication is to take place; setting the coding parameters; and the like. Additionally, it includes measuring the signal-to-noise ratio of each of the subchannels, calculating the bit-allocation tables characteristic of each under given conditions of transmission, and exchanging these tables with other modems with which a given modem communicates. For more detailed discussion of these procedures, refer to the application of Richard Gross et al., cited above and incorporated herein by reference. These procedures can require from seconds to tens of seconds. In a new installation, the time required is inconsequential. However, in an already-operating installation, the time required to initialize or re-initialize the system after a suspension of operation in connection with power conservation is generally unacceptable, since it is typically desired to have the modem respond to request for service nearly instantaneously.

Accordingly, it is an object of the invention to provide a multicarrier transmission system having a low power sleep mode and a rapid-on capability.

Further, it is an object of the invention to provide a multicarrier transmission system for use in digital subscriber line communications that can rapidly switch from a sleep mode to a full-on condition.

Still another object of the invention is to provide a DSL system that can readily be integrated into a computer having a low power sleep mode and which is capable of rapid return to full operation.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention description below refers to the accompanying drawings, of which:

Figure 1 is a block and line diagram of a multicarrier transmission system in accordance with a preferred embodiment of the present invention;

Figure 1A is a portion of an exemplary chart showing a possible bit distribution among subchannels;

Figure 1B illustrates a timing signal used in accordance with the invention;

Figure 2 is a flow diagram of the operation of the present invention; and

Figure 3 is a block and line diagram of still another aspect of the present invention.

DETAILED DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

For purposes of explanation, the present invention will be described in the context of an ADSL system having a first transceiver located at the site of a customer's premises (referred to hereinafter as the "CPE transceiver") and a second transceiver located at a local central telephone office (hereinafter referred to as the "CO transceiver"). The two are interconnected for communication by means of a common telephone line over which voice and data are to be transmitted, and the CO transceiver is commonly connected into a broader network such as the Internet to and from which data is to be communicated. The system will be described as using Fourier transform technology for modulation and demodulation of the data to be transmitted. It will be understood, however, that the invention is not limited to this environment, and is applicable to point-to-point communications is other environments, and with other forms of modulation/demodulation. Further, since the CPE transceiver and CO transceiver are very similar, the invention will be explained in connection with a detailed illustration of the CPE transceiver only.

In Figure 1, a DSL transceiver 10 in accordance with the present invention has a transmitter section 12 for transmitting data over a digital subscriber line 14 and a receiver section 16 for receiving data from the line. The transmitter section 12 is formed from an input buffer and converter (IBC) 18 that receives a serial string of data (e.g., binary digits) b_i to be

transmitted and converts the data into a plurality of pairs of complex-valued symbols X_i and their conjugates $X_{N-i} = X^*_i$, i = 0, 1, ...N. Typically, the buffer 18 holds at least a frame of data (a frame comprising the amount of data to be transmitted during one symbol period). The pairs of symbols X_i and X^*_i are applied to an Inverse Fast Fourier Transform (IFFT) 20 to provide real time output signals X_j, j = 0, 1, ...N/2 -1. The latter in turn are converted to serial form in a parallel-to-serial convener (PSC) 22 and then applied to a digital-to-analog converter (DAC) 24 for application to a line driver 26. The converter 24 may apply a cyclic prefix to the signals X_j to combat intersymbol interference caused by the transmission medium. The driver 26 may incorporate a gain control section (GC) 26a for controlling the signal amplitude (and thus power) as it is applied to a communication channel such as the digital subscriber line 14.

IFFT 20 may be viewed as a data modulator. The symbols X_i , and their conjugates $X_{N-i,}$ correspond to data points defining signal vectors in a quadrature amplitude modulation (QAM) constellation set. The converter 18 forms the respective symbols from the input data with the aid of a bit allocation table (BAT) 28 which specifies, for each subchannel, the number of bits to be carried by the symbol transmitted over that subchannel, and thus defines the data point to be associated with the symbol. This table is typically calculated at the transceiver and is transmitted to other transceivers with which the instant transceiver communicates, to thereby enable them to decode the symbols received by them from the instant transceiver.

The number of bits which each symbol carries is determined by the characteristics of the subchannel over which the symbol is to be transmitted, and particularly by the signal-to-noise ratio of the subchannelsubcbannel. Procedures for this calculation are known. Figure lA shows an example of such a table as formed and stored at transceiver 10. Thus, the symbol to be transmitted over subchannel 50 may be determined to have an allocation of six bits; that of subchannel 51, six bits; that of subchannel 52, seven bits, etc.

A Clock 30 controls the timing of the operation of the transmitter 12. It supplies input to a Controller 32 which controls the individual units of the transmitter. In the case of the CO transceiver, the clock 30 typically is a master clock to which a remote transceiver, such as at a subscriber premises, will be synchronized. In the case of a transceiver at the subscriber premises, such as is shown here for purposes of illustration, the clock is derived from the master

clock at the central office as described more fully below in connection with the receiver portion of the transceiver.

A Frame Counter (FC) 24 connected to the controller 32 maintains a count of the number of frames of data transmitted from or received by the transceiver 10. The clock 30 maintains the count in counter 34 synchronous with that of a corresponding counter (not shown) in the CO transceiver. In DSL systems, typically, data is communicated in the form of a sequence of data frames (e.g., sixty-eight frames for ADSL as specified in ITU Document G.992.2), followed by a synchronization frame, each frame having a duration of one symbol period of approximately two hundred and fifty microseconds. Together, the sixty-nine frames comprise a "superframe". Thus, the counter 34 typically maintains a count modulo sixty-nine. Finally, a State Memory (SM) 36 connected to the controller 32 records the state of the transceiver for reasons discussed more fully below.

Turning now to the receiver section 16, it is formed from a line conditioner (LC) 50; an analog-to-digital converter (ADC) 52; a serial-to-parallel converter 54; a Fast Fourier Transform (FFT) section 56; a decoder 58; and a parallel-to-serial converter 60. The conditioner 50 compensates for transmission distortions introduced by the line 14, and commonly includes a frequency-domain equalizer (FDQ) 50a; a time-domain equalizer (TDQ) 50b; and an echo canceller (EC) 50c, among other elements. The ADC 52 converts the received signal to digital form and applies it to the serial-to-parallel converter 54. The converter 54 removes any cyclic prefix that may have been appended to the signal before it was transmitted, and applies the resultant signal to the FFT 56 which effectively "demodulates" the received signal. The output of the FFT is applied to decoder 58 which, in conjunction with a bit-allocation-table 6462, recovers the symbols X_i and X^*_{-i} and the bits associated with them. The output of detector 58 is applied to the parallel-to-serial converter 60 which restores the data stream, b_i, that was originally applied to the transmitter. The controller 32 also controls the operation of the receiver portion 16 of the transceiver 10.

During normal (non-sleep mode) operation, a phase-lock loop (PLL) 62 receives from the FFT 56 a timing reference signal 62a (see Figure lA) via a line 62b. The timing reference signal 62a is transmitted from the transmitter with which the receiver 16 communicates (e.g., the CO transmitter). This signal is advantageously a pure tone of fixed frequency and phase which is

synchronized with the Master Clock in the transmitter; its frequency defines the frame rate of the transceivers. Other forms of timing signal may, of course, be used, but use of a pure tone has the advantage of simplicity and reliability even when portions of the transceiver are powered down in accordance with the invention. The PLL 62 locks itself to this signal and drives clock 30 in synchronism with the Master Clock in the driving transmitter. This also synchronizes frame counter 34 of the CPE transceiver to the corresponding frame counter of the CO transceiver. Control of the receiver section is provided by the controller 32.

In the sleep mode, the FFT 56 is preferably dormant. Accordingly, the timing reference signal for PLL 62 is provided from the output of the analog to digital convener 52 via a detector 64 which extracts the timing signal from the signal appearing on line 14 during sleep mode, by calculating the DFT of the synchronizing pilot tone. Controller 32 controls the switching of the input to PLL 62 between these two sources so that the PLL 62 remains locked to the CO transceiver timing reference.

As noted earlier, the transceiver of the present invention will commonly be incorporated in a computer such as a personal computer; indeed, it may be implemented as an integral part of such a computer, which may have a power conservation capability for activation when the computer is not in active operation. It is thus desirable that the transceiver be able to suspend operations and enter a "sleep" mode in which it consumes reduced power when it is not needed for data transmission or reception, but nonetheless be able to resume transmission or reception almost instantaneously, e.g., within a few frames.

Further, when the ADSL transceiver is implemented as an integral part of a computer, it may often be the case that the processing power of the computer is, at a given moment, devoted to another task such as graphics, word processing, and the like, and is thus unable to service the transceiver. In such circumstances, it is possible that a frame that is assembled for transmission to the CO transceiver, and thence to some network connected to it, is incomplete, and thus would generate errors if transmitted. Accordingly, the transceiver of the present invention is responsive to such conditions by entering an "idle" state in which it ceases active transmission of data while the computer is elsewhere occupied. This state is similar in many ways to the sleep mode state although, of course, its purpose is not power conservation, and thus in the idle state the power to selected portions of the transceiver may, but need not, be reduced. The idle state maintains

synchronous signaling between the CPE and CO transceivers but no data is transmitted. On receipt of the idle indicator from the CPE, the CO transceiver transmits idle cells to the network to maintain connection with the network.

Referring now more particularly to Figure 2, the power down operation of the CPE transceiver begins on receipt of a power down indication (step 80) by the CPE transceiver controller 32. The power down indication may be applied to the controller 32 from an external source such as a personal computer in which the transceiver is included; it may be generated within the transceiver itself as a result of monitoring the input buffer 18 and determining that no data has been applied to it for a given time interval or that the buffer has not been filled despite passage of a symbol time; it may be responsive to a power down command from the CO transceiver; or it may be generated in response to other conditions.

Considering for the moment the first two cases, the CPE transceiver responds to the indication by transmitting to the CO transceiver an "Intend To Enter Sleep Mode" notification (step 82). This notification indicates that the transceiver is about to undergo a change of state, and may take any of a variety of forms; preferably it is a message, but may also comprise a tone, an inverted sync signal, a flag, or even the cessation of data transmission itself. The notification may advantageously be transmitted over one of the embedded operations channels of the system. It provides the CO transceiver an opportunity to prepare itself to enter sleep mode, and also to signal the CPE transceiver if entrance into sleep mode is not appropriate or desirable at the particular moment.

If entrance into sleep mode is permissible at this time; the CO transceiver responds to the power down or idle signal by transmitting an "Acknowledge Sleep Mode" notification (step 84) to the CPE transceiver. This and subsequent notifications described in connection with the sleep or idle mode may similarly take any of a variety of forms such as described above for the "Intend To Enter Sleep Mode" notification, but again preferably is in the form of a message transmitted over an embedded operations channel.

After it has received acknowledgment from the CO transceiver, the CPE transceiver transmits an "Entering Sleep Mode" notification (step 86) to the CO transceiver and ceases transmission, either immediately or after a given number of frames. The CO transceiver detects this notification; transmits its own "Entering Sleep Mode" notification (step 88); and enters sleep

mode (step 90). In pursuance of this, the CO transceiver stores its state in its own state memory corresponding to the state memory 36~~38~~ of CPE transceiver 10. The state of the CO or CPE transceivers preferably includes at least the frequency and time-domain equalizer coefficients (FDQ; TDQ) and the echo-canceller coefficients (ECC) of its receiver portion and the gain of its transmitter portion; the transmission and reception data rates; the transmission and reception coding parameters; the transmission fine gains; and the Bit Allocation Tables. The CO transceiver continues to advance the frame count and superframe count during the period of power-down in order to ensure synchrony with the remote CPE transceiver when communications are resumed. In order to maintain synchronization during the power down or idle state, the CO transceiver continues to transmit to the CPE transceiver the synchronizing pilot tone 62a. It may, at this time, perform its own power reduction. In particular, it may reduce or cut off power to the digital modulator/demodulator portions of its transmitter and receiver sections (corresponding to the IFFT 20 and FFT 56 of the CPE transceiver, Fig. 1); this provides a significant power reduction. Further, it may reduce power to parts of the analog circuitry. Power will be maintained, of course, to at least that portion of the analog driver circuitry which transmits the pilot tone and other control signals to the CPE transceiver, and to line circuits required to monitor the line 14 for signals from the CPE transceiver.

In a central office, the rest of the equipment is still operating, and while the link between the CO transceiver and the CPE transceiver is in a sleep state, user data provided by the CO transceiver will be benign idle data such as ATM IdleCells~~Idle Cells~~ or HDLC Flag octets, and not generate false data errors to other equipment.

In response to the "Entering Sleep Mode" notification from the CO transceiver, the CPE transceiver enters the sleep mode (step 92). In particular, it stores its state (step 94) in state memory 38; as noted above in connection with the CO transceiver, this includes preferably at least the frequency and time-domain equalizer coefficients (FDQ; TDQ) and the echo-canceller coefficients (ECC) of its receiver and the gain of its transmitter; the transmission and reception data rates; the transmission and reception coding parameters; the transmission fine gains; and the Bit Allocation Tables. The phase and frequency offset of the phase-locked loop 62 is maintained by continued operation of the loop. The CPE transceiver 10 then reduces power to the digital modulator/demodulator circuitry comprising IFFT 20 and FFT 56, as well as to and transmitter

data line drivers 26. However, it continues to advance the frame counter 34 in accordance with the received synchronizing signal 62a. However, the CPE controller 32 now causes this signal to be applied to the PLL 62 from the output of the ADC 52 (Fig. 1) via the detector 64, which implements the DFT of a single tone, instead of directly from the output of the FFT 56 as was previously the case. This enables the FFT 56 to be powered down. The CPE and CO transceivers then operate in sleep mode (steps 95 and 97, respectively) until they awaken.

During the sleep mode state, the CO transceiver continues to monitor (step 90) the data subscriber line 14 for an "Exiting Sleep Mode" signal from the CPE transceiver (step 96). The CPE transceiver transmits this signal when its controller receives an "Awaken" indication (step 98) from an external source such as a computer in which it is installed or from other sources, or when its controller detects the presence of new data in the input buffer 18. In response to the "Awaken" signal, the CPE transceiver retrieves its stored state from the state memory 38; restores full power to its circuitry; and restores the output of the FFT 56 to the input of the PLL 62 (step 96). The CO transceiver, on detecting the "Exit Sleep Mode" notification from the CPE transceiver (step 99), thereupon exits sleep mode by restoring its state and restoring power. On waking up from sleep mode, the CPE transceiver can begin transmitting immediately or after only a few frames delay, since it need not repeat the initialization that was earlier required to establish the requisite parameters (e.g., frequency and time-domain equalizer coefficients (FDQ; TDQ, echo-canceller coefficients (ECC), transmitter gains; transmission and reception data rates; transmission and reception coding parameters; transmission fine gains; and Bit Allocation Tables) required for reliable communications. The same is true for the CO transceiver.

The present invention enables rapid resumption of transmissions, whether recovering from a power down or from an enforced idle condition due to temporary unavailability of processor resources in the case of an embedded transceiver, i.e., a transceiver implemented largely software and sharing CPU processing power with the other applications which may from time to time divert CPU resources from the transceiver. In particular, the transceiver of the present invention is capable of recovering full data transmission capabilities within a period of a few frames.

On resuming communication, it may be desirable for the CPE transceiver to transmit several frames of test (known) data (step 100) before resuming transmission of user data. This

enables the system to verify that system conditions have not changed so significantly as to require renewed initialization. If the CO transceiver receives these without error, it notifies the CPE transceiver (step 102) and the latter resumes full user data transmission (step 104 and 106). Otherwise, reinitialization must be performed (steps 104 and 108) before user data transmission occurs. A similar procedure may be employed for the transmission by the CO transceiver, and need not be described in further detail.

It will be understood that the order of certain of the steps described above may be changed, and that some steps may be omitted or added. For example, instead of initiating sleep mode at the CPE transceiver as shown in Figure 2, the CO transceiver may initiate sleep mode. In such a case, the flow of notifications will be as shown in Figure 2, but with the positions of CO and CPE transceivers reversed. Further, in some cases it may be desirable to omit the preparatory notifications of steps 82 and 84 and commence entrance into sleep mode as at steps 86 and 88. This will speed entrance into sleep mode, but is more prone to error.

It should also be understood that it is possible, and in various circumstances may be desirable, to operate in a "partial" sleep mode, in which only part of each transceiver is powered down. For example, where data transfer is one-way (when, for example, receiving video at the CPE transceiver from the CO transceiver without any upstream data being sent in return to the CO), the CO receiver and the CPE transmitter may operate in the sleep mode, while the CO transmitter and the CPE receiver are operating in full power mode.

As noted earlier, it is possible to implement major portions of the CPE and CO transceivers in software. In some applications, a dedicated CPU will be used for this purpose; in others, the CPU will be shared with other applications. Even when the sleep mode power conservation procedures described above are not necessary, when the transceivers are implemented in a shared-CPU environment, it may often be necessary to enter an idle mode that is similar to the sleep mode described above in order to maintain synchronization between the transceivers whenever the CPU is unable to service the transceivers. This is accomplished in accordance with the present invention by providing an Interface Transmission Unit (ITU) between the CPU and the data subscriber line which generates an idle indicator whenever the CPU is unavailable for servicing the transceiver which and transmits it to the remote transceiver to maintain the latter in synchronism with the former.

In particular, referring now to Figure 3, an Interface Transmission Unit (ITU) 200 in accordance with the present invention is interposed between a CPU 202 and the data subscriber line 14. ~~The~~The unit 200 includes a PCI bus interface 204, a data buffer 206, an analog-to-digital and digital-to-analog converter 208, a controller 210, an idle indicator generator 212, and an analog front end 214.

In normal operation, the CPU passes data and control signals to the ITU 200 via the bus interface unit 204. Data from the CPU that is to be transmitted over the line 14 is stored in the buffer 206 and passed through the digital-to-analog converter portion of unit 208 for application to the line 214 through the analog front end. Conversely, data that is received from the line 14 is passed through the digital-to-analog converter portion of unit 208 to the buffer 206 and thence to the CPU 202 via the interface 204. The CPU processes the data flowing in the different directions in the manner illustrated in connection with Figure 1, i.e., it performs the requisite IFFT and FFT transforms on the data as appropriate. The idle indicator generator 212 may be inactive in this state.

When the CPU must divert its resources elsewhere for servicing applications having higher priority at the moment, the controller 210 activates the idle indicator generator 212 which generates a synchronous idle indicator symbol for transmission to the other transceiver with which the present transceiver is communicating. For example, the CPU may affirmatively notify the controller 210 that this is about to occur. Alternatively, the controller may monitor the buffer 206 and note its filling with data by the CPU has been interrupted for some time period. The idle indicator symbol is preferably of the same duration as a data frame, so that the remote transceiver can process it in the normal manner. However, it must be distinct from any valid data frame so that it can be detected and distinguished without ambiguity. It may comprise a tone, a collection of tones, a collection of tones modulated by bits, with similar of different phases, an inverted sync signal, or even the absence of signal. The CO transceiver responds to receipt of the idle symbol by itself transmitting idling data to the network or other devices with which it is connected so that erroneous data will not be transmitted. When the CPU returns to servicing its associated transceiver, the idle generator 212 suspends operation, preferably on command of the controller 210.

Even when the transceiver is not implemented as part of the shared resources of a CPU, it may nonetheless be beneficial to transmit an idle signal as described above when the transceiver is in sleep mode. This minimizes the likelihood that erroneous data may be emitted, for example, to a network by a CO transceiver when a CPE transceiver with which it is communicating is in sleep mode.

From the foregoing, it 'will be seen that we have provided a multitone transceiver system that capable of operating wholly or partially in a sleep mode, both for purposes of power conservation as well as to accommodate itself to integration with, or incorporation into, computer systems having a power conservation mode. The transceiver system also is adapted to implementation in software under circumstances where the CPU on which the software runs is shared with other applications which may sometimes preempt resources needed for the transceiver.

ABSTRACT OF THE DISCLOSURE

A multicarrier transceiver is provided with a sleep mode in which it idles with reduced power consumption when it is not needed to transmit or receive data. The full transmission and reception capabilities of the transceiver are quickly restored when needed, without requiring the full (and time-consuming) initialization commonly needed to restore such transceivers to operation after inactivity.

MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Application No. 13/152,558, filed June 3, 2011, now U.S. Patent No. 8,437,382, which is a continuation of U.S. Application No. 12/615,946, filed November 10, 2009, now U.S. Patent No. 7,978,753, which is a continuation of U.S. Application No. 11/425,507, filed June 21, 2006, now U.S. Patent No. 7,697,598, which is a continuation of U.S. Application No. 11/289,516, filed November 30, 2005, which is a continuation of U.S. Application No. 11/090,183, filed March 28, 2005, which is a continuation of U.S. Application No. 10/778,083, filed February 17, 2004, which is a continuation of U.S. Application No. 10/175,815, filed June 21, 2002, which is a continuation of U.S. Application No. 09/581,400, filed June 13, 2000, now U.S. Patent No. 6,445,730, which is a 371 of International Application No. PCT/US99/01539, filed January 26, 1999, which claims the benefit of and priority to U.S. Application No. 60/072,447, filed January 26, 1998 entitled "Multicarrier Transmission System with a Low Power Sleep Mode and with Instant-On Capability" each of which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

The invention relates to multicarrier transmission systems, and comprises method and apparatus for establishing a power management sleep state in a multicarrier system.

SUMMARY OF THE INVENTION

Multicarrier transmission systems provide high speed data links between communication points. Such systems have recently been introduced for communications over the local subscriber loop that connects a telephone service subscriber to a central telephone office; in this important application they are commonly referred to as "xDSL" systems, where the "x" specifies

a particular variant of DSL (digital subscriber loop) communications, e.g., ADSL (asynchronous digital subscriber loop), HDSL (High-Speed Digital Subscriber Loop), etc. These will be referred to generically herein simply as "DSL" systems.

In such systems, a pair of transceivers communicate with other by dividing the overall bandwidth of the channel interconnecting the subscriber and the central office into a large number of separate subchannels, each of limited bandwidth, operating in parallel with each other. For example, one common system divides the subscriber line channel into two hundred and fifty six subchannels, each of 4.3 kilohertz bandwidth. A first group of these (e.g., one hundred ninety six) is allocated to communications from the central office to the subscriber (this is known as the "downstream" direction); a second group (e.g., thirty-two) is allocated to communications from the subscriber to the central office (this is known as the "upstream" direction). The remaining subchannels are allocated to administrative, overhead and control (AOC) functions.

Data to be communicated over the link is divided into groups of bits, one group for each subchannel. The group of bits allocated to a given subchannel is modulated onto a carrier whose frequency is specific to that channel. Typically, quadrature amplitude modulation (QAM) is used for this purpose, and the group of bits is mapped into a vector defined by one of the points of a "constellation" which specifies the allowable data points for transmission over that subchannel at a particular time. Each vector or data point thus comprises a unique symbol representing a specific bit configuration for transmission as a group over its associated subchannel. During the time period allocated for transmission of a symbol (commonly referred to as a "symbol period" or "frame"), each subchannel transmits its symbol in parallel with all other subchannels so that large amounts of data can be transmitted during each frame.

The number of bits carried by a symbol is dependent on the characteristics of the subchannel over which it is to be transmitted. This may vary from one subchannel to another. The principal determinant is the signal-to-noise ratio of the subchannel. Accordingly, this parameter is measured from time to time in order to ascertain its value for each subchannel, and thus determine the number of bits to be transmitted on the particular subchannel at a given time.

The telephone channel is subject to a number of impairments which must be compensated for in order to ensure reliable transmission. Phase (delay) distortion of the transmitted signal is typically the most limiting of these impairments. This distortion is frequency-dependent, and

thus components of a signal at different frequencies are shifted by varying amounts, thereby distorting the signal and increasing the likelihood of erroneous detection unless provision is made to combat it. To this end, frequency domain equalizers (FDQ) and time domain equalizers (TDQ) are commonly incorporated into the transmission channel in order to equalize the phase (time) delay across the channel frequency band. Other impairments also exist. For example, frequency-dependent signal attenuation adversely affects signal transmission on the telephone line. This is compensated by the use of gain equalizers on the line, while echo on the line is handled by the use of echo cancellers.

The problem of signal impairment is especially serious in those xDSL configurations which carry the DSL communications on a common line with ordinary voice communications but which omit the use of a "splitter" at either the subscriber premises the central office or both. A "splitter" is basically a filter which separates the low-frequency voice communications (e.g., from zero to four kilohertz) from the higher frequency data communications (which may extend up into the megahertz band) and provides a strong degree of isolation between the two. In the absence of a splitter, unique provisions must be made to accommodate voice and data communications on the same line. For a more detailed description of the problem and its solution, see the co-pending application of Richard Gross et al. entitled "Splitterless Multicarrier Modem", Serial No. PCT/US98 21442, filed October 9, 1998, and assigned to the assignee of the present invention, the disclosure of which is incorporated herein by reference.

Because of their extensive use in Internet communications as well as in other applications, DSL transceivers are commonly maintained in the "on" state, ready to transmit or receive once they have been installed and initialized. Thus, such modems consume a significant amount of power, even when they are not actively transmitting or receiving data. It is generally desirable to limit this power consumption, both for environmental reasons as well as to prolong the life of the equipment. Further, such modems may be implemented or incorporated in part or in whole in computer equipment such as in personal computers for home and business use, and such computers increasingly incorporate power conservation procedures. See, for example, U.S. Patent No. 5,428,790, "Computer Power Management System", issued June 27, 1995 on the application of L. D. Harper. Thus, it is desirable to provide an ADSL modem which can

accommodate power conservation procedures in equipment with which it is associated, as well as independently of such equipment as may be appropriate.

Because of the complexity of DSL transceivers, and the conditions under which they must operate, it is necessary to initialize them prior to the transmission and reception of data. This initialization includes, *inter alia,* channel corrections such as "training" the frequency-domain and time-domain equalizers and the echo cancellers; setting the channel gains; negotiating the transmission and reception data rates; adjusting the fine gains on the subchannels over which communication is to take place; setting the coding parameters; and the like. Additionally, it includes measuring the signal-to-noise ratio of each of the subchannels, calculating the bit-allocation tables characteristic of each under given conditions of transmission, and exchanging these tables with other modems with which a given modem communicates. For more detailed discussion of these procedures, refer to the application of Richard Gross et al., cited above and incorporated herein by reference. These procedures can require from seconds to tens of seconds. In a new installation, the time required is inconsequential. However, in an already-operating installation, the time required to initialize or re-initialize the system after a suspension of operation in connection with power conservation is generally unacceptable, since it is typically desired to have the modem respond to request for service nearly instantaneously.

Accordingly, it is an object of the invention to provide a multicarrier transmission system having a low power sleep mode and a rapid-on capability.

Further, it is an object of the invention to provide a multicarrier transmission system for use in digital subscriber line communications that can rapidly switch from a sleep mode to a full-on condition.

Still another object of the invention is to provide a DSL system that can readily be integrated into a computer having a low power sleep mode and which is capable of rapid return to full operation.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention description below refers to the accompanying drawings, of which:

Figure 1 is a block and line diagram of a multicarrier transmission system in accordance with a preferred embodiment of the present invention;

Figure 1A is a portion of an exemplary chart showing a possible bit distribution among subchannels;

Figure 1B illustrates a timing signal used in accordance with the invention;

Figure 2 is a flow diagram of the operation of the present invention; and

Figure 3 is a block and line diagram of still another aspect of the present invention.

DETAILED DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

For purposes of explanation, the present invention will be described in the context of an ADSL system having a first transceiver located at the site of a customer's premises (referred to hereinafter as the "CPE transceiver") and a second transceiver located at a local central telephone office (hereinafter referred to as the "CO transceiver"). The two are interconnected for communication by means of a common telephone line over which voice and data are to be transmitted, and the CO transceiver is commonly connected into a broader network such as the Internet to and from which data is to be communicated. The system will be described as using Fourier transform technology for modulation and demodulation of the data to be transmitted. It will be understood, however, that the invention is not limited to this environment, and is applicable to point-to-point communications is other environments, and with other forms of modulation/demodulation. Further, since the CPE transceiver and CO transceiver are very similar, the invention will be explained in connection with a detailed illustration of the CPE transceiver only.

In Figure 1, a DSL transceiver 10 in accordance with the present invention has a transmitter section 12 for transmitting data over a digital subscriber line 14 and a receiver section 16 for receiving data from the line. The transmitter section 12 is formed from an input buffer and converter (IBC) 18 that receives a serial string of data (e.g., binary digits) b_i to be transmitted and converts the data into a plurality of pairs of complex-valued symbols X_i and their conjugates $X_{N-i} = X^*_i$, i = 0, 1, ...N. Typically, the buffer 18 holds at least a frame of data (a frame comprising the amount of data to be transmitted during one symbol period). The pairs of

symbols X_i and X^*_i are applied to an Inverse Fast Fourier Transform (IFFT) 20 to provide real time output signals X_j, j = 0, 1, ...N/2 -1. The latter in turn are converted to serial form in a parallel-to-serial convener (PSC) 22 and then applied to a digital-to-analog converter (DAC) 24 for application to a line driver 26. The converter 24 may apply a cyclic prefix to the signals X_j to combat intersymbol interference caused by the transmission medium. The driver 26 may incorporate a gain control section (GC) 26a for controlling the signal amplitude (and thus power) as it is applied to a communication channel such as the digital subscriber line 14.

IFFT 20 may be viewed as a data modulator. The symbols X_i , and their conjugates $X_{N-i,}$ correspond to data points defining signal vectors in a quadrature amplitude modulation (QAM) constellation set. The converter 18 forms the respective symbols from the input data with the aid of a bit allocation table (BAT) 28 which specifies, for each subchannel, the number of bits to be carried by the symbol transmitted over that subchannel, and thus defines the data point to be associated with the symbol. This table is typically calculated at the transceiver and is transmitted to other transceivers with which the instant transceiver communicates, to thereby enable them to decode the symbols received by them from the instant transceiver.

The number of bits which each symbol carries is determined by the characteristics of the subchannel over which the symbol is to be transmitted, and particularly by the signal-to-noise ratio of the subchannel. Procedures for this calculation are known. Figure lA shows an example of such a table as formed and stored at transceiver 10. Thus, the symbol to be transmitted over subchannel 50 may be determined to have an allocation of six bits; that of subchannel 51, six bits; that of subchannel 52, seven bits, etc.

A Clock 30 controls the timing of the operation of the transmitter 12. It supplies input to a Controller 32 which controls the individual units of the transmitter. In the case of the CO transceiver, the clock 30 typically is a master clock to which a remote transceiver, such as at a subscriber premises, will be synchronized. In the case of a transceiver at the subscriber premises, such as is shown here for purposes of illustration, the clock is derived from the master clock at the central office as described more fully below in connection with the receiver portion of the transceiver.

A Frame Counter (FC) 24 connected to the controller 32 maintains a count of the number of frames of data transmitted from or received by the transceiver 10. The clock 30 maintains the

count in counter 34 synchronous with that of a corresponding counter (not shown) in the CO transceiver. In DSL systems, typically, data is communicated in the form of a sequence of data frames (e.g., sixty-eight frames for ADSL as specified in ITU Document G.992.2), followed by a synchronization frame, each frame having a duration of one symbol period of approximately two hundred and fifty microseconds. Together, the sixty-nine frames comprise a "superframe". Thus, the counter 34 typically maintains a count modulo sixty-nine. Finally, a State Memory (SM) 36 connected to the controller 32 records the state of the transceiver for reasons discussed more fully below.

Turning now to the receiver section 16, it is formed from a line conditioner (LC) 50; an analog-to-digital converter (ADC) 52; a serial-to-parallel converter 54; a Fast Fourier Transform (FFT) section 56; a decoder 58; and a parallel-to-serial converter 60. The conditioner 50 compensates for transmission distortions introduced by the line 14, and commonly includes a frequency-domain equalizer (FDQ) 50a; a time-domain equalizer (TDQ) 50b; and an echo canceller (EC) 50c, among other elements. The ADC 52 converts the received signal to digital form and applies it to the serial-to-parallel converter 54. The converter 54 removes any cyclic prefix that may have been appended to the signal before it was transmitted, and applies the resultant signal to the FFT 56 which effectively "demodulates" the received signal. The output of the FFT is applied to decoder 58 which, in conjunction with a bit-allocation-table 64, recovers the symbols X_i and X^*_i and the bits associated with them. The output of detector 58 is applied to the parallel-to-serial converter 60 which restores the data stream, b_i, that was originally applied to the transmitter. The controller 32 also controls the operation of the receiver portion 16 of the transceiver 10.

During normal (non-sleep mode) operation, a phase-lock loop (PLL) 62 receives from the FFT 56 a timing reference signal 62a (see Figure lA) via a line 62b. The timing reference signal 62a is transmitted from the transmitter with which the receiver 16 communicates (e.g., the CO transmitter). This signal is advantageously a pure tone of fixed frequency and phase which is synchronized with the Master Clock in the transmitter; its frequency defines the frame rate of the transceivers. Other forms of timing signal may, of course, be used, but use of a pure tone has the advantage of simplicity and reliability even when portions of the transceiver are powered down in accordance with the invention. The PLL 62 locks itself to this signal and drives clock 30 in

synchronism with the Master Clock in the driving transmitter. This also synchronizes frame counter 34 of the CPE transceiver to the corresponding frame counter of the CO transceiver. Control of the receiver section is provided by the controller 32.

In the sleep mode, the FFT 56 is preferably dormant. Accordingly, the timing reference signal for PLL 62 is provided from the output of the analog to digital convener 52 via a detector 64 which extracts the timing signal from the signal appearing on line 14 during sleep mode, by calculating the DFT of the synchronizing pilot tone. Controller 32 controls the switching of the input to PLL 62 between these two sources so that the PLL 62 remains locked to the CO transceiver timing reference.

As noted earlier, the transceiver of the present invention will commonly be incorporated in a computer such as a personal computer; indeed, it may be implemented as an integral part of such a computer, which may have a power conservation capability for activation when the computer is not in active operation. It is thus desirable that the transceiver be able to suspend operations and enter a "sleep" mode in which it consumes reduced power when it is not needed for data transmission or reception, but nonetheless be able to resume transmission or reception almost instantaneously, e.g., within a few frames.

Further, when the ADSL transceiver is implemented as an integral part of a computer, it may often be the case that the processing power of the computer is, at a given moment, devoted to another task such as graphics, word processing, and the like, and is thus unable to service the transceiver. In such circumstances, it is possible that a frame that is assembled for transmission to the CO transceiver, and thence to some network connected to it, is incomplete, and thus would generate errors if transmitted. Accordingly, the transceiver of the present invention is responsive to such conditions by entering an "idle" state in which it ceases active transmission of data while the computer is elsewhere occupied. This state is similar in many ways to the sleep mode state although, of course, its purpose is not power conservation, and thus in the idle state the power to selected portions of the transceiver may, but need not, be reduced. The idle state maintains synchronous signaling between the CPE and CO transceivers but no data is transmitted. On receipt of the idle indicator from the CPE, the CO transceiver transmits idle cells to the network to maintain connection with the network.

Referring now more particularly to Figure 2, the power down operation of the CPE transceiver begins on receipt of a power down indication (step 80) by the CPE transceiver controller 32. The power down indication may be applied to the controller 32 from an external source such as a personal computer in which the transceiver is included; it may be generated within the transceiver itself as a result of monitoring the input buffer 18 and determining that no data has been applied to it for a given time interval or that the buffer has not been filled despite passage of a symbol time; it may be responsive to a power down command from the CO transceiver; or it may be generated in response to other conditions.

Considering for the moment the first two cases, the CPE transceiver responds to the indication by transmitting to the CO transceiver an "Intend To Enter Sleep Mode" notification (step 82). This notification indicates that the transceiver is about to undergo a change of state, and may take any of a variety of forms; preferably it is a message, but may also comprise a tone, an inverted sync signal, a flag, or even the cessation of data transmission itself. The notification may advantageously be transmitted over one of the embedded operations channels of the system. It provides the CO transceiver an opportunity to prepare itself to enter sleep mode, and also to signal the CPE transceiver if entrance into sleep mode is not appropriate or desirable at the particular moment.

If entrance into sleep mode is permissible at this time; the CO transceiver responds to the power down or idle signal by transmitting an "Acknowledge Sleep Mode" notification (step 84) to the CPE transceiver. This and subsequent notifications described in connection with the sleep or idle mode may similarly take any of a variety of forms such as described above for the "Intend To Enter Sleep Mode" notification, but again preferably is in the form of a message transmitted over an embedded operations channel.

After it has received acknowledgment from the CO transceiver, the CPE transceiver transmits an "Entering Sleep Mode" notification (step 86) to the CO transceiver and ceases transmission, either immediately or after a given number of frames. The CO transceiver detects this notification; transmits its own "Entering Sleep Mode" notification (step 88); and enters sleep mode (step 90). In pursuance of this, the CO transceiver stores its state in its own state memory corresponding to the state memory 36 of CPE transceiver 10. The state of the CO or CPE transceivers preferably includes at least the frequency and time-domain equalizer coefficients

(FDQ; TDQ) and the echo-canceller coefficients (ECC) of its receiver portion and the gain of its transmitter portion; the transmission and reception data rates; the transmission and reception coding parameters; the-transmission fine gains; and the Bit Allocation Tables. The CO transceiver continues to advance the frame count and superframe count during the period of power-down in order to ensure synchrony with the remote CPE transceiver when communications are resumed. In order to maintain synchronization during the power down or idle state, the CO transceiver continues to transmit to the CPE transceiver the synchronizing pilot tone 62a. It may, at this time, perform its own power reduction. In particular, it may reduce or cut off power to the digital modulator/demodulator portions of its transmitter and receiver sections (corresponding to the IFFT 20 and FFT 56 of the CPE transceiver, Fig. 1); this provides a significant power reduction. Further, it may reduce power to parts of the analog circuitry. Power will be maintained, of course, to at least that portion of the analog driver circuitry which transmits the pilot tone and other control signals to the CPE transceiver, and to line circuits required to monitor the line 14 for signals from the CPE transceiver.

In a central office, the rest of the equipment is still operating, and while the link between the CO transceiver and the CPE transceiver is in a sleep state, user data provided by the CO transceiver will be benign idle data such as ATM IdleCells or HDLC Flag octets, and not generate false data errors to other equipment.

In response to the "Entering Sleep Mode" notification from the CO transceiver, the CPE transceiver enters the sleep mode (step 92). In particular, it stores its state (step 94) in state memory 38; as noted above in connection with the CO transceiver, this includes preferably at least the frequency and time-domain equalizer coefficients (FDQ; TDQ) and the echo-canceller coefficients (ECC) of its receiver and the gain of its transmitter; the transmission and reception data rates; the transmission and reception coding parameters; the transmission fine gains; and the Bit Allocation Tables. The phase and frequency offset of the phase-locked loop 62 is maintained by continued operation of the loop. The CPE transceiver 10 then reduces power to the digital modulator/demodulator circuitry comprising IFFT 20 and FFT 56, as well as to and transmitter data line drivers 26. However, it continues to advance the frame counter 34 in accordance with the received synchronizing signal 62a. However, the CPE controller 32 now causes this signal to be applied to the PLL 62 from the output of the ADC 52 (Fig. 1) via the detector 64, which

implements the DFT of a single tone, instead of directly from the output of the FFT 56 as was previously the case. This enables the FFT 56 to be powered down. The CPE and CO transceivers then operate in sleep mode (steps 95 and 97, respectively) until they awaken.

During the sleep mode state, the CO transceiver continues to monitor (step 90) the data subscriber line 14 for an "Exiting Sleep Mode" signal from the CPE transceiver (step 96). The CPE transceiver transmits this signal when its controller receives an "Awaken" indication (step 98) from an external source such as a computer in which it is installed or from other sources, or when its controller detects the presence of new data in the input buffer 18. In response to the "Awaken" signal, the CPE transceiver retrieves its stored state from the state memory 38; restores full power to its circuitry; and restores the output of the FFT 56 to the input of the PLL 62 (step 96). The CO transceiver, on detecting the "Exit Sleep Mode" notification from the CPE transceiver (step 99), thereupon exits sleep mode by restoring its state and restoring power. On waking up from sleep mode, the CPE transceiver can begin transmitting immediately or after only a few frames delay, since it need not repeat the initialization that was earlier required to establish the requisite parameters (e.g., frequency and time-domain equalizer coefficients (FDQ; TDQ, echo-canceller coefficients (ECC), transmitter gains; transmission and reception data rates; transmission and reception coding parameters; transmission fine gains; and Bit Allocation Tables) required for reliable communications. The same is true for the CO transceiver.

The present invention enables rapid resumption of transmissions, whether recovering from a power down or from an enforced idle condition due to temporary unavailability of processor resources in the case of an embedded transceiver, i.e., a transceiver implemented largely software and sharing CPU processing power with the other applications which may from time to time divert CPU resources from the transceiver. In particular, the transceiver of the present invention is capable of recovering full data transmission capabilities within a period of a few frames.

On resuming communication, it may be desirable for the CPE transceiver to transmit several frames of test (known) data (step 100) before resuming transmission of user data. This enables the system to verify that system conditions have not changed so significantly as to require renewed initialization. If the CO transceiver receives these without error, it notifies the CPE transceiver (step 102) and the latter resumes full user data transmission (step 104 and 106).

Otherwise, reinitialization must be performed (steps 104 and 108) before user data transmission occurs. A similar procedure may be employed for the transmission by the CO transceiver, and need not be described in further detail.

It will be understood that the order of certain of the steps described above may be changed, and that some steps may be omitted or added. For example, instead of initiating sleep mode at the CPE transceiver as shown in Figure 2, the CO transceiver may initiate sleep mode. In such a case, the flow of notifications will be as shown in Figure 2, but with the positions of CO and CPE transceivers reversed. Further, in some cases it may be desirable to omit the preparatory notifications of steps 82 and 84 and commence entrance into sleep mode as at steps 86 and 88. This will speed entrance into sleep mode, but is more prone to error.

It should also be understood that it is possible, and in various circumstances may be desirable, to operate in a "partial" sleep mode, in which only part of each transceiver is powered down. For example, where data transfer is one-way (when, for example, receiving video at the CPE transceiver from the CO transceiver without any upstream data being sent in return to the CO), the CO receiver and the CPE transmitter may operate in the sleep mode, while the CO transmitter and the CPE receiver are operating in full power mode.

As noted earlier, it is possible to implement major portions of the CPE and CO transceivers in software. In some applications, a dedicated CPU will be used for this purpose; in others, the CPU will be shared with other applications. Even when the sleep mode power conservation procedures described above are not necessary, when the transceivers are implemented in a shared-CPU environment, it may often be necessary to enter an idle mode that is similar to the sleep mode described above in order to maintain synchronization between the transceivers whenever the CPU is unable to service the transceivers. This is accomplished in accordance with the present invention by providing an Interface Transmission Unit (ITU) between the CPU and the data subscriber line which generates an idle indicator whenever the CPU is unavailable for servicing the transceiver which and transmits it to the remote transceiver to maintain the latter in synchronism with the former.

In particular, referring now to Figure 3, an Interface Transmission Unit (ITU) 200 in accordance with the present invention is interposed between a CPU 202 and the data subscriber line 14. The unit 200 includes a PCI bus interface 204, a data buffer 206, an analog-to-digital

and digital-to-analog converter 208, a controller 210, an idle indicator generator 212, and an analog front end 214.

In normal operation, the CPU passes data and control signals to the ITU 200 via the bus interface unit 204. Data from the CPU that is to be transmitted over the line 14 is stored in the buffer 206 and passed through the digital-to-analog converter portion of unit 208 for application to the line 214 through the analog front end. Conversely, data that is received from the line 14 is passed through the digital-to-analog converter portion of unit 208 to the buffer 206 and thence to the CPU 202 via the interface 204. The CPU processes the data flowing in the different directions in the manner illustrated in connection with Figure 1, i.e., it performs the requisite IFFT and FFT transforms on the data as appropriate. The idle indicator generator 212 may be inactive in this state.

When the CPU must divert its resources elsewhere for servicing applications having higher priority at the moment, the controller 210 activates the idle indicator generator 212 which generates a synchronous idle indicator symbol for transmission to the other transceiver with which the present transceiver is communicating. For example, the CPU may affirmatively notify the controller 210 that this is about to occur. Alternatively, the controller may monitor the buffer 206 and note its filling with data by the CPU has been interrupted for some time period. The idle indicator symbol is preferably of the same duration as a data frame, so that the remote transceiver can process it in the normal manner. However, it must be distinct from any valid data frame so that it can be detected and distinguished without ambiguity. It may comprise a tone, a collection of tones, a collection of tones modulated by bits, with similar of different phases, an inverted sync signal, or even the absence of signal. The CO transceiver responds to receipt of the idle symbol by itself transmitting idling data to the network or other devices with which it is connected so that erroneous data will not be transmitted. When the CPU returns to servicing its associated transceiver, the idle generator 212 suspends operation, preferably on command of the controller 210.

Even when the transceiver is not implemented as part of the shared resources of a CPU, it may nonetheless be beneficial to transmit an idle signal as described above when the transceiver is in sleep mode. This minimizes the likelihood that erroneous data may be emitted, for

example, to a network by a CO transceiver when a CPE transceiver with which it is communicating is in sleep mode.

From the foregoing, it 'will be seen that we have provided a multitone transceiver system that capable of operating wholly or partially in a sleep mode, both for purposes of power conservation as well as to accommodate itself to integration with, or incorporation into, computer systems having a power conservation mode. The transceiver system also is adapted to implementation in software under circumstances where the CPU on which the software runs is shared with other applications which may sometimes preempt resources needed for the transceiver.

ABSTRACT OF THE DISCLOSURE

A multicarrier transceiver is provided with a sleep mode in which it idles with reduced power consumption when it is not needed to transmit or receive data. The full transmission and reception capabilities of the transceiver are quickly restored when needed, without requiring the full (and time-consuming) initialization commonly needed to restore such transceivers to operation after inactivity.

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Filer:	Jason Vick/Joanne Vos
Attorney Docket Number:	6936-28-CON-7
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt

EFS ID:	15701706
Application Number:	13887889
International Application Number:	
Confirmation Number:	8684
Title of Invention:	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY
First Named Inventor/Applicant Name:	John A. Greszczuk
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-28-CON-7
Receipt Date:	06-MAY-2013
Filing Date:	
Time Stamp:	16:23:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1600
RAM confirmation Number	3631
Deposit Account	191970
Authorized User	
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ADS.pdf	1508521 4b8a4c0a01e68e5e3b362df1601deaaff585ed02	no	8
Warnings:					
Information:					
2		AMEND_PRELIM_01.pdf	308434 abebc82410c820a2b666ea97a30731130a7e0af4	yes	5

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Preliminary Amendment	1	1
Specification	2	2
Claims	3	4
Abstract	5	5

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3		Application_FINAL.pdf	103379 f5b3a5fa9a1d5ff9fe6d87e69ef481ea2ece4d82	yes	18

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	13
Claims	14	17
Abstract	18	18

Warnings:					
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4	Drawings-only black and white line drawings	Figures_FINAL.pdf	44675 e0c71a86b7cb7a05e1a2175ecc95d01df6e7bdd8	no	4
Warnings:					
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5		Substitute_Spec_Marked_Up.pdf	104245 744edec6c39d11cff798a87175bc867d6bb8cce8	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	14
	Abstract	15	15

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6		Substitute_Spec_Clean.pdf	99222 509cf7e65e0636b1b09f40adf2ee6da6c10a79c0	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	14
	Abstract	15	15

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Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	33416 774d61b6aae136e9c6823fc8acee33091c86cc12	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2201892		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (03-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6936-28-CON-7
	Application Number	
Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	John	A.	Greszczuk	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Inventor 2 Remove

Legal Name

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	Halil		Padir	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6936-28-CON-7
	Application Number	
Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	

City	N. Andover	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

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City	N. Andover	State/Province	MA
Postal Code	01845	Country i	US

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Michael	A.	Tzannes	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Lexington	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	17 Carley Road		
Address 2			
City	Lexington	State/Province	MA
Postal Code	012173	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	62574		
Email Address	jvick@sheridanross.com	Add Email	Remove Email

Application Information:

Title of the Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY		
Attorney Docket Number	6936-28-CON-7	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6936-28-CON-7
	Application Number	
Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	62574		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
	Continuation of	13/152558	2011-06-03	8437382	2013-05-07
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/152558	Continuation of	12/615946	2009-11-10	7978753	2011-07-12
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/615946	Continuation of	11/425507	2006-06-21	7697598	2010-04-13
Prior Application Status	Abandoned			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/425507	Continuation of	11/289516	2005-11-30		
Prior Application Status	Abandoned			Remove	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6936-28-CON-7
	Application Number	
Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11/289516	Continuation of	11/090183	2005-03-28
Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11/090183	Continuation of	10/778083	2004-02-17
Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
10/778083	Continuation of	10/175815	2002-06-21
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
10/175815	Continuation of	09/581400	2000-06-13	6445730	2002-09-03

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
09/581400	a 371 of international	PCT/US99/01539	1999-01-26
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US99/01539	non provisional of	60/072447	1998-01-26

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6936-28-CON-7
	Application Number	
Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6936-28-CON-7
	Application Number	
Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	TQ DELTA, LLC		
Mailing Address Information:			
Address 1	805 LAS CIMAS PARKWAY		
Address 2	SUITE 240		
City	AUSTIN	**State/Province**	TX
Country [i]	US	Postal Code	78746
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6936-28-CON-7
	Application Number	
Title of Invention	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	

Mailing Address Information:			
Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

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NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Jason H. Vick/			Date (YYYY-MM-DD)	2013-05-06
First Name	Jason H.	Last Name	Vick	Registration Number	45285

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				Filing Date	May 6, 2013
				First Named Inventor	John A. Greszczuk
				Art Unit	
				Examiner Name	
Sheet	1	of	6	Attorney Docket Number	6936-28-CON-7

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Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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				Examiner Name	
Sheet	2	of	6	Attorney Docket Number	6936-28-CON-7

UNPUBLISHED U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code[2] (if known)	Filing Date MM-DD-YYYY	Name of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
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Sheet	3	of	6	Attorney Docket Number	6936-28-CON-7

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				First Named Inventor	John A. Greszczuk
				Art Unit	
				Examiner Name	
Sheet	4	of	6	Attorney Docket Number	6936-28-CON-7

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				First Named Inventor	John A. Greszczuk
				Art Unit	
				Examiner Name	
Sheet	5	of	6	Attorney Docket Number	6936-28-CON-7

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				Examiner Name	
Sheet	6	of	6	Attorney Docket Number	6936-28-CON-7

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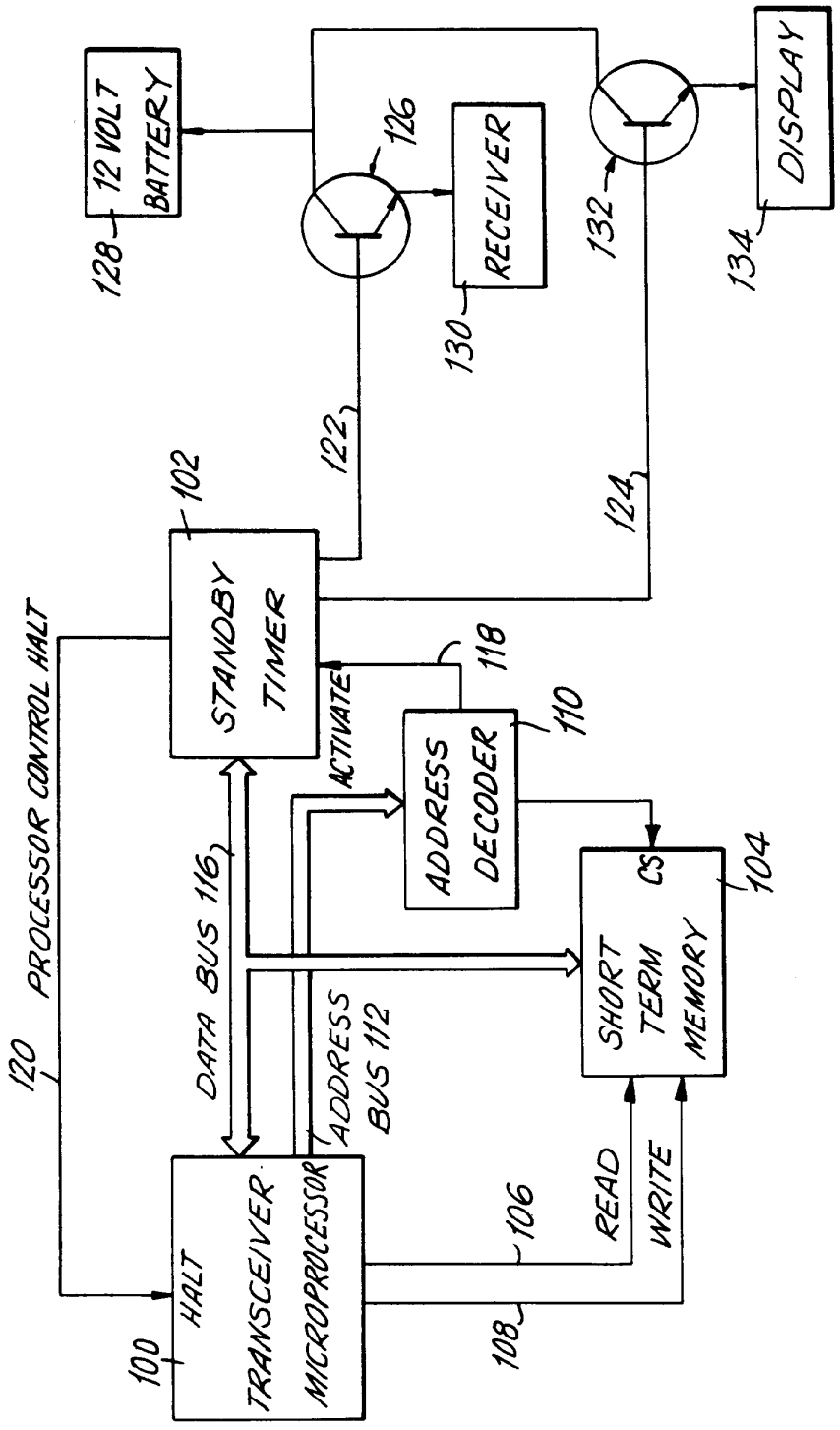
(54) **Power saving arrangement and method in portable cellular telephone system.**

(57) Battery power consumption of a cellular telephone is minimized during the stand-by mode by detecting when a received message is intended for another telephone, and for reducing battery power to at least one of the electronic components at the telephone when the transmitted message is intended for another telephone. Power is restored when the next transmitted message is expected to be received by the telephone.

EP 0 473 465 A1

Jouve, 18, rue Saint-Denis, 75001 PARIS

FIG.5


12 VOLT BATTERY
128
126
RECEIVER
130
132
DISPLAY
134
122
124
102
STANDBY TIMER
PROCESSOR CONTROL HALT
120
ACTIVATE
118
ADDRESS DECODER
110
DATA BUS 116
ADDRESS BUS 112
CS
SHORT TERM MEMORY
104
HALT
TRANSCEIVER MICROPROCESSOR
100
106
READ
WRITE
108

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention generally relates to a power conserving arrangement for, and a method of, minimizing battery power consumption during stand-by operation of a portable, battery-operated, mobile station and, more particularly, a cellular telephone in a cellular telephone system.

2. Description of Related Art

A typical cellular telephone system includes a plurality of base stations or towers, each serving a pre-assigned geographical cell or region. Each base station transmits messages to a multitude of mobile stations, e.g. cellular telephones, in its region. Each telephone includes a transceiver and a decoder under microprocessor control.

During a stand-by mode of operation, each telephone waits to receive a telephone call. The message transmitted by a respective base station may be a so-called "global" message intended for all telephones, or, most frequently, an individual message intended for just one specific telephone. Hence, the individual message contains a unique mobile identification number (MIN), i.e. the telephone number. Each telephone has its unique MIN pre-stored in an on-board memory.

Many messages are transmitted by a respective base station and, of all those many messages, only a very small amount, if any, are intended for a particular telephone. Nevertheless, each telephone, during the stand-by mode of operation, continuously receives and decodes all messages transmitted by the respective base station until the decoder of a particular telephone recognizes its MIN, after which, the telephone operates in a talk (call in progress) mode. The telephone transmits and receives data, including voice data, to and from the base station in the talk mode.

It will be seen that conventional cellular telephones in current use consume electrical power in both the talk and the stand-by modes. In current portable battery-operated telephones, the on-board battery typically has a working lifetime of approximately 8 hours in the stand-by mode, and about 1-2 hours in the talk mode. The battery must then be re-charged or replaced to continue telephone service. A major electrical current consumer on-board the battery-operated cellular telephone during the stand-by mode is the receiver section of the transceiver which, as previously described, is continuously on while the telephone is waiting to decode its MIN. The microprocessor and other electronic components on-board the telephone are also energized during the stand-by mode and additionally contribute to current drain on the battery. The need to increase the battery working lifetime between re-charges and/or battery replacement is self-evident.

To aid in understanding the invention described herein, a brief review of the prior art structure of the message transmitted by the base station during stand-by operation is presented. The message is a digital stream of bits, and may have obe or more words. Usually, a message includes two words. FIG. 1 schematically shows the prior art structure of each word of the message. Each word contains forty bits. The first twenty-eight bits are message data containing, among other things, the MIN and/or a global message and/or a channel assignment message, etc. The last twelve bits are a sequence or parity field of check bits (BCH) and is a block code parity check sum. The BCH parity field confirms that the message data in the first twenty-eight bits were correctly received.

To overcome the problem of messages that are sometimes lost by rapidly changing radio signals, each word of the message is transmitted from the base station to each portable telephone five times. For a message to be validated, each word must be correctly received at least three out of the five times before the telephone will respond to the message. In addition, to compensate for burst errors, words are interleaved and transmitted in a format based on whether the MIN is odd or even.

FIG. 2 schematically shows the prior art structure of the interleaved format wherein each word A (designated for even telephone numbers) and each word B (designated for odd telephone numbers) is repeated five times and, for each repetition, the even word A is alternated with the odd word B. In addition, FIG. 2 shows a dotting sequence D which is a sequence of ten bits that advises the telephone that a synchronization word S is coming. The dotting sequence produces a 5 kHz frequency signal which is a precursor and a gross indicator that a message is about to start. The synchronization word is a sequence of eleven bits, and includes a synchronization pattern by which an internal clock of the telephone is synchronized to the base station transmitter.

Also imposed on the message data stream are busy-idle bits which are schematically shown in FIG. 3. A busy-idle bit is sent every ten bits of the message to indicate the status of the system channel. If the busy-idle bit is set to logic 1, then the channel is not busy. If the busy-idle bit is set to logic 0, then the channel is busy. The data rate for transmitted bits is 10 kbps. Hence, as shown in FIG. 2, 463 bits are transmitted in 46.3 msec, and is the total time in which one odd and one even word is transmitted five times in an interleaved format.

As previously noted, a message may, and typically does, contain more than one word. When this happens, each word also advises the on-board microprocessor that more words for the complete message are coming.

FIG. 4 schematically shows the prior art structure

and duration of a complete message that consists of two words wherein word C is the second word of the message for an even telephone number which had word A as the first word, and wherein word D is the second word of the message for an odd telephone number which had word B as the first word. A two-word message takes 92.6 msec to be completely transmitted.

SUMMARY OF THE INVENTION

1. Objects of the Invention

It is a general object of this invention to advance the state of the art of cellular telephone systems.

It is another object of this invention to increase the battery working lifetime between recharges and/or battery replacement in cellular telephone systems.

Another object of this invention is to prolong the working lifetime of portable, battery-operated, cellular telephones in the stand-by mode.

A further object of this invention is to substantially reduce power consumption in such portable cellular telephones.

2. Features of the Invention

In keeping with these objects, and others which will become apparent hereinafter, one feature of this invention resides, briefly stated, in a power conserving arrangement for, and a method of, minimizing battery power consumption at one mobile station, particularly a portable, battery-operated cellular telephone, during a stand-by mode of operation in which messages transmitted by a base station of a system, particularly a cellular telephone system, are received by on-board receiver means at the cellular telephone.

The invention comprises detector means for detecting when a transmitted message received by the receiver means at the telephone is intended for another station in a non-calling state. In response to detection of the non-calling state, this invention proposes the use of power conserving means operative for reducing battery power to at least one on-board electronic means at the telephone. The battery power reduction is maintained by the power conserving means for a time period whose duration lasts until another transmitted message is expected to be received by the receiver means at the telephone.

The power conserving means includes control means, preferably a control switch switchable between a pair of switching states in which battery power is supplied and denied,respectively, to one or more of the various electronic means at the telephone. Battery power may be supplied or denied to the aforementioned receiver means, or a powered display means, or a microprocessor which controls overall operation of the telephone. The various electronic means can be simultaneously or sequentially supplied or denied battery power.

The control switch is switchable between its switching states by a settable stand-by timer means under the control of the microprocessor. The microprocessor determines the aforementioned time period between successive messages, and sets the timer to generate a timer output signal for controlling the control switch upon elapse of said time period. A memory store and an address store may be used for storing data and addresses, respectively, of data needed by the microprocessor to resume operation in the event that the latter is de-energized during the stand-by mode. Hence, when the detector means determines that a given word of a transmitted message is not intended for a particular telephone, the microprocessor can determine the amount of time until the next word is expected to be received. The receiver means is de-energized during this time period. Since the receiver means is a major electrical current consumer, a substantial reduction of power consumption at the telephone is obtained. Additional power savings can be obtained by de-energizing other electronic means at the telephone. The receiver means, as well as the other electronic means, are re-energized upon the elapse of said time period. The microprocessor sets the stand-by timer means for this time period.

The duration of the time period is variable, and depends upon when the first word of a message is confirmed as being intended for another telephone. This could occur at the first, second, third, fourth or fifth repetition of the word.

The novel features which are considered as characteristic of the invention are set forth in particular in the appended claims. The invention itself, however, both as to its construction and its method of operation, together with additional objects and advantages thereof, will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic representation of the structure of a word transmitted in a cellular telephone system according to the prior art;

FIG. 2 is a schematic representation of the structure of an odd word and an even word transmitted in an interleaved format in a cellular telephone system according to the prior art;

FIG. 3 is a schematic representation of a portion of a word of a message specifically showing busy-idle bits imposed on the data stream according to the prior art;

FIG. 4 is a schematic representation of the structure of a two-word message transmitted by a cellular telephone system according to the prior art;

FIG. 5 is an electrical schematic diagram of a

power conserving arrangement for minimizing battery power consumption in accordance with this invention; and

FIG. 6 is a flow chart depicting the operation of a transceiver microprocessor used in the power conserving arrangement in accordance with this invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 5, reference numeral 100 generally identifies a programmed transceiver microprocessor for controlling operation of a portable, battery-operated cellular telephone. The structure and operation of the microprocessor 100 are well known in the art. For example, the entire contents of The Bell System Technical Journal, Vol. 58, No. 1, January 1979, are hereby incorporated herein by reference.

The operation of the microprocessor is schematically shown in flow chart form in FIG. 6. As previously described, during the stand-by mode, the microprocessor 100 is programmed to wait for the dotting sequence D (block 200), to thereupon time align with the synchronization word S (block 202), and thereupon to receive and decode the first reception of the first word of the message (block 204), i.e. word A1 for an even MIN, or word B1 for an odd MIN. After the first reception of the first word is decoded, the parity field is checked (block 206) to validate whether the word A1 or B1 was correctly received and decoded. If the parity field does not validate the decoding of the first reception of the first word, then the microprocessor 100 receives and decodes the second reception of the first word (block 208), i.e. A2 or B2. In analogous manner, the reception and decoding of the third, fourth and fifth receptions of the first word continue until the parity field validates the reception and decoding of a word.

As soon as the parity field has validated the decoding of a received word, then the incoming MIN of the received word (MIN_r) is compared (in block 210) to a pre-stored MIN (MIN_s) of the telephone. If a match is made, then the telephone executes the message (block 212). If a match is not made, then the microprocessor 100 next checks to see if the incoming message is a global message intended for all telephones (block 214). If the incoming message is not a global message, and if the match between the incoming MIN and the pre-stored MIN is not made, then the microprocessor knows that the incoming message is not intended for this particular telephone and, in fact, is intended for some other telephone. The detection of this "non-calling" state is the triggering event employed by the power conserving arrangement of this invention to conserve battery power by reducing, and preferably interrupting, battery power to one or more electronic components, Particularly the receiver circuit of the transceiver, at the telephone. As described below, power reduction or interruption is maintained for a time period of variable duration which begins upon the first validation of a word, and which expires when the next transmitted message is expected to be received.

Returning to FIG. 5, the microprocessor 100 is operatively connected to a settable stand-by timer 102. Advantageously, the timer is a CMOS timer which can be obtained from Exar Corporation as Model No. XR2206. A short-term memory store 104 is operatively connected to the microprocessor 100 by read line 106 and write line 108. The memory store 104 is operative for storing data from the microprocessor. An address decoder 110 is operatively connected to the microprocessor by an address bus 112, and is also connected to the memory store 104 by an address line 114. The address decoder 110 stores the addresses of the data stored in the memory store 104. A bi-directional data bus 116 interconnects the microprocessor 100, the stand-by timer 102 and the memory store 104.

The stand-by timer 102 is connected to the address decoder 110 by an activate line 118, and is also connected to the microprocessor via a control halt line 120.

The timer 102 has at least one timed output line and, as shown in FIG. 5, a pair of timed output lines 122, 124. Output line 122 is connected to a control switch 126 operatively connected between a battery 128 and the receiver section 130 of the transceiver. Output line 124 is connected to a control switch 132 operatively connected between the battery 128 and another electronic component at the telephone, e.g. a powered display 134.

Returning to FIG. 6, as soon as the microprocessor has detected the non-calling state, it calculates the time period until the next word is expected to be received (block 216). This time period may be calculated by the following formula:

For telephones that decode even words A,

$T = 48.4 \text{ msec} - 8.8 \text{ msec} (n) + 46.3 \text{ msec} (NAWC)$;

For telephones that decode odd words B,

$T = 44.0 \text{ msec} - 8.8 \text{ msec} (n) + 46.3 \text{ msec} (NAWC)$;

wherein n is the number of words that have been repeated,

NAWC is the number of additional different words to come, and

T is the time period between transmitted messages.

The above numerical times are presented for the specific words and transmission times set forth above in connection with FIGs. 1-4. Since even words A precede odd words B, the time period T varies depending on whether the telephone decodes even words or odd words.

Hence, the microprocessor has calculated the time to the next word. It stores necessary operating

parameters such as the control channel number, the malfunction timer value, etc. into the short-term memory store 104 via data bus 116, and into the address decoder 110 via the address bus 112 (block 218). The microprocessor then initiates the stand-by timer 102 (block 220) which, in turn, generates a control halt output signal on line 120 to power down the microprocessor during the time period T. The stand-by timer 102 also generates timer output signals on control line 122, 124 to actuate control switches 126, 132 between its switching states, and either reduces or interrupts battery power from the battery 128 to the receiver 130 and the powered display 134. The timer output signals on lines 122, 124 may be either simultaneously or sequentially generated. Due to initialization of displays, data bus devices,and radio frequency stabilizers, certain electronic components at the transceiver may be selectively inhibited. Frequency synthesizers, i.e. a radio frequency oscillator, may require a finite time to stabilize, e.g. on the order of three msec. Hence, the frequency synthesizer, if turned off during the stand-by mode, may need to be activated at least three msec prior to reactivation of all the other electronic components turned off during the stand-by mode. In addition, the frequency synthesizer, as well as other data dependent devices, such as a data register, may need to be refreshed with an initialization sequence after activation.

Upon expiration of the calculated time period (block 222), the stand-by timer 102 switches the control switches 126, 132 to their former states in which power is returned to the receiver 130 and the display 134, as well as the microprocessor 100. This restoration of power (block 224) may be simultaneous or sequential among the various electronic components. The data stored in the address decoder 110 and the memory store 104 is retrieved, and the telephone, once again, starts the stand-by mode by waiting for the dotting sequence (block 200).

Hence, one or more electronic components at the telephone are de-energized between messages. This saves electrical power since there is no reason for the receiver, as well as other electronic components at the telephone, to be energized between messages. The only component that needs to be energized at all times is, of course, the stand-by timer 102, but this component consumes far less power than the receiver 130, the display 134, the microprocessor 100, as well as any of the other electronic components at the telephone. For timing accuracy, the on-board reference clock (crystal oscillator) should never be de-energized.

Although the above invention has been described in connection with cellular telephones, it is not intended to be so limited since the power conserving arrangement and method of this invention can be used advantageously with beepers, pagers, and, in short, any system having multiple mobile stations which are self-identifiable upon receipt of transmitted messages.

The timing calculations set forth above are based on the U.S.-industry standard set by the Electronic Industries Association (EIA) and published as EIA-553, "Mobile Station-Land Station Compatability Specification, 1990".

Other industry standards can be used. For example, in Europe, and particularly in the United Kingdom, the industry standard known as TACS was published in "United Kingdom Total Access Communications Systems Mobile Station-Land Station Compatability Specification", Issue 4, August 1989.

In the TACS system, the dotting sequence produces a 4 kHz frequency signal, and the data rate for transmitted bits shown in FIG. 3 would be 8 kbps. The 2,463 bits referred to in FIG. 2 would be transmitted in 57.875 msec. The two-word message referred to in FIG. 4 would take 115.75 msec.

The aforementioned time period for a TACS system may be calculated by the following formula:

For telephones that decode even words A,

$$T = 60.5 \text{ msec} - 11 \text{ msec}\,(n) + 57.875\,(NAWC)$$

For telephones that decode odd words B,

$$T = 55.0 \text{ msec} - 11 \text{ msec}\,(n) + 57.875\,(NAWC)$$

wherein n is the number of words that have been repeated,

NAWC is the number of additional different words to come, and

T is the time period between transmitted messages.

It will be understood that each of the elements described above, or two or more together, also may find a useful application in other types of constructions differing from the types described above.

While the invention has been illustrated and described as embodied in a power saving arrangement and method in portable cellular telephone system, it is not intended to be limited to the details shown, since various modifications and structural changes may be made without departing in any way from the spirit of the present invention.

Without further analysis, the foregoing will so fully reveal the gist of the present invention that others can, by applying current knowledge, readily adapt it for various applications without omitting features that, from the standpoint of prior art, fairly constitute essential characteristics of the generic or specific aspects of this invention and, therefore, such adaptations should and are intended to be comprehended within the meaning and range of equivalence of the following claims.

What is claimed as new and desired to be protected by Letters Patent is set forth in the appended claims.

Claims

1. In a system having a base station operative for transmitting messages to portable, battery-operated, mobile stations, each having on-board electronic means including receiver means operative for receiving the transmitted messages in a stand-by mode, a power-conserving arrangement for minimizing battery power consumption at one mobile station during the standby mode, said arrangement comprising:
   (a) detector means for detecting when a transmitted message received by the receiver means at said one mobile station is intended for another station in a non-calling state; and
   (b) power-conserving means responsive to detection of the non-calling state, for reducing battery power to at least one of the electronic means at said one mobile station, and for maintaining the battery power reduction for a time period whose duration lasts until another transmitted message is expected to be received by the receiver means at said one mobile station.

2. The arrangement according to claim 1, wherein the mobile stations are cellular telephones having unique identification numbers incorporated in the transmitted messages, and wherein the detector means is operative for detecting the unique identification number for the telephone of said one mobile station in a calling state,and for detecting other identification numbers intended for other telephones in the non-calling state; and wherein the power-conserving means is responsive to detection of the other identification number for said telephone.

3. The arrangement according to claim 2, wherein the power-conserving means includes control means operatively connected to said at least one electronic means, and operative for controlling battery power to said at least one electronic means.

4. The arrangement according to claim 3, wherein the control means is a control switch operatively connected to the receiver means, and switchable between a pair of switching states in which battery power is supplied and denied, respectively, to the receiver means.

5. The arrangement according to claim 4, wherein the control switch is also operatively connected to a powered display means, and respectively supplies and denies battery power to the display means in the switching states.

6. The arrangement according to claim 3, wherein the power-conserving means includes settable stand-by timer means operatively connected to the control means, and operative for generating a timer output signal for controlling the control means upon elapse of said time period.

7. The arrangement according to claim 6, wherein the control means is operatively connected to a plurality of said electronic means, and wherein the timer output signal simultaneously controls all said electronic means.

8. The arrangement according to claim 6, wherein the control means is operatively connected to a plurality of said electronic means, and wherein the timer output signal sequentially controls all said electronic means.

9. The arrangement according to claim 6, wherein the detector means includes a programmed microprocessor operatively connected to the stand-by timer means, and operative for setting the stand-by timer means to generate the timer output signal upon elapse of said time period, said programmed microprocessor including means for determining said time period between successive messages.

10. The arrangement according to claim 9, wherein the control means is a control switch operatively connected to the programmed microprocessor, and switchable between switching states in which battery power is supplied and denied, respectively, to the programmed microprocessor.

11. The arrangement according to claim 10, wherein the power-conserving means includes a memory means for storing data from the programmed microprocessor, and an address means for storing addresses of the stored data during said time period.

12. The arrangement according to claim 1, wherein the power-conserving means restores battery power upon the elapse of said time period.

13. The arrangement according to claim 12, wherein the power-conserving means includes means for initializing data-dependent electronic means prior to elapse of said time period.

14. In a cellular telephone system operative for transmitting messages to portable, battery-operated, mobile cellular telephones, each having on-board electronic means including receiver means operative for receiving the transmitted messages in a stand-by mode, a power-conserving arrange-

ment for minimizing battery power consumption at one cellular telephone during the stand-by mode, said arrangement comprising:

(a) detector means for detecting when a transmitted message received by the receiver means at said one cellular telephone is intended for another cellular telephone in a non-calling state; and

(b) power-conserving means responsive to detection of the non-calling state, for reducing battery power to at least one of the electronic means at said one cellular telephone, and for maintaining the battery power reduction for a time period whose duration lasts until another transmitted message is expected to be received by the receiver means at said one cellular telephone.

15. In a system having a base station operative for transmitting messages to portable, battery-operated, mobile stations, each having on-board electronic means including receiver means operative for receiving the transmitted messages in a stand-by mode, a method for minimizing battery power consumption at one mobile station during the stand-by mode, said method comprising the steps of:

(a) detecting when a transmitted message received by the receiver means at said one mobile station is intended for another station in a non-calling state; and

(b) reducing battery power to at least one of the electronic means at said one mobile station in response to detection of the non-calling state, and maintaining the battery power reduction for a time period whose duration lasts until another transmitted message is expected to be received by the receiver means at said one mobile station.

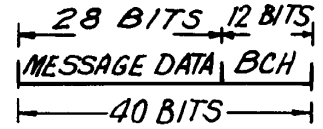


FIG.1
PRIOR ART

WORD BIT STRUCTURE

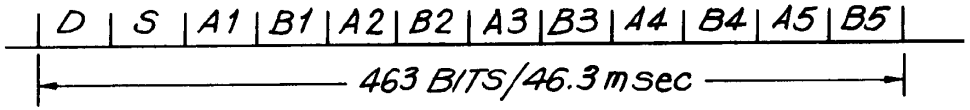


FIG.2
PRIOR ART

MESSAGE WORD STRUCTURE

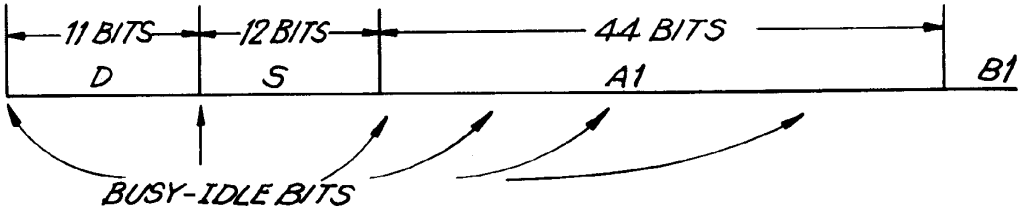


FIG.3
PRIOR ART

BUSY-IDLE BIT SUPERPOSITION

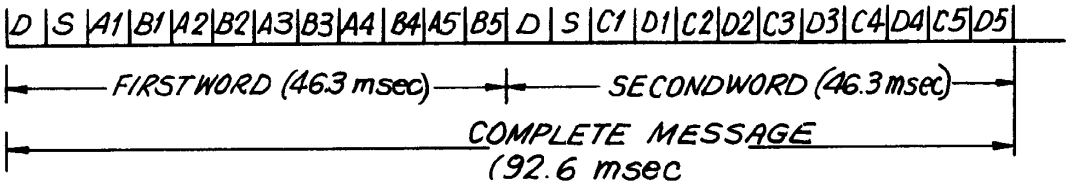
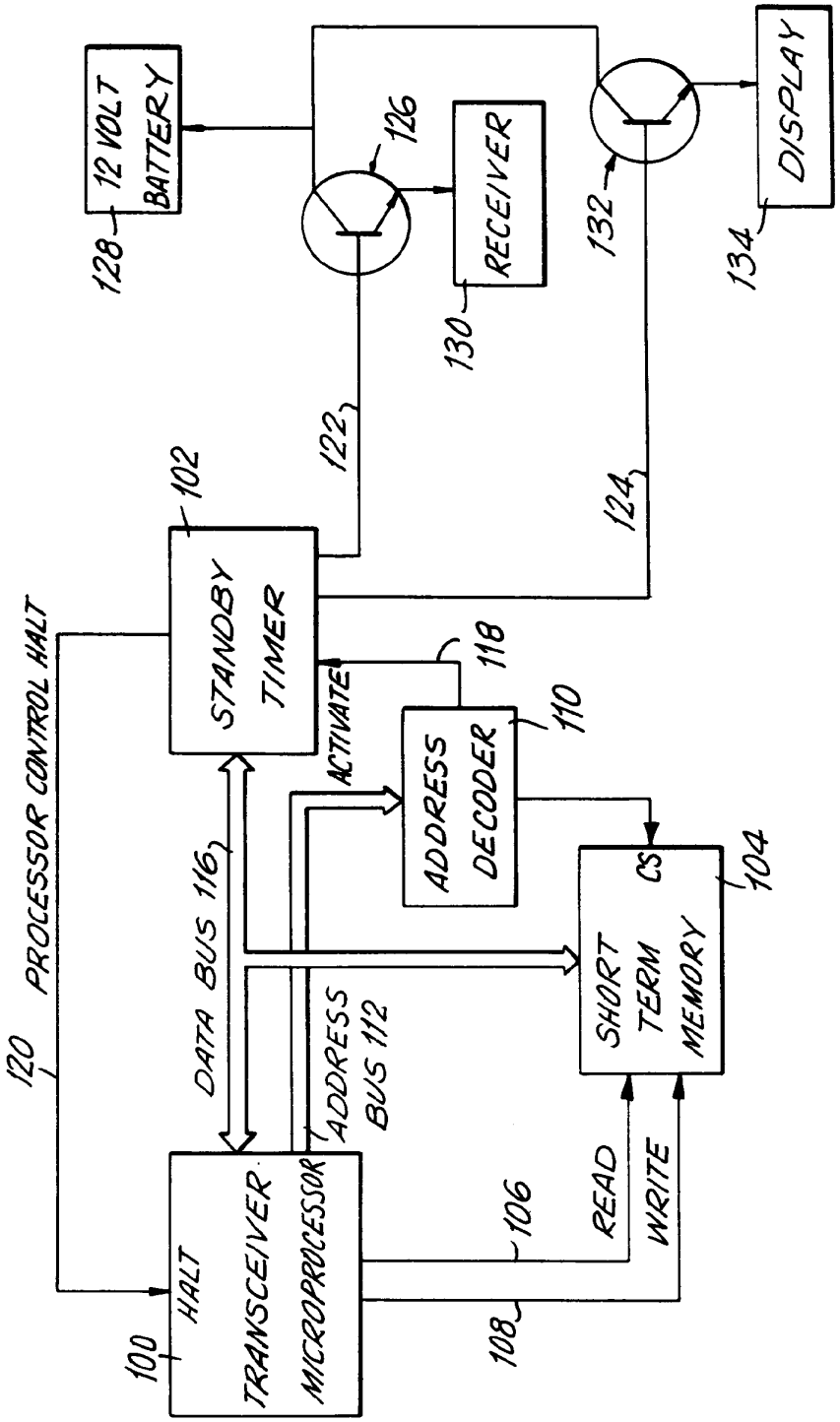


FIG.4
PRIOR ART

TWO-WORD MESSAGE

FIG.5


12 VOLT BATTERY
128
126
RECEIVER
130
132
DISPLAY
134
122
124
102
STANDBY TIMER
ACTIVATE
118
ADDRESS DECODER
110
PROCESSOR CONTROL HALT
120
DATA BUS 116
ADDRESS BUS 112
CS
SHORT TERM MEMORY
104
HALT
TRANSCEIVER
MICROPROCESSOR
100
106
READ
WRITE
108

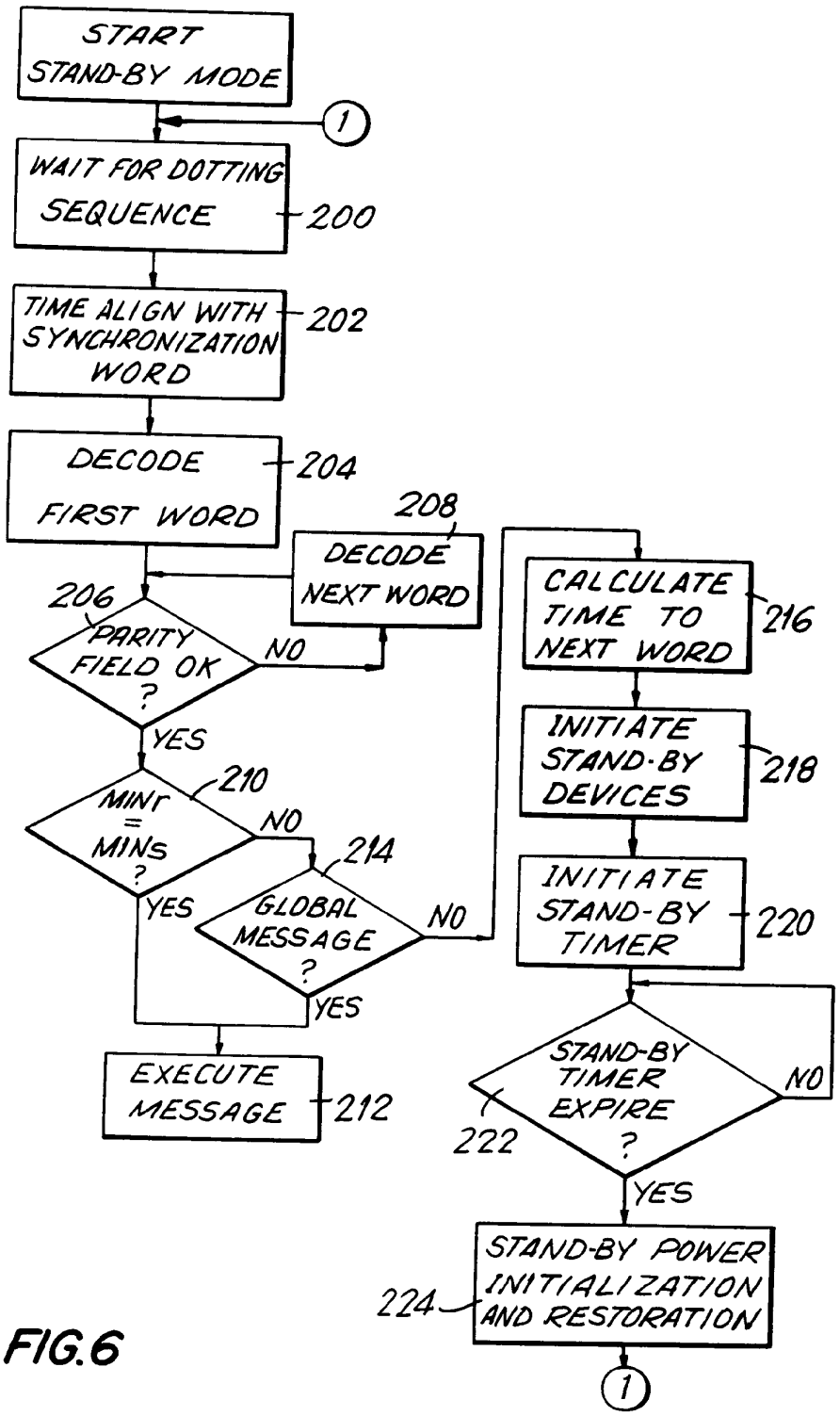

START STAND-BY MODE
1
WAIT FOR DOTTING SEQUENCE
200
TIME ALIGN WITH SYNCHRONIZATION WORD
202
DECODE FIRST WORD
204
208
DECODE NEXT WORD
206
PARITY FIELD OK ?
NO
YES
MINr = MINs ?
210
NO
214
GLOBAL MESSAGE ?
NO
YES
YES
EXECUTE MESSAGE
212
CALCULATE TIME TO NEXT WORD
216
INITIATE STAND-BY DEVICES
218
INITIATE STAND-BY TIMER
220
STAND-BY TIMER EXPIRE ?
222
NO
YES
STAND-BY POWER INITIALIZATION AND RESTORATION
224
1

FIG.6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 40 1413

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X Y Y	EP-A-0 358 166 (SANYO) * The whole document * ---	1-4,12, 14,15 5-7,9- 11 13	H 04 M 1/72 H 04 Q 7/04 H 04 B 1/16
Y	WO-A-8 805 248 (MOTOROLA) * Page 9, lines 16-26; page 11, lines 5-15; page 13, lines 1-6; figure 4 * ---	5-7,9- 11	
Y A	EP-A-0 361 350 (NEC) * Abstract; column 1, lines 25-36 * ---	13 8	
A	EP-A-0 171 071 (NEC) * Page 8, lines 6-12; figure 1 * -----	9	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 04 M
H 04 Q
H 04 B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	03-10-1991	MONTALBANO F.M.G.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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(54) Reconfigurable transceiver for asymmetric communication systems

(57) A transceiver (5) for an asymmetric communication system such as asymmetric digital subscriber line (ADSL) includes a configuration register (71) defining operation at either a central office (CO) or a remote terminal (RT). The configuration register (71) includes a control bit (72) for selecting either CO or RT mode. The transceiver (5) includes a signal processing module (70) configured according to the state of the control bit (72). For example, a digital interface (70) converts transmit data into transmit symbols and converts received symbols into receive data. The digital interface (70) uses a large memory (158) as a buffer in the transmit path and a small memory (160) as a buffer in the receive path in CO mode. In RT mode, the digital interface (70) uses the small memory (160) in the transmit path and the large memory (158) in the receive path. The selective configuration allows a single integrated circuit to be used in both CO and RT equipment.

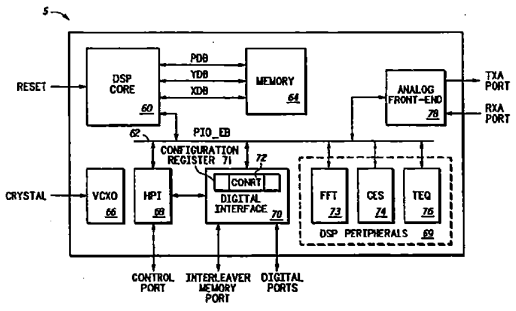

FIG.2

EP 0 840 474 A2

Description

Field of the Invention

This invention relates generally to communications, and more particularly, to a transceiver for an asymmetric communication system.

Background of the Invention

In order to make high data rate interactive services such as video and internet access available to more residential and small business customers, high-speed data communications paths are required. Although fiber optic cable is the preferred transition media for such high data rate services, it is not readily available in existing communication networks and the expense of installing fiber optic cabling is prohibitive. Current telephone wiring connections, which consist of copper twisted-pair media, were not originally designed to support the data rates or bandwidth required for interactive services such as video on demand or even high speed internet connections. Asymmetric Digital Subscriber Line (ADSL) technology has been developed to increase the effective bandwidth of existing twisted-pair connections, allowing interactive services to be provided without requiring the installation of fiber optic cable.

Discrete multi-tone (DMT) is a multi-carrier technique which divides the available bandwidth of twisted-pair copper media connections into mini-subchannels or bins. The DMT technique has been adopted in the ANSI T1.413 standard (ADSL standard). In the ADSL standard, DMT is used to generate 250 separate 4.3125 kilohertz subchannels from 26 kilohertz to 1.1 megahertz for downstream transmission to an end user. Likewise, DMT is used to generate 26 subchannels from 26 kilohertz to 138 kilohertz for upstream transmission by an end user. The asymmetric transmission protocol implemented by the ADSL standard requires a higher rate of data transmission from a central office to a remote terminal and a lower rate of data transmission from a remote terminal to a central office. As a result, different processing sequences are required at the remote terminal and central office ends. Currently available systems utilize printed circuit board designs which are configured to operate as either a central office end or a remote terminal end and may not be used interchangeably as an opposite end. Thus, because such separate system designs are necessary, these separate systems must include separate design overhead, separate data bases and separate firmware files. Furthermore, each of the separate data bases, separate designs, and separate firmware files must all be designed, produced, and maintained with finite resources.

Brief Description of the Drawings

FIG. 1 illustrates, in block diagram form, an Asymmetric Digital Subscriber Line (ADSL) system in accordance with the present invention;

FIG. 2 illustrates, in block diagram form, an ADSL transceiver in accordance with the present invention;

FIG. 3 illustrates, in partial block and partial logic diagram form, the ADSL transceiver of FIG. 2 configured to operate at a central office;

FIG. 4 illustrates, in partial block and partial logic diagram form, the ADSL transceiver of FIG. 2 configured to operate at a remote terminal;

FIG. 5 illustrates, in block diagram form, the digital interface of the ADSL transceiver of FIG. 2;

FIG. 6 illustrates, in block diagram form, the circular echo synthesis module of the ADSL transceiver of FIG. 2;

FIG. 7 illustrates, in block diagram form, the fast Fourier transform module of the ADSL transceiver of the present invention;

FIG. 8 illustrates, in block diagram form, the time domain equalization module of the ADSL transceiver of the present invention; and

FIG. 9 illustrates, in block diagram form, the analog front-end of the ADSL transceiver of the present invention.

Detailed Description of the Drawings

According to the present invention, an ADSL transceiver includes a flexible architecture that allows the ADSL transceiver to be configured through software so that identical hardware blocks may be used to perform multiple tasks. Thus, the ADSL transceiver may be configured through software to operate as either a central office or a remote terminal without requiring a substantial amount of added circuitry. Therefore, although the ADSL standard requires that a transmission data rate at a remote terminal be significantly lower than a transmission data rate at the central office, the amount of processing that is performed at either the central office end or the remote terminal end is nearly identical. For example, when the central office end is processing data provided at a high rate in its transmit path, the remote terminal end is processing high rate data in its receive path. Similarly, when the remote terminal end is processing data provided at a low rate in its transmit path, the central office end is processing low rate data in its receive path. The ADSL transceiver recognizes that processing functions in the transmit and receive paths of each of the central office and remote terminal ends are similar in nature. Thus, hardware processing circuitry designed to accommodate data transmitted and received at higher data rates may also be used to handle data transmitted at lower rates. Stated another way, an ADSL transceiver according to the present invention recognizes that a particular processing function may be utilized in either a transmit or receive data path depending on whether the ADSL transceiver of the present

invention is configured to be the central office or the remote terminal end.

In the illustrated embodiment, the transceiver architecture is designed using a digital signal processor (DSP) core. It should be noted however that other types of processor cores could also be implemented. According to the present invention, peripheral modules, or processing elements, of the transceiver communicate with the DSP processor and are implemented as peripheral modules to the DSP processor. The DSP processor may access each of the peripheral modules through a standard memory read/write operation or through one of six programmable DMA channels. The DSP processor core may be implemented as a core of an DSP56301 single chip DSP, which is available from Motorola, Inc., of Austin, Texas.

One of the peripheral modules of the transceiver is a host processor interface which allows an external user to issue commands to configure the transceiver for operation as either the central office or the remote terminal. Furthermore, the host interface may also be accessed by the DSP processor core. It should be noted that the firmware required for performing processing tasks associated with both the central office and remote terminal is resident on the single-chip transceiver implementation of the present invention. The use of both firmware and the recognition that hardware resources may be reused allows an ADSL transceiver according to the present invention to selectively transfer data between the hardware resources and allows memory associated with the transceiver to comply with the standard set forth in the ADSL standard.

As previously mentioned, the peripheral modules of the transceiver are designed to be configurable by the DSP processor core to process tasks as either the central office or the remote terminal. One such peripheral module, a digital interface, must be able to communicate data at both a high rate and a low rate. For a high rate data path, large memories are required for frame and constellation buffers used therein. Small memories are adequate to handle the status storage in a low rate data path. Therefore, the digital interface of the present invention includes a single large memory and a single small memory for a frame buffer, and another large memory and a small memory for the constellation buffer. When at the central office, the digital interface peripheral is configured to have the large memories in the transmit path and the small memories in the receive path. At the remote terminal, the configuration is reversed. A more detailed description of operation of the digital interface peripheral will subsequently be provided.

In addition to the digital interface, a hardware fast Fourier transform (FFT) module is designed to be able to perform both a fast Fourier transform operation and an inverse fast Fourier transform operation. When the transceiver of the present invention is designed to operate as a central office, it is placed in the transmit path and is coupled to telephone line 15, and has an output coupled to software filters 22. Both echo canceller 40 and software filters 22 have outputs coupled to an input of software FFT 20. Software FFT 20 has an output coupled to low rate digital interface 18. Low rate digital interface 18 is bidirectionally coupled to small memory 14, and has an output for providing a digital output stream.

Remote terminal 30 includes a software filters block 32, a software inverse fast Fourier transform (IFFT) 34, a low rate digital interface 36, an analog and line interface 38, an echo canceller 40, a small memory 42, a large memory 44, a hardware filters block 46, a hardware fast Fourier transform (FFT) 48, and a high rate digital interface 50. Low rate digital interface 36 receives a DIGITAL INPUT STREAM. In remote terminal 30, low rate digital interface 36 is bidirectionally coupled to small memory 42, and has an output coupled to software IFFT 34. Software IFFT 34 has an output coupled to both the software filters 32 and echo canceller 40. Software filters block 32 has an output coupled to analog and line interface 38. Analog and line interface 38 is bidirectionally coupled to telephone line 15 and has an output coupled to hardware filters block 46. Both echo canceller 40 and hardware filters block 46 are coupled to an input of hardware FFT 48. Hardware FFT 48 has an output coupled to high rate digital interface 50. High rate digital interface 50 is bidirectionally coupled to large memory 44. High rate digital interface 50 provides a DIGITAL OUTPUT STREAM.

FIG. 2 illustrates an ADSL transceiver 5 in accordance with the present invention. ADSL transceiver 5 is a single integrated circuit which includes a DSP core 60, a memory 64, a voltage controlled oscillator (VCXO) 66, a host processor interface (HPI) 68, a plurality of DSP peripherals 69, a digital interface 70, and an analog front-end (AFE) 78. Note the terms "analog front end" and "analog and line interface" are used interchangeably in this specification. Digital interface 70 includes a configuration register 71 storing a control bit 72 labeled "CONRT". DSP peripherals 69 are hardware peripherals including a fast Fourier transform (FFT) module 73, a circular echo synthesis (CES) module 74, and a time domain equalizer (TEQ) module 76.

DSP core 60 has an input terminal for receiving a reset signal labeled "RESET". DSP core 60 is bidirectionally coupled to memory 64 via three dedicated buses labeled "PDB", "YDB", and "XDB". DSP core 60 is also bidirectionally coupled to a peripheral bus labeled "PIO_EB" bus 62. VCXO 66 has an input terminal for connection to a crystal and receives a signal labeled "CRYSTAL" thereon. HPI 68 bidirectionally communicates with an external host processor via a port labeled "CONTROL PORT" and bidirectionally communicates with digital interface 70. Digital interface 70 bidirectionally communicates with external memory via a port labeled "INTERLEAVER MEMORY PORT" and additional ports which supply or receive labeled "DIGITAL PORTS". DSP core 60 bidirectionally communicates

with HPI 68, digital interface 70, FFT module 73, CES module 74, TEQ module 76, and analog front-end 78 via PIO_EB bus 62. Analog front-end 78 provides information via a signal labeled "TXA PORT" and receives information via a signal labeled "RXA PORT".

FIG. 3 illustrates, in block diagram form, a configuration of ADSL transceiver 5 when operating as central office 10. When configured as central office 10, ADSL transceiver 5 comprises a digital interface 70, a gains block 80, an inverse fast Fourier transform (IFFT) 82, a clip scale 84, a clip filter 85, cyclic prefix (CP) adder 86, a high pass filter/droop correction filter 88, an analog front-end 78, a high pass filter 92, a circular echo synthesis (CES) module 94, an adder 96, an adder 98, a time domain equalizer (TEQ) module 100, a fast Fourier transform (FFT) module 102, a phase detector 104, and a frequency domain equalizer (FEQ) 106. Central office 10 also comprises a FREC 81, an IFFT 83, and a scale 87.

Digital interface 70 has an output coupled to gains block 80 to provide a signal labeled "OUTPUT DATA". Gains block 80 has an output coupled to IFFT 82 and FREC 81. FREC 81 has an output coupled to IFFT 83. IFFT 83 has an output coupled to scale 87. Scale 87 has an output coupled to adder 98. IFFT 82 has an output coupled to clip scale 84 and clip filter 85. IFFT 82 is coupled to clip scale 84 to implement an IFFT scale factor. Clip scale 84 is coupled to scale 87. An output of clip filter 85 is coupled to cyclic prefix adder 86 and CES module 94. Cyclic prefix (CP) adder 86 has an output coupled to high pass filter/droop correction filter 88. High pass filter/droop correction filter 88 has an output coupled to analog front-end 78. Analog front-end 78 has an input for receiving a signal labelled "RXA PORT", an output for providing a signal labeled "TXA PORT", and an output coupled to high pass filter 92. High pass filter 92 has an output coupled to adder 96. CES module 94 has an output coupled to adder 96. Adder 96 has an output coupled to adder 98. Adder 98 has an output coupled to TEQ/CP strip module 100. TEQ module 100 has an output coupled to FFT module 102. FFT module 102 has an output coupled to both FEQ 106 and phase detector 104. Phase detector 104 has an output coupled to analog front-end 78. FEQ 106 has an output coupled to digital interface 70 providing a signal labeled "INPUT DATA".

FIG. 4 illustrates ADSL transceiver 5 configured to operate as a remote terminal 30. Remote terminal 30 comprises a digital interface 70, a gains block 120, an inverse fast Fourier transform (IFFT) module 122, a clipping block 124, a CP adder and high pass filter 126, a droop correction filter 128, a circular echo synthesis (CES) write 130, an FREC 132, a circular echo synthesis (CES) module 134, an analog front-end 78, a time domain equalization (TEQ)/high pass filter module 136, a high pass filter and CP stripper 138, adder 142, a fast Fourier transform (FFT) module 140, adder 144, and frequency domain equalizer (FEQ) 146.

Digital interface 70 has an output coupled to gains block 120 to provide the OUTPUT DATA signal. Gains block 120 has an output coupled to IFFT module 122. IFFT module 122 has an output coupled to clipping block 124. Clipping block 124 has an output coupled to FREC 132, CES write 130, and cycle prefix (CP) adder and high pass filter 126. CP adder and high pass filter 126 has an output coupled to droop correction filter 128. Droop correction filter 128 has an output coupled to analog front-end 78. Analog front-end 78 has an input for receiving the RXA PORT signal, an output for providing the TXA PORT signal, and an output coupled to TEQ/high pass filter module 136. TEQ/high pass filter module 136 has an output coupled to high pass filter and CP strip 138. High pass filter and CP stripper 138 has an output coupled to adder 142. CES write 130 has an output coupled to CES module 134. CES module 134 has an output coupled to adder 142. Adder 142 has an output coupled to FFT module 140. FFT module 140 has an output coupled to adder 144. FREC 132 has an output coupled to adder 144. Adder 144 has an output coupled FEQ 146. FEQ 146 has an output coupled to digital interface 70 to provide an INPUT DATA signal.

FIG. 5 illustrates digital interface 70 in greater detail. Digital interface 70 generally includes a constellation circuit 150, a transmit circuit 166, a receive circuit 168, and a frame buffer circuit 170. Constellation circuit 150 includes a CONRT bit 72, a multiplexer 156, a multiplexer 154, a large memory 158, a small memory 160, multiplexer 162, and a multiplexer 164. Frame buffer circuit 170 comprises a multiplexer 172, a multiplexer 174, a large memory 176, a small memory 178, a multiplexer 180, and a multiplexer 182.

The INPUT DATA signal is provided to a first input of multiplexer 156 and a first input of multiplexer 154. An output of transmit circuit 166 is coupled to a second input of each of multiplexers 154 and 156. CONRT bit 72 is coupled to an enable input of multiplexer 154, multiplexer 156, multiplexer 162, multiplexer 164, multiplexer 172, multiplexer 174, multiplexer 180, and multiplexer 182. An output of multiplexer 156 is coupled to small memory 160. An output of small memory 160 is coupled to a first input of each of multiplexers 162 and 164. An output of multiplexer 154 is coupled to large memory 158. Large memory 158 has an output coupled to a second input of each of multiplexers 162 and 164. An output of multiplexer 162 provides the OUTPUT DATA signal. An output of multiplexer 164 is coupled to receive circuit 168. Receive circuit 168 is coupled to a first input of each of multiplexers 172 and 174. A FRAME INPUT signal is provided to a second input of each of multiplexers 172 and 174. An output of multiplexer 172 is coupled to small memory 178. An output of multiplexer 174 is coupled to large memory 176. An output of small memory 178 is coupled to a first input of each of multiplexers 180 and 182. An output of large memory 176 is coupled to a second input of multiplexers 180 and 182. The output of multiplexer 182 is cou-

pled to transmit circuit 166. An output of multiplexer 180 provides a FRAME OUTPUT signal.

FIG. 6 illustrates circular echo synthesis (CES) module 74 in greater detail. CES module 74 includes a coefficient memory 200, a parameter registers portion 202, a command and status register 204, a decode and control circuit 206, a present data buffer 208, a subtractor 210, a subtract terms buffer 212, a past data buffer 214, a process control circuit 216, a multiply and accumulate circuit (MAC) 218, and an output data buffer 220.

PIO_EB bus 62 is coupled to coefficient memory 200, parameter registers portion 202, command and status register 204, decode and control circuit 206, present data buffer 208 and output data buffer 220. Coefficient memory 200 has an output coupled to MAC 218. Decode and control circuit 206 has an output coupled to each of coefficient memory 200, parameter registers portion 202, command and status register 204, present data buffer 208, and output data buffer 220. Parameter registers portion 202 has an output coupled to process control circuit 216. Command and status register 204 has an output coupled to process control circuit 216. Decode and control circuit 206 has an output coupled to process control circuit 216. Process control circuit 216 has an output coupled to present data buffer 208. Present data buffer 208 has an output coupled to past data buffer 214 and subtractor 210. Subtractor 210 has an output coupled to subtract terms buffer 212. Process control circuit 216 has an output coupled to subtract terms buffer 212 and past data buffer 214. Subtract terms buffer 212 has an output coupled to MAC 218, and an output coupled to output data buffer 220. Process control circuit 216 has an output coupled to MAC 218. MAC 218 is coupled to output data buffer 220. Process control circuit 216 has an output coupled to output data buffer 220.

FIG. 7 illustrates fast Fourier transform (FFT) module 73 in greater detail. FFT module 73 comprises a register decode circuit 300, a command and status register 302, an FFT control circuit 304, an IN register 306, a transform engine 308, and an out register 310. PIO_EB bus 62 is coupled to register decode circuit 300, command and status register 302, IN register 306, and out register 310. Register decode circuit 300 has an output coupled to command and status register 302, FFT control circuit 304, IN register 306, and out register 310. A plurality of outputs of FFT control circuit 304 are coupled to PIO_EB bus 62. IN register 306 has an output coupled to transform engine 308. FFT control circuit 304 has an output coupled to out register 310 and transform engine 308. Transform engine 308 has an output coupled to out register 310.

FIG. 8 illustrates time domain equalization (TEQ) module 76 in greater detail. TEQ module 76 comprises a coefficient register 400, an input register 402, a tap coefficient memory 404, a multiplexer (MUX) 406, a receive sample memory 408, a multiply-accumulate circuit (MAC) 410, a process control circuit 412, a decode and control circuit 414, output register 416, and a command and status register 418. PIO_EB bus 62 is coupled to each of coefficient register 400, input register 402, decode and control circuit 414, output register 416, and command and status register 418. Coefficient register 400 has an output coupled to tap coefficient memory 404. Tap coefficient memory 404 has an output coupled to a first input of MAC 410. Decode and control circuit 414 has outputs coupled to coefficient register 400, input register 402, process control circuit 412, output register 416, and command and status register 418. Input register 402 is coupled to MUX 406. Process control circuit 412 has an output coupled to MAC 410. Command and status register 418 has an output coupled to MUX 406, and output register 416. MAC 410 has an output coupled to MUX 406. MUX 406 has an output coupled to receive sample memory 408. Receive sample memory 408 has an output coupled to a second input of MAC 410.

FIG. 9 illustrates, in block diagram form, analog front-end 78 of FIG. 2. Analog front-end 78 includes a register 504, an interpolating filter 500, a modulator 502, a digital-to-analog converter (DAC) 506, an analog smoothing filter 507, a driver 508, a programmable equalizer (PEQ) 514, an analog-to-digital converter (ADC) 512, a decimation filter 513, a register 510, a voltage controlled oscillator (VCXO) 518, a clock block 516, and a register 520. Additionally, analog front-end 78 is coupled to an external circuit comprising an external line driver labeled "TXLD" 604, a hybrid circuit 606, an attenuator 602, a crystal 600, an inductor-capacitor high pass (LC HP) filter 608, and a POTS splitter 620.

PIO_EB bus 62 is coupled to registers 504, 510 and 520. PIO_EB bus 62 is also coupled to control register 522. Register 504 has an output coupled to an interpolating filter 500. Interpolating filter 500 has an output coupled to modulator 502. Modulator 502 has an output coupled to DAC 506. DAC 506 has an output coupled to analog smoothing filter 507. Analog smoothing filter 507 has an output coupled to driver 508. Driver 508 has an output coupled to TXLD 604. TXLD 604 has an output coupled to hybrid circuit 606. Hybrid circuit 606 is bidirectionally coupled to LC HP filter 608. LC HP filter 608 is bidirectionally coupled to POTS splitter 620. Hybrid circuit 606 also has an output coupled to attenuator 602. Attenuator 602 has an output coupled to PEQ 514 of AFE 78. PEQ 514 has an output coupled to ADO 512. ADO 512 has an output coupled to decimation filter 513. Decimation filter 513 has an output coupled to register 510. Control register 522 has an output coupled to VCXO register 520 and clock block 516. VCXO register 520 has an output coupled to VCXO 518. VCXO 518 is coupled to clock block 516, and crystal 600. Clock block 516 has outputs for providing clocks to analog and digital components labeled "ANALOG CLOCKS" and "DIGITAL CLOCKS", respectively.

DESCRIPTION OF OPERATION

Referring to FIG. 1, ADSL system 1 illustrates the required configuration for each of central office 10 and remote terminal 30. As previously mentioned, when central office 10 is processing data transmitted at a high rate in its transmit path, remote terminal 30 is processing high rate data in its receive path. Similarly, when remote terminal 30 is processing data transmitted at a low rate in its transmit path, central office 10 is processing low rate data in its receive path. As functions implemented in hardware are typically executed more quickly than those implemented in software, for optimal speed, central office 10 implements selected functions in its transmit path in hardware when it is transmitting data at a high rate. Similarly, remote terminal 30 will implement functions in its receive path in hardware when it is receiving data transmitted at a high data rate. When remote terminal 30 is transmitting data at a lower rate, the functions to be executed in the transmit path may be implemented in software. As well, central office 10 may also implement functions in its receive path in software when data is provided at a lower data rate by remote terminal 30. The use of hardware functions on data paths having high transfer rates and software functions on data paths having lower data transfer rates is illustrated in FIG. 1. There, the desired implementation of central office 10 and remote terminal 30 are illustrated.

According to the present invention, a single ADSL transceiver 5 provides a flexible and configurable circuit which may be programmed to operate as either central office 10 or remote terminal 30 (as illustrated in FIG. 1). ADSL transceiver 5 provides hardware processing resources whose inputs and outputs may be selectively configured by a user to implement either central office 10 or remote terminal 30 in an efficient manner. Stated another way, ADSL transceiver 5 may be selectively configured as either a central office 10 or a remote terminal 30 and is not required to be exclusively one or the other. This selectivity allows a single integrated circuit to be designed and manufactured for both CO and RT equipment.

FIG. 2 illustrates ADSL transceiver 5 in greater detail. DSP core 60 accesses each of a plurality of transceiver peripheral modules via PIO_EB bus 62. The plurality of peripheral modules include host processor interface (HPI) 68, digital interface 70, FFT module 73, CES module 74, TEQ module 76, and analog front-end 78. It should be noted that peripherals having additional functionality may be added as needed and the present invention is not limited to the particular peripheral modules disclosed herein. DSP core 60 accesses each peripheral module through a standard memory read/write operation or through one of six programmable DMA channels. The DMA channels may be selectively programmed to access each of the plurality of peripheral modules in a different order as required by the configuration of ADSL transceiver 5 as central office 10 or as remote terminal 30. HPI 68 allows an external user to issue commands to configure transceiver 5 as either central office 10 or remote terminal 30. Once the user has configured ADSL transceiver 5 to function as either central office 10 or remote terminal 30, DSP core 60 selects the appropriate firmware for executing the desired function from memory 64 via the program data bus (PDB).

The manner by which transceiver 5 is selected to be CO or RT may be set by the user through HPI 68, or may be auto-configured via twisted pair signal 15 in the manner described in copending application attorney docket no. SC-90263A. In order to reconfigure transceiver 5 to operate as either CO or RT, it is necessary to drive a control signal to each affected module. In the illustrated embodiment, each affected module has a configuration register which stores the control bit for that module. In other embodiments, however, the transceiver may have a global configuration register which provides the same control signal to each affected module, or other appropriate means such as a dedicated pin. As an example, FIG. 2 illustrates configuration register 71 of digital interface 70. Configuration register 71 stores the CONRT control bit, which when set to a binary 1, indicates that digital interface 70 is to operate in central office equipment, and when set to binary 0, indicates that digital interface 70 is to operate in remote terminal equipment.

Assume the external user desires to configure ADSL transceiver 5 as central office 10. FIG. 3 illustrates this configuration in greater detail. It should be noted that in FIG. 3 all shaded blocks are implemented as hardware and all unshaded blocks are implemented as firmware. As previously mentioned, the firmware is stored in memory 64. Digital interface 70 receives a plurality of serial digital data streams via the plurality of digital ports. Digital interface 70 provides those functions which are responsible for data transport. Digital data may be transported on any one of a plurality of programmable bearer channels. The plurality of programmable bearer channels are multiplexed together in a data buffer where they are synchronized into an appropriate one of the plurality of programmable bearer channels as determined by the ADSL standard. The framed data is then subjected to various operations. The data resulting from these operations is provided to a constellation output buffer (not shown in detail herein) as a plurality of complex numbers representing DMT tones. The complex numbers are subsequently transferred via the OUTPUT DATA signal.

The OUTPUT DATA signal is provided to gains block 80. Gains block 80 represents firmware which multiplies the data values transferred via the OUTPUT DATA signal by a calculated gain value which was previously computed as the product of three separate values. A first value used to generate the calculated gain value is a constellation normalizing constant which scales a plurality of constellations so that they all have a same

average energy. A second value is a fine adjustment gain which is computed during initialization as part of a bit-loading algorithm. A third value is an equalizer gain which appropriately scales the carriers of ADSL transceiver 5 to undo the ripple in an analog pass band. The constellation normalizing constant and the equalizer gain are known before initialization begins, and their product is used at all times. The fine adjustment gain is included in the gain value once steady state transmission has begun and is changed only if a bit swapping operation takes place.

Gains block 80 provides adjusted data to IFFT 82 via a DMA channel of DSP core 60. IFFT 82 corresponds to FFT module 73 of FIG. 2 configured as an inverse fast Fourier transform. IFFT 82 subsequently converts the adjusted data values from the frequency domain to the time domain. Together, clip scale 84 and clip filter 85 provide the necessary limiting of input data values to prevent overflow in subsequent operations. It should be noted that an IFFT scale factor must be provided to clip scale 84 to calculate the clip scale value. Cyclic prefix adder 86 adds a cyclic prefix to a frame of data currently being operated upon. The cyclic prefix includes the last 32 samples of the frame which is copied and placed at the beginning of the same frame. The resulting frame is stored in memory 64 of ADSL transceiver 5.

From cyclic prefix (CP) adder 86, the resulting frame is provided to High pass filter/Droop correction filter 88. Because ADSL transceiver 5 is functioning as a central office, the High pass filter/Droop correction filter 88 function is implemented by TEQ module 76 of FIG. 2, which receives data via the DMA and performs a high pass filter operation using a biquad filter as well as droop correction using an FIR filter. TEQ module 76 will subsequently be described in greater detail in conjunction with FIG. 8 below.

High pass filter/Droop correction filter 88 provides an output to analog front-end 78. This is accomplished via a third DMA channel of DSP core 60 which moves the results of the operations executed by TEQ module 76 to Analog front-end 78 which performs a filtering and a digital-to-analog conversion operation to provide an analog signal via the TXA PORT. It should be noted that when ADSL transceiver 5 is configured as central office 10, the ADSL standard requires that transceiver 5 transmit data to the remote terminal at a higher rate than the remote terminal transmits data back to the central office. Furthermore, it should be noted that because data is transmitted at the higher rate, where necessary, functions to be executed in the transmit path of central office 10 are implemented as hardware (as indicated by the shaded boxes).

Analog front-end 78 receives the analog RXA PORT signal. This analog signal is converted by an analog-to-digital converter and the resulting digital signal is transferred via a fourth DMA channel to memory 64. From there, transceiver 5 implements the remaining functions of central office 10 in firmware residing in memory 64. First, a high pass filter operation 92 is executed using firmware. Next, adder 96 preconditions a resulting signal for the subsequent echo cancellation operation. Adder 98 then removes an echo from the preconditioned signal. Subsequently, TEQ/CP strip module 100 performs time domain equalization, which shortens the response of the channel, and removes the cyclic prefix. FFT module 102 then performs a translation of the signal provided by TEQ module 100 from the time domain to the frequency domain. FEQ 106 subsequently performs frequency equalization on the resulting signal to generate the INPUT DATA signal. FEQ 106 is implemented to undo any magnitude and phase distortion the signal may have experienced in the channel. Digital interface 70 recovers digital data from the INPUT DATA signal which is further operated upon to provide data in a framed format. The framed data is subsequently demultiplexed and provided to each of the plurality of serial digital data outputs provided by the plurality of digital ports.

Transceiver 5 also implements a scheme for echo cancellation. FREC 81 receives the adjusted data provided by gains block 80 and creates an estimate of the echo in the frequency domain. IFFT 83 subsequently converts the estimate from the frequency domain to the time domain. Scale 87 then scales the time domain estimate of the echo to match the scaling done in the transmit path. Scale 87 provides an estimated echo value. CES module 94 receives data from clip filter 85 via one of the DMA channels of DSP 60. CES module 94 corresponds to CES module 74 of FIG. 2. CES module 94 removes the effect of interference in the echo signal. The cancellation value generated by CES module 94 is subsequently subtracted from a filtered receive signal provided by high pass filter 92. The estimated echo value provided by scale 87 is then subtracted using adder 98.

A signal generated by FFT module 102 is also provided to phase detector 104. Phase detector 104 derives timing information from a pilot tone of the receive signal. This information is then used to lock a sampling clock of the analog-to-digital and digital-to-analog converters in analog front-end 78.

FIG. 4 illustrates ADSL transceiver 5 configured to operate as remote terminal 30. When operating as remote terminal 30, digital interface 70 provides those functions which are responsible for data transport. Digital data may be transported on any one of a plurality of programmable bearer channels. The data values communicated by the plurality of programmable bearer channels are multiplexed together in a data buffer, and then synchronized into data transmission frames which comply with the ADSL standard. The framed data is then subject to various operations. The data resulting from these operations is provided in a constellation output buffer as complex numbers representing DMT tones. The complex numbers are subsequently pro-

vided to gains block 120.

Gains block 120 implements a similar function to gains block 80 of FIG. 3. Specifically, gains block 120 adjusts the complex numbers provided by the OUTPUT DATA to generate a plurality of adjusted gain values. The adjusted gain values are provided to IFFT module 122. It should be noted that IFFT module 122 is implemented in firmware whereas IFFT 82 of FIG. 3 is implemented in hardware. IFFT module 122 is implemented in firmware because when ADSL transceiver 5 is operating as remote terminal 30, the data rate at which it is required to transmit information is slow enough to implement the transfer function in software. IFFT module 122 converts the adjusted gain values from the frequency domain to the time domain.

Subsequently, the converted values are provided to clipping block 124. Clipping block 124 limits the output value to prevent overflow in subsequent operations. The limited values are then provided to CP adder and high pass filter 126 and prepended with a cyclic prefix (CP), and, unlike high pass filter/droop correction filter 88 of FIG. 3, high pass filter 126 is implemented in firmware. Again, high pass filter 126 is implemented in firmware rather than hardware because the data transmission rate required by remote terminal 30 is slow enough to allow for the use of firmware. The filtered values provided by high pass filter 126 are subsequently provided to droop correction filter 128. As with high pass filter 126, droop correction filter 128 is implemented as firmware rather than hardware because a lower data transmission rate is used. Droop correction filter 128 subsequently provides the corrected, filtered values to analog front-end 78 via a first DMA channel of DSP core 60. Analog front-end 78 performs a filtering operation and a digital-to-analog conversion operation to provide an analog signal via the TXA PORT.

An analog signal is provided to analog front-end 78 via an RXA PORT. Analog front-end 78 subsequently performs an analog-to-digital conversion and provides a digital signal to TEQ/high pass filter module 136 via a second DMA channel of DSP core 60. TEQ/high pass filter module 136 corresponds to TEQ module 76 of FIG 2. TEQ/high pass filter module 136 performs a time domain equalization function to shorten a channel response of the digital input signal. TEQ/high pass filter module 136 also performs a high pass filter function. It should be noted that TEQ/high pass filter module 136 and the high pass filter function implemented therein are implemented in hardware because they are in the receive path of remote terminal 30. As previously discussed, the receive path of remote terminal 30 is required to receive data at a highest data transmission rate.

An output of TEQ/high pass filter module 136 is provided to DSP core 60 via a third DMA channel of DSP core 60. DSP core 60 performs a second high pass filter function in high pass filter 138 and stores a result in memory 64. High pass filter 138 is implemented in firmware. The output of high pass filter 138 is stripped of the cyclic prefix (CP) and provided to adder 142. A result of adder 142 is provided to FFT module 140. FFT module 140 performs a time domain to frequency domain conversion in hardware. It should be noted that FFT module 140 corresponds to FFT module 73 of FIG. 2. A result of the operation executed by FFT module 140 is provided to adder 144 via a fourth DMA channel of DSP core 60. An output of adder 144 is provided to FEQ 146 which corrects any magnitude and phase distortion the signal may have experienced in the channel. The output of FEQ 146 is then sent to digital interface 70. Digital interface 70 operates on the input data and provides it to a frame buffer. The data in the frame buffer is then demultiplexed into the plurality of digital data streams provided by the plurality of digital ports.

As with central office 10, remote terminal 30 implements an echo cancellation scheme. To implement this scheme, an output of clipping block 124 is converted to the frequency domain and FREC 132 generates an echo estimate in response thereto. Additionally, CES write 130 provides data transferred from memory 64 to CES module 134. It should be noted again that CES module 134 corresponds to CES module 74 of FIG. 2. In CES module 134, a cancellation signal is calculated for removing the effects of interference from the echo in the receive signal. The cancellation signal is subsequently subtracted from the received signal using adder 142. Additionally, the estimated echo value is subtracted from a filtered and demodulated value provided by FFT module 140 using adder 144.

DESCRIPTION OF THE PERIPHERAL MODULES

Digital interface 70 is illustrated in greater detail in FIG. 5. During operation, a user will write the CONRT bit 72 to indicate whether or not ADSL transceiver 5 should operate as a central office or a remote terminal. If ADSL transceiver 5 should be operated as a central office, CONRT bit 72 is set to a logic level 1. When the CONRT bit 72 is set to a logic level 1, data transferred via frame input signal is provided to multiplexer 172 and multiplexer 174. Multiplexer 172 will not pass the information to small memory 178. However, multiplexer 174 will pass the information to large memory 176. Large memory 176 will subsequently provide a corresponding data value to each of multiplexer 180 and 182. Again, the CONRT bit selectively enables multiplexers 180 and 182. When so enabled, multiplexer 182 provides data by large memory 186 to transmit circuit 166. However, multiplexer 180 does not output any data. Transmit circuit 166 passes the data to each of the multiplexers 154 and 156. There, the CONRT bit selectively enables each of multiplexers 154 and 156 to provide data to large memory 158 and small memory 160, respectively. Because the CONRT bit is a logic level 1, multiplexer 154 provides the access information to large memory 158. Subsequently, multiplexer 162 provides the data output from

large memory 158 as an output data signal. Thus, it is illustrated that when digital interface 70 is configure by the CONRT bit 72 to operate as a central office, larger buffers, large memory 158 and large memory 176, are utilized along the transmit path which is the path from FRAME INPUT to OUTPUT DATA because ADSL transceiver 5 will be required to provide data at a higher transmission rate and, therefore, enough data must be buffered to provide the output data signal at the required transmission rate without waiting. Also, when ADSL transceiver is configured to operate as the central office, input data is provided at a slower data rate. Therefore, only small buffer memories are required and implemented in the receive path of the digital interface, which is the path from INPUT DATA to frame output of the present invention. Note that while the digital interface 70 accesses the CONRT bit directly, a different or mirror control register can reside in a peripheral to avoid accessing a register over the system bus.

FIG. 6 illustrates, in block diagram form, circular echo synthesis (CES) module 74 of ADSL transceiver 5 of FIG. 2. CES module 74 performs the time domain echo cancellation of ADSL transceiver 5. CES module 74 removes the effects of the intersymbol interference from the echo symbols and makes the echo symbols look like a circular convolution of the transmitted symbol and the echo channel response. Creating the circular convolution is necessary in order to allow further frequency domain echo cancellation to estimate and remove the echo with simple block arithmetic rather than long linear convolutions or complex finite impulse response (FIR) filter operations.

In general, CES module 74 inputs the digital transmit signal and filters this signal in a digital finite impulse response (FIR) filter. The coefficients of the filter represent the impulse response of the channel, and are estimated at initialization. The output of this filter is an estimate of the echo of the transmit signal reflected back into the received signal. By subtracting the output of this filter from the received signal, CES module 74 is able to construct a more accurate representation of the signal sent by the remote station.

CES module 74 performs different operations depending on whether ADSL transceiver 5 is configured as CO or as RT. When configured as RT, CES module 74 interpolates a digital representation of the analog transmit signal to provide a digital cancellation signal. When configured as CO, CES module 74 performs a different operation to provide the digital cancellation signal. In the CO case, CES module 74 receives a digital representation of the analog transmit signal and decimates said second cancellation signal to provide the cancellation signal. In either case, transceiver 5 subtracts the cancellation signal from the received signal to provide a preconditioned version of the received signal for echo cancellation. The reuse of the same hardware in CES module 74 between CO and RT mode allows a significant savings in circuit area.

In greater detail, CES module 74 is a hardware peripheral coprocessor which communicates with DSP core 60 over PIO_EB bus 62 through decode and control circuit 206. CES module 74 acts as a slave device which DSP core 60 is able to read from and write to. Decode and control circuit 206 decodes a 12-bit address conducted on PIO_EB bus 62 to recognize operations that DSP core 60 conducts with CES module 74. When decode and control circuit 206 recognizes an access from DSP core 60, it provides the control signals to the other internal blocks of CES module 74 which are necessary to load data into the registers or buffers and to write data onto PIO_EB bus 62.

Command and status register 204 provides the primary mechanism for communication between DSP core 60 and CES module 74. Command and status register 204 provides configuration and control bits for CES module 74 and contains flags that can be read by DSP core 60. The commands include software reset, CES enable, cyclic prefix indicator, and enable signals for the interrupt request that indicates a CES calculation is done.

Parameter registers portion 202 hold parameters that CES module 74 uses during its echo cancellation calculations. The parameters include the amount of symbol misalignment, the echo channel impulse response length, and certain boundary values to perform the addressing of the data buffers. Parameter registers portion 202 are loaded during initialization and remain static during operation of CES module 74. Coefficient memory 200 provides buffering for echo channel impulse response coefficients. These coefficients are determined during the initial training period and loaded into coefficient memory 200 by DSP core 60. CES module 74 requires samples of the past, present, and next transmit symbols in order to perform the time domain echo cancellation. These samples must be available during the echo cancellation calculations. These samples are stored in present data buffer 208 and past data buffer 214.

Subtractor 210 takes the difference between a sample in past data buffer 214 and the corresponding sample in present data buffer 208. The differences, provided at the output of subtractor 210, are stored in subtract terms buffer 212. The subtract terms are multiplied by the estimated echo channel impulse response coefficients to form the cancellation vector. The multiplication and summing operation occurs in MAC 218, which does the actual calculation of the cancellation vector elements. Each cycle during the calculation, MAC 218 reads a subtraction term from the subtract terms buffer 212 and a corresponding echo channel impulse response coefficient from coefficient memory 200.

Process control circuit 216 is a state machine controller which coordinates all of the functions in CES module 74. Process control circuit 216 controls MAC 218, subtract terms buffer 212, and coefficient memory 200, to implement the interpolation or decimation

required to match transmit and receive sample rates. When configured as CO, each transmit symbol contains 512 samples plus a 32 sample cyclic prefix, while each receive symbol contains only 64 samples plus a 4-sample cyclic prefix. Since CES module 74 generates the cancellation vector at the highest rate, it contains 544 samples. CES module 74 thus decimates the cancellation vector by a factor of eight to match the receive data sample rate. CES module 74 accomplishes the decimation by discarding seven of every eight elements of the cancellation vector. Rather than perform all of the calculations needed for all the elements of the cancellation vector, however, CES module 74 only calculates the elements that will be used.

When configured as RT, each transmit symbol contains 64 samples plus a 4-sample cyclic prefix. Each transmit symbol must be interpolated up to the higher rate before the echo cancellation calculation is performed. This is accomplished by inserting seven zeros between each transmit data sample. The result is that seven of every eight subtraction terms that are generated will be zero. Rather than performing the calculations associated with the subtraction terms which are zero, CES module 74 only performs the calculations on the non-zero terms.

FIG. 7 illustrates, in block diagram form, fast Fourier transform (FFT) module 73 of ADSL transceiver 5. FFT module 73 performs forward and inverse transformations between the time domain and frequency domain. These conversions are necessary to form and interpret the complex symbols used in the discrete multi-tone (DMT) system of ADSL. These transformations are performed on the asymmetric data which is transmitted at a high rate from the CO to the RT. Thus, when ADSL transceiver 5 is configured as CO, FFT module 73 performs an inverse FFT operation on a digital representation of the analog transmit signal. When ADSL transceiver 5 is configured as RT, FFT module 73 performs an FFT operation on a digital representation of the analog receive signal using the same circuitry.

Command and status register 302 is a unified register for communication between DSP core 60 and FFT module 73. Command and status register 302 is only connected to the GDB portion of PIO_EB bus 62. Control bits in command and status register 302 are provided to enable interrupts and DMA requests to DSP core 60. Interrupts occur for the input ready, output ready, and error conditions. DMA requests occur for input and output vector transfer. Command and status register 302 also includes bits to indicate the state of FFT module 73 to DSP core 60.

IN register 306 is a 24-bit register which receives input data from both the Module DMA Data Bus (MDDB) and Global Data Bus (GDB) portions of PIO_EB bus 62. This input data is in fractional two's complement form that represent either time domain samples, or frequency domain complex samples. In the illustrated embodiment, FFT module 73 discards the four least significant bits to adapt the 24-bit quantity to the 20-bit internal size. Out register 310 provides the output of the transform operation to DSP core 60. The output data is in the form of 24-bit fractional two's complement numbers that represent either time domain samples, or frequency domain complex samples. FFT module 73 sets the four least significant bits to zero to convert the 20-bit internal size into the 24-bit external format.

Transform engine 308 is an arithmetic unit which performs arithmetic and logical operations necessary for the FFT and IFFT algorithms. Quadrature amplitude modulation involves the multiplication of a complex phasor x by a sinusoidal modulation function, such as the complex exponential. This modulation function is called the carrier. DMT modulation extends this process by taking a vector of complex phasors and performing a dot-product of these with a vector of evenly spaced carriers. This DMT modulation is then equivalent to the discrete Fourier transform (DFT). The DFT is discrete in both time and frequency. Mathematically, the forward complex DFT performs the following calculation:

$$X_k = S\, x_n W_N^{nk} \qquad [1]$$

where $W_N = e^{-j2\pi/N}$, N defines the length of the DFT, and the summing interval is from n = 0 to (N - 1).

The inverse complex DFT, or IDFT, performs the following calculation:

$$x_n = (1/N)\, S\, X_k W_N^{-nk} \qquad [2]$$

where the summing interval is from k = 0 to (N - 1).

FFT module 73 allows configuration as either CO or RT by recognizing that the same arithmetic hardware can be used to perform the calculations of equations [1] and [2]. Thus, transform engine 308 includes a register file, separate X and Y random access memories (RAMs), an arithmetic logic unit, a read-only memory (ROM) for storing parameters, a multiply-and-accumulate unit (MAC), a separate accumulator, and a rounding function which are used commonly when FFT module is configured as either CO or RT, thus saving circuit area and allowing transceiver 5 to efficiently implement both functions.

FFT control circuit 304 is a state machine which controls the operation of transform engine 308 and out register 310. In addition, if a corresponding enable bit in command and status register 302 is set, FFT control circuit 304 provides the interrupt request or DMA request to DSP core 60 via PIO_EB bus 62. FFT control circuit 304 starts the transform engine after the input vector has been completed. The input vector is received by in register 306. FFT control then performs the DFT or IDFT as appropriate on that new vector. Finally, FFT control circuit 304 causes the output of transform engine 308 to be written into out register 310, and updates command and status register 302, possibly issuing an interrupt or DMA request. FFT control circuit

304 continues this writing sequence until the output vector is finished, at which time FFT control circuit 304 signals that the output buffer is ready.

FIG. 8 illustrates, in block diagram form, time domain equalization (TEQ) module 76 of transceiver 5. TEQ module 76 includes two flexible filter structures that can be used to perform a variety of filtering tasks. When transceiver 5 is configured as CO, TEQ module 76 is placed in the transmit path. DSP core 60 provides coefficients to TEQ module 76 to configure the FIR filter to perform roll off compensation for the analog filter. The FIR filter compensates for the droop in the transmit spectrum caused by the comb filter in the following digital-to-analog converter. TEQ module 76 configures the biquad filter to operate on the output of the FIR filter. The biquad filter is an IIR filter and DSP core 60 configures it to operate as a high-pass filter which limits the amount of low frequency energy in the transmitted ADSL signal.

When configured as RT, the FIR filter structure is used to perform a filtering operation that effectively shortens the response length of the channel. The shortened length is one greater than the length of the cyclic prefix in order to eliminate intersymbol and intercarrier interference in the received data. In RT mode, TEQ module 76 configures the biquad filter to operate on input data received from DSP core 60. The biquad filter structure also is used in the receive path to implement one of the two biquad filters required to remove signal energy in the POTS (plain old telephone system) frequency band from the received ADSL signal.

Command and status register 418 is a unified register for communication between DSP core 60 and TEQ module 76. Command and status register 418 is only connected to the GDB portion of PIO_EB bus 62. Control bits in command and status register 418 are provided to configure and control the FIR and biquad filters and contain status flags that can be read by DSP core 60. Control information includes software reset, enable signals for each filter, enable signals for interrupt requests or DMA requests to transfer input and output data, and an enable signal to allow FIR filter coefficients to be loaded into tap coefficient memory 404.

TEQ module 76 is a hardware coprocessor that communicates with DSP core 60 over PIO_EB bus 62. TEQ module 76 acts as a slave device which is read from and written to by DSP core 60. Decode and control circuit 414 performs address decoding and handshaking for received commands. When a command has been decoded, decode and control circuit 414 provides the control signals to the other blocks of TEQ module 76 to operate in the selected mode. Process control circuit 412 is a state machine controller that coordinates the functions in TEQ module 76. Process control circuit 412 loads the tap coefficients for the filters, receives the appropriate input data and loads it into receive sample memory 408, coordinates the multiply-accumulate function in MAC 410, and stores the filtered output sample to output register 416.

TEQ module 76 includes several blocks which have both FIR and biquad filter portions and these separate portions are noted where appropriate. Input register 402 has a first portion for receiving input data for the FIR filter, and a second portion for receiving input data for the biquad filter. For each new sample that DSP core 60 provides to input register 402, TEQ module 76 provides one filtered output sample to a corresponding portion of output register 416. A first portion of coefficient register 400 receives and stores an FIR filter tap coefficient which is thereafter stored in a first portion of tap coefficient memory 404. A second portion of coefficient register 400 receives and stores a biquad filter coefficient which is thereafter stored in a second portion of tap coefficient memory 404. These coefficients are determined during training and in the illustrated embodiment, tap coefficient memory 404 stores seventeen 22-bit FIR filter tap coefficients and five 22-bit biquad filter coefficients. Receive sample memory 408 has a first portion for storing the 17 most recent samples of data as they are received at input register 402 for use in the FIR filter, and a second portion for storing the current sample and two previously computed intermediate node values for use in the biquad filter. MAC 410 includes a single multiply-and-accumulate unit, which first multiplies the FIR filter coefficients by the corresponding samples and accumulates the sum of seventeen multiplications before providing the filtered result to output register 416. It then multiplies the input data and stored intermediate data samples by the five biquad tap coefficients in tap coefficient memory 404, and accumulates these products into the new intermediate and filtered values. The result of the biquad filter operation is a filtered sample which is provided to output register 416.

MUX 406 is selectable between CO and RT mode to selectively provide alternate sources of input data for the biquad filter. When the transceiver is in steady state operation and configured as a CO or an RT, the command and status register 418 configures MUX 406 to select the output of the FIR MAC operation to input to the biquad filter portion of receive sample memory 408. During training, when configured as RT, the command and status register 418 configures MUX 406 to select input data received by the biquad portion of input register 402 to input to the biquad filter portion of receive sample memory 408. The reconfiguration of the source of input data for the biquad filter allows TEQ module 76 to share resources and transceiver 5 to efficiently operate as either CO or RT.

FIG. 9 illustrates, in block diagram form, analog front-end (AFE) 78 of transceiver 5. Analog front-end 78 includes a DAC function which is implemented by interpolating filter 500, modulator 502, DAC 506, and analog smoothing filter 507, for use in the transmit path, and an ADC function implemented by ADC 512 and decimation filter 513 for use in the receive path. Analog front-end 78 is selectively configured to operate differently in either

CO or RT mode because of the asymmetric nature of the ADSL communication system. There are two aspects of this asymmetric nature.

First, the receive path is relatively high-rate data if transceiver 5 is configured as RT, but relatively low-rate data if transceiver 5 is configured as CO. When configured as an RT, the receive path of the transceiver utilizes both second-order stages of the cascaded fourth-order sigma-delta modulator to convert the analog data to digital data, and the entire decimation filter 513 is used to implement a fifth order decimation on the output from the modulators. When configured as a CO, the receive path of the transceiver utilizes a single second-order stage of the cascaded sigma-delta modulator to convert the received analog data to digital data, and only a portion of the decimation filter 513 is used to implement a third-order decimation on the output from the modulators.

Second, the RT transmitter requires a different interpolator than the CO transmitter. As such, the configuration register value CONRT is used to determine what interpolation order should be used. In one embodiment, an interpolation order of three is used when in CO mode, and an order of five is used when in RT mode. In addition, it would be understood by one skilled in the art, that the smoothing filter 507 characteristics can vary based on whether operating in RT mode or in CO mode.

Control register 522 is a unified register for communication between DSP core 60 and analog front-end 78. Control register 522 is only connected to the GDB portion of PIO_EB bus 62. Control bits in command and status register 418 are provided to select between CO and RT modes, to select the oversampling ratio of DAC 506, to configure PEQ 514, to enable a power cut clipping and impulse approximation clipping algorithms, and to enable low power mode.

VCXO 518 is a pulled-crystal oscillator designed for use with external crystal 600. VCXO 518 has a nominal frequency which is set by crystal 600 but the frequency may be "pulled" higher or lower based on the value stored in VCXO register 520. The central office crystal will lock onto the frequency of the free running crystal at the remote terminal. Thus if transceiver 5 is RT, VCXO will normally be free running. The output of VCXO 518 is used by clock block 516 to generate both the ANALOG CLOCKS and the DIGITAL CLOCKS.

Register 504 stores an input to the AFE 78. The interpolator 500 performs a twenty-five times sample rate increase when in CO mode, and a 200 times sample rate increase when configured as an RT. When configured as RT, the interpolator provides a four stage cascaded integrated comb (CIC) filter to accommodate the high filtering requirements of the RT transmitter. When configured as CO, the interpolator only provides a second-order CIC filter. Preferably, the interpolator includes four stages, only two of which are used in CO mode. The modulator is a second order sigma-delta modulator with a three-bit quantizer. DAC 506 converts the 3-bit output of modulator 502 and converts it into an analog signal. The analog lowpass filter reduces quantization noise which modulator 502 has shifted out of the passband. Driver 508 is a variable gain driver which in conjunction with TXLD 604 provides a 20 dBm signal to a 200 ohm differential resistive load that is the series connection of 100 ohms of source resistance and 100 ohms of line impedance, assuming a 1:1 transformer is used.

Attenuator 602 is formed with off-chip discrete elements and an on-chip variable resistance. The off-chip discrete elements include series 1 kilo-ohm resistors in series with positive and negative outputs of hybrid circuit 606, and a 120 nano-farad capacitor in series with a 20 milli-Henry inductor connected between the positive and negative outputs. The on-chip resistance can provide values of open, 10.6kΩ, 4.8kΩ, 3.0kΩ, 2.0kΩ, . . . , 200Ω, to produce attenuation of 0dB, 1.5dB, 3dB, . . . , 21dB with the external 1KΩ resistor pair. PEQ 514 is an analog filter which provides a variable gain and provides a zero in the transfer function if the appropriate bit in control register 522 is set.

ADO 512 is a multi-bit, fourth-order sigma-delta ADC which is a cascade of two single bit second-order loops. When transceiver 5 is configured as RT, ADC 512 uses the whole fourth order modulator, and the output of the two cascaded loops are input to a recombination filter. When transceiver 5 is configured as CO, however, ADC only uses one of the second order loops without the recombination filter. The output of the modulator is decimated in a 28-bit digital CIC filter, which provides a large amount of lowpass filtering. Again in CO mode ADC 512 uses only a portion of the decimator that ADC 512 uses in RT mode. The decimator converts the one-bit output into 28-bit words, of which the most significant 24 bits are read by DSP core 60. Register 510 then stores the 24-bit word for subsequent reading by DSP core 60 via PIO_EB bus 62.

The implementation of the invention described herein is provided by way of example only. However, many other implementations may exist for executing the functions described herein. While the present invention has been illustrated and described with reference to specific embodiments, further modifications and improvements will occur to those skilled in the art. For example, the control signal which configures peripheral modules in either CO or RT mode may be received and stored in a global register and driven to the peripheral modules, received at an input pin and driven to the peripheral modules, or stored locally within a control register in each peripheral module. Furthermore, the type of signal processing functions which are altered depending on the selection as CO or RT may vary from the examples cited herein. Also, in an actual embodiment different portions of the signal processing function may be implemented by hardware and firmware. It is to be understood, therefore, that this invention is not lim-

ited to the particular forms illustrated herein and that the appended claims cover all modifications that do not depart from the scope of this invention.

Claims

1. A transceiver (5) for an asymmetric communication system, characterized by:

   a transmit port adapted for coupling to an asymmetrical communication link, said transmit port transmitting data at a first data rate;
   a receive port adapted for coupling to said asymmetrical communication link, said receive port receiving data at a second data rate;
   a signal processor (60, 62, 64, 66, 68, 70, 72, 75, 76, 78) having a data input terminal for receiving a digital transmit signal, a data output terminal for providing a digital receive signal, an input terminal coupled to said receive port, and an output terminal coupled to said transmit port, said signal processor (60, 62, 64, 66, 68, 70, 72, 75, 76, 78) converting said digital transmit signal into a digital representation of an analog transmit signal having a frequency content, and converting a digital representation of an analog receive signal into said digital receive signal according to a frequency content of said digital representation of the analog receive signal;
   said signal processor (60, 62, 64, 66, 68, 70, 72, 75, 76, 78) characterized by:

      control means (71) for determining whether said first data rate is a first predetermined data rate and said second data rate is a second predetermined data rate, or whether said first data rate is said second predetermined data rate and said second data rate is said first predetermined data rate; and
      a signal processing module having an input coupled to said control means (71) and operable in first and second modes in response to said control means being in a first logic state (CO) or a second logic state (RT), respectively,
      wherein said transceiver (5) is selectively operable at either end of said asymmetrical communication link.

2. The transceiver (5) of claim 1 wherein said signal processing module comprises a digital interface (70) which converts said digital transmit signal into a plurality of transmit symbols at said first data rate, and converts a plurality of receive symbols received at said second data rate into said digital receive signal.

3. The transceiver (5) of claim 2 wherein said digital interface (70) uses a first memory buffer for converting said digital transmit signal into said plurality of transmit symbols and uses a second memory buffer which is smaller than said first memory buffer for converting said plurality of receive symbols into said digital receive signal when said control means indicates said first logic state (CO), and wherein said digital interface (70) uses said second memory buffer for converting said digital transmit signal into said plurality of transmit symbols and uses said first memory buffer for converting said plurality of receive symbols into said digital receive signal when said control means indicates said second logic state (RT).

4. The transceiver (5) of claim 1 wherein said signal processing module comprises a circular echo synthesis (CES) module (74) which interpolates a transmit signal representation based on the digital representation of an analog transmit signal to provide a cancellation signal when said control means indicates said first logic state (CO), and which generates a second cancellation signal in response to said transmit signal representation and decimates said second cancellation signal to provide said cancellation signal when said control means indicates said second logic state (RT), wherein said signal processor (60, 62, 64, 66, 68, 70, 72, 75, 76, 78) subtracts said cancellation signal from a receive signal representation based on the digital representation of an analog receive signal.

5. The transceiver (5) of claim 1 wherein said signal processing module comprises a fast Fourier transform (FFT) module (73) which performs an inverse FFT on a first transmit signal representation based on the digital representation of an analog transmit signal to provide a second transmit signal representation based on the digital representation of an analog transmit signal when said control means indicates said first logic state (CO), and which performs an FFT on a first receive signal representation based on the digital representation of an analog receive signal to provide a second receive signal representation based on the digital representation of an analog receive signal when said control means indicates said second logic state (RT).

6. The transceiver (5) of claim 1 wherein said signal processing module comprises a filter, wherein when said control means indicates said first logic state (CO) said filter filters a first transmit signal representation based on the digital representation of an analog transmit signal to provide a second transmit signal representation based on the digital representation of an analog transmit signal, and wherein when control means indicates said second

logic state (RT) said filter filters a first receive signal representation based on the digital representation of an analog transmit signal to provide a second transmit signal representation based on the digital representation of an analog transmit signal.

7. The transceiver (5) of claim 1 wherein said signal processing module comprises an analog front end module (78) characterized by:

an interpolator having an input for receiving a first transmit signal representation based on the digital representation of an analog transmit signal, and an output; and
an oversampled modulator having an input coupled to said output of said interpolator, and an output coupled to said transmit port,
wherein when said control means indicates said first logic state (CO) said interpolator has a first predetermined order and wherein when said control means indicates said second logic state (RT) said interpolator has a second predetermined order.

8. A transceiver (5) for an asymmetric communication system, comprising:

a transmit port adapted for coupling to an asymmetrical communication link, said transmit port transmitting data at a first data rate;
a receive port adapted for coupling to said asymmetrical communication link, said receive port receiving data at a second data rate;
an internal bus (62);
a data processor (60) coupled to said internal bus (62) for accessing memory locations via said internal bus (62) in response to a program;
a digital interface (70) coupled to said internal bus (62) which processes a digital transmit signal into a plurality of transmit symbols at said first data rate, and processes a plurality of receive symbols received at said second data rate into a digital receive signal;
a plurality of signal processing peripherals (73, 74, 76) coupled to said internal bus (62), wherein said data processor in conjunction with said plurality of signal processing peripherals processes said plurality of transmit symbols into a digital representation of an analog transmit signal, and processes a digital representation of an analog receive signal into said plurality of receive symbols; and
a control means (71) for indicating whether said first data rate is a first predetermined data rate and said second data rate is a second predetermined data rate, or whether said first data rate is said second predetermined data rate and said second data rate is said first predetermined data rate;
said control bit further determining a mode of operation of at least one said digital interface (70) and said plurality of signal processing peripherals (73, 74, 76).

9. The transceiver (5) of claim 8 wherein said data processor (60) further characterized by:

an analog front end module (78) having an input terminal coupled to said receive port, an output coupled to said transmit port, and a bi-directional terminal coupled to said internal bus, wherein said analog front end module (78) processes the digital representation of an analog transmit signal into an analog transmit signal, and processes an analog receive signal into the digital representation of the analog receive signal.

10. The transceiver (5) of claim 8 in which each of said plurality of signal processing peripherals (73, 74, 76) having a control means for indicating whether said first data rate is a first predetermined data rate and said second data rate is a second predetermined data rate, or whether said first data rate is said second predetermined data rate and said second data rate is said first predetermined data rate.

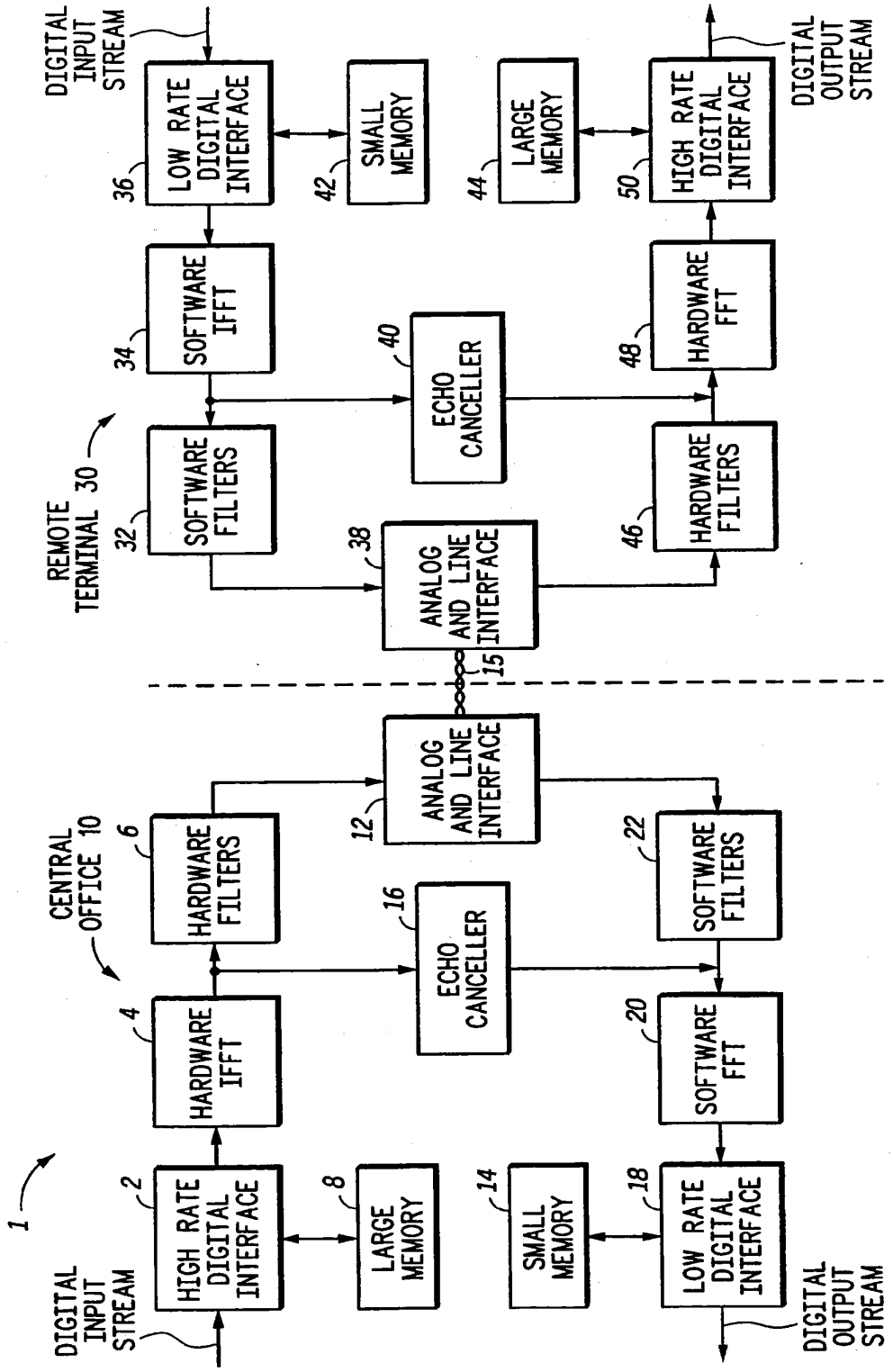

FIG. 1

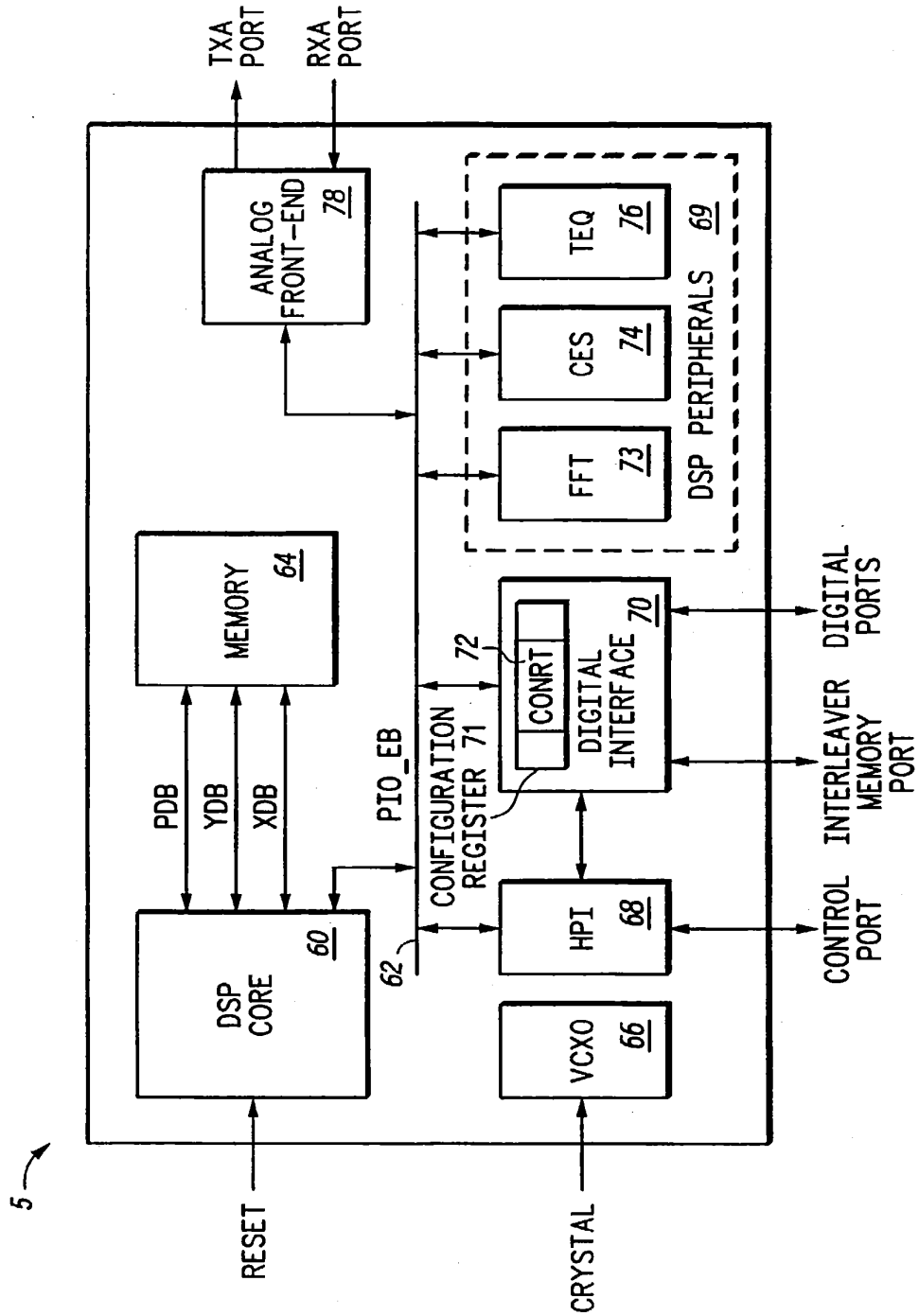

FIG.2

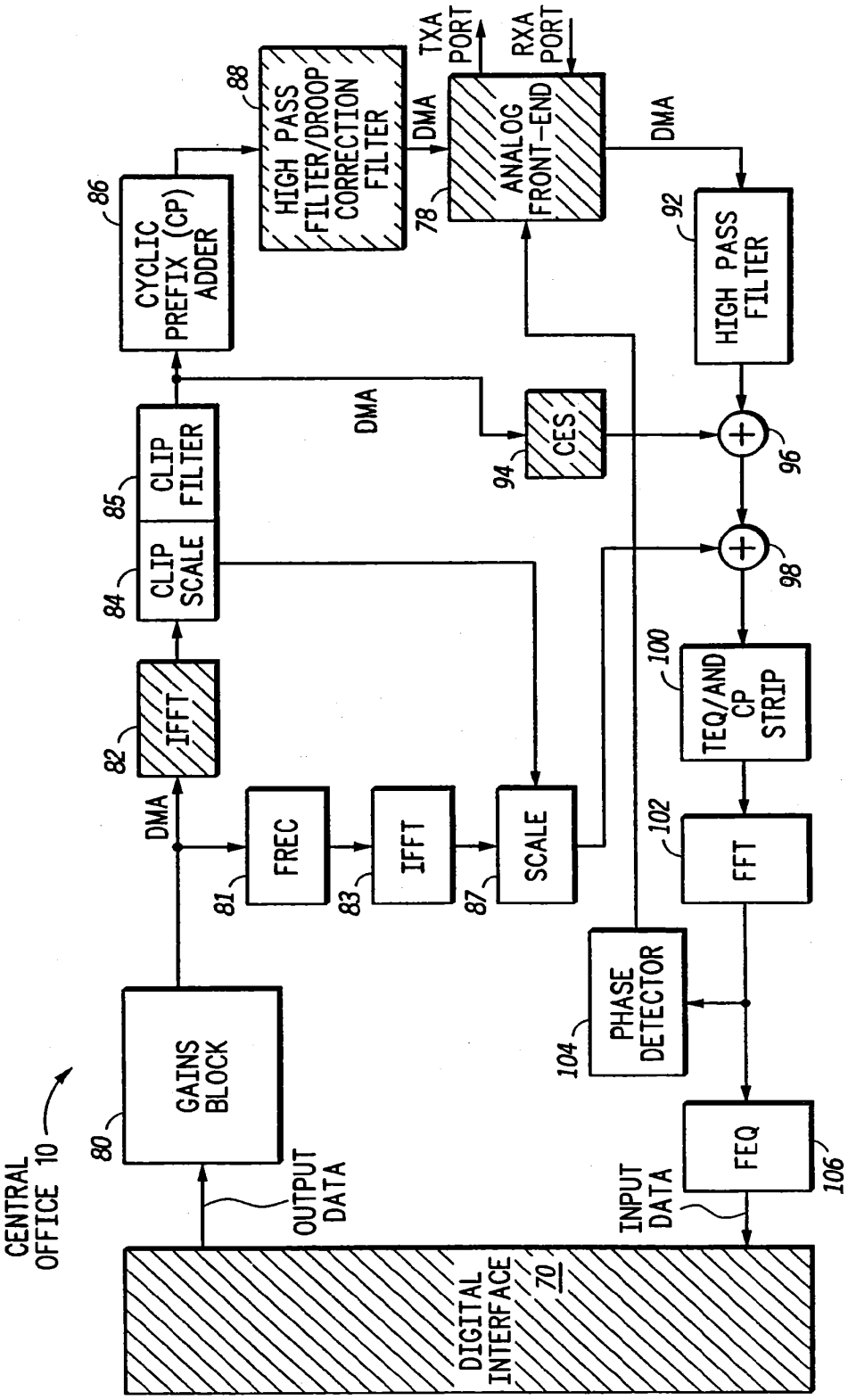

FIG.3

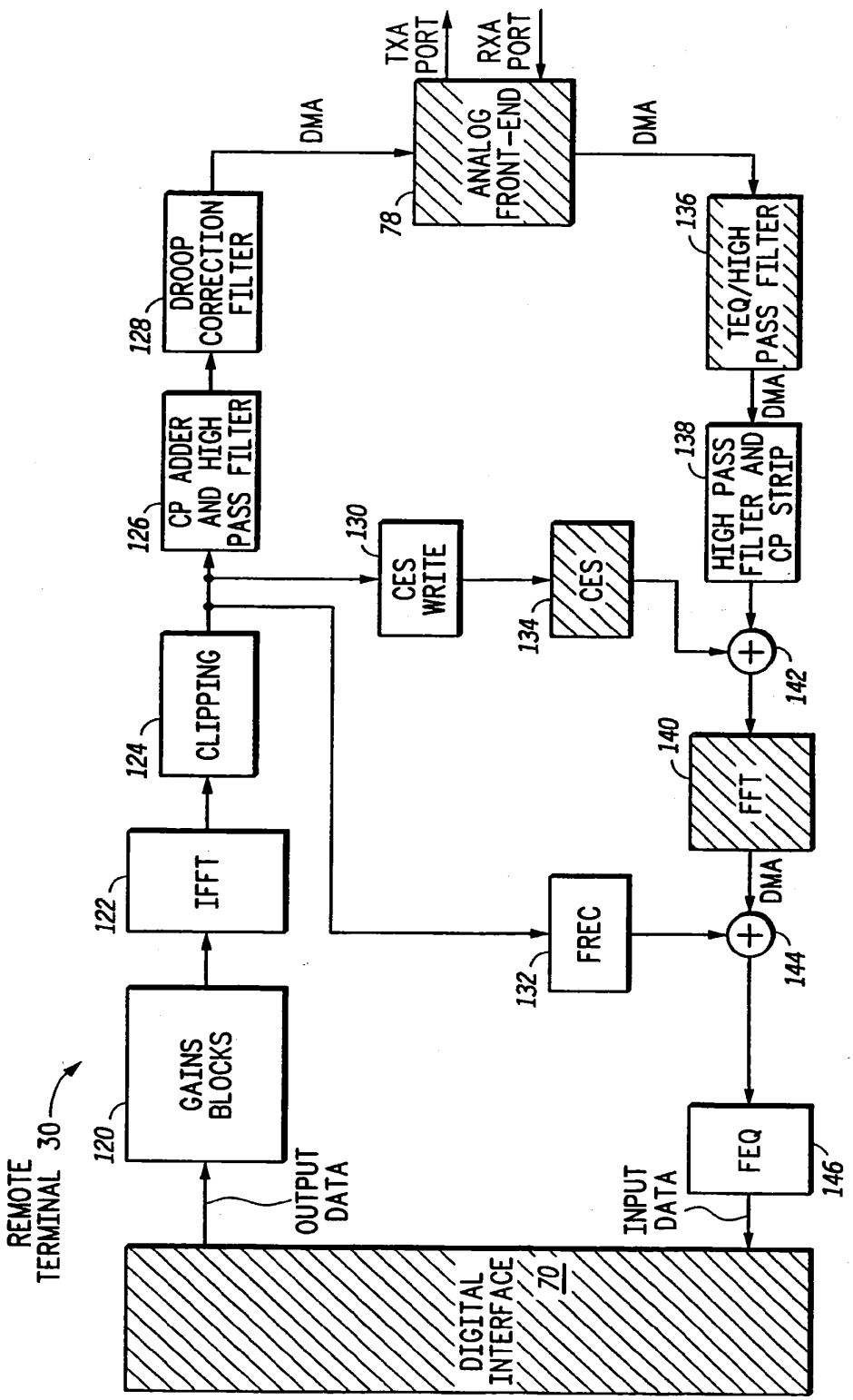

FIG. 4

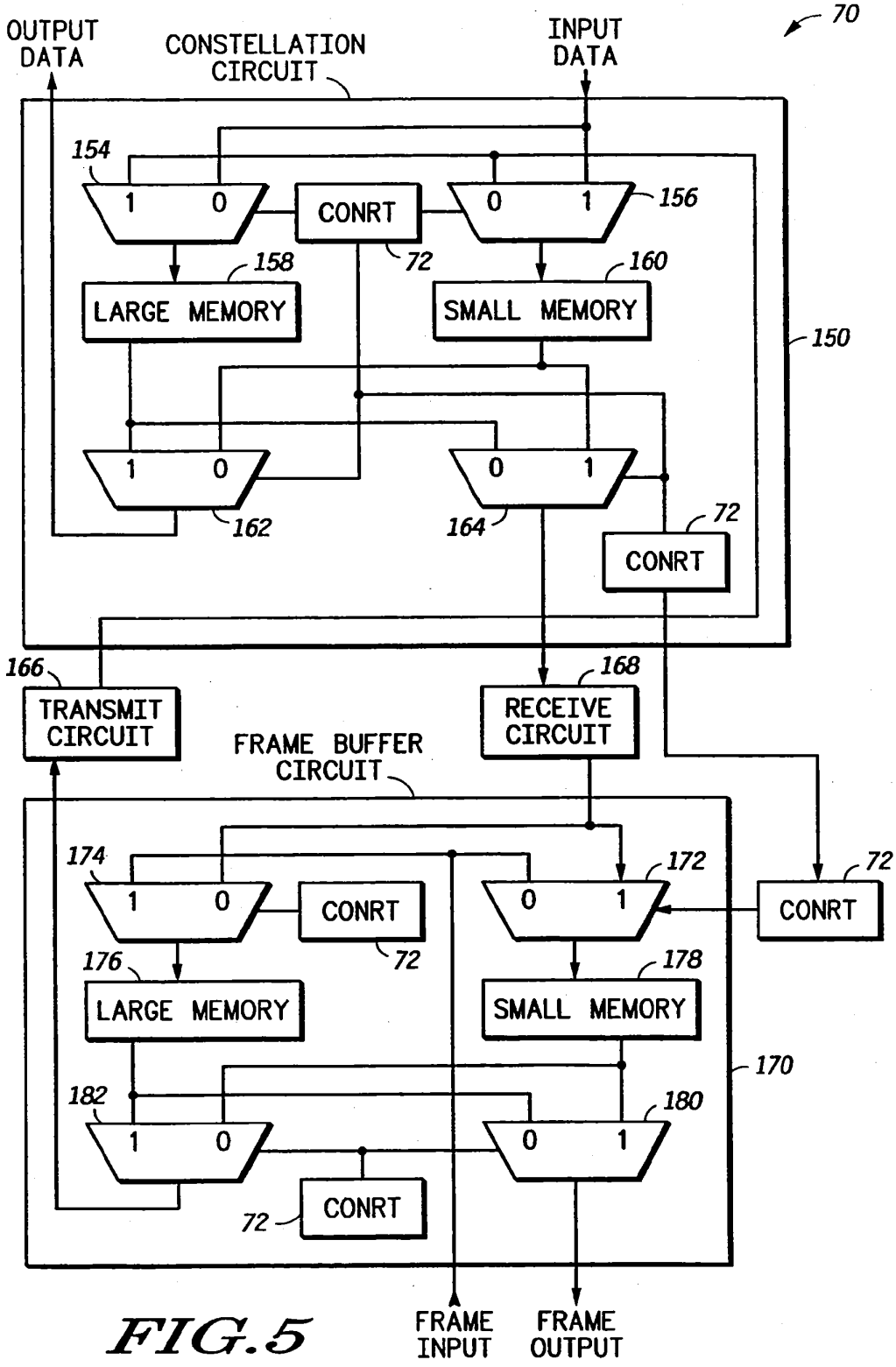

FIG. 5

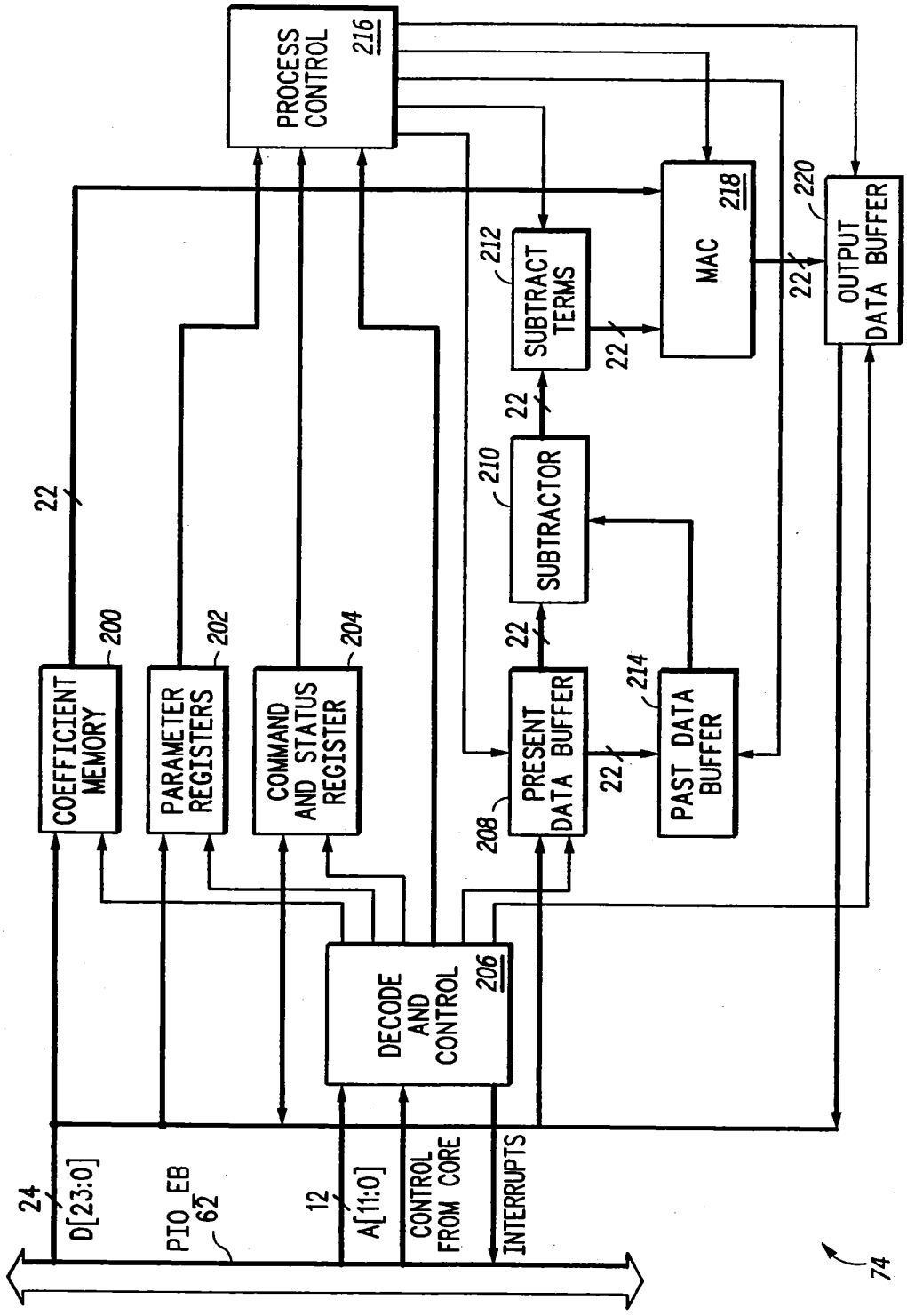

FIG. 6

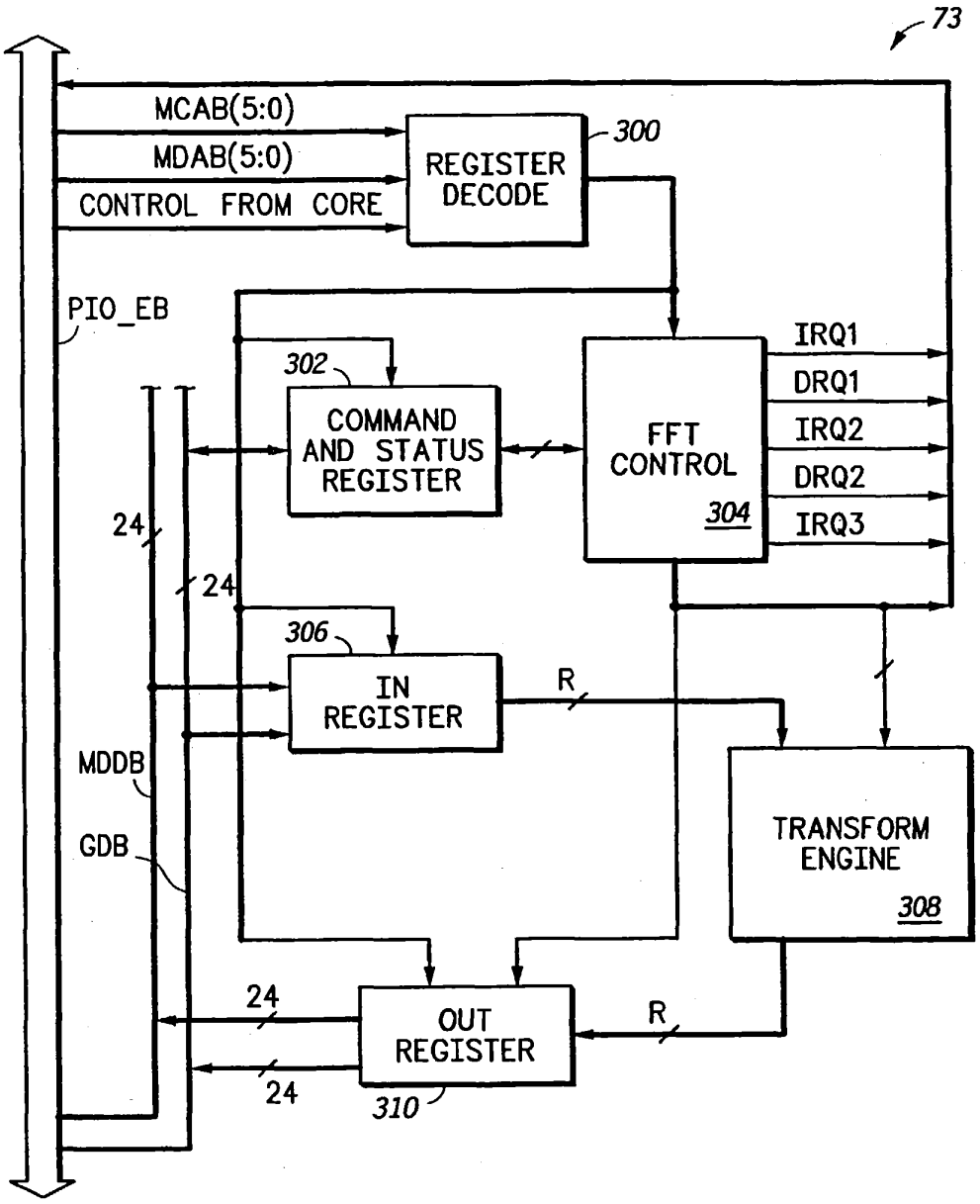

FIG. 7

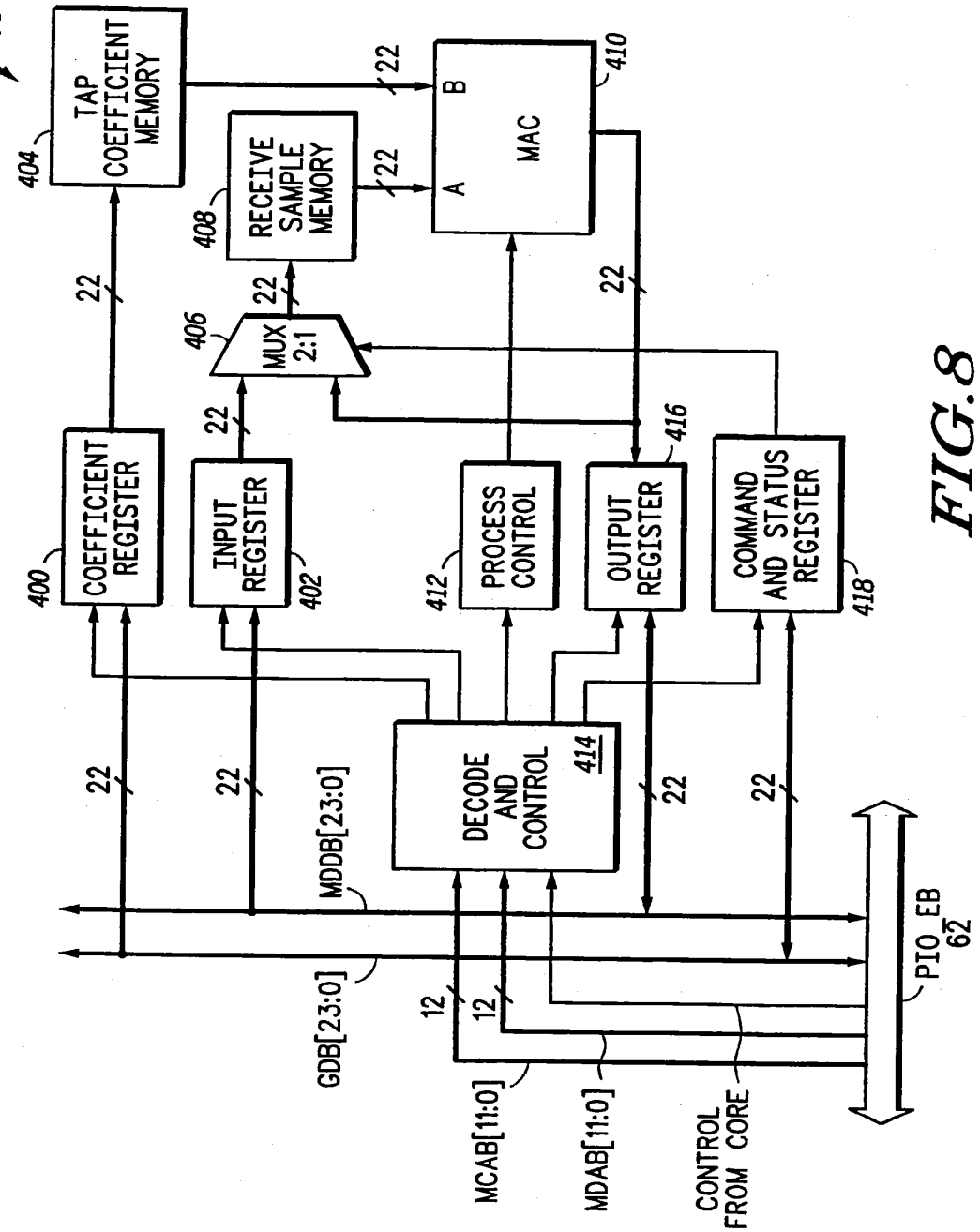

FIG.8

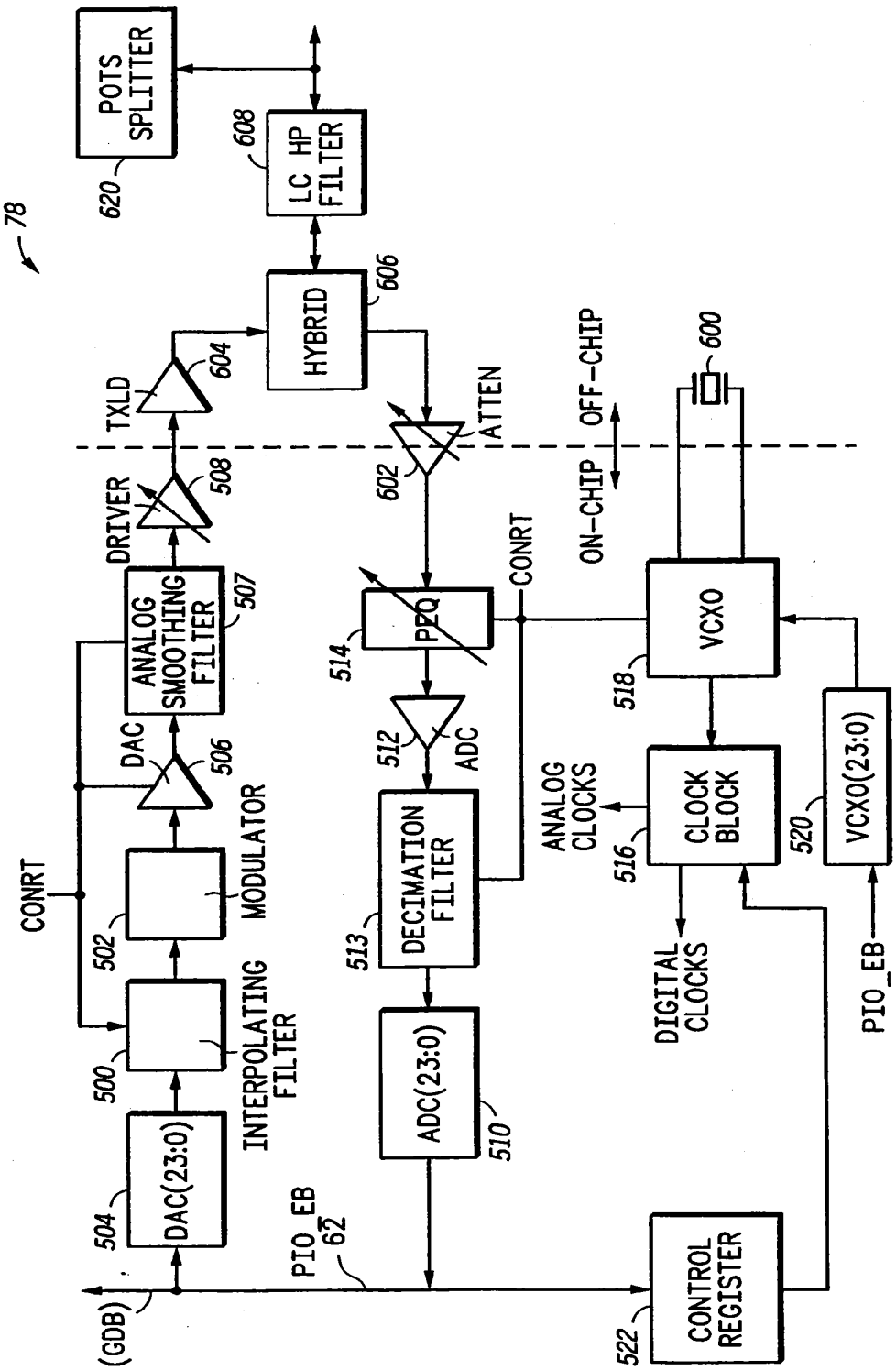

FIG.9

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(54) Reconfigurable transceiver for asymmetric communication systems

(57) A transceiver (5) for an asymmetric communication system such as asymmetric digital subscriber line (ADSL) includes a configuration register (71) defining operation at either a central office (CO) or a remote terminal (RT). The configuration register (71) includes a control bit (72) for selecting either CO or RT mode. The transceiver (5) includes a signal processing module (70) configured according to the state of the control bit (72). For example, a digital interface (70) converts transmit data into transmit symbols and converts received symbols into receive data. The digital interface (70) uses a large memory (158) as a buffer in the transmit path and a small memory (160) as a buffer in the receive path in CO mode. In RT mode, the digital interface (70) uses the small memory (160) in the transmit path and the large memory (158) in the receive path. The selective configuration allows a single integrated circuit to be used in both CO and RT equipment.

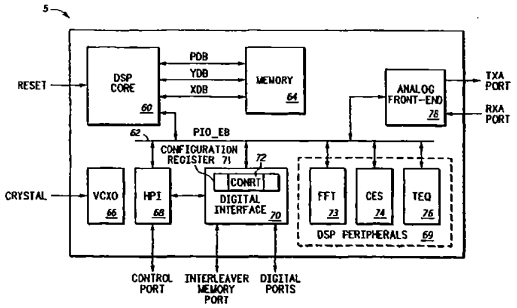

FIG.2

EP 0 840 474 A3

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 11 8661

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	WO 95 17046 A (BELL COMMUNICATIONS RES) 22 June 1995 (1995-06-22) * abstract; claims 1,15,16,18,19; figure 3 * * page 1, line 26 - line 29 * * page 2, line 26 - page 3, line 10 * * page 4, line 10 - line 21 * * page 12, line 1 - line 7 * * page 13, line 10 - line 25 * * page 14, line 8 - line 14 * * page 15, line 24 - line 32 * ---	1-10	H04L5/14 H04L27/26 H04L27/00
A	US 4 597 073 A (STAPLES LEVEN E) 24 June 1986 (1986-06-24) * abstract; claims 1,4,10; figure 2 * * column 1, line 40 - line 48 * * column 2, line 17 - line 32 * * column 2, line 66 - column 3, line 5 * * column 3, line 40 - line 43 * * column 4, line 13 - line 16 * * column 4, line 59 - column 5, line 11 * * column 6, line 21 - line 26 * --- -/--	1-3,8-10	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	12 June 2001	Masche, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 11 8661

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	HO M ET AL: "DISCRETE MULTITONE ECHO CANCELATION" IEEE TRANSACTIONS ON COMMUNICATIONS,US,IEEE INC. NEW YORK, vol. 44, no. 7, 1 July 1996 (1996-07-01), pages 817-825, XP000594718 ISSN: 0090-6778 * abstract * * page 817, column 2, line 11 - line 12 * * page 817, column 2, line 40 - line 48 * * page 819, column 2, line 27 - line 39 * * page 820, column 2, line 2 - line 8 * * page 821, column 1, line 1 - page 822, column 1, line 2; figure 3 * * page 823, column 1, line 23 - line 29 * * page 824, column 1, line 39 - column 2, line 7 * * paragraph [CONCLUSION] * ---	1-10	
A	US 4 890 316 A (WALSH DALE M ET AL) 26 December 1989 (1989-12-26) * abstract; claim 1 * * column 2, line 17 - line 50 * * column 4, line 42 - line 62 * * column 5, line 47 - line 53 * * column 7, line 44 - line 65 * * column 11, line 56 - line 65 * * column 12, line 17 - line 57 * * column 15, line 15 - line 21 * -----	1-4,6-10	TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	12 June 2001	Masche, C

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& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 97 11 8661

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12-06-2001

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WO 9517046 A	22-06-1995	NONE	
US 4597073 A	24-06-1986	NONE	
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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平5－95315

(43)公開日　平成５年(1993)４月16日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０４Ｂ　7/26		Ｘ　6942－5Ｋ		
	１０９　Ｆ	7304－5Ｋ		

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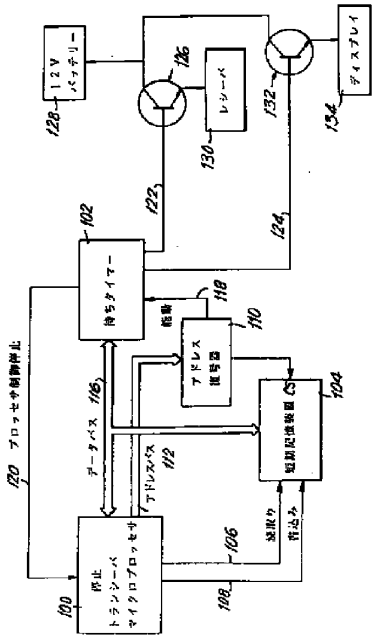
(74)代理人　弁理士　中村　稔　（外７名）

(54)【発明の名称】　携帯用細胞状電話システムの電力節減装置とその方法

(57)【要約】

【目的】　細胞状電話システムにおける電話機の電力消費をかなり低減することである。

【構成】　細胞状電話機のバッテリ電力消費が、受信したメッセージがほかの電話機に向けられている場合、検出により待ちモードの間、最小になり、伝送されたメッセージがほかの電話機へ向けられている場合、電話機の電子構成要素例えば、受信機１３０あるいはディスプレイ１３０等少なくとも一つへのバッテリ１２８の電力を低減するためスイッチ１２６、１３２を開くものである。次の伝送されたメッセージが、電話機により受信されると見込まれ場合、スイッチ１２６、１３２が閉じて電力が復帰する。



1

【特許請求の範囲】

【請求項１】　携帯用バッテリ作動の移動局へメッセージを送るように作動する基地局を有するシステムにおいて、各移動局が、待ちモードにおいて伝送されたメッセージを受信するように作動する受信手段より成る搭載された電子手段を有し、待ちモードの間、一つの移動局におけるバッテリ電力消費を最小にする電力節減装置において、

(1)　前記一つの移動局の受信手段により受信された伝送メッセージが、非呼出し状態でほかの局に向けられている場合を検出する検出手段と、

(2)　非呼出し状態の検出に応答し、前記一つの移動局の少なくとも一つの電子手段へのバッテリ電力を低減し、ほかの伝送メッセージが前記一つの移動局の受信手段により受信されると見込まれるまで、持続時間が続く時限の間、バッテリ電力低減を維持する電力節減手段と、

より成ることを特徴とする電力節減装置。

【請求項２】　移動局が伝送メッセージに組み込まれた固有の識別番号を有する細胞電話機であり、検出手段が、呼出し状態で前記の一つの移動局の電話機の固有の識別番号を検出するように作動し、また非呼出し状態においてほかの電話機に向けられたほかの識別番号を検出ように作動し、電力節減手段が前記電話機のほかの識別番号の検出に応答することを特徴とする請求項１に記載の電力節減装置。

【請求項３】　電力節減手段が前記の少なくとも一つの電子手段へ作動状態に接続した制御装置を有し、また前記の少なくとも一つの電子手段へのバッテリ電力を制御するように作動することを特徴とする請求項２に記載の電力節減装置。

【請求項４】　制御装置が、受信手段へ作動状態に接続した制御スイッチにして、バッテリ電力が受信手段へそれぞれ供給されまた阻止されない対のスイッチング状態の間を切換え可能であることを特徴とする請求項３に記載の電力節減装置。

【請求項５】　制御スイッチが給電されたディスプレイ手段へも作動状態に接続し、ディスプレイ手段へのバッテリ電力をスイッチング状態でそれぞれ供給しまた阻止することを特徴とする請求項４に記載の電力節減装置。

【請求項６】　電力節減手段が、制御手段へ作動状態に接続した設定可能な待ちタイマー手段を有し、前記時限が経過すると制御手段を制御するタイマー出力信号を発生するように作動することを特徴とする請求項３に記載の電力節減装置。

【請求項７】　制御手段が複数の前記電子手段に作動状態で接続し、タイマー出力信号が前記の電子手段をすべて同時に制御することを特徴とする請求項６に記載の装置。

【請求項８】　制御手段が複数の前記電子手段に作動状態に接続し、タイマー出力信号が前記電子手段をすべて連続的に制御することを特徴とする請求項６に記載の電力節減装置。

2

【請求項９】　検出手段が、待ちタイマー手段へ作動状態に接続したプログラムされたマイクロプロセッサを有し、また前記時限が経過するとタイマー出力信号を発生する待ちタイマー手段を設定するように作動し、前記プログラムされたマイクロプロセッサが連続するメッセージの間で前記時限を決定する手段を有していることを特徴とする請求項６に記載の電力節減装置。

【請求項１０】　制御手段が、プログラムされたマイクロプロセッサへ作動状態に接続した制御スイッチであり、またバッテリ電力がプログラムされたマイクロプロセッサへそれぞれ供給されまた阻止されるスイッチング状態の間を切換え可能であることを特徴とする請求項９に記載の電力節減装置。

【請求項１１】　電力節減手段が、プログラムされたマイクロプロセッサからデータを格納する記憶手段と、前記時限の間格納されたのアドレスを格納するアドレス手段とを有することを特徴とする請求項１０に記載の電力節減装置。

【請求項１２】　電力節減手段が前記時限の経過と共にバッテリ電力を復活することを特徴とする請求項１に記載の電力節減装置。

【請求項１３】　電力節減手段が、前記時限の経過前にデータ依存電子手段を始動する手段を有することを特徴とする請求項１２に記載の電力節減装置。

【請求項１４】　携帯用バッテリ作動の移動細胞電話機へメッセージを送るように作動する細胞式電話システムにおいて、各細胞電話機が、待ちモードにおいて伝送メッセージを受信するように受信手段より成る搭載された電子手段を有し、待ちモードの間一つの細胞電話機のバッテリ電力を最小にする電力節減装置において、

(1)　前記一つの細胞電話機の受信手段により受信された伝送メッセージが非呼出し状態でほかの細胞電話に向けられている場合を検出する検出手段と、

(2)　非呼出し状態の検出に応答し、前記一つの細胞電話機の少なくとも一つの電子手段へのバッテリ電力を低減し、ほかの伝送されたメッセージが前記一つの細胞電話機の受信手段により受信されると見込まれるまで、持続時間が続く時限の間、バッテリ電力低減を維持する電力節減手段と、

より成ることを特徴とする前記の電力節減装置。

【請求項１５】　携帯用バッテリ作動の移動局へメッセージを送るように作動する基地局を有するシステムにおいて、各移動局が、待ちモードにおいて伝送されたメッセージを受信するように作動する受信手段より成る搭載された電子手段を有し、待ちモードの間、一つの移動局のバッテリ電力消費を最小にする方法において、

(1)　前記一つの移動局の受信手段により受信された伝

送メッセージが、非呼出し状態でほかの局へ向けられている場合を検出するステップと、

(2)　非呼出し状態の検出に応答して前記一つの移動局の少なくとも一つの電子手段へのバッテリ電力を低減し、また、ほかの伝送メッセージが前記一つの移動局の受信手段により受信されると見込まれるまで持続時間が続く時限の間、バッテリ電力の低減を維持するステップと、

より成ることを特徴とする電力節減方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、一般的には、携帯用バッテリ作動移動局の待ち動作中のバッテリ電力消費を最小にする電力節減の装置とその方法に関し、具体的には、細胞状電話システム（Cellular telephone system）の細胞状電話機（Cellular telephone）に関する。

【０００２】

【従来の技術】一般的細胞状電話システムは、複数の基地局すなわちタワーより成っており、各基地局は、予め割り付けられた地理的細胞すなわち領域を受け持っている。各基地局は、メッセージをその領域内の多数の移動局、例えば、細胞電話機へ送る。各電話機は、トランシーバとマイクロプロセッサにより制御された復号器とを有している。

【０００３】待ち動作中に、各電話機は、電話呼出しを受信するのを待っている。各基地局から送られたメッセージは、すべての電話機に向けられた、いわゆる“全域メッセージ”であるか、あるいは、最も頻繁には、一つの特定の電話機に向けられた個々のメッセージである。従って、個々のメッセージは、独自の移動識別番号（以降、ＭＩＮと呼称）、すなわち、電話番号を有している。各電話機は、搭載された記憶装置に事前に格納された、その独自のＭＩＮを有する。

【０００４】多くのメッセージが、各基地局によって送られ、これらの多くのメッセージのなかで、たとえあるにしても、極く少量のメッセージだけが、特定の電話機に対して向けられている。それでも、各電話機は、待ちモードの動作の間、特定の電話機がそのＭＩＮを認識するまで、各基地局によって送られたすべてのメッセージを連続して受信し、復号し、その後に、電話は通話（進行中の呼出し）モードで動作する。電話は、通信モードで、音声データより成るデータを、基地局から基地局へ送る。

【０００５】現在使用されている普通の細胞電話機が、通話と待ちのどちらのモードでも電力を消費することは、明らかである。現在の携帯用バッテリ作動電話機では、搭載バッテリは、一般に、待ちモードで約８時間と通話モードで約１～２時間の動作寿命時間を有する。従って、バッテリは、引続いて電話機を使用するために、再充電あるいは交換されなければならない。待ちモード

においてバッテリ作動細胞電話機に搭載された主な電力消費機器は、前述のように、電話機がそのＭＩＮを復号するのを待っている間、連続してオンの状態にあるトランジスタの受信器の部分である。電話機に搭載されたマイクロプロセッサとほかの電子構成要素も、待ちモードの間、動作状態であり、そのほかに、バッテリの電力を消費する。再充電あるいはバッテリ交換を行う間のバッテリの作動寿命を増大する必要は、自明のことである。

【０００６】ここで説明された発明を容易に理解するために、待ち動作において基地局により送られメッセージの従来技術の概要を簡単に説明する。メッセージは、ビットより成る数字の流れであり、１つ以上のワードより成っている。普通、メッセージは二つのワードを有する。図１は、メッセージの各ワードの従来技術の構造を図示している。各ワードは、４０ビットより成っている。最初の２８ビットは、ほかのメッセージのなかで、ＭＩＮ、全体メッセージ、あるいはチャンネル割付けメッセージなどより成るメッセージデータである。最後に１２ビットは、検査ビット（ＢＣＨ）のシーケンスあるいはパリティ領域であり、ブロックコードパリティ検査和である。ＢＣＨパリティ領域は、最初の２８ビット内のメッセージデータが正しく受信されたか、あるいは、されなかったかを確認する。

【０００７】時には急激に変化するラジオ信号により失れるメッセージの問題を解消するために、メッセージの各ワードが、基地局から各携帯電話へ５回送られる。検査されるべきメッセージについて、各ワードは、電話機がメッセージに応答する前に、５回のうち３回以上正しく受信しなければならない。さらに、バースト誤りを補償するため、ワードは交互に配置されて、ＭＩＮが奇数か偶数かによってフォーマットで送られる。

【０００８】図２は、従来技術の、交互配置されたフォーマットの構造を示しており、この場合、各ワードＡ（偶数の電話番号に対し指定されている）と各ワードＢ（奇数の電話番号に対し指定されている）とが、５回繰り返えされ、各繰返し毎に、偶数ワードＡは、奇数ワードＢと交替する。そのほかに、図２は、同期化ワードＳが入信していることを電話機に知らせる１０ビットのシーケンスである点順シーケンスＤを示す。点順シーケンスは、プリカーソルとメッセージが開始しようとしていることを示す総括標識とである５KHz周波数の信号を発生する。同期化ワードは、１１ビットのシーケンスであって、電話機の内部クロックが基地局の送信機に同期化される同期化パターンを有する。

【０００９】また、図３に図示されている話し中－アイドルビットは、メッセージデータの流れに割り当てられている。話し中－アイドルビットは、メッセージの１０ビット毎に送られて、システム・チャンネルの状態を示す。話し中－アイドルビットが論理１にセットされると、チャンネルは話し中でない。話し中－アイドルビッ

5

トが論理０にセットされると、チャンネルは話し中である。送られたビットのデータ速度は、１０キロビット／秒である。従って、図２に示すように、４６３ビットは、46.3ミリ秒で送られ、一つの奇数ワードと一つの偶数ワードが５回交互配置フォーマットで送られる時間の合計である。

【００１０】前述のように、メッセージは、一つ以上のワードを有することが出来、普通、そのようにワードを有している。このような場合には、各ワードも、全メッセージに対し多くのワードが送られていることを、搭載のマイクロプロセッサへ知らせる。図４は、従来技術の、二つのワードより成る完全メッセージの構造と持続時間を図示しており、この場合、ワードＣは、ワードＡを第１のワードとして有していた偶数の電話番号に対するメッセージの第２のワードであり、ワードＤは、ワードＢを第一ワードとして有していた奇数の電話番号に対するメッセージの第２のワードである。２ワードメッセージは、完全に送られるのに92.6ミリ秒かかる。

【００１１】

【本発明の概要】1.　本発明の目的

本発明の一般的目的は、細胞状電話システムの技術状態を向上することである。本発明のほかの目的は、細胞状電話システムにおける再充電あるいはバッテリ交換の間のバッテリ作動寿命時間を増大することである。

【００１２】本発明のそのほかの目的は、待ちモードにおける携帯用バッテリ作動細胞状電話機の作動寿命時間を延長することである。本発明のさらにほかの目的は、この種の携帯用細胞電話機の電力消費をかなり低減することである。

2.　本発明の特色

以後に明らかになるこれらの、またほかの目的に関連して、本発明の一つの特色は、手短かに言えば、システムの、具体的には細胞状電話システムの基地局により送られたメッセージが、細胞電話機に搭載された受信装置により受信される待ちモードの動作の間、一つの移動局、具体的には携帯用バッテリ作動細胞電話機のバッテリ電力消費を最小にする電力節減装置とその方法にある。

【００１３】本発明は、電話機で受信装置によって受信された伝送メッセージが、非呼出し状態のほかの局に向けられたときに、検出する検出装置より成っている。非呼出し状態の検出に応答して、本発明は、電話機の一つ以上の搭載された電子装置へのバッテリ電力を低減するために作動する、電力節減装置の使用を提案する。バッテリ電力の低減は、ほかの伝送メッセージが電話機で受信装置によって受信されると見込まれるまで、その持続時間が続く時間の間、電力節減装置により維持される。

【００１４】電力節減装置は、制御スイッチを有し、好適には、バッテリ電力が、電話機の一つ以上の各種電子装置へ、それぞれ、送られるか、あるいは阻止される一対のスイッチング状態の間を切換え可能な制御スイッチ

6

を有する。バッテリ電力は、前述の受信装置、あるいは給電されるディスプレイ装置、あるいは電話機の全体の動作を制御するマイクロプロセッサへ、送られるか、あるいは阻止される。各種電子装置は、同時にあるいは連続的に、バッテリ電力を送られるかあるいは阻止される。

【００１５】制御スイッチは、マイクロプロセッサに制御されて、設定可能な待ちタイマ装置により、そのスイッチング状態を切換え可能である。マイクロプロセッサは、連続したメッセージ間の時限を決定し、前記時限が経過すると、制御スイッチを制御するタイマ出力信号を発生するようにタイマをセットする。一時記憶装置とアドレス記憶装置は、マイクロプロセッサが、待ちモードの間、電源を切られている場合に、マイクロプロセッサが必要とするデータとアドレスとを、それぞれ、格納するのに使用される。従って、検出装置が、伝送されたメッセージの所定のワードが特定の電話に向けられていないことを確認すると、マイクロプロセッサは、次のワードが受信されると見込まれるまでの時間量を限定する。受信機は、この間、電源が切られている。受信装置は主要な電力消費機器であるので、電力消費のかなりの低減が達成される。ほかの省電力は、電話機のほかの電子装置の電源を切ることにより行われる。受信装置とほかの電子装置は、前述の時限が経過すると、再び電力が送られる。マイクロプロセッサは、この時限に関して待ちタイマ装置をセットする。

【００１６】この時限の持続時間は可変であり、メッセージの第１ワードが、ほかの電話機に向けられているとして、何時確認されるかによって決まる。これは、ワードの最初の、第２、第３、第４、あるいは第５の繰り返しで、行われる。本発明の特性としてみなされる新しい特色は、付属の特許請求の範囲に詳細に記載されている。しかし、本発明自体は、その構造と作動方法のいずれに関し、ほかの目的と利点とを併せて、付属図面と関連して読まれると、特定の実施例についての次の説明から最もよく理解されるであろう。

【００１７】

【実施例】図５に関して、参照番号１００は、一般に、携帯用バッテリ作動細胞電話機の動作を制御するプログラムされたトランシーバのマイクロプロセッサを示す。マイクロプロセッサ１００の構造と作動は、本技術分野においてよく知られている。例えば、ベル・システム・テクニカル・ジャーナル（The Bell System Tech-nical Journal）、５８巻１号，１９７９年１月、の全内容が、参考にここに織り込まれている。

【００１８】マイクロプロセッサの動作は、図６に流れ図で図示されている。前記のように、待ちモードの間、マイクロプロセッサ１００は、点順シーケンスＤを待ち（ブロック２００）、そこで同期化ワードＳと時間合せして（ブロック２０２）、さらにメッセージの最初のワ

7

ードの第１回の受信、すなわち、偶数のＭＩＮについてはワードＡ１、あるいは、奇数のＭＩＮについてはワードＢ１を受信して復号するように（ブロック２０４）プログラムされている。最初のワードの第１回の受信が復号された後、パリティ領域は検査されて（ブロック２０６）、ワードＡ１あるいはＢ１が正確に受信されて復号されたか、されないかを確認する。パリティ領域が、最初のワードの第１回受信の復号化を確認しない場合には、マイクロプロセッサ１００は、最初のワードの第２回の受信、すなわちＡ２あるいはＢ２を受信して復号する（ブロック２０８）。アナログ方式で、最初のワードの第３、第４、第５回の受信の受入れと復号化は、パリティ領域がワードの受入れと復号化を確認するまで続く。

【００１９】パリティ領域が、受信したワードの復号化を確認すると直ちに、受信したワード（ＭＩＮｒ）の送られて来たＭＩＮは、電話機の事前格納されたＭＩＮ（ＭＩＮｓ）と比較される（ブロック２１０）。突合せが行われる場合、次に、電話機はメッセージを実行する（ブロック２１２）。突合せが行われない場合、次に、マイクロプロセッサ１００は、かかって来たメッセージがすべての電話に向けられた全体メッセージであるか、どうかを確認するために検査する（ブロック２１４）。送られて来たメッセージが全体メッセージでない場合、また、送られたＭＩＮと格納されていたＭＩＮとの間の突合せが行われない場合、マイクロプロセッサは、送られたメッセージがこの特定の電話に向けられたのでなく、実際には、ある他の電話機に向けられたものであることを知っている。この非呼出し状態の検知は、本発明の電力節減装置により採用された引き金となる作業であって、本装置は、電話機の一つ以上の電子構成要素へのバッテリ電力を低減することにより、好適には中断することにより、バッテリ電源を節減する。次に説明するように、電力の低減あるいは中断は、ワードの妥当性検査で始まる可変持続時間の間、維持され、それは、次に伝送されたメッセージが受信されると見込まれた時に、終了する。

【００２０】図５に関し、マイクロプロセッサ１００は、作動可能に設定可能な待ちタイマー１０２に接続している。都合のよいことに、このタイマーは、エクサー・コーポレーション（Exar Corporation）から型式No.ＸＲ２２０６として入手することが出来る。短期記憶装置１０４は、読取り回線１０６と書込み回線１０８とにより、作動可能にマイクロプロセッサ１００へ接続している。記憶装置１０４は、作動してマイクロプロセッサからデータを格納する。アドレス復号器１１０は、アドレスバス１１２により、作動可能にマイクロプロセッサへ接続し、アドレス回線１１４により、記憶装置１０４へも接続している。アドレス復号器１１０は、記憶装置１０４に格納されたデータのアドレスを格納している。

8

双方向性データバス１１６は、マイクロプロセッサ１００、待ちタイマー１０２、及び記憶装置１０４を相互に接続している。

【００２１】待ちタイマー１０２は、能動回線１１８により、アドレス復号器１１０へ接続し、また、制御停止回線１２０を経て、マイクロプロセッサへも接続している。タイマー１０２には、少なくとも一本のタイミングされた出力回線と、図５に示すように、一組のタイミングされた出力回線１２２と１２４が結線されている。出力回線１２２は、バッテリ１２８とトランシーバの受信部１３０との間に作動可能に接続された制御スイッチ１２６へ接続している。出力回線１２４は、バッテリ１２８と、電話機のほかの電子構成要素、例えば、給電されたディスプレイ１３４との間に作動可能に接続された制御スイッチ１３２へ接続している。

【００２２】図６に再び参照すると、マイクロプロセッサは、非呼出し状態を検知すると、直ちに、次のワードが受信されると見込まれるまでの時間を計算する（ブロック２１６）。この時間は、次の式により計算される。すなわち、偶数のワードＡを復号する電話機について、Ｔ＝４８．４ｍｓ－８．８ｍｓ（ｎ）＋４６．３ｍｓ（ＮＡＷＣ）、奇数のワードＢを復号する電話機について、Ｔ＝４４．０ｍｓ－８．８ｍｓ（ｎ）＋４６．３ｍｓ（ＮＡＷＣ）、ここで、ｎは、繰返されたワードの個数であり、ＮＡＷＣは、受信するほかの異なるワードの個数であり、Ｔは、送られたメッセージ間の時間である。

【００２３】上記の時間の数値は、図１から図４に関連して上述の特定のワードと伝送回数に関して表される。偶数のワードＡは、偶数のワードＢより先行するので、時間Ｔは、電話機が偶数ワードか、あるいは、奇数ワードを復号するかによって変わる。従って、マイクロプロセッサは、次のワードまでの時間を計算した。マイクロプロセッサは、必要な作動変数、例えば、制御チャンネル番号、故障タイマー値などを、データバス１１６を経て短期記憶装置１０４へ、また、アドレスバス１１２を経てアドレス復号器１１０へ格納する（ブロック２１８）。次に、マイクロプロセッサは、待ちタイマー１０２を始動して（ブロック２２０）、タイマー１０２は、順番に、制御停止信号を回線１２０に発生して、時間Ｔの間マイクロプロセッサへの電力を低下する。また、待ちタイマー１０２は、タイマー出力信号を出力回線１２２と１２４に発生して、制御スイッチ１２６と１３２をそのスイッチング状態の間で駆動し、バッテリ１２８から受信器１３０と給電されたディスプレイ１３４とへのバッテリ電力を低下するか、あるいは、中断する。回線１２２と１２４のタイマー出力信号は、同時か、あるいは、連続的に発生する。ディスプレイ、データバス関連装置、ラジオ周波数安定装置の始動により、トランシーバのいくつかの電子構成要素は、選択的に抑止される。周波数合成装置、すなわち、ラジオ周波数発振器は、安

9

定する一定の時間、例えば、３ms程度の時間が必要である。従って、周波数合成装置は、待ちモードの間作動停止したならば、待ちモードの間停止したほかの電子構成要素が、すべて再び作動する前に、少なくとも３ms間作動する必要がある。さらに、周波数合成装置とデータ・レジスタなどのほかのデータ依存装置とは、作動後、始動シーケンスによって再生されなければならない。

【００２４】計算された時間が経過すると（ブロック２２２）、待ちタイマー１０２は、制御スイッチ１２６と１３２を、電力がマイクロプロセッサ１００のほかに受信機１３０とディスプレイ１３４へ復活する前の状態へ切換える。この電力の復活（ブロック２２４）は、各種の電子構成要素の間で同時にあるいは連続的に行われる。アドレス復号器１１０と記憶装置１０４とに格納されたデータは検索され、再度、電話機は、点順シーケンスを待つことにより、待ちモードを開始する（ブロック２００）。

【００２５】従って、電話機の一つ以上の電子構成要素は、メッセージの間で、電力が停止される。受信機と電話機のほかの電子構成要素が、メッセージの間で給電される理由はないので、これによって、電力は節減される。当然のことであるが、常に電力を受けることが必要である唯一の構成要素は、待ちタイマー１０２であるが、この構成要素は、受信機１３０、ディスプレイ１３４、マイクロプロセッサ１００及び電話機のそのほかのすべての電子構成要素よりもはるかに少ない電力を消費する。正確なタイミングのためには、搭載した基準クロック（水晶発振器）は、決して休止してはならない。

【００２６】上記の本発明は、細胞電話に関して説明されたが、本発明の電力節減装置と方法は、信号発振装置（beeper）、ページャー（Pager）、及び、要するに、伝送されたメッセージを受信して自己確認が可能である多数の移動局を有するすべてのシステムで有利に使用されるので、そのように限定されるものではない。上記のタイミングの計算は、電子工業協会（ＥＩＡ）により制定され、“移動局－陸上局両立性使用、１９９０”、ＥＩＡ－５５３として出版された米国工業規格にもとずいている。

【００２７】ほかの工業規格は、仕様することが出来る。例えば、欧州において、特に英国において、ＴＡＣＳとして知られた工業規格が、１９８９年９月第４版、“英国、全体的アクセス通信システム移動局－陸上局両立性仕様”で出版されている。ＴＡＣＳシステムでは、点順シーケンスは、４KHz周波数の信号を発生し、従って、第３に示された伝送されたビットのデータ速度は、

10

８ヒロビット／秒である。図２に引用された2.４６３ビットは、５７.８７５ミリ秒で伝送される。図４に引用された２ワードメッセージは、１１５.７５ミリ秒かかる。

【００２８】上述のＴＡＣＳシステムの時間は、次に式により計算される。

偶数

偶数のワードＡを復号する電話機について、Ｔ＝６０.５ms－１１ms（ｎ）＋５７.８７５（ＮＡＷＣ）、奇数のワードＢを復号する電話機について、Ｔ＝５５.０ms－１１ms（ｎ）＋５７.８７５（ＮＡＷＣ）、ここで、ｎは、繰返されたワードの個数であり、ＮＡＷＣは受信するほかの異なるワードの個数であって、Ｔは、伝送されたメッセージの時間である。

【００２９】上記の各要素、あるいは、それらを二つ以上併せたものは、上述の形式と異なったほかの形式の構造に、有用な用途が見出されることが、理解されるであろう。本発明は、携帯用細胞状電話システムの電力節減装置と方法で具体化されて、図示、説明されたが、各種の修正と構造の変更は、本発明の精神から何ら逸脱することなく、行われるので、示された詳細に限定されるものではない。

【００３０】さらに分析することなく、当事者以外の人は、現在の知識をもって、従来技術の立場から、本発明の包括的あるいは個別的面の重要な特徴を公正に構成している面を失うことなく、それを各種の用途に使用出来る本発明の要点は、前述の内容によって十分に明らかにされ、従って、このような適用は、添付の特許請求の範囲と同等の意味と範囲のなかで、理解されるものである。

【図面の簡単な説明】

【図１】従来技術による細胞状電話システムに伝送されたワードの構造を表す図である。

【図２】従来技術による細胞状電話システムに交互配置様式で伝送された奇数ワードと偶数ワードの構造を表す図である。

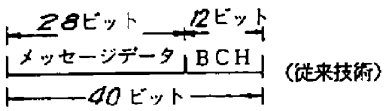
【図３】従来技術によるデータの流れに加えられた話し中－アイドルビットを明確に示すメッセージのワードの一部分を表す図である。

【図４】従来技術による細胞状電話システムにより伝送された２ワードメッセージの構造を表す図である。

【図５】本発明によるバッテリ電力消費を最小にする電力節減装置の電気構成図である。

【図６】本発明による電力節減装置に使用されたトランシーバ・マイクロコンピュータの動作を示す流れ図である。

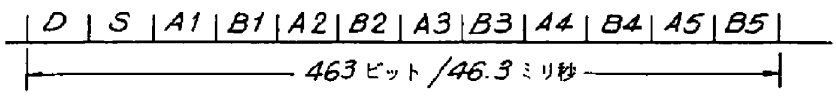
【図１】



（従来技術）

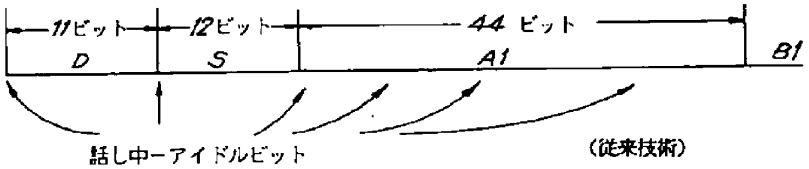
ワードビット構造

【図２】



メッセージワード構造　　（従来技術）

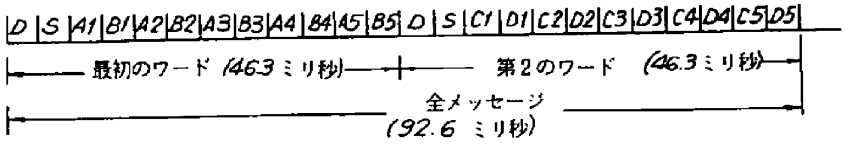
【図３】



（従来技術）

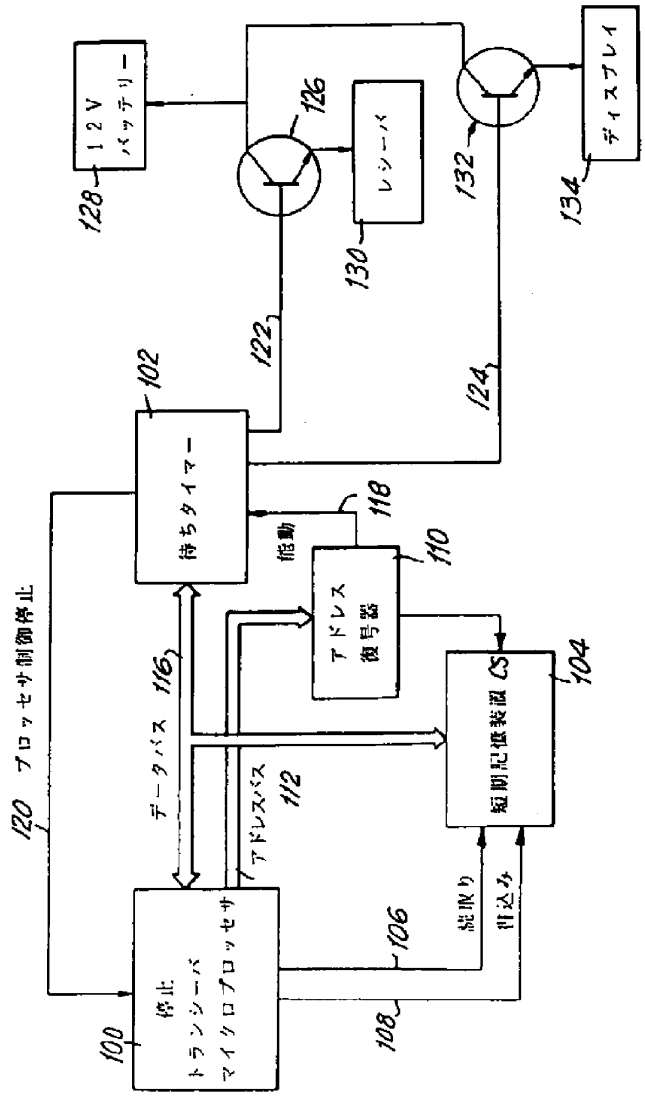
話し中ーアイドルビット重畳

【図４】

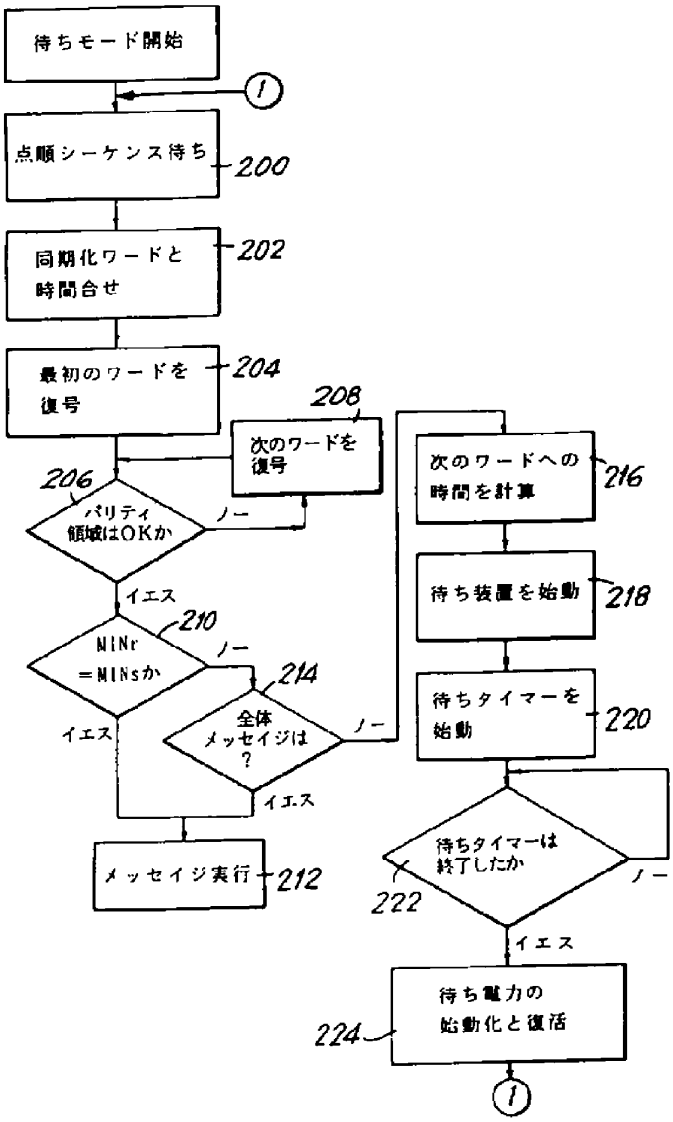


2ワードメッセージ　　（従来技術）

【図５】



【図６】



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KIKUCHI HIDEO
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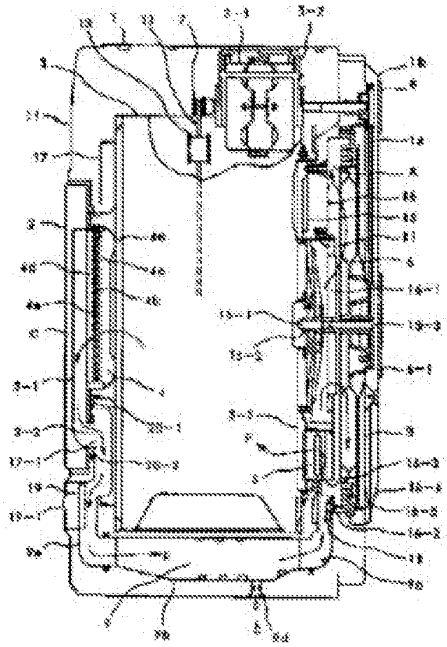
(54) CLOTHES DRIER

(57)Abstract:
PURPOSE: To provide a clothes drier which allows a user to know easily a collecting state of waste thread of a waste thread collecting device, and also, executes simply cleaning, eliminates extension of a drying time, prevents waste of use electric power, and improves operability.
CONSTITUTION: An outer frame 1 is provided with an opening/closing door 2, a waste thread collecting device 4 installed on the inside surface of the opening/closing door 2, a drying drum 3 contained in the outer frame 1, and a both blade fan 6, and the opening/closing door 2 is provided with a door duct 2-1 and its communicating port 2-2 in its inside. Also, the outer frame 1 is provided with a circulating duct 9 in its inside, and provided with an airtight circulating air course by heating air which starts from the double-flow blade fan 6, passes through the drying drum 3, the waste thread collecting device 4, the door duct 2-1 and its communicating port 2-2, and a circulating duct 9, and returns to the double-flow blade fan 6, and the waste thread collecting device 4 is provided between the drying drum 3 in the air passage and the door duct 2-1.



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最終頁に続く

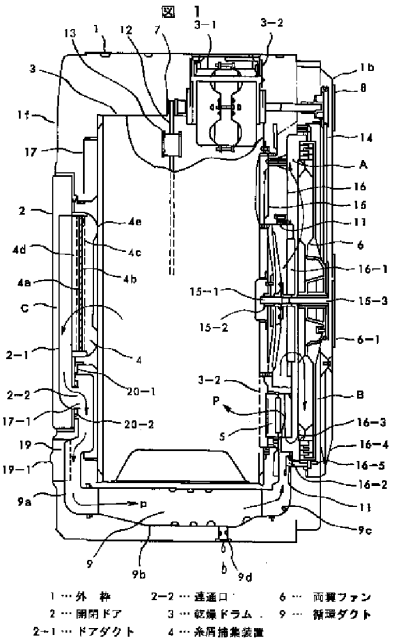
(54)【発明の名称】　衣類乾燥機

(57)【要約】

【目的】　糸屑捕集装置の糸屑の溜り具合を使用者に容易に判らしめ、かつ、簡単に清掃できるようにして、乾燥時間の延長をなくし、使用電力の浪費を防止し操作性を向上させた衣類乾燥機を提供する。

【構成】　外枠１に開閉ドアー２と、前記開閉ドアー２の内面上に設置した糸屑捕集装置４と、外枠１内に収納した乾燥ドラム３と、そのドラム３の後部に両翼ファン６とを備え、前記開閉ドアー２はその内部にドアーダクト２－１およびその連通口２－２を設け、前記外枠１はその内部に循環ダクト９を設け、前記両翼ファン６から始まり、前記乾燥ドラム３と前記糸屑捕集装置４と前記ドアーダクト２－１およびその連通口２－２と、前記循環ダクト９とを経由し、前記両翼ファン６に戻る加熱空気による気密な循環風路を設け、前記糸屑捕集装置４は、風路中の前記乾燥ドラム３と前記ドアーダクト２－１との間に設けたものである。

図１



【特許請求の範囲】
【請求項１】　外枠前面部に設けた衣料を投入する開閉ドアーと、前記開閉ドアーの内面上に設置した糸屑捕集装置と、外枠内に収納した乾燥ドラムと、そのドラムの後方部に、循環と冷却と熱交換とを行なう両翼ファンとを備えた衣類乾燥機において、
前記開閉ドアーは、その内部にドアーダクトおよびその連通口を設け、
前記外枠は、その内部に循環ダクトを設け、
前記両翼ファンから始まり、前記乾燥ドラムと、前記糸屑捕集装置と、前記ドアーダクトおよびその連通口と、前記循環ダクトとを経由し、前記両翼ファンに戻る加熱空気による気密な循環風路を設け、
前記糸屑捕集装置は、この循環風路中の前記乾燥ドラムと前記ドアーダクトとの間に設けたことを特徴とする衣類乾燥機。
【請求項２】　連通口は、開閉ドアーに設けた糸屑捕集装置の下方部に設けたことを特徴とする請求項１記載の衣類乾燥機。
【請求項３】　糸屑捕集装置と連通口間との風路は、開閉ドアー外表面と空間部を隔てたドアーダクトにより、前記糸屑捕集装置と前記連通口間を連通して構成されることを特徴とする請求項２記載の衣類乾燥機。
【請求項４】　糸屑捕集装置とドアーダクトおよび連通口からなる風路は、開閉ドアーを閉止することにより外枠内に設けた循環ダクトと連結され循環風路を構成することを特徴とする請求項３記載の衣類乾燥機。
【請求項５】　連通口は、気密加工を施した循環ダクト開口部の内周に嵌合するよう、その連結口を凸部形状としたことを特徴とする請求項４記載の衣類乾燥機。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、衣類乾燥機に係り、操作性の優れた糸屑捕集装置と一台の両翼ファンにより循環風路を形成する衣類乾燥機に関するものである。特に、乾燥時間の短縮、省電力化が必要なランドリータイプの場合に利用される。
【０００２】
【従来の技術】従来の衣類乾燥機は、特に、乾燥ドラム式においては、乾燥時に衣類から発生する糸屑などを除去する必要があった。この発生した糸屑が、乾燥するための循環風路内に侵入し、循環風路を塞ぎ、その風量が少なくなり、乾燥時間が長くなるなど、乾燥運転機能に支障をきたしていた。そのため、発生した糸屑を捕集するため、衣類通過後の循環風路部内に、網状のフィルタで構成される糸屑捕集装置を設けていた。この糸屑捕集装置の設置場所は、乾燥衣類を通過した風下、すなわち、乾燥ドラムの後面部に設けてあるものが主であった。
【０００３】しかし、糸屑捕集装置によって捕集された糸屑は、循環風路内の圧力損失を招き、循環風量の低下を生じ、乾燥機能の低下の原因となる。そのため、捕集により堆積した糸屑は、一定時間毎に除去してやる必要がある。近年は、ランドリータイプの衣類乾燥機は、洗濯機の上部にスタンドを介して設置され、使用される場合が多くなってきた。このため乾燥ドラム後部にある糸屑捕集装置は、手が届きにくくなり、手入れしずらく、糸屑が除去されず使用されていた。このような衣類乾燥機は乾燥時間が長くなり、循環ファンがオーバロードとなり、電力浪費が大となるという欠点があった。
【０００４】上記の問題を解決するため、次のような提案がなされている。糸屑捕集装置を衣料投入用の開閉ドアーに組込み、乾燥ドラムの回転力により回転する除去用はけを糸屑捕集フィルタの表面に摺動自在に設けたものである。しかし、この技術においては、捕集された糸屑の再付着を防ぐため、乾燥ドラムへの送風を停止する必要があり、また、乾燥後の空気は循環せず、衣類乾燥機外へ排気されていた。このため、衣類乾燥機の機構が複雑となり、熱ロスも大きいという欠点があった。なお、これに関連するものとしては、例えば、実開昭５８－７５５９８記載の技術が知られている。
【０００５】さらに、上記欠点を解決するため、次のような提案がされている。衣類出入口を開閉する扉に、衣類乾燥用の循環風路とは別に、乾燥ドラム内の空気を循環させる装置を設け、かつ、循環される空気から糸屑を捕集するフィルタ、並びにフィルタカバーを設けたものである。しかし、この技術においては、糸屑を捕集するための空気循環装置を設けるため、二台のファンが必要となり、衣類乾燥機の機構が複雑となり、コストも高くなる欠点があった。これに関連するものとしては、例えば、実開平３－２５１２９７記載の技術が知られている。
【０００６】
【発明が解決しようとする課題】上記従来技術の衣類乾燥機では、糸屑の堆積状態が使用者に容易にわからず、循環風路の目づまりを起こし、循環風量が減少し、乾燥運転時間が長くなり、電力消費と熱ロスが大であり、機構が複雑となり、コストも高くなるという問題を有していた。本発明は、上記従来の問題点を解決するためになされたものであり、使用者が糸屑の堆積状態を把握し、捕集した糸屑を容易に清掃できる糸屑捕集装置を乾燥機に取りつけ、簡単な構成をもち、乾燥運転時間が短く、省エネルギー、且つ、操作性を向上させた衣類乾燥機を提供することにある。
【０００７】
【課題を解決するための手段】上記目的を達成するために、衣類乾燥機に係る本発明の構成は、外枠前面部に設けた衣料を投入する開閉ドアーと、前記開閉ドアーの内面上に設置した糸屑捕集装置と、外枠内に収納した乾燥ドラムと、そのドラムの後方部に、循環と冷却と熱交換

とを行なう両翼ファンとを備え、前記開閉ドアーは、その内部にドアーダクトおよびその連通口を設け、前記外枠は、その内部に循環ダクトを設け、前記両翼ファンから始まり、前記乾燥ドラムと、前記糸屑捕集装置と、前記ドアーダクトおよびその連通口と、前記循環ダクトとを経由し、前記両翼ファンに戻る加熱空気による気密な循環風路を形成し、前記糸屑捕集装置は、この循環風路中の前記乾燥ドラムと前記ドアーダクトとの間に設けたものである。また、連通口は、開閉ドアーに設けた糸屑捕集装置の下方部に設け、糸屑捕集装置と連通口間との風路は、開閉ドアー外表面と空間部を隔てたドアーダクトにより、前記両者間を連通したものである。さらに、糸屑捕集装置とドアーダクトおよび連通口からなる風路は、開閉ドアーを閉止することにより外枠内に設けた循環ダクトと連結され、循環風路を形成するようにしたものである。連通口は、その形状を凸形とし、気密加工を施した循環ダクト開口部の内周に嵌合するようにしたものである。

【０００８】

【作用】上記各技術的手段の働きは次のとおりである。本発明の構成によれば、外枠前面部に衣料を投入する開閉ドアーと、前記ドアーの内面上に設置した糸屑捕集装置と、外枠内に収納した乾燥ドラムと、そのドラムの後方部に両翼ファンとを備え、前記開閉ドアーには、その内部にドアーダクトおよびその連通口を設け、前記外枠の内部には循環ダクトを設け、前記両翼ファンから始まり、前記乾燥ドラムと、前記糸屑捕集装置と、前記ドアーダクトおよびその連通口と、前記循環ダクトとを経由し、前記両翼ファンに戻る加熱空気による気密な循環風路を形成し、前記糸屑捕集装置は、この循環風路中の前記乾燥ドラムと前記ドアーダクトとの間に設けたので、両翼ファンにより循環風路におくられた加熱空気は、循環風路の気密構造のため、他に流れること無く、糸屑捕集装置を通過し、含んでいる糸屑が除去されることになる。開閉ドアーをあけると、糸屑捕集装置内に捕集された糸屑の存在を使用者が容易に確認でき、糸屑捕集装置の清掃も簡単に行える。

【０００９】

【実施例】以下本発明の一実施例を図１ないし図３を参照して説明する。

〔実施例　１〕図１は、本発明の一実施例に係る衣類乾燥機の断面図、図２は、図１の衣類乾燥機の主要部背面図、図３は、図１の衣類乾燥機ドアー部の部分拡大図である。図１において、１は外枠、１ｆは外枠前板、１ｂは外枠後板、２は開閉ドアー、２-１はドアーダクト、２-２は連通口、３は乾燥ドラム、３－１は乾燥ドラム駆動モータ、４は糸屑捕集装置、５は加熱空気用発熱体、６は両翼ファン、７はドラム駆動プーリ、８はファン駆動プーリ、９は循環ダクト、９ａは循環ダクト前部、９ｂは循環ダクト中部、９ｃは循環ダクト後部、９ｄは循環ダクト排水口、１１は循環ダクト接続管、１２はドラムベルト、１３は張力付加プーリ、１４はファンベルト、１５はドラム後方支持板、１５－１はドラムシャフト、１５－２はドラム軸受、１６はファンケーシング、１６－１はファン吸込口、１６－２は流水路、１６－３はファン吐出口、１６－４は仕切板、１６－５はケーシング接続管、１７はドラム前方支持体、１７－１は開口部、１９は制御装置、１９－１はパネルベース、２０ａはパッキン（１）、２０ｂはパッキン（２）、Ａは循環側、Ｂは冷却側、Ｃは空間部である。

【００１０】本実施例の構成を説明する。図１、２、３において、外枠１の前面部には、衣料を投入する開閉ドアー２を設け、その内部には、乾燥ドラム３が収納されている。この乾燥ドラム３の後方部（本実施例においては、開閉ドアー２側を前方とし、その反対側を後方とする）には、循環作用と冷却作用と熱交換作用とを一台にて行なう両翼ファン６を配し、前記開閉ドアー２内面上には、前記乾燥ドラム３内の乾燥物から発生した糸屑を除去する糸屑捕集装置４を設置されている。ドアーダクト２－１が前記開閉ドアー２内の空間部に、循環ダクト９が前記外枠１内にそれぞ設けられ、連通口２－２により、この両者は接続されている。これによって、前記両翼ファン６から始まり、前記乾燥ドラム３と、前記糸屑捕集装置４と、前記開閉ドアー２内の空間部に設けたドアーダクト２－１およびその連通口２－２と、前記外枠１内に設けた循環ダクト９とからなり、再び前記両翼ファン６に戻る気密な循環風路を形成している。そして、この風路に乾燥用加熱空気を循環させるため、風路内には、加熱空気用発熱体５が設けられている。

【００１１】本実施例の構成細部を詳しく説明する。乾燥ドラム３の前側は、前記外枠１の外枠前板１ｆに取付られたドラム前方支持体１７に支持され、その後側は、ドラムシャフト１５-１にドラム軸受１５-２を介して軸支され、回転自在となっている。このドラムシャフト１５-１は、外枠１内の後方部に取付られたドラム後方支持板１５に固定されている。また、乾燥ドラム３は、ドラム駆動プーリ７および張力付加プーリ１３により張力を与えられたドラムベルト１２により、回転するようになっている。このドラム駆動プーリ７および張力付加プーリ１３には、外枠１内の上部に備えたモータベース３－２を介して取付けられた駆動モータ３－１の回転力が伝達される。

【００１２】糸屑捕集装置４は、密目のフィルター（１）４ａと粗目のフィルター（２）４ｂとを重ね、この両面をガード４ｃにて保護し、フィルター部材４ｄが形成されている。このフィルター部材４ｄは、衣類の出し入れを行う開閉ドアー２の内面に取付けられ、その表側にはフィルター部材カバー４ｅを装着する。これらフィルター部材４ｄ，フィルター部材カバー４ｅは、それぞれ取外しできるように着脱自在となっている。糸屑捕集

装置４のドアー側は、開閉ドアー２の外表面と空間部Ｃを隔てて設けられたドアーダクト２－１により連通口２-２を経由して循環ダクト前部９ａと気密を保持して連結されている。加熱空気発熱体５は、空気を加熱し、前記循環風路に熱風を供給するための発熱体である。前記加熱空気発熱体５は、前記ファンケーシング１６のファン吐出口１６-３の風下側に設置されており、乾燥ドラム３内には、前記発熱体５に対向して乾燥ドラム流入口３-３を備えられている。

【００１３】両翼ファン６が、乾燥ドラム３の後方の位置に、ファンケーシング１６に納められ設置されている。ファンケーシング１６は、前記後方支持板１５に固定されている。両翼ファン６は、前記乾燥ドラム駆動モータ３－２により、ファン駆動プーリ８、ファンベルト１４、さらに、当該両翼ファン６に取付けられたファン従動プーリ６-１を介して回転するようになっている。また、両翼ファン６は、ファンケーシング１６を仕切板１６-４の表裏にて、循環側Ａ、冷却側Ｂとに仕切り、循環側Ａは乾燥ドラム３内の加熱乾燥空気の循環し、冷却側Ｂは、外気の吸入、排気を行い、両側を気密に分離させる表裏両翼タイプとなっている。

【００１４】ファンケーシング１６は、気密構造となっており、ファン吸込口１６-１を有し、乾燥ドラム３，糸屑捕集装置４，ドアダクト２－１，連通口２-２を経由して循環ダクト前部９ａと、途中に循環ダクト排水口９ｄを備えた循環ダクト中部９ｂおよび循環ダクト後部９ｃと連り、循環風路を形成している。また、開閉ドアー２閉止時における開閉ドアー２とドラム支持体１７の開口部１７－１および連通口２－２との気密保持は、各々パッキン（１）２０ａ、パッキン（２）２０ｂでなされる。さらに、ドアーダクト２－１と連通口２－１との接続部は、パッキン（２）２０ｂの内側へ、ドアーダクト２－１からの凸部形状によりオーバーハング角θで接続するように構成されている。

【００１５】外枠裏板１ｂは、衣類乾燥機本体後面を覆う裏板で、外枠１の後面に取付けられている。制御装置１９は前記モータ４、発熱体５などの運転を制御する装置であり、パネルベース１９－１を介して外枠前板１ｆに取付けられている。次に、前記ファンケーシング１６の下部の構造について詳述する。ファンケーシング１６の最下部は、ファンケーシング１６と一体形成されたケーシング接続管１６－５を有し、循環ダクト後部９ｄと一体形成された循環ダクト接続管１１が各々で気密を保持して接続され、流水路１６－２が設けられている。

【００１６】上記のように構成された本実施例による衣類乾燥機の動作について説明する。衣類乾燥機の電源スイッチ（図示せず）をＯＮすると、駆動モータ４、加熱空気用発熱体５が通電され、前記駆動モータ４の回転により乾燥ドラム３および両翼ファン６が回転する。乾燥ドラム３内の空気は、両翼ファン６により、乾燥ドラム３→糸屑捕集装置４→ドアーダクト２－１→連通口２－２→循環ダクト前部９ａ→循環ダクト中部９ｂ→循環ダクト後部９ｃ→ファン吸込口１６－１→ファンケーシング１６の循環側Ａ→ファン吐出口１６－３→加熱空気用発熱体５→乾燥ドラム流入口３－３→乾燥ドラム３と循環風路内を加熱空気となってを循環する。循環風路は気密構造となっているため、糸屑を含んだ加熱空気が糸屑捕集装置４を通過し、その糸屑が除去される。図１、２、３の矢印およびＰは、循環風路内を加熱空気の循環方向を示し、図２に示すＰは、乾燥ドラム３内空気の循環方向を示すものである。

【００１７】乾燥ドラム３内の衣類は、加熱された温風が接触し、衣類の水分が蒸発し、高温高湿、例えば、約５５℃ ９９％の蒸気が循環される。また、ファンケーシング１６の冷却側Ｂは、外気が吸入，排気される。これにより両翼ファン６の表裏により乾燥ドラム３内の循環蒸気と外気の熱交換が行われ循環蒸気が凝縮される。凝縮された水分は、循環側Ａの流水路１６－２を介して循環ダクト後部９ｄを経て循環ダクト中部９ｂへ導かれ、循環ダクト排水口９ｃより機体外へと排出される。このようにして、衣類が乾燥される。

【００１８】糸屑捕集装置４は、その流入する加熱温風が、乾燥ドラム３出口の温風であり、衣類通過後の高温高湿の空気である。このため、外気に近い開閉ドアー２を循環風路とした場合、外気との熱交換により多量の結露水を生じる。開閉ドアー２の外表面とに空間部Ｃを設けてドアーダクト２－２を構成しているため、空間部Ｃの断熱作用により、熱交換量が著しく低減される。しかし、結露水を皆無とすることは極めて困難である。そこで、ドアーダクト２－１の下部は、連通口２－２に向かってなだらかな曲面で、かつ、傾斜構造となっている。また、連通口２－２は、パッキン(２)２０ｂの内周部に入り込み、嵌合するよう凸部形状で嵌合接続するよう構成されている。そのため結露水がスムーズに排出すると共に、循環風路外への漏れも防止される。

【００１９】また乾燥運転の後半おいては、糸屑捕集装置４に流入する循環風は、高温、例えば、約７０～７５℃となるが、空間部Ｃの断熱作用により、開閉ドアー２の外表面の温度は低い温度に抑えられる。これにより、使用者の熱的安全性も十分確保できる。さて、洗濯機の上部にスタンドを介して衣類乾燥機を設置する場合、いわゆる、ランドリータイプの衣類乾燥機においては、糸屑捕集装置４は、衣類乾燥終了後開閉ドアー２をあけると、使用者のほぼ眼の高さに存在するため、糸屑の溜り具合が容易に確認でき、掃除する場合にも簡単に着脱できる高さ状態である。従って、糸屑捕集装置４のフイルタは清浄であり、目詰まりがなくなり、操作性が向上する。

【００２０】

【発明の効果】以上詳細に説明したように、本発明によ

れば、使用者が糸屑の堆積状態を把握し、捕集した糸屑を容易に清掃できる糸屑捕集装置を乾燥機に取りつけ、簡単な構成をもつ、乾燥運転時間の短く、省エネルギー、且つ、操作性を向上させた衣類乾燥機を提供することができる。

【図面の簡単な説明】

【図１】本発明の一実施例に係る衣類乾燥機の断面図である。

【図２】図１の衣類乾燥機の主要部の背面図である。

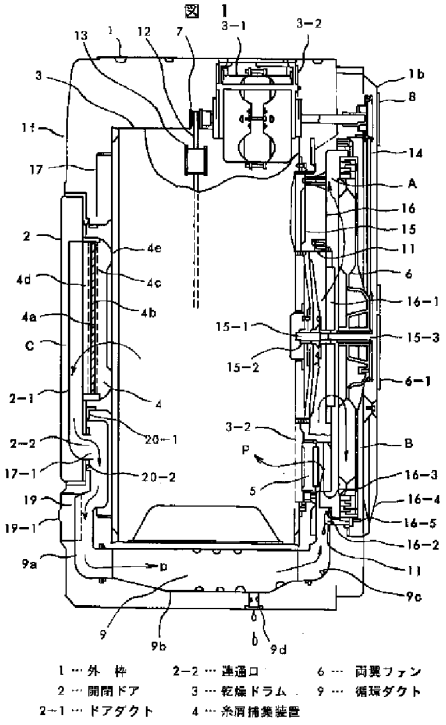
【図３】図１の衣類乾燥機ドアー部の部分拡大図である。

【符号の説明】

１　外枠
１ｆ　外枠前板
１ｂ　外枠後板
２　開閉ドアー
２－１　ドアーダクト
２－２　連通口
３　乾燥ドラム
３－１　駆動モータ
３－２　モータベース
３－３　ドラム流入口
４　糸屑捕集装置
４ａ　フィルター（１）
４ｂ　フィルター(２)
４ｃ　ガード
４ｄ　フィルター部材
４ｅ　フィルター部材カバー
５　加熱空気発熱体
６　両翼ファン
６－１　ファン従動プーリ
７　ドラム駆動プーリ
８　ファン駆動プーリ
９　循環ダクト
９ａ　循環ダクト前部
９ｂ　循環ダクト中部
９ｃ　循環ダクト後部
９ｄ　循環ダクト排水口
１１　循環ダクト接続管
１２　ドラムベルト
１３　張力付加プーリ
１４　ファンベルト
１５　ドラム後方支持板
１５－１　ドラムシャフト
１５－２　ドラム軸受
１５－３　ファンシャフト
１６　ファンケーシング
１６－１　ファン吸込口
１６－２　流水路
１６－３　ファン吐出口
１６－４　仕切板
１６－５　ケーシング接続管
１７　ドラム前方支持体
１７－１　開口部
１９　制御装置
１９－１　パネルベース
２０ａ　パッキン（１）
２０ｂ　パッキン（２）
Ａ　循環側
Ｂ　冷却側
Ｃ　空間部
Ｐ　乾燥空気循環方向
θ　オーバハング角

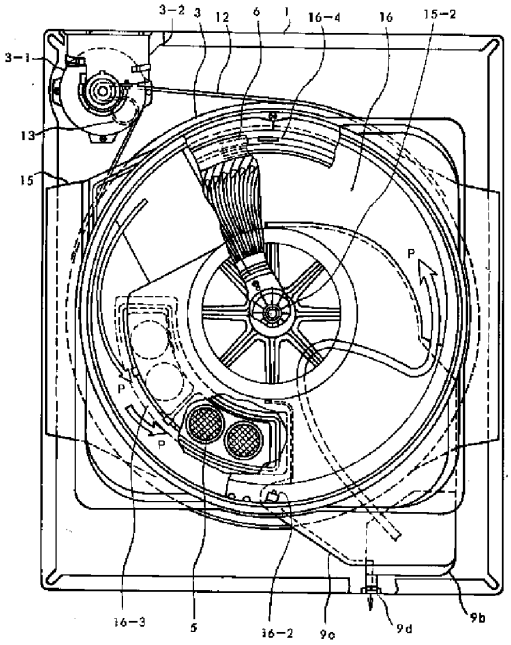
【図1】

図 1



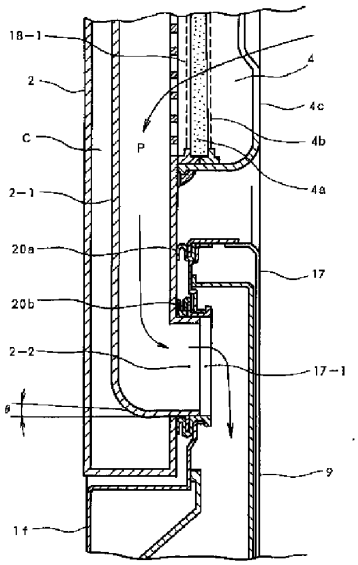
【図2】

図 2



【図3】

図 3



フロントページの続き

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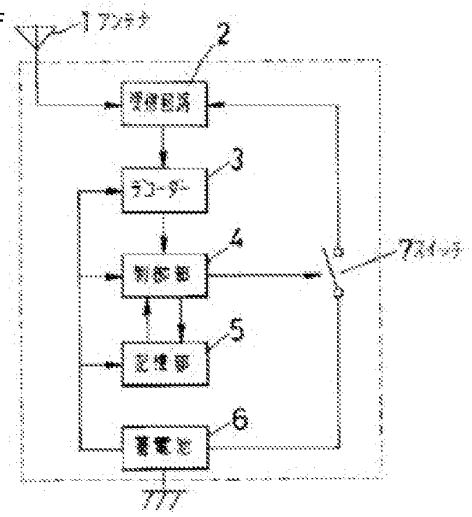
(71)Applicant : MATSUSHITA ELECTRIC WORKS LTD
(72)Inventor : MAEDA KAZUNARI
OYA AKIRA

(54) INTERMITTENT RECEPTION SYSTEM

(57)Abstract:
PURPOSE: To attain sure detection and to reduce power consumption even when an intermittent reception interval of a receiver is extended.
CONSTITUTION: A leader part of a radio signal sent from a transmitter is formed to be m-sets of frames comprising blocks with m-bits data strings. A receiver uses a storage section 5 to store the arrangement state of bits of the leader part of the radio signal in advance and a control section 4 compares a data content in m-bits to be received with the storage content when optional consecutive m-bits of the leader part are received. Thus, the receiver discriminates a start position of a data part and controls it that no reception is executed before the data part is not started.



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Ｈ０４Ｂ　7/26		Ｘ　9297－5Ｋ		

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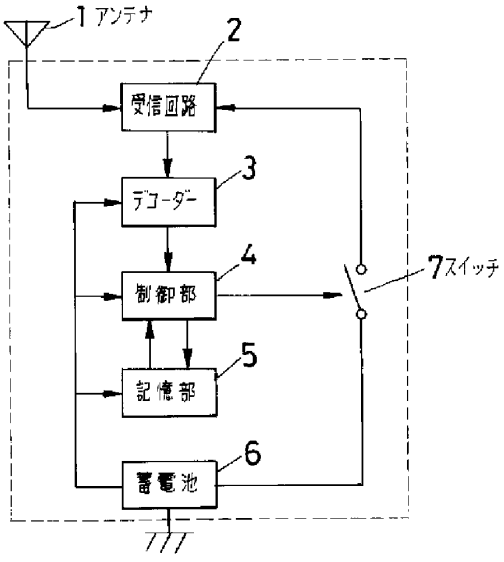
(54)【発明の名称】　間欠受信方式

(57)【要約】
【目的】　受信機の間欠受信間隔を長くしても、確実に検出するとともに、消費電力を低減させる。
【構成】　送信機から送出される無線信号のリーダー部を、ｍビットのデータ列で構成されるブロックからなるフレームをｍ個並べたものとし、受信機では、予め無線信号のリーダー部のビットの配置状態を記憶部５に記憶しておき、リーダー部の任意の連続ｍビットを受信したときに、制御部４で、受信したｍビットのデータ内容と前記記憶内容とを比較することにより、データ部の開始位置を判断し、データ部が開始するまでの間、受信動作を行わないように制御する。



【特許請求の範囲】
【請求項１】　無線信号を受信する受信回路と、受信信号を解読するデコーダーと、データを記憶する記憶部と各部を制御する制御部および電源としての蓄電池を有して成る受信機とリーダー部とデータ部とで構成された無線信号を送出する送信機とからなる無線装置の間欠受信方式において、前記無線信号のリーダー部を、ｍビットのデータ列で構成されるブロックからなるフレームをｍ個並べたものとし、受信機では、前記リーダー部の任意の連続ｍビットを受信し、受信したｍビットのデータ内容により、制御部で、データ部の開始位置を判断するようにし、データ部が開始するまでの間、受信動作を行わないように制御するようにしたことを特徴とする間欠受信方式。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、蓄電池を電源として用いる受信機の間欠受信方式に関するものである。
【０００２】
【従来の技術】従来、無線装置において、この種の受信機は、消費電力を抑えるため、通常、間欠受信を行う。受信機が間欠受信を行っている場合、送信機から送信されるリーダー部とデータ部とからなる無線信号のリーダー部を検出すると、受信機は間欠受信動作から連続受信動作へと移行し、データ部の受信を行うのである。一般に、リーダー部を確実に受信できるように、リーダー部の長さは受信機の間欠受信間隔の長さよりも長く設定されるのである。
【０００３】
【発明が解決しようとする課題】ところが、受信機の消費電力を小さくするために、間欠受信間隔の長さを長くすると、送信機から送信される無線信号のリーダー部の長さを長くしなければならなくなる。リーダー部の長さを長くすると、受信機がリーダー部を検出してからデータ部の検出を開始するまでの時間が長くなってしまい、受信機の消費電力が大きくなるという問題があった。
【０００４】本発明は、上記の点に鑑みてなしたものであり、その目的とするところは、受信機の間欠受信間隔を長くしても、確実に検出するとともに、消費電力を低減させるようにした間欠受信方式を提供することにある。
【０００５】
【課題を解決するための手段】本発明は、無線信号を受信する受信回路と、受信信号を解読するデコーダーと、データを記憶する記憶部と各部を制御する制御部および電源としての蓄電池を有して成る受信機とリーダー部とデータ部とで構成された無線信号を送出する送信機とからなる無線装置の間欠受信方式において、前記無線信号のリーダー部を、ｍビットのデータ列で構成されるブロックからなるフレームをｍ個並べたものとし、受信機では、前記リーダー部の任意の連続ｍビットを受信し、受信したｍビットのデータ内容により、制御部で、データ部の開始位置を判断するようにし、データ部が開始するまでの間、受信動作を行わないように制御するようにしたことを特徴とするものである。
【０００６】
【作用】本発明の間欠受信方式にあっては、送信機から送出される無線信号のリーダー部を、ｍビットのデータ列で構成されるブロックからなるフレームをｍ個並べたものとし、受信機では、予め無線信号のリーダー部のビットの配置状態を記憶しておき、リーダー部の任意の連続ｍビットを受信したときに、制御部では、受信したｍビットのデータ内容と前記記憶内容とを比較することにより、データ部の開始位置を判断し、データ部が開始するまでの間、受信動作を行わないように制御するようにしている。
【０００７】
【実施例】以下、本発明の一実施例を図面に基づき説明する。
【０００８】図１は、本発明に係る受信機の一実施例を示すブロック図である。１は受信アンテナ、２は受信回路、３は受信回路２で受信した受信信号のデータ内容を解読するデコーダー、４は各部を制御する制御部、５はデータを記憶しておく記憶部であり、特に、本実施例では、送信機（図示せず）からの無線信号のリーダー部のビット内容を予め記憶しておくものである。６は前記各部に電源を供給する蓄電池である。７は制御部４からの信号により受信回路１への電源供給のオンオフを切り換えるスイッチである。
【０００９】送信機から送出される無線信号は、図２に示したようにリーダー部とそれに続くデータ部とからなる。リーダー部は、例えば、８ビットからなるフレームを８個連続させたもので構成される。各フレームのデータ列は各々異なっており、本実施例では、第１フレームから順を追って、「１」のビットの数が１つづつ増えていくようにしてある。
【００１０】記憶部５では、前記無線信号のリーダー部の各フレームのデータ列の内容（「０」または「１」の数およびその配置状況）を、図４に示すような形式で予め記憶しておくのである。つまり、第１フレームでは、ｍｓｂのビットのみが「１」であり、第２フレーム以降は順に「１」のビットが１つづつ増えていき、第８フレームでは、ｍｓｂから１ｓｂまで全てのビットが「１」となっているのである。
【００１１】図３のタイミングチャートにより、間欠受信の動作を説明する。ａは間欠受信の間隔であり、ｂはリーダー部の受信が終了した時点からデータ部の受信が開始されるまでの時間を示している。リーダー部の長さは間欠受信の間隔ａの長さよりも長く設定される。
【００１２】制御部４では、受信したリーダー部の連続

した任意の８ビットを検出し、この連続した８ビットのビット配列により、データ部の開始時点までの時間を算出し、その時間まで、受信を行わないようにスイッチ７をオフしておくのである。

【００１３】データ部の開始時点までの時間の算出の例としては、例えば、受信したリーダー部の連続８ビットが「００００１１００」であるなら、受信終了点は第２フレームの第５ビットであり、第２フレーム第６ビットから第８フレームの第８ビットまでの時間は受信を行わないようにすればよい。また、受信したリーダ部の連続８ビットが「１００００００１」であるなら、受信終了点は第４フレームの第２ビットであり、第４フレームの第３ビットから第８フレームの第８ビットまでの時間は受信をしないようにすればよいのである。

【００１４】このように、本実施例によれば、受信機の間欠受信間隔を長くし、より確実に受信されるように無線信号のリーダー部の時間を長くしても、受信機では受信した時点でリーダー部のどの部分を受信したかが認識できるので、その後、データ部の開始位置まで、受信動作を休止させることが可能となり、消費電力を低減することができるのである。

【００１５】

【発明の効果】以上のように、本発明の受信方式によれば、送信機から送出される無線信号のリーダー部を、ｍビットのデータ列で構成されるブロックからなるフレームをｍ個並べたものとし、受信機では、予め無線信号のリーダー部のビットの配置状態を記憶しておき、リーダー部の任意の連続ｍビットを受信したときに、制御部では、受信したｍビットのデータ内容と前記記憶内容とを比較することにより、データ部の開始位置を判断し、データ部が開始するまでの間、受信動作を行わないようにしたので、受信機の間欠受信間隔を長くしても、確実に検出するとともに、消費電力を低減させるようにした間欠受信方式が提供できた。

【図面の簡単な説明】

【図１】本発明に係る受信機の一実施例を示すブロック図である。

【図２】同上に係る無線信号のフォーマット図である。

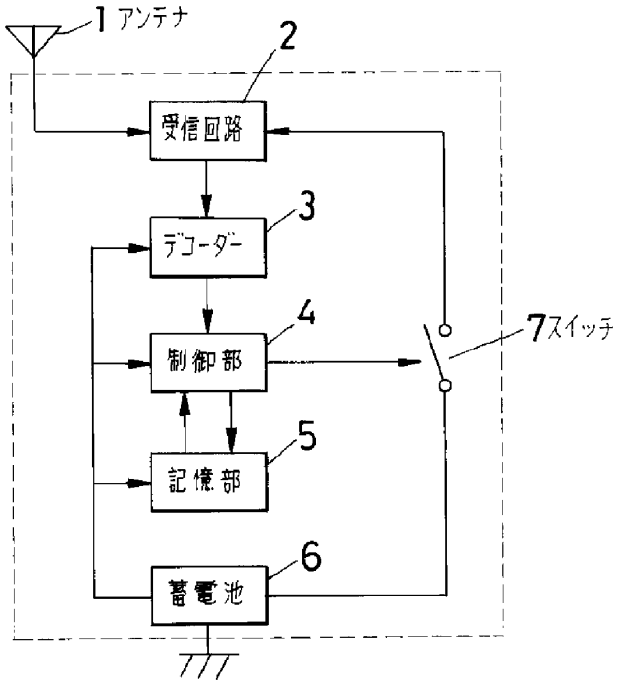
【図３】同上の動作説明のためのタイムチャートである。

【図４】同上に係る記憶部の記憶内容を示す模式図である。

【符号の説明】

１　受信アンテナ
２　受信回路
３　デコーダー
４　制御部
５　記憶部
６　蓄電池
７　スイッチ

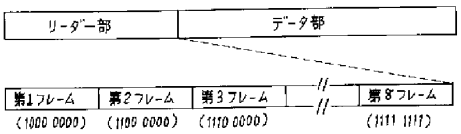
【図１】



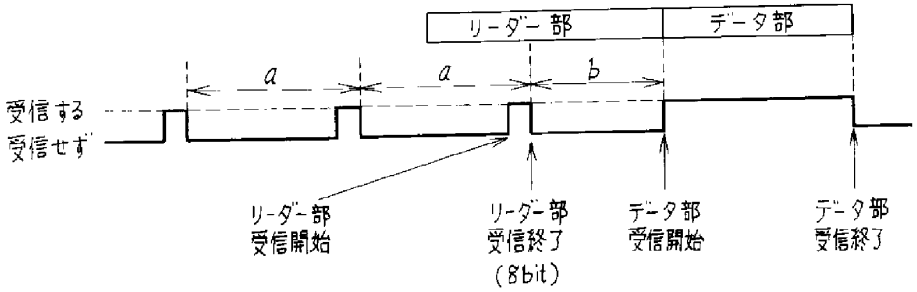
【図４】

第１フレーム	msb	1000	0000	lsb
第２フレーム	msb	1100	0000	lsb
第３フレーム	msb	1110	0000	lsb
第４フレーム	msb	1111	0000	lsb
第５フレーム	msb	1111	1000	lsb
第６フレーム	msb	1111	1100	lsb
第７フレーム	msb	1111	1110	lsb
第８フレーム	msb	1111	1111	lsb

【図2】


リーダー部
データ部
第1フレーム
第2フレーム
第3フレーム
第8フレーム
(1000 0000)
(1100 0000)
(1110 0000)
(1111 1111)

【図3】


リーダー部
データ部
a
a
b
受信する
受信せず
リーダー部
受信開始
リーダー部
受信終了
(8bit)
データ部
受信開始
データ部
受信終了

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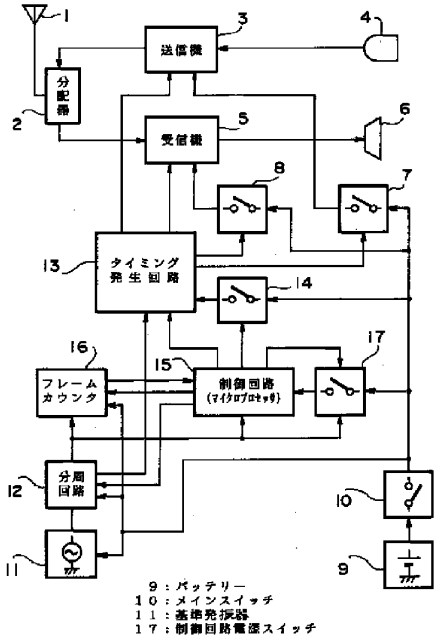
(54)【発明の名称】　無線電話機

(57)【要約】

【目的】　待ち受け受信時にも制御回路への電源の供給を停止できる、消費電力の少ない無線電話機を得る。

【構成】　分周回路からのフレーム信号を計数するフレームカウンタを設け、このフレームカウンタのフレーム値に基づいてタイミング発生回路等の制御を行う制御回路に、前記フレーム信号でオン、自身の発生する制御信号でオフして、メインスイッチを経由した電源の、当該制御回路への供給を制御する制御回路電源スイッチを付加し、またバッテリーバックアップされた補助メモリに当該無線電話機の動作状態を記憶・保持させ、またタイミング発生回路によるタイミング制御を、分周回路からのフレームパルスとフレームカウンタからのフレーム値に基づいて行う。



1

【特許請求の範囲】

【請求項1】　メインスイッチを経由したバッテリーからの電源を受けて基準信号を発生する基準発振器と、前記基準発振器の発生する基準信号を分周する分周回路と、前記分周回路より出力されるフレーム信号を計数するフレームカウンタと、前記分周回路より出力されるフレームパルスに基づいて送受信のタイミングを制御するタイミング発生回路と、前記フレームカウンタより読み込んだフレーム値に基づいて、前記分周回路、フレームカウンタ、タイミング発生回路の制御を行う制御回路と、前記分周回路からのフレーム信号でオン、前記制御回路からの制御信号でオフにされて、前記メインスイッチを経由したバッテリーからの電源の前記制御回路への供給を制御する制御回路電源スイッチとを備えた無線電話機。

【請求項2】　前記バッテリーをバックアップする補助バッテリーと、前記バッテリーの電圧が低下した場合に前記補助バッテリーに切り換えるバッテリーバックアップ回路と、前記メインスイッチと連動し、前記バッテリーバックアップ回路にて切り換えられたバッテリーもしくは補助バッテリーからの電源を、前記基準発振器、分周回路およびフレームカウンタに供給するバックアップ電源スイッチと、前記バックアップ電源スイッチを介して電源の供給を受け、当該無線電話機の動作状態を記憶・保持する補助メモリとを備えたことを特徴とする、請求項1に記載の無線電話機。

【請求項3】　前記タイミング発生回路が、前記送受信のタイミングを、前記分周回路より出力されるフレームパルスと、前記フレームカウンタより読み込んだフレーム値に基づいて制御することを特徴とする、請求項1または2に記載の無線電話機。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明は、パワーセーブモードでの動作が可能な、ディジタル無線電話装置等の無線電話機に関するものである。

【０００２】

【従来の技術】図４は従来の無線電話機を示すブロック図である。図において、１は電波の送受信が行われるアンテナであり、２はこのアンテナ１への送信高周波信号とアンテナ１からの受信高周波信号とを分配統合する分配器である。３は音声電気信号を前記送信高周波信号に変換する送信機であり、４は音声を前記音声電気信号に変換するマイクロホンである。５は前記受信高周波信号を音声電気信号に変換する受信機であり、６はその音声電気信号を音声に変換するレシーバである。７は前記送信機３に供給される電源をオン・オフする送信系電源スイッチであり、８は前記受信機５に供給される電源をオン・オフする受信系電源スイッチである。９はこの無線電話機全体の電源を供給するバッテリー、１０はこのバッテリー９からの電源供給のオン・オフを行うメインスイッチであり、前記送信系電源スイッチ７および受信系電源スイッチ８はそれぞれこのメインスイッチ１０を介してバッテリー９に接続されている。

2

【０００３】また、１１はバッテリー９からの電源の供給をメインスイッチ１０より直接受けて発振し、基準信号を発生する基準発振器であり、１２はこの基準発振器１１の発生する基準信号を分周する分周回路である。１３はこの分周回路１２より出力されるフレームパルスに基づいて、前記送信器３、受信機４、送信系電源スイッチ７、受信系電源スイッチ８などの制御を行って、送受信のタイミングを制御するタイミング発生回路であり、１４はメインスイッチ１０を介してバッテリー１０に接続され、タイミング発生回路１３に供給される電源をオン・オフするタイミング回路電源スイッチである。１５は前記分周回路１２の出力するフレーム信号に基づいて、分周回路１２、タイミング発生回路１３、タイミング回路電源スイッチ１４などの制御を行う制御回路としてのマイクロプロセッサである。なお、このマイクロプロセッサ１５への電源供給は、メインスイッチ１０より直接行われている。

【０００４】次に動作について説明する。メインスイッチ１０がオンになると、それによって電源が供給されたマイクロプロセッサ１５は動作を開始して分周回路１２を初期化する。その後、待ち受け受信を行う場合には、タイミング発生回路１３に指示して送信系電源スイッチ７と受信系電源スイッチ８をオフにさせ、さらに自身でタイミング回路電源スイッチ１４をオフにする。これによって電源の供給を受けているのは、基準発振器１１、分周回路１２、およびマイクロプロセッサ１５の３つとなる。マイクロプロセッサ１５は分周回路１２からのフレーム信号をそのソフトウェアで計数してフレームのタイプを判定し、そのフレームが当該無線電話機に該当する制御チャンネルであった場合には、タイミング回路電源スイッチ１４をオンにしてタイミング発生回路１３を動作させ、そのタイミング発生回路１３に送信系電源スイッチ７と受信系電源スイッチ８をオンさせるように指示する。このようにして、マイクロプロセッサ１５はフレーム毎にそのフレームタイプに応じた制御をタイミング発生回路１３に対して行っている。

【０００５】

【発明が解決しようとする課題】従来の無線電話機は以上のように構成されているので、待ち受け受信時においても、特定のフレームタイミングで制御チャンネルを受信するために、絶えずフレームをソフトウェア的に監視している必要があり、マイクロプロセッサ１５には常に電源を供給しておかなければならないという問題点があった。

【０００６】この発明は、上記のような問題点を解消するためになされたもので、待ち受け受信時には制御回路

3

の電源をオフにすることができる無線電話機を得ることを目的とする。

【０００７】

【課題を解決するための手段】請求項１に記載の発明に係る無線電話機は、分周回路より出力されるフレーム信号を計数するフレームカウンタを設け、そのフレームカウンタより読み込んだフレーム値に基づいて、分周回路、フレームカウンタ、タイミング発生回路等の制御を行う制御回路に、分周回路からのフレーム信号でオン、制御回路自身からの制御信号でオフして、メインスイッチを経由したバッテリーからの電源の制御回路への供給を制御する制御回路電源スイッチを付加したものである。

【０００８】また、請求項２に記載の発明に係る無線電話機は、バッテリーの電圧が低下した場合に補助バッテリーに切り換えるバッテリーバックアップ回路を経由した電源を、メインスイッチと連動するバックアップ電源スイッチにて基準発振器、分周回路、フレームカウンタ等に供給するバックアップ電源スイッチと、このバックアップ電源スイッチを介して電源の供給を受け、当該無線電話機の動作状態を記憶・保持する補助メモリを設けたものである。

【０００９】また、請求項３に記載の発明に係る無線電話機は、タイミング発生回路による送受信のタイミング制御を、分周回路より出力されるフレームパルスと、フレームカウンタより読み込んだフレーム値に基づいて行うものである。

【００１０】

【作用】請求項１に記載の発明における制御回路は、分周回路より出力されるフレーム信号を計数しているフレームカウンタより読み込んだフレーム値に基づいて、分周回路、フレームカウンタ、タイミング発生回路等の制御を行うとともに、分周回路からのフレーム信号でオンして当該制御回路への電源の供給を制御する制御回路電源スイッチを、自身の送出する制御信号でオフすることにより、待ち受け受信時における制御回路への電源の供給を停止するとともに、その電源のオン・オフによってフレーム情報が失われることのない無線電話機を実現する。

【００１１】また、請求項２に記載の発明における補助メモリは、バッテリーバックアップ回路を経由した電源の供給をバックアップ電源スイッチを介して受け、当該無線電話機の動作状態を記憶・保持することにより、通話中にバッテリーの交換を行っても、呼が切断されることなく、バッテリーが装着されれば通話を再開できる無線電話機を実現する。

【００１２】また、請求項３に記載の発明におけるタイミング発生回路は、分周回路からのフレームパルスと、フレームカウンタからのフレーム値に基づいて、送受信のタイミング制御を行うことにより、制御回路の処理負荷を軽減する。

4

【００１３】

【実施例】実施例１．以下、この発明の実施例１を図について説明する。図１は請求項１に記載した発明の一実施例を示すブロック図である。図において、１はアンテナ、２は分配器、３は送信機、４はマイクロホン、５は受信機、６はレシーバ、７は送信系電源スイッチ、８は受信系電源スイッチ、９はバッテリー、１０はメインスイッチ、１１は基準発振器、１２は分周回路、１３はタイミング発生回路、１４はタイミング回路電源スイッチ、１５は制御回路としてのマイクロプロセッサであり、図４に同一符号を付した従来のそれらと同一、もしくは相当部分であるため、詳細な説明は省略する。

【００１４】また、１６は分周回路１２より出力されるフレーム信号を計数し、外部よりその計数値を読み取ることが可能なフレームカウンタである。１７は分周回路１２からのフレーム信号でオン、マイクロプロセッサ１５自身の発生する制御信号でオフとなり、当該マイクロプロセッサ１５へのメインスイッチ１０を経由したバッテリー９からの電源の供給を制御する制御回路電源スイッチである。なお、マイクロプロセッサ１５は、フレームカウンタ１６より読み込んだフレーム値に基づいて、分周回路１２、フレームカウンタ１６、タイミング発生回路１３等の制御を行うとともに、待ち受け受信時には制御回路電源スイッチ１７をオフにして自身への電源の供給を停止している。

【００１５】次に動作について説明する。メインスイッチ１０がオンになると、このメインスイッチ１０を介してバッテリー９からの電源の供給を受けた基準発振器１１が発振を開始し、分周回路１２はこの基準発振器１１の発生した基準信号を分周してフレーム信号を生成する。制御回路電源スイッチ１７はこのフレーム信号を受けてオンとなり、それによって電源が供給されたマイクロプロセッサ１５は動作を開始して分周回路１２およびフレームカウンタ１６の初期化を行う。その後、待ち受け受信を行う場合には、タイミング発生回路１３を通じて送信系電源スイッチ７および受信系電源スイッチ８をオフにし、また、マイクロプロセッサ１５が直接、タイミング回路電源スイッチ１４および制御回路電源スイッチ１７をオフにする。これによって電源の供給を受けているのは、基準発振器１１、分周回路１２、およびフレームカウンタ１６の３つとなり、分周回路１２は基準発振器１１からの基準信号を分周してフレーム信号の生成を継続し、フレームカウンタ１６はそのフレーム信号の計数を継続する。

【００１６】一方、制御回路電源スイッチ１７は、分周回路１２より送出されるフレーム信号を受けるとオンとなってマイクロプロセッサ１５は動作を開始する。動作を開始したマイクロプロセッサ１５はまず、フレームカウンタ１６からフレーム値を読み取ってそのフレームの

5

タイプを判定し、そのフレームが当該無線電話機に該当する制御チャンネルであった場合には、タイミング回路電源スイッチ１４をオンにしてタイミング発生回路１３を動作させ、そのタイミング発生回路１３に送信系電源スイッチ７と受信系電源スイッチ８をオンさせるように指示する。また、前記フレーム値が該当する制御チャンネルでなかった場合には、マイクロプロセッサ１５は制御信号を制御回路電源スイッチ１７に送ってそれをオフにし、自分自身への電源の供給を停止する。これによってマイクロプロセッサ１５は、次のフレーム信号が分周回路１２より送出されるまで電源の供給が遮断され、当該マイクロプロセッサ１５で消費される電流を節約することができる。

【００１７】実施例２．次に、この発明の実施例２を図について説明する。図２は請求項２に記載した発明の一実施例を示すブロック図で、相当部分には図１と同一符号を付してその説明を省略する。図において、１８はバッテリー９をバックアップする補助バッテリーであり、１９はバッテリー９の電圧が低下した場合に補助バッテリー１８に切り換えるバッテリーバックアップ回路である。２０はメインスイッチ１０と連動して動作し、バッテリーバックアップ回路１９にて切り換えられたバッテリー９もしくは補助バッテリー１８からの電源を、基準発振器１１、分周回路１２およびフレームカウンタ１６に供給するバックアップ電源スイッチである。２１はこのバックアップ電源スイッチ２１を介して電源の供給を受け、当該無線電話機の動作状態を記憶・保持する補助メモリである。

【００１８】次に動作について説明する。ここで、基本的な動作は実施例１の場合と同様であるため、その説明は省略する。マイクロプロセッサ１５はその時々の当該無線電話機の動作状態を補助メモリ２１に送って記憶・保持させている。今、通話中にバッテリー９が消耗してその電圧が低下した場合、バッテリーバックアップ回路１９はバッテリー９より供給していた電源を補助バッテリー１８からのものに切り換える。これにより、基準発振器１１、分周回路１２およびフレームカウンタ１６は正常に動作を継続し、補助メモリ２１は当該無線電話機のその時の動作状態を保持し続ける。従って、ここで交換のためにバッテリー９をはずしても、通話は途切れるが呼が切断されることはなく、新しいバッテリー９を再度装着すれば、通話を再開することができる。

【００１９】実施例３．なお、上記実施例では、タイミング発生回路１３による送受信のタイミングの制御を、分周回路１２より出力されるフレームパルスに基づいて行う場合について説明したが、このフレームパルスとフレームカウンタ１６より読み込んだフレーム値とに基づいて行うようにしてもよい。図３は請求項３に記載したそのような発明の一実施例を示すブロック図であり、各部には図１の相当部分と同一の符号を付してその説明を

6

省略する。この図３に示した実施例は、フレームカウンタ１６からのフレーム値がタイミング発生回路１３に入力されている点で図１に示したものと異なっている。

【００２０】このように、フレームカウンタ１６の計数したフレーム値もタイミング発生回路１３に入力することにより、タイミング発生回路１３はフレームを自分自身で判断し、マイクロプロセッサ１５の介入を減らして送信機３、受信機４、送信系電源スイッチ７、および受信系電源スイッチ８を制御することが可能となる。そのため、マイクロプロセッサ１５の処理負荷を大幅に軽減することができる。

【００２１】

【発明の効果】以上のように、請求項１に記載の発明によれば、分周回路より出力されるフレーム信号を計数するフレームカウンタを設け、そのフレームカウンタより読み込んだフレーム値に基づいて、分周回路、フレームカウンタ、およびタイミング発生回路などの制御を行う制御回路に、分周回路からのフレーム信号でオン、制御回路自身からの制御信号でオフとなって、メインスイッチを経由したバッテリーからの電源の、当該制御回路への供給を制御する制御回路電源スイッチを付加するように構成したので、待ち受け受信時に制御回路への電源の供給を停止することが可能となって、消費電流の削減がはかれ、結果として待ち受け受信時間を長くすることのできる無線電話機が得られる効果がある。

【００２２】また、請求項２に記載の発明によれば、バッテリーバックアップ回路、バックアップ電源スイッチを経由して電源が供給される補助メモリに、当該無線電話機の動作状態を記憶・保持させるように構成したので、通話中にバッテリーの交換を行っても、呼が切断されることなく、バッテリーが装着されればそのまま通話を再開できる無線電話機が得られる効果がある。

【００２３】また、請求項３に記載の発明によれば、タイミング発生回路による送受信のタイミング制御を、分周回路より出力されるフレームパルスとフレームカウンタより読み込んだフレーム値とに基づいて行うように構成したので、制御回路の処理負荷を大幅に軽減することができる無線電話機が得られる効果がある。

【図面の簡単な説明】

【図１】この発明の実施例１による無線電話機を示すブロック図である。

【図２】この発明の実施例２による無線電話機を示すブロック図である。

【図３】この発明の実施例３による無線電話機を示すブロック図である。

【図４】従来の無線電話機を示すブロック図である。

【符号の説明】

９　バッテリー

１０　メインスイッチ

１１　基準発振器

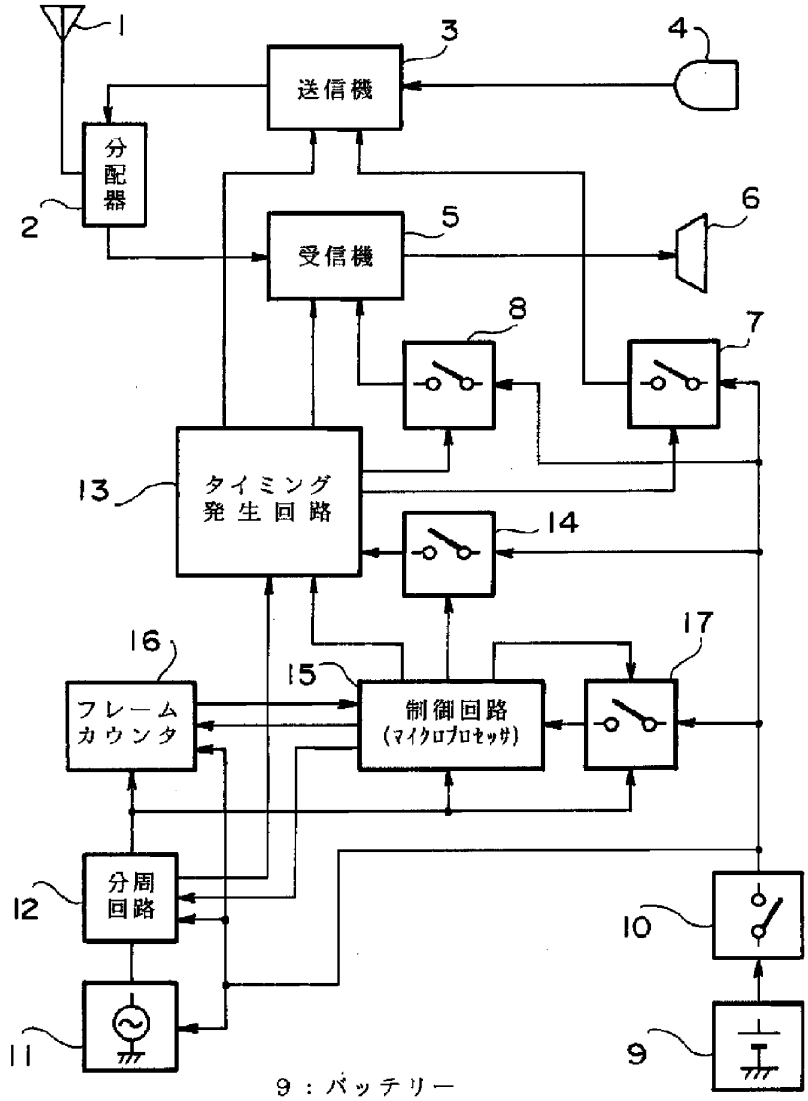
7

１２　分周回路
１３　タイミング発生回路
１５　制御回路（マイクロプロセッサ）
１６　フレームカウンタ
１７　制御回路電源スイッチ

8

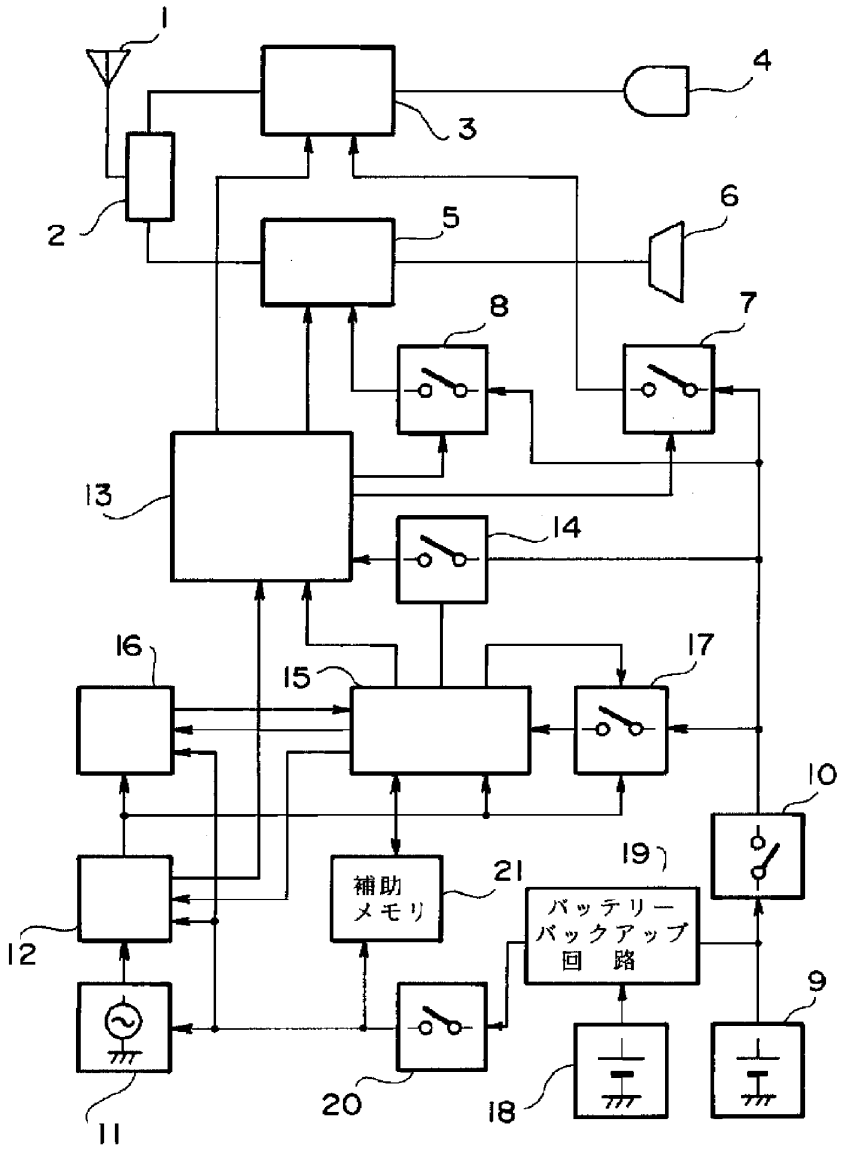
１８　補助バッテリー
１９　バッテリーバックアップ回路
２０　バックアップ電源スイッチ
２１　補助メモリ

【図１】



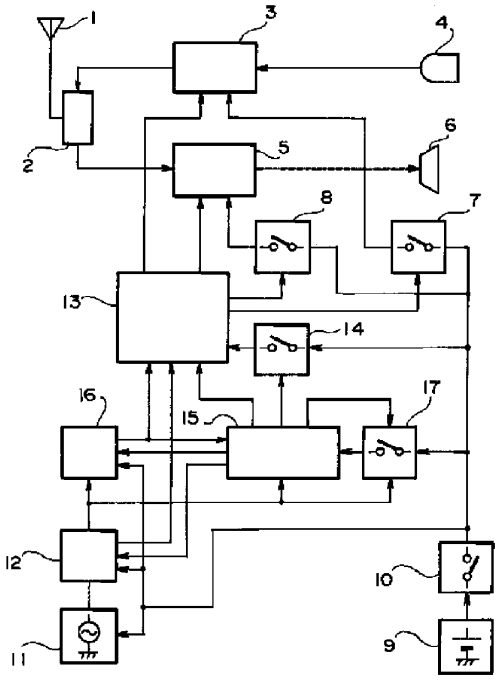
９：バッテリー
１０：メインスイッチ
１１：基準発振器
１７：制御回路電源スイッチ

【図2】

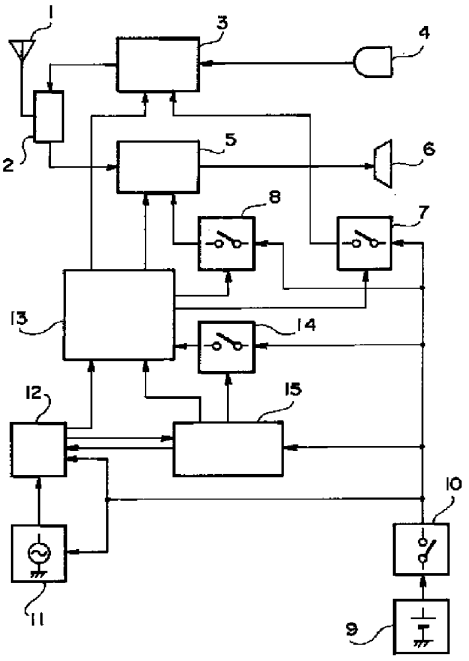


１８：補助バッテリー
２０：バックアップ電源スイッチ

【図3】



【図4】



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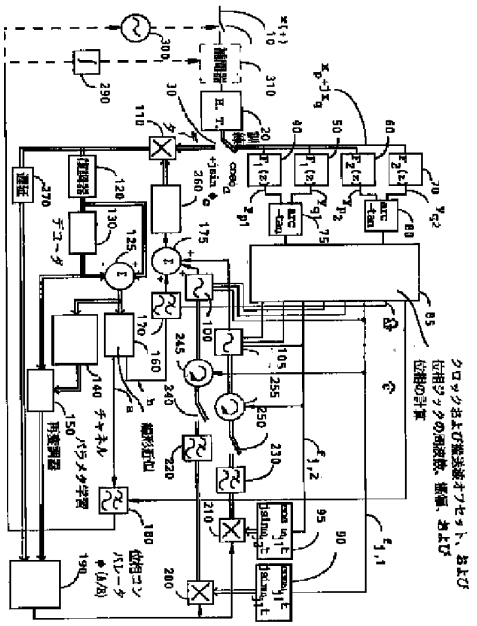
(54)【発明の名称】　多重搬送波モデムにおけるクロツク及び搬送波周波数オフセツト、及び位相ジツタの修正方法及び装置

(57)【要約】

【目的】　本発明の目的は、伝送媒体によって賦課された位相ジッタ及び周波数オフセットの障害、及び送信用及び受信用多重搬送波モデムの間のクロック周波数差の障害を修正する方法を提供することである。

【構成】　本方法は２つのモード、即ち複数のパイロットトーンを使用する訓練モードと、複数の搬送波上に変調されたランダムデータを使用するデータモードとからなる。訓練モード中に位相ジッタの周波数が推定され、修正信号のパラメタが初期化される。データモード中にこの修正信号を使用して障害を補償し、次いで位相誤差の推定から修正信号が更新される。受信した（単一搬送波ではなく）多重搬送波信号に伝送媒体内の不完全成分によって賦課されたクロック及び搬送波周波数オフセット、及び位相ジッタは、従来は種々の要因が介在するために修正困難乃至は不可能とされていたが、本発明はこれを解消する。



1

【特許請求の範囲】

【請求項１】　受信した多重搬送波信号に伝送媒体内の不完全成分によって賦課された位相ジッタを推定し、補償する方法であって、

（ａ）ある時間間隔中に受信した多重搬送波に、局部的に生成した修正信号（位相ジッタの効果を修正するために必要な位相シフトの推定）を乗じて修正済の受信した多重搬送波信号を発生する段階、

（ｂ）修正済多重搬送波信号を復調し、復号して伝送されたデータの推定を発生し、次いでこのデータを再変調することによって参照信号を発生する段階、

（ｃ）修正済多重搬送波信号の位相と参照信号の位相との差である位相誤差信号を計算する段階、

（ｄ）段階（ｂ）において計算された位相誤差信号を濾波して局部的に生成する修正信号のパラメタ（該修正信号の複数の成分の振幅、周波数、及び位相、もしくは同じ情報を含む何等かの等価集合）に必要な変化の推定を生成する段階、

（ｅ）段階（ｄ）のパラメタを前記変化によって更新し、修正信号の新しいパラメタを生成する段階、及び

（ｆ）爾後の各時間間隔中に段階（ａ）乃至（ｅ）を繰り返す段階

からなる方法。

【請求項２】　さらに、

（ｇ）受信した多重搬送波信号を、局部的に生成したクロック信号に同期してサンプルする段階、

（ｈ）段階（ｇ）において入手したサンプルをブロックにアセンブルする段階、

（ｉ）各ブロックの受信後に、段階（ｅ）の更新を遂行する段階、及び

（ｊ）受信した多重搬送波信号の爾後のブロック内のサンプルに、新しいパラ
メタによって定義される修正信号を乗ずる段階をも含む請求項１の方法。

【請求項３】　参照信号を、

（ｋ）修正済の受信した多重搬送波信号を復調し、復号して複数の各搬送波上にどのデータが変調されているかを推定する段階、

（ｌ）この復調及び復号の結果を濾波し、各搬送波周波数における伝送媒体の振幅及び修正済の位相レスポンスを推定する段階、

（ｍ）これらの振幅及び位相レスポンスを使用し、複数の搬送波を推定したデータで再変調し、位相ジッタを有していない理想的な受信した多重搬送波信号を参照信号として生成する段階、及び

（ｎ）修正済の受信した多重搬送波信号と、再変調された参照信号とを比較して位相誤差信号を生成する段階によって計算する請求項２の方法。

【請求項４】　修正信号は、位相ジッタが存在すると決定された幾つかの周波数（ジッタ周波数と呼ばれる）の

2

成分からなり、さらに、

（ｏ）位相誤差信号に、前記ジッタ周波数の複素正弦信号を相関させる段階、及び

（ｐ）前記相関の結果を用いて、幾つかの正弦波発生器（識別されたジッタ周波数の修正信号の成分を生成する）のパラメタに施すべき変化を定義する段階をも含む請求項３の方法。

【請求項５】　パラメタは、ルックアップテーブルのアドレス、及び修正信号の成分を生成するために該テーブルの出力信号に適用する乗数である請求項４の方法。

【請求項６】　受信した多重搬送波信号に伝送媒体内の不完全成分によって賦課された周波数オフセットを推定し、補償する方法であって、

（ａ）ある時間間隔中に受信した多重搬送波に、局部的に生成した修正信号（周波数オフセットの効果を修正するために必要な位相シフトの推定）を乗じて修正済の受信した多重搬送波信号を発生する段階、

（ｂ）修正済の受信した多重搬送波信号を復調し、復号して複数の各搬送波上にどのデータが変調されているかを推定する段階、

（ｃ）段階（ｂ）の結果を濾波して各搬送波周波数における伝送媒体の修正済の位相レスポンスを推定する段階、

（ｄ）媒体の修正済の位相レスポンスを周波数の線形関数に近似させる段階、及び

（ｅ）線形関数の周波数ゼロにおける接片が、修正信号の位相と受信した多重搬送波信号の全ての搬送波に共通の位相との差によってもたらされるものと解釈し、この周波数ゼロにおける接片を低域濾波及び積分し、そしてこの濾波の結果を使用して修正信号の低周波数成分を更新する段階からなる方法。

【請求項７】　複数の搬送波上に変調されたデータを伝送媒体を介して受信するモデムにおいて、局部的に生成したサンプリングクロックの周波数と遠隔送信モデム内のクロックの周波数との差を修正する方法であって、

（ａ）受信した多重搬送波信号を局部的に生成したクロック信号に同期してサンプルする段階、

（ｂ）補間パラメタに従ってこれらのサンプル間を補間し、局部的に生成したクロックの周波数で取られたサンプルを遠隔送信モデム内のクロックの周波数で補間したサンプルに変換する段階、

（ｃ）補間したサンプルを復調し、復号して複数の各搬送波上にどのデータが変調されているかを推定する段階、

（ｄ）復調及び復号の結果を濾波して各搬送波周波数における伝送媒体の位相レスポンスを推定する段階、

（ｅ）伝送媒体のこの位相レスポンスを周波数の線形関数に近似させる段階、

（ｆ）周波数の線形関数の勾配が送信機及び受信機のサンプリング周波数の差によってもたらされるものと解釈

3

する段階、及び
（ｇ）この勾配を低域濾波してその結果を前記補間パラメタとして使用する段階からなる方法。
【請求項８】　濾波された勾配をフェーズロックドループ（局部的に生成したクロックの周波数を調整して遠隔送信機のクロックに整合させる）の制御のために使用する請求項７の方法。
【請求項９】　位相ジッタ、周波数オフセット、及び局部的に生成したサンプリングクロックの周波数と遠隔送信モデム内のクロックの周波数との差によって害され得る多重搬送波データ信号を受信するモデムにおいて、前記害を修正するために局部的に生成する修正信号の初期パラメタを計算する方法であって、
（ａ）複数のパイロットトーンからなる訓練信号の受信中に修正信号のパラメタの初期値を計算する段階、
（ｂ）帯域通過フィルタによってパイロットトーンを分離して連続するサンプリング時にそれらの位相を計算する段階、
（ｃ）これらの位相を解析して時間の線形及び正弦関数を識別する段階、
（ｄ）時間の正弦関数の周波数、振幅、及び位相を推定する段階、
（ｅ）段階（ｄ）の推定を使用して正弦波発生器のパラメタを初期化する段階、
（ｆ）段階（ｃ）の線形関数の勾配を比較して周波数オフセット及びクロック周波数差の両者の推定を生成する段階、
（ｇ）周波数オフセットの推定を使用して修正信号のゼロ周波数成分を初期化する段階、
（ｈ）クロック周波数差の推定を使用して低域通過フィルタの状態を初期化する段階、及び
（ｉ）低域通過フィルタの出力信号を使用して補間器（局部的に生成したクロック信号に同期して取られたサンプル間を補間する）を制御し、遠隔送信モデム内のクロック周波数でのサンプルを生成する段階からなる方法。
【請求項１０】　低域通過フィルタの出力信号をフェーズロックドループ（局部的に生成するクロックの周波数及び位相を調整して遠隔送信モデムのクロックの周波数及び位相に整合させる）の制御のために使用する請求項９の方法。
【請求項１１】　受信信号のサンプルを、高速フーリエ変換（ＦＦＴ）及び逆ＦＦＴ（ＩＦＦＴ）アルゴリズムを使用するブロック内で処理する請求項１の方法。
【請求項１２】　受信信号のサンプルを、ＦＦＴ及びＩＦＦＴアルゴリズムを使用するブロック内で処理する請求項６の方法。
【請求項１３】　受信信号のサンプルを、ＦＦＴ及びＩＦＦＴアルゴリズムを使用するブロック内で処理する請求項７の方法。

4

【請求項１４】　受信信号のサンプルを、ＦＦＴ及びＩＦＦＴアルゴリズムを使用するブロック内で処理する請求項９の方法。
【請求項１５】　時間の正弦関数の周波数、振幅、及び位相を、複数のパイロットトーンの位相の集合にＦＦＴを遂行することによって推定する請求項９の方法。
【請求項１６】　受信した多重搬送波信号に伝送媒体内の不完全成分によって賦課された位相ジッタを推定し、補償する装置であって、ある時間間隔中に受信した多重搬送波に、局部的に生成した修正信号（位相ジッタの効果を修正するために必要な位相シフトの推定）を乗じて修正済の受信した多重搬送波信号を発生する装置、修正済多重搬送波信号を復調し、復号して伝送されたデータの推定を発生し、次いでこのデータを再変調することによって参照信号を形成する装置、修正済多重搬送波信号の位相と参照信号の位相との差である位相誤差信号を計算する装置、位相誤差信号を濾波して前記局部的に生成する修正信号のパラメタに必要な変化の推定を生成する装置、パラメタを前記変化によって更新して修正信号の新しいパラメタを生成する装置、及び爾後の各時間間隔中に乗算、計算、濾波、及び更新の動作を繰り返させる装置を具備する装置。
【請求項１７】　受信した多重搬送波信号を局部的に生成したクロック信号に同期してサンプルする装置、サンプリング装置のサンプルをブロックにアセンブルするバッファ装置、各ブロックを受信した後にパラメタの更新を遂行する装置、及び受信した多重搬送波信号の爾後のブロック内のサンプルに、新しいパラメタによって定義される修正信号を乗ずる装置をも含む請求項１の方法。
【請求項１８】　修正済の受信した多重搬送波信号を復調し、復号して複数の各搬送波上にどのデータが変調されているかを推定することによって修正信号を計算する装置、この復調及び復号手段からの結果を濾波して各搬送波周波数における伝送媒体の振幅及び修正済の位相レスポンスを推定する装置、これらの振幅及び位相レスポンスを使用して複数の搬送波を推定したデータで再変調し、位相ジッタを有していない理想的な受信した多重搬送波信号を参照信号として生成する装置、及び修正済の受信した多重搬送波信号と再変調された参照信号とを比較して位相誤差信号を生成する装置をも含む請求項１７の装置。
【請求項１９】　修正信号が重大な位相ジッタが存在すると決定された幾つかの周波数（ジッタ周波数と呼ばれる）の成分を含む状況に適合する請求項１８の装置であって、位相誤差信号に前記ジッタ周波数の複素正弦信号を相関させる装置、各ジッタ周波数において定義された振幅及び位相の余弦波及び正弦波のサンプルを生成する装置、相関動作の結果を使用して振幅及び位相に施すべき変化を定義する装置、及び余弦波及び正弦波のサンプルを加算して修正信号を生成する装置をも含む請求項１

5

８の装置。

【請求項２０】　余弦波発生器及び正弦波発生器はルックアップテーブル及び乗算器によって実現され、これらのルックアップテーブルは必要な周波数及び位相を有する修正信号の成分を生成し、乗算器はこれらの成分の振幅を調整する請求項１９の装置。

【請求項２１】　受信した多重搬送波信号に伝送媒体内の不完全成分によって賦課された周波数オフセットを推定し、補償する装置であって、ある時間間隔中に受信した多重搬送波に、局部的に生成した修正信号（周波数オフセットの効果を修正するために必要な位相シフトの推定）を乗じて修正済の受信した多重搬送波信号を発生する装置、修正済の受信した多重搬送波信号を復調し、復号して複数の各搬送波上にどのデータが変調されているかを推定する装置、　復調及び復号手段からの結果を濾波して各搬送波周波数における伝送媒体の修正済の位相レスポンスを推定する装置、伝送媒体の位相レスポンスを周波数の線形関数に近似させ、修正する装置、及び線形関数の周波数ゼロにおける接片が修正信号の位相と受信した多重搬送波信号の全ての搬送波に共通の位相との差によってもたらされるものと解釈し、この周波数ゼロにおける接片を低域濾波し、そしてこの濾波の結果を使用して修正信号のゼロ周波数成分を更新する装置を具備する装置。

【請求項２２】　複数の分離した搬送波上に変調されたデータを伝送媒体を介して受信するモデムにおいて、局部的に生成したサンプリングクロックの周波数と遠隔送信モデム内のクロックの周波数との差を修正する装置であって、受信した多重搬送波信号を局部的に生成したクロック信号に同期してサンプルする装置、補間パラメタに従ってサンプリング手段から得られたサンプル間を補間し、局部的に生成したクロックの周波数で取られたサンプルを遠隔送信モデム内のクロックの周波数で補間したサンプルに変換する装置、補間したサンプルを復調し、復号して複数の各搬送波上にどのデータが変調されているかを推定する装置、復調及び復号手段の結果を濾波して各搬送波周波数における伝送媒体の位相レスポンスを推定する装置、伝送媒体のこの位相レスポンスを周波数の線形関数に近似させる装置、周波数の線形関数の勾配が送信機及び受信機のサンプリング周波数の差によってもたらされるものと解釈する装置、及びこの勾配を低域濾波してその結果を前記補間パラメタとして使用する装置を具備する装置。

【請求項２３】　複数の分離した搬送波上に変調されたデータを伝送媒体を介して受信するモデムにおいて、局部的に生成したサンプリングクロックの周波数と遠隔送信モデム内のクロックの周波数との差を修正する装置であって、受信した多重搬送波信号を局部的に生成したクロック信号に同期してサンプルする装置、局部的に生成するクロック信号の位相を制御してそれを遠隔送信モデム内のクロックと同期させる装置、サンプルを復調し、復号して複数の各搬送波上にどのデータが変調されているかを推定する装置、復調及び復号手段の結果を濾波して各搬送波周波数における伝送媒体の位相レスポンスを推定する装置、伝送媒体のこの位相レスポンスを周波数の線形関数に近似させる装置、周波数の線形関数の勾配が送信機及び受信機のサンプリング周波数の差によってもたらされるものと解釈する装置びこの勾配を低域濾波してその結果を局部的に生成するクロック信号の位相の制御のために使用する装置　　を具備する装置。

【請求項２４】　位相ジッタ、及び局部的に生成したサンプリングクロックの周波数と遠隔送信モデム内のクロックの周波数の周波数オフセット及び差によって害され得る多重搬送波データ信号を受信するモデムにおいて、前記害を修正するために局部的に生成する修正信号の初期パラメタを計算する装置であって、複数のパイロットトーンからなる訓練信号の受信中に修正信号のパラメタの初期値を計算する装置、帯域通過フィルタによってパイロットトーンを分離して連続するサンプリング時にそれらの位相を計算する装置、これらの位相を解析して時間の線形及び正弦関数を識別する装置、時間の正弦関数の周波数、振幅及び位相を推定する装置、推定手段が発生した推定を使用して正弦波発生器のパラメタを初期化する装置、解析手段が計算した線形関数の勾配を比較して周波数オフセット及びクロック周波数差の両者の推定を生成する装置、周波数オフセットの推定を使用して修正信号のゼロ周波数成分を初期化する装置、クロック周波数差の推定を使用して低域通過フィルタの状態を初期化する装置、及び低域通過フィルタの出力信号を使用して補間器（局部的に生成したクロック信号に同期して取られたサンプルの間を補間する）を制御し、遠隔送信モデム内のクロックの周波数でのサンプルを生成する装置を具備する装置。

【請求項２５】　低域通過フィルタの出力信号をフェーズロックドループ（局部的に生成するクロックの周波数及び位相を調整して遠隔送信モデムのクロックの周波数及び位相に整合させる）の制御のために使用する請求項２４の装置。

【請求項２６】　受信した多重搬送波信号のサンプルを、高速フーリエ変換（ＦＦＴ）及び逆ＦＦＴ（ＩＦＦＴ）アルゴリズムを使用するブロック内で処理する請求項１６の装置。

【請求項２７】　受信した多重搬送波信号のサンプルを、ＦＦＴ及びＩＦＦＴアルゴリズムを使用するブロック内で処理する請求項２１の装置。

【請求項２８】　受信した多重搬送波信号のサンプルを、ＦＦＴ及びＩＦＦＴアルゴリズムを使用するブロック内で処理する請求項２２の装置。

【請求項２９】　受信した多重搬送波信号のサンプル

を、ＦＦＴ及びＩＦＦＴアルゴリズムを使用するブロック内で処理する請求項２４の装置。使用する装置

【請求項３０】　位相ジッタの成分の周波数を複数のパイロットトーンの位相の集合にＦＦＴを遂行することによって推定する請求項１５の装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、一般的にはデータ送信及び受信に関し、特定的には複数の搬送波を変調するために使用された高速データの受信に関する。この変調方法は、直交的に多重化された直角振幅変調（ＯＭＱＡＭ）、動的に割り当てられた多重ＱＡＭ（ＤＡＭＱＡＭ），直交周波数分割多重化（ＯＦＤＭ）等多くの名前で呼ばれているが、ここでは多重搬送波変調と呼ぶ。

【０００２】

【従来の技術】一般的に、データ通信リンクの送信及び受信モデム内の発信器（周波数源）は同期することができず、受信モデムはそれ自身をデータレート及び受信した信号の（１または複数の）搬送波周波数に順応させる特別な回路または信号処理アルゴリズムを使用しなければならない。このタスクはクロック及び搬送波回復と呼ばれることが多い。

【０００３】このタスクは、若干の伝送媒体（最も顕著には、一般的なスイッチ型電話回路網（ＧＳＴＮ））に、図１に示すように周波数オフセット及び位相ジッタが導入されることによって複雑になる。ここではｆで表している周波数オフセットは、（１または複数の）搬送波の（１または複数の）周波数とローカル受信機内で生成する（１または複数の）参照搬送波の周波数との差である。この差は（ａ）送信機が使用している（１または複数の）搬送波と、受信機内の（１または複数の）参照搬送波との周波数差、及び（ｂ）回路網内の周波数分割多重化（ＦＤＭ）装置における変調搬送波及び復調搬送波の周波数間の不一致、の両方または何れか一方によってもたらされ得る。ＧＳＴＮでは混合されたオフセットは結果的に５Ｈｚにもなり得る。位相ジッタは受信した信号の位相変調と考えられ、幾つかの離散した識別可能な周波数成分を有していることが多い。電源周波数及び電話の呼鈴周波数（合衆国においてはそれぞれ60Ｈｚ及び20Ｈｚ）が一般的な成分である。搬送波回復回路またはアルゴリズムは、受信した信号に及ぼすそれらの効果を改善するために周波数オフセット及び位相ジッタを追跡しなければならない。　データ変調された単一の搬送波信号からクロック及び搬送波を回復（周波数オフセット及び位相ジッタの追跡を含む）する回路及びアルゴリズムは周知である（例えば、1988年、ジョン・ウイリー刊 J. A.C. ビンガム著「モデム設計の理論と実際」を参照されたい）。従来技術の殆ど全ては１つの形状の、または別の形状のフェーズロックドループ（ＰＬＬ）を使用しており、設計者は長い間これらのループの内部遅延の有

害な効果を認識してきた。搬送波回復の場合には、もし適応等化器の遅延（典型的には約 10 ms）がループ内に含まれていれば、位相ジッタの追跡は極めて困難であり、多分不可能でさえあると理解されてきた。従って、ループからこの遅延を除去するための特別なアルゴリズムが開発されている（例えば 1976 年３月の Bell Syst.Tech.J.の第 55 巻 317-334頁に所載の D.D. ファルコナーの論文「２次元通信システムにおける遅帯的適応等化及び搬送波回復」を参照されたい）。

【０００４】多重搬送波変調においては、データはビットのブロックにグループ化される。バラン（合衆国特許 4,438,511号）及びヒューズ・ハートグス（合衆国特許 4,679,227号）のシステムではブロックは 1000 ビット以上からなることができる。各搬送波はこれらのビットの僅か数ビットによって変調され、変調は１ブロックの持続時間の間一定に保たれる。従ってこの持続時間即ち記号周期は単一搬送波モデムの記号周期の数百倍になり得る。さらに、この記号周期は追跡すべき位相ジッタの成分の周期より遥かに大きくなり得る。

【０００５】多重搬送波受信機における信号処理は記号レートで遂行しなければならず、また受信した信号に関する情報（その中に含まれているデータ及びその不完全性＜周波数オフセット、位相ジッタ等＞）は各ブロックが記号レートで遂行された後でなければ使用できず、受信した信号に関する情報（その中に含まれているデータ及びその不完全性＜周波数オフセット、位相ジッタ等＞）は各ブロックが処理された後でなければ使用できない。それ故、130 msにも及ぶ（殆どの適応等化器を通る遅延の10倍以上）この１記号周期の遅延は搬送波回復ループ内部に現れ、普通のジッタ追跡を不可能ならしめる。

【０００６】多重搬送波変調に伴う長い記号周期は、多重搬送波信号に賦課された位相ジッタの追跡を、単一搬送波信号の場合よりも遥かに困難な問題にする。１つの提案（1985年８月のIEEE Intl.Conf.Commun.Rec.の 661-665頁に所載の B. ヒロサキらの論文「直交的に多重化されたＱＡＭ技術に基づく19.2 kビット／秒音声帯データモデム」）では、非変調パイロットトーンを一組の（各搬送波に１つずつ）適応ジッタ予測器へ入力し、出力信号を各変調された搬送波上のジッタを打ち消すように導いている。この方策は幾つかの欠点を有している。使用可能周波数帯の縁に配置された１つのパイロットから入手できるジッタに関する情報量は極めて少なく、タップ付き遅延線型の予測器は単一のトーンを濾波するには余り適しておらず、そしてこの方法は（特に多数の搬送波を使用している場合には）大量の計算を必要とする。

【０００７】別の問題は、ジッタ周波数が予め分かっているとは限らないこと（電源周波数及び呼鈴周波数は国によって異なる）、及び他の源が重大な成分を生成し得

9

ることである。周波数を識別する方法は種々発表されているが（例えば、1981年、スタンフォード大学の R.O. シュミットの理学博士学位論文「多重エミッタ位置及びスペクトル推定への信号サブスペースアプローチ」に記載のＭＵＳＩＣアルゴリズム、及び 1986 年 10 月のIEEETrans. ASSP 第 ASSP-34巻 1340-1342頁の R. ロイ、A.パウルラジ、及び T. カイラスの論文「ＥＳＰＲＩＴ－雑音内のシッソイドのパラメタの推定へのサブスペース回転アプローチ」に記載のＥＳＰＲＩＴアルゴリズム）、それらは全て極めて大量の計算を必要とし、また位相ジッタの周波数を決定する特定の問題には言及していない。

【０００８】多重搬送波変調に対する初期の反対理由の多くは、周波数の諸問題が満足の行くように解決されなかったこと、及び多分解決できなかったことから、位相ジッタの修正は不可能であるとの仮定に基づいていた。

【０００９】

【発明の概要】本発明の好ましい実施例においては、搬送波回復ループの内部で発生する記号遅延の問題を、多重搬送波信号の効率的な検出及び復号に必要なブロック処理の概念と、オフセット及びジッタに対する必要補償を有する局部修正信号を生成するのに必要な直列処理の概念とを組み合わせることによって解決している。本発明では、これは、直列モード及びブロックモードの組み合わせにフィードバック（閉ループとしても知られている）アルゴリズムまたは回路を使用することによって行う。

【００１０】しかし、これらのフィードバックアルゴリズムは、主としてデータ変調された信号を受信しながら連続動作するように設計されており、それらの適応はかなり遅く、また追跡すべき位相ジッタ成分の周波数が分っていることを前提としている。

【００１１】それ故、データを伝送するためにチャネルを接続する時にはデータ信号の前に、幾つかのパイロットトーンからなる訓練信号を先行させる。受信機においては、これらのトーンを濾波によって分離し、それらの位相を時間の関数として計算し、これらの関数を解析して（ａ）クロックオフセット、（ｂ）搬送波オフセット、及び（ｃ）位相ジッタの全ての重要成分の振幅、周波数、及び位相の初期推定を形成する。

【００１２】次に、これらの推定を使用して、位相修正信号を生成する回路またはアルゴリズムを初期化する。この位相修正信号はデータ変調された信号の受信中に以下のように使用される。

【００１３】１．直列モードにおいては、受信した信号のサンプルに、この位相修正信号（ジッタ及びオフセット周波数における成分からなる）を乗じて修正済信号のサンプルを発生する。

【００１４】２．次に、これらの修正済サンプルのブロックを復調し、復号して（例えば、合衆国特許4,679,227 号に記載されているようにして）推定済の受信したデータのブロックを発生する。これらのデータを、復調された（しかし復号されていない）サンプルと共に使用してチャネルの振幅及び位相特性の推定を更新する他に、後述の段階５で説明する搬送波及びクロックオフセットを推定するためのアルゴリズムまたは回路への入力として使用する。

【００１５】３．次いで受信したデータを再変調して参照信号のサンプルのシーケンスを発生し、直列モードではこれらのサンプルの位相と修正済サンプルの位相とを比較して位相誤差のサンプルのシーケンスを生成する。

【００１６】４．次にこれらの位相誤差のサンプルを解析し、位相修正信号を生成するために使用するアルゴリズムまたは回路のパラメタに対する必要更新を計算する。

【００１７】５．復調され、復号されたデータ間の差を解析し、濾波して残留搬送波オフセット及びクロック周波数オフセットの推定を形成する。搬送波オフセットの推定を使用して回路またはアルゴリズムの（位相修正信号を生成する）パラメタを更新し、また同様にクロックオフセットの推定を使用して受信した信号の最初のサンプリング時、またはこれらのサンプルを操作する補間器の何れかを制御する。

【００１８】６．このようにして更新された位相修正信号及びサンプリング時を使用してデータ信号の次のブロックを受信し、データ信号の爾後の各ブロック毎に上述の段階１乃至５を繰り返す。

【００１９】

【実施例】図１に示すようなデータ伝送リンクの送信機及び受信機は、それぞれ発振器（通常は水晶制御型）を含む。発振器は、送信及び受信信号をサンプルする周波数、これらの信号のデータレート、及び変調に使用する搬送波の周波数を制御する。

【００２０】受信機は、そのサンプリングレートを送信機のサンプリングレートにロックするために回路または信号処理アルゴリズムを使用する。クロックオフセット ε は、受信機内の自然（即ちロックされていない）サンプリングレート f_r と送信機内で使用されているサンプリングレート f_t との比によって定義され、以下の数１によって表される。

【００２１】

【数１】

$$f_{r,t} = (1+\varepsilon)\, f_t$$

回路及びアルゴリズムは復調に使用する搬送波の周波数を受信した信号に固有の周波数にロックするためにも使用される。（ａ）送信機の発振器の周波数と受信機の発振器の周波数との差、及び（ｂ）変調器内の発振器の周波数（f_t）とＦＤＭ装置の復調器内の発振器の周波数（f_r）との差の組み合わせによってもたらされ得る受信した搬送波と受信機内のロックされていない自然周

11

波数との共通周波数差（オフセット）をΔｆと定義する。

【００２２】ＦＤＭ装置内の発振器は位相ジッタを受けやすい。これらの源は典型的には相加的であり、それらの和は図１に示すように変調及び復調の両方または何れか一方のための搬送波の位相に影響する。説明の簡略化のために、２つの周波数f_1及びf_2のみに重大な位相シフトが存在し、これらのジッタ成分が振幅A_1及びA_2と、位相θ_1及びθ_2とを有するものとする。周波数ｆにおいて受信した信号の各成分は、ジッタが無い場合には：$\sin[\omega t+\theta]$で、またジッタが有る場合には：$\sin[\omega t+\theta+A_1\sin(\omega_1 t+\theta_1)+A_2\sin(\omega_2 t+\theta_2)]$で表すことができる。但し、（信号及びジッタの）全ての周波数に対して$\omega=2\pi f$である。

【００２３】図２に示すように、このようにして変造された実受信済信号x(t)は先ずスイッチ１０によってレートｆ　（＝1/T）で、及びあるタイミングオフセットτをもってサンプルされヒルバート変換器２０（例えば1974年２月のBell Syst.Tech.J. の第53巻363-390 頁に所載のL.R.ラバイナー及びR.W.シェイファーの論文「最小最大ディジタルヒルバート変換器の挙動に関して」を参照されたい）によって複素信号 x（nT +τ）+ j x（nT *

12

* +τ）に変換される。データチャネルを最初に接続する際には訓練アルゴリズムが使用される。これは図２に“訓練”位置にあるスイッチ３０によって記号的に表してある。

【００２４】「訓練モード」図１の送信機からの訓練信号は、周波数f_1及びf_2（第１の実施例では 1000Hz 及び 2000Hz ）の２つのパイロットトーンからなる。この訓練信号はスイッチ１０によってサンプルされ、ヒルバート変換器２０によって変換され、そして以下のように処理される。

【００２５】１．これらのトーンの実数部分及び虚数部分（同相成分及び直交成分としても知られる）を帯域通過フィルタ４０－７０によって分離し、サンプルされた信号$y_1(n)$,$y_1(n)$,$y_2(n)$, 及び$y_2(n)$を生成する。理想的にはこれらの各フィルタのレスポンスは、１つのパイロットトーンにおいて最大となり、他のパイロットトーンにおいてはゼロとなるようにすべきである。典型的な伝達関数（変換変数ｚに関して）は、下記の数２ａ及び数２ｂのようである。

【００２６】

【数２ａ】

$$F_1(z)=Y_{p1}(z)/X_p(z)=Y_{q1}(z)/X_q(z)=(z^2-2r\cos\theta_2 z+1)/(z^2-2r\cos\theta_1 z+r^2)$$

【００２７】

【数２ｂ】

$$F_2(z)=Y_{p2}(z)/X_p(z)=Y_{q2}(z)/X_q(z)=(z^2-2r\cos\theta_1 z+1)/(z^2-2r\cos\theta_2 z+r^2)$$

但し、ｉ＝１、２に対して、$\theta = 2\pi f/f$

２．４つのフィルタの出力信号は逆正接演算器７５及び８０に印加され、２つの分離されたトーンから時刻 t＝nT ＋τに取られた各サンプル対の位相が，下記の数３に従って計算される。

【００２８】

【数３】

$$\phi_1(n)=\tan^{-1}\{y_{q1}(n)/y_{p1}(n)\}$$

複数の（好ましくは２の整数乗であって、好ましい実施例では 1024 に等しい）サンプルの位相が順次に計算され、記憶される。次でこれらは段階３－５で説明するように、プロセッサ８５においてブロックとして処理される。

【００２９】３．各位相　ϕ (n)及び$\phi_2(n)$は、周知の最小平均自乗誤差（ＬＭＳＥ）法（例えば 1985 年、プレンティスホール刊、B.ウィドロウ及び S.D. スターンズ著「適応信号処理」を参照されたい）を使用して、即ち下記の数４によって時間の線形関数（変数ｎによるＴの増分で測定）に近似される。

【００３０】

【数４】

$$\phi_1(n)\fallingdotseq\alpha_{1n}+p_1 \quad (1=1,\ 2\text{に対して})$$

ここに、α_1 、p_1 、α_2 及びp_2 は、各位相の勾配及びゼロ時の接片のＬＭＳ推定である。位相ϕ_1 及びϕ_2の例、及びそれらへの最良線形近似を図３に示す。図３には、明瞭化のために、１つのジッタ成分しか示してない。

【００３１】４．次に、搬送波及びクロック周波数オフセットΔｆ及びεが、以下の数５ａ及び数５ｂによって、勾配α_1 及びα_2 から推定される。

【００３２】

【数５ａ】

$$\Delta f=(\alpha_1 f_2-\alpha_2 f_1)/(\alpha_2-\alpha_1)$$

【００３３】

【数５ｂ】

$$1+\varepsilon=2\pi(f_2-f_1)/f_s(\alpha_2-\alpha_1)$$

５．次に、位相関数の残留非線形部分に対するスペクトル解析（第１の実施例では高速フーリエ変換＜ＦＦＴ＞を使用）$\phi'(n)=\phi(n)-\alpha n-p$ （ｉ＝１，２に対して）　を遂行し、位相ジッタの成分の振幅Ａ　、周波数ｆ　、及び位相θ　（図示の２成分の場合、ｋ＝１、２）を推定する。

【００３４】６．２つのパイロットトーンの幾つかの（第１の実施例では１つだけ）ブロックが送信、受信、及び処理された後、Ａ　、ｆ　、及びθ　の推定値を使用して正弦波発生器１００及び１０５の係数及び初期状

13

態を計算する。これで訓練モードが完了する。

【００３５】スイッチ３０をデータ位置に戻し、多重搬送波上に変調されたデータを受信して処理を続行する。

【００３６】「データモード」

＜搬送波回復＞

１．搬送波周波数オフセット及び位相ジッタによって害されていると考えられるデータ変調された多重搬送波信号 x(t) のヒルバート変換されたサンプルは順次に乗算器１１０に印加され、ルックアップテーブル２６０から生成した修正信号のサンプル $\cos\phi + j \sin\phi$ が乗ぜられる。

【００３７】乗算器１１０の出力信号（修正済サンプル）はブロックにアセンブルされ、遅延要素２７０内に記憶され、また以下のように処理される。

【００３８】２．乗算器１１０からの出力信号のブロックは復調器１２０への入力であり、1974年プレンティスホール刊、E.O.ブリガム著「FFT 及びその応用」（FFT の一般理論）及び D. ヒューズ・ハートグスの合衆国特許 4,679,227号（FFT の多重搬送波変調への応用）に示されているように、復調器１２０において修正済信号のサンプルのブロックにＦＦＴが遂行される。復調器１２０の出力はデコーダ１３０に印加され（これも上記合衆国特許4,679,227 号に記載されているように）伝送されたデータが推定される。

【００３９】３．復調器１２０及びデコーダ１３０から＊の出力信号は減算器１２５に印加される。復調され、復号された信号間の振幅及び位相の差である減算器１２５の出力信号は、プロセッサ１４０に印加され（上記合衆国特許 4,679,227号に記載されているように）サブルーチンがチャネルの特性を推定する。

14

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$$\phi_e(n) = \tan^{-1}[\{x_q(n)y_p(n) - x_p(n)y_q(n)\} / \{x_p(n)y_p(n) + x_q(n)y_q(n)\}]$$

しかし、訓練位相中にループは初期化されているから、修正済信号と参照信号との間の差は小さく、数６の逆正接関数はその独立変数によって近似させることができる。さらに、逆正接関数の独立変数内の除算は省略できることが分っており、下記の位相誤差の簡易インディケータを使用することができる。

【００４４】

【数７】

$$\phi_e(n) \fallingdotseq x_q(n)y_p(n) - x_p(n)y_q(n)$$

これは乗算器２００及び２１０に印加される。

【００４５】７．乗算器２００及び２１０において、位相誤差信号のサンプルϕ　に、ルックアップテーブル９０及び９５によって生成された識別済ジッタ周波数の余弦波及び正弦波のサンプル（即ち複素サンプル）が乗ぜられる。これらの乗算の複素積は低域通過フィルタ２２０及び２３０にそれぞれ印加される。フィルタ２２０及び２３０は典型的には下記の数８の形状の伝達関数と、ゼロの利得とを有し、ポール（K z_1及びz_2）はループの過渡レスポンスを最適化するように（1979年、ジョン・ウィリー刊、F.M.ガードナー著「フェーズロック技術」に示されているように）普通のＰＬＬ理論にしたがって選択される。

【００４６】

【００４０】４．データの各ブロックを受信した後に更新されるプロセッサ１４０のサブルーチンからの推定は、デコーダ１３０からの伝送されたデータの推定と共に再変調器１５０に印加されて逆ＦＦＴが遂行され、参照信号Ｂが生成される。

【００４１】５．減算器１２５からの位相差はプロセッサ１６０にも印加され、線形近似サブルーチンは図５に示すように周波数の線形関数 af + b への位相のＬＭＳＥ近似を計算する。定数項 bは合成した修正信号の位相の誤差を特徴付けるものであり、b を表す信号は低域通過フィルタ１７０に印加される。

【００４２】６．次いで、位相コンパレータ１９０は、遅延要素２７０内に記憶している修正済信号Ａと、再変調器１５０からの参照信号Ｂとの間の位相差である位相誤差信号のサンプルを順次に計算する。もし２つの信号を、それぞれ{x（n）+ j x（n)}及び{ y（n）+ j y（n)}で表せば、この位相差は下記の数６によって正確に与えられる。

【００４３】

【数６】

$$\phi_e(n) = \tan^{-1}[\{x_q(n)y_p(n) - x_p(n)y_q(n)\} / \{x_p(n)y_p(n) + x_q(n)y_q(n)\}]$$

【数８】

$$P(z) = K(z-z_1) / (z-1)(z-z_2)$$

乗算及び低域濾波動作は協働して、位相誤差信号を各複素ジッタ成分に相関させる。

【００４７】８．上記段階６及び７は１ブロックの持続時間の間遂行され次いでフィルタ２２０及び２３０の出力信号はそれぞれスイッチ２４０及び２５０によってサンプルされて修正信号の位相誤差の各成分の推定を発生する。しかし、１ブロック中に計算されるこれらの誤差成分は、爾後のブロックのために使用される修正信号のパラメタを更新するために使用される。ブロック周期は必ずしも何れかのジッタ成分の周期の整数倍である必要はないから、各成分は回転器２４５及び２５５において角ω　T（＝2 πf　T）（これは各識別済ジッタ成分が１ブロック周期内に回転する角度である）だけ移動させなければならない。サンプルされ、回転された誤差成分は正弦波発生器１００及び１０５のパラメタを更新するために使用され、これらは次のブロック中に乱されることなく継続する。

【００４８】正弦波発生器１００及び１０５は幾つかの異なる方式で実現でき、それらを更新する好ましい方法はこの実現の態様に依存する。図４に示す好ましい実施例では誤差成分の実数部分ε　及び虚数部分びε　は振

15

幅及び位相誤差 ε_A 及び $\varepsilon\phi$ に変換され、これらの誤差は

$$A_{jk}' = A_{jk} + \delta\varepsilon_A k \text{、及び}$$
$$\phi_{jk}' = \phi_{jk} + \delta\varepsilon\phi k$$

に従って修正信号の各成分の振幅 A 及び位相 ϕ を増分させるために使用される。但し、δ は小さい階段状の大きさの乗数である。この更新された位相 ϕ は余弦波及び正弦波ルックアップテーブルのためのアドレスとして使用され、２つの出力信号には更新された振幅が乗ぜられる。

【００４９】９．正弦波発生器１００及び１０５、及びフィルタ１７０の実出力信号は加算器１７５に印加されて複合修正位相角

$$\phi_c = 2\pi\Delta f nT_r + \sum_{k=1}^{2} A_k \cos(2\pi f_k nT_r + \theta_k)$$

が形成される。これはオフセット及びジッタを補償するために必要な位相シフトの推定である。この ϕ は、複素修正信号のサンプルを生成するために正弦及び余弦ルックアップテーブル２６０に印加される。

【００５０】＜データモード＞

線形近似アルゴリズム１６０（搬送波回復の５項で説明済）によって計算された勾配項はサンプリング位相 τ の誤差を特徴付けるものであり、低域通過フィルタ１８０に印加される。このフィルタの典型的な伝達関数は、z 変数に関して、

$$F(z) = K(z - z_1) / (z - z_2)$$

であり、ポール z_1 及びポール z_2 は過渡レスポンスと雑音帯域との間で妥協を得るように標準ＰＬＬ理論に従って選択することができる。

【００５１】このフィルタの出力信号は下記の２つの方法の一方に使用することができる。（図２に破線によって示す）。

【００５２】（ａ）この信号を電圧制御発振器（ＶＣＯ）３００へフィードバックして最初のサンプリングスイッチ１０を制御するために使用する。もしくは

（ｂ）スイッチ１０は非調整（開ループ）発振器によって制御し、積分器２９０において積分したフィルタの出力は補間器３１０を制御するために使用する（例えば1973年６月のProc., IEEEに所載のR.W.シェイファー及びL.R.ラバイナーの論文「補間へのディジタル信号処理アプローチ」を参照されたい）。

16

【００５３】当業者ならば、本発明をその思想及び本質的な特性から逸脱することなく他の特定形状で実施できるであろう。従って、以上の説明は例示に過ぎず、本発明の範囲を限定するものではないことを理解されたい。

【図面の簡単な説明】

【図１】クロック及び搬送波周波数オフセット、及び搬送波位相ジッタを受けたデータ伝送リンクの概要ブロック図であり、

【図２】本発明の実施例の総合ブロック線図であって、フィードフォワード訓練モード及びフィードバックデータモードを示し、

【図３】１つのジッタ成分のみが存在する場合の２つのパイロットトーンの典型的な位相／周波数プロットであり、

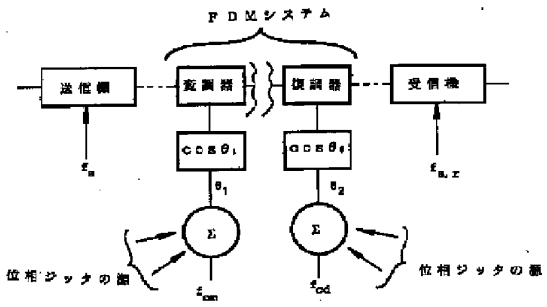
【図４】位相修正信号の正弦波成分を発生する発生器の一方をルックアップテーブルで実現した例を、振幅及び位相を更新する装置と共に示し、

【図５】多数の搬送波の典型的な位相／周波数プロットである。

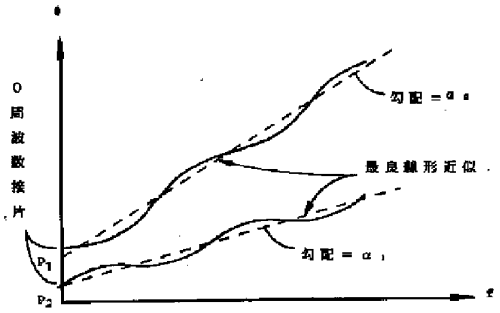
【符号の簡単な説明】

１０、３０、２４０、２５０　スイッチ
２０　ヒルバート変換器
４０、５０、６０、７０　帯域通過フィルタ
７５、８０　逆正接演算器
８５、１４０、１６０　プロセッサ
９０、９５、２６０　ルックアップテーブル
１００、１０５　正弦波発生器
１１０、２００、２１０　乗算器
１２０　復調器
１２５　減算器
１３０　デコーダ
１５０　再変調器
１７０、１８０、２２０、２３０　低域通過フィルタ
１９０　位相コンパレータ
２４５、２５５　回転器
２７０　遅延要素
２９０　積分器
３００　電圧制御発振器
３１０　補間器

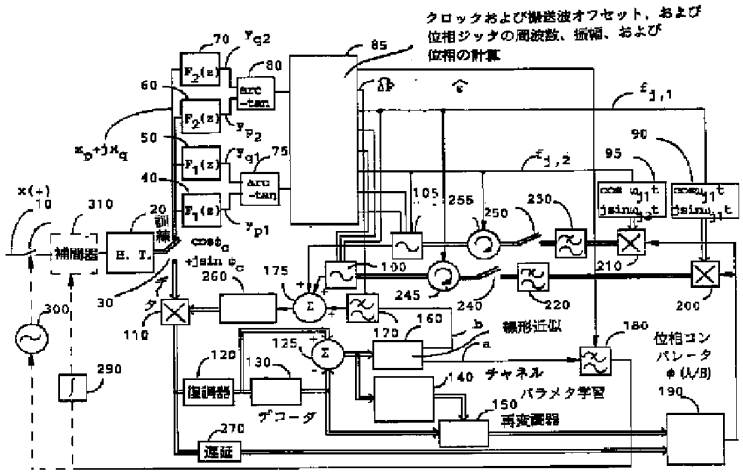
【図１】



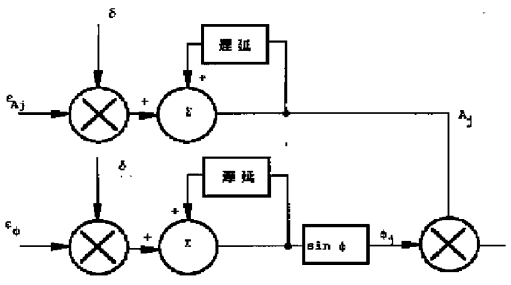
【図３】



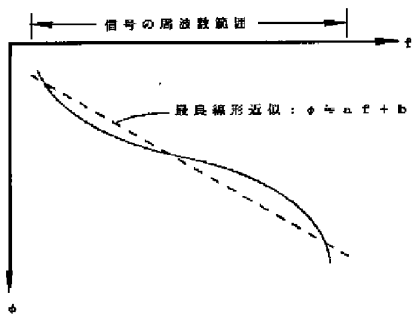
【図２】



【図４】



【図５】



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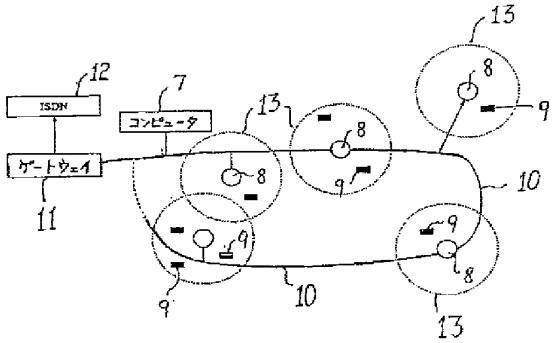
(54)【発明の名称】　ワイヤレスＬＡＮ

(57)【要約】

【目的】　本発明は、多重通路伝送環境内において１０ＧＨｚを越える周波数で動作可能なワイヤレスＬＡＮ、ピールツーピールワイヤレスＬＡＮ、ワイヤレストランシーバ及びデータの伝送方法を提供することを目的とする。

【構成】　これは、伝送の情報ビットレートの逆数は多重通路伝送通路の重要なものの間の時間遅延差に比較して短い多重通路伝送通路の存在における適当な性能を可能にする技術の組み合わせによって達成される。ＬＡＮにおいて、移動トランシーバは各々は対応する演算能力を有する可搬電子装置に接続されそれにより駆動される。



1

【特許請求の範囲】

【請求項１】　データ源及び／又は目的地を構成するために各々が互いに接続された複数のハブトランシーバと、各々が所定の範囲内において前記ハブトランシーバの一つと無線伝送によって通信可能な複数の移動トランシーバとよりなり、前記移動トランシーバの各々は演算能力を有する対応する可搬電子装置に接続可能であってそれにより駆動可能であり、前記無線伝送は１０ＧＨｚを越える周波数を有し、全てのトランシーバは多重通路伝送環境において受信及び発信するよう構成され、前記トランシーバの伝送の情報ビットレートの逆数は前記多重通路伝送環境の伝送通路の重要なものの間の時間遅延差に比較して短いことを特徴とするワイヤレスＬＡＮ。

【請求項２】　各々が所定の範囲内において他の類似したトランシーバと無線伝送によって通信可能な複数の移動トランシーバを有し、前記移動トランシーバの各々は対応する演算能力を有する可搬電子装置に接続可能であってそれにより駆動可能であり、前記無線伝送は１０ＧＨｚを越える周波数を有し、全てのトランシーバは多重通路伝送環境において受信及び発信するよう構成され、前記トランシーバの伝送の情報ビットレートの逆数は前記多重通路伝送環境の伝送通路の重要なものの間の時間遅延差に比較して短いことを特徴とするピールツーピールワイヤレスＬＡＮ。

【請求項３】　相互作用チャンネル探査；非相互作用接続のために十分な冗長度をもってのフォーワードエラー補正；少なくとも選択されたデータの再伝送による相互作用エラー補正にとって十分な冗長度をもっての変調；及びチャンネル間のデータの割当の選択よりなる技術の群から選択される一つ以上の技術を使用することによって伝送が強められることを特徴とする請求項１又は２記載のＬＡＮ。

【請求項４】　伝送は、前記所定の範囲に亘る伝送特性が比較的一定な時間にわたって各々が伝送されるデータの小さなパケットに分割されることを特徴とする請求項３記載のＬＡＮ。

【請求項５】　データのコーディングは、各々が異なる周波数の搬送波の集合に関して実行されることを特徴とする請求項１乃至４のうちいずれか１項記載のＬＡＮ。

【請求項６】　各々の独立した搬送波の変調は、搬送波振幅及び／又は位相（ｍＱＡＭ）の多重レベル変調であることを特徴とする請求項５記載のＬＡＮ。

【請求項７】　前記ｍＱＡＭは、振幅シフトキーイング（ＡＳＫ）；多重レベルＡＳＫ（ｍＡＳＫ）；置換変調；２値位相シフトキーイング（ＢＰＳＫ）；多重レベル位相シフトキーイング（ｍＰＳＫ）；振幅位相キーイング（ＡＰＫ）；及び多重レベルＡＰＫ（ｍＡＰＫ）よりなる変調種族の形であることを特徴とする請求項６記載のＬＡＮ。

【請求項８】　所定のセル範囲内において少なくとも一つのハブトランシーバと複数の移動トランシーバとの間で又は前記移動トランシーバの間でデータを伝送する方法であって、前記データ伝送は１０ＧＨｚを越える周波数を有する多重通路伝送であり、各々の前記移動トランシーバは対応する演算能力を有する可搬電子装置に接続可能であってそれにより駆動され、前記伝送の情報ビットレートの逆数は前記多重通路伝送環境の伝送通路の重要なものの間での時間遅延差に比較して短いことを特徴とするデータ伝送方法。

【請求項９】　相互作用チャンネル探査；非相互作用接続のために十分な冗長度でのフォーワードエラー補正；少なくとも選択されたデータの再伝送による相互作用エラー補正にとって十分な冗長度での変調；及びチャンネル間のデータの割当の選択よりなる技術の群から選択される一つ以上の技術を使用することによって伝送が強められることを特徴とする請求項８記載の方法。

【請求項１０】　伝送は、前記所定の範囲に亘る伝送特性が比較的一定である時間にわたって各々が伝送されるデータの小さなパケットに分割されることを特徴とする請求項９記載の方法。

【請求項１１】　データのコーディングは、各々が異なる周波数の搬送波の集合に関して実行されることを特徴とする請求項８乃至１０のうちいずれか１項記載の方法。

【請求項１２】　各々の独立した搬送波の変調は、搬送波振幅及び／又は位相（ｍＱＡＭ）の多重レベル変調であることを特徴とする請求項１１記載の方法。

【請求項１３】　前記ｍＱＡＭは、振幅シフトキーイング（ＡＳＫ）；多重レベルＡＳＫ（ｍＡＳＫ）；置換変調；２進位相シフトキーイング（ＢＰＳＫ）；多重レベル位相シフトキーイング（ｍＰＳＫ）；振幅位相キーイング（ＡＰＫ）；及び多重レベルＡＰＫ（ｍＡＰＫ）よりなる変調種族の形であることを特徴とする請求項１２記載の方法。

【請求項１４】　多重通路伝送環境において１０ＧＨｚを越える周波数を有する無線伝送を発信し受信するように動作可能であり、トランシーバの伝送の情報ビットレートの逆数は前記多重通路伝送環境の伝送通路の重要なものの間の時間遅延差に比較して短いことを特徴とするワイヤレストランシーバ。

【請求項１５】　伝送は搬送波の集合の変調によることを特徴とする請求項１４記載のトランシーバ。

【請求項１６】　トランシーバは、搬送波の集合の前記変調の発生及び検出のための高速フーリエ変換装置及び逆高速フーリエ変換装置を組み込んだ変調／復調システムを有することを特徴とする請求項１５記載のトランシーバ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は演算能力を有する装置を

3

互いに通信可能にするローカルエリアネットワーク（ＬＡＮ）に係り、特に装置が無線伝送により通信するワイヤレスＬＡＮに関する。

【０００２】

【従来の技術】近年、パーソナルコンピュータはビジネスや商業において益々重要な道具になってきており、現在多くの従業者達はそのようなコンピュータを操作することに彼等の１日の仕事の大きな部分を費やしている。同様に、ビジネス組織は益々、その従業者がオフィス環境の回りに又は内に広がるローカルエリアネットワークに接続されたパーソナルコンピュータや同等の端末により情報にアクセス可能にするだけでなくそのように強いるように彼等の仕事を構成している。

【０００３】従来、そのようなローカルエリアネットワークは導電材又は光ファイバの何れかによって配設されており、これはオフィス構内を広範囲にわたって配線することを必要とする。この配線は、もし例えばオフィス内の間仕切りが調節される時には適合されなければならない。また、多数のパーソナルコンピュータが小さな領域内で操作されるような教室や個人指導装置に必要とされる配線は非常に大きなものとなる。

【０００４】更に、演算能力を有する移動可能又は可搬の装置の売上は、最近増大する傾向にある。これらはラップトップ／ノートブック及び手持ちコンピュータを含む。そのようなコンピュータの購入の主な動機は普通のオフィス環境の外でその演算力を使用できる能力であるが、一旦可搬型コンピュータが購入されると、例えば”大学構内”のような近接した幾つかの建物に渡って広がったビジネス組織のＬＡＮにアクセス可能なように、可搬型コンピュータの使用者がコンピュータを持っていき同僚のオフィスに近接して使用することができるようにオフィス構内で可搬性を使用したいという欲求が持ち上がる。

【０００５】これは一使用者の可搬型コンピュータを如何なる特定の場所においてもオフィスＬＡＮに差し込むことを可能にする差し込みプラグ接続器により可能であるが、ＬＡＮは単一のオフィス内で２つ以上の接続点を提供しないため一般的に不便であり、可搬型コンピュータはその可搬性を失ってしまう。従って、そのような可搬型の装置がワイヤレス又は無線結合により接続可能なＬＡＮへの要求が持ち上がっている。

【０００６】しかし、そのようなワイヤレスＬＡＮは従来低データ伝送速度に実質的に限定されていた。普及した商業的受容性を達成するためには、比較的高い伝送速度、従って１ＧＨｚ以上のオーダーの周波数で伝送する必要がある。以下に説明するように、そのような高周波数での伝送は特有な問題に直面する。市販されているワイヤレスＬＡＮの一つには、ＡＬＴＡＩＲの商品名でモトローラ社から販売されているものがある。このシステムは約１８ＧＨｚで動作するが、最大データ伝送速度は

4

約３－６Ｍｂｉｔ／ｓに限定される。このシステムの有用な検討及びこれらの周波数でのオフィス環境内でのワイヤレス受信の問題は、ＩＥＥＥネットワークマガジン、１９９１年１１月号、２１－２６ページのＥ．Ｍｉｔｚｌａｆｆによる”ＷＩＮ環境内における無線伝播及び耐多重通路技術”に記載されている。

【０００７】この技術設計者は、不十分な性能及び１０Ｍｂｉｔ／ｓのデータ信号でさえ適合できるに等しい必要のあるハードウェアの大型のサイズ費用及び電力消費は、そのために多重通路伝播の問題がワイヤレス建物内ネットワーク（ＷＩＮ）システムにおいて解決することはできないと結論した。同様に、多重通路の問題に対抗するために使用されるであろうスペクトル拡散技術は、有効に使用するには広すぎる帯域幅（１０Ｍｂｉｔ／ｓに対して３００ＭＨｚ）を使用する。

【０００８】その代わり、モトローラ社及びＭｉｔｚｌａｆｆにより採用された解決策は、”最良の品質”の通路及び対応するアンテナの”切り換え”を達成するためにシステムプロセッサにより周期的に点検される３６の可能な伝送路を生じる６ビームの指向性アンテナシステムである。この手順はシステムに実質的な容積と費用とを付加する。この手順は、本質的に指向性のアンテナの使用により多重通路伝送の問題を単通路伝送環境へ変換することである。

【０００９】本発明の目的は、データ又は情報ビットレート（データ”周期”）が重要な伝送路間の時間遅延差に対して短くなるような高ビットレートを有する多重通路伝送環境におけるワイヤレスＬＡＮを提供することである。

【００１０】

【課題を解決するための手段】本発明の一つの面によれば、データ源及び／又は目的地を構成するために各々が互いに接続された複数のハブトランシーバと、各々が所定の範囲内において前記ハブトランシーバの一つと無線伝送によって通信可能な複数の移動トランシーバとよりなり、前記移動トランシーバの各々は演算能力を有する対応する可搬電子装置に接続可能であってそれにより駆動可能であり、前記無線伝送は１０ＧＨｚを越える周波数を有し、全てのトランシーバは多重通路伝送環境において受信及び発信するよう構成され、前記トランシーバの伝送の情報ビットレートの逆数は前記多重通路伝送環境の伝送通路の重要なものの間の時間遅延差に比較して短い構成のワイヤレスＬＡＮが開示される。

【００１１】本発明の他の面によれば、各々が所定の範囲内において他の類似したトランシーバと無線伝送によって通信可能な複数の移動トランシーバを有し、前記移動トランシーバの各々は対応する演算能力を有する可搬電子装置に接続可能であってそれにより駆動可能であり、前記無線伝送は１０ＧＨｚを越える周波数を有し、全てのトランシーバは多重通路伝送環境において受信及

5

び発信するよう構成され、前記トランシーバの伝送の情報ビットレートの逆数は前記多重通路伝送環境の伝送通路の重要なものの間の時間遅延差に比して短い構成のピールトゥピールワイヤレスＬＡＮが開示される。

【００１２】本発明の更に他の面によれば、所定のセル範囲内において少なくとも一つのハブトランシーバと複数の移動トランシーバとの間で又は前記移動トランシーバの間でデータを伝送する方法であって、前記データ伝送は１０ＧＨｚを越える周波数を有する多重通路伝送であり、各々の前記移動トランシーバは対応する演算能力を有する可搬電子装置に接続可能であってそれにより駆動され、前記伝送の情報ビットレートの逆数は前記多重通路伝送環境の伝送通路の重要なものの間での時間遅延差に比較して短い構成の方法が開示される。

【００１３】好ましくは、伝送は以下の技術、即ち相互作用チャンネル探査；非相互作用接続のために十分な冗長度でのフォーワードエラー補正；少なくとも選択されたデータの再伝送による相互作用エラー補正にとって十分な冗長度での変調；及びチャンネル間のデータの割当のうち一つ以上を使用することによって強められる。無線伝送は、所定の範囲に亘る伝送特性が比較的一定である時間にわたって各々が伝送されるデータの小さなパケットに分割されることが好ましい。

【００１４】データの符号化は、各々がサブチャンネルを構成し好ましくは搬送波振幅及び／又は位相（ｍＱＡＭ）の多重レベル変調である各々の独立した搬送波の変調と共の異なる周波数を有する搬送波の集合に対して好適に実行される。変調種族ｍＱＡＭは、振幅シフトキーイング（ＡＳＫ）、多重レベルＡＳＫ（ｍＡＳＫ）、置換変調、２値位相シフトキーイング（ＢＰＳＫ）、多重レベル位相シフトキーイング（ｍＰＳＫ）、振幅位相キーイング（ＡＰＫ）、多重レベルＡＰＫ（ｍＡＰＫ）等を含む。

【００１５】

【実施例】図１は一般のオフィス環境における家具２及び送信機３及び受信機４を含む部屋１を模式的に示す。１０ＧＨｚを越える周波数での無線伝送では送信機３から受信機４への多重通路モードが生じる。部屋１の壁（及び床及び天井）から及び部屋１内の家具２等からの反射が多重通路伝送を生じさせる。

【００１６】図２に示されるように、多重通路伝送の影響は、受信機４が送信機３から受信機４に直接来る遅延の無い信号５と、遅延の無い信号５の受信後に受信される多数の遅延信号６とを受信することである。遅延信号６の強さは普通いくらか減衰している。ある条件においては、遅延の無い信号５の強さも、時には遅延信号６より減衰する。

【００１７】遅延信号６の結果として、最初の記号のエコーが次の記号の受信をマスクしないように単一の記号が伝送される間の時間（記号時間）の長さが実質的に遅

6

延時間より長いことが必要である。この必要性は、その様な環境内においてデータを伝送し得る速度に対して厳しい上限を課してきた。更に、図３に示されるように、オフィス環境は無線伝送にとって決して良い環境では無い。図３は、６０と６１ＧＨｚの間の１ＧＨｚ帯域における周波数の関数としての受信信号の強さを示す短時間の典型的なチャンネル特性を示す。受信される強さは決して一定ではなく、特に様々な周波数減衰が生じている。更に、図３に点線で示されるように、減衰の生じる周波数は部屋内の移動のために時間の関数として変化する。そのような通信チャンネルは時間変化周波数選択減衰チャンネルと呼ばれる。

【００１８】類似しているが異なる通信チャンネルが電話及び長距離無線通信の両者において知られており、一般的に等化として知られている様々な方式がそのようなチャンネルが起こす問題を解決するために使用されている。しかし、これらの分野においてそのような減衰が温度又は大気条件の変化によるものであるため、一旦そのような電話及び長距離無線通信チャンネルが確立されたなら減衰特性は比較的ゆっくりと変化する。また、電話への応用において、等化を行うときにチャンネル減衰はチャンネルの中心付近において一般的に低いという利点を得ることができる。これはオフィス又は室内環境の場合には無い。

【００１９】むしろ、上述のオフィス環境において、図３の点線で示された伝送特性の変化は、例えば誰かが机の上に置かれた書類カバンを開けたという単純な動作により引き起こされる。書類カバンの持ち上げられた蓋が特性の変化を生じさせる。同様な非常に短期間の変化が、受信機４自体が移動する、又はドアが開く、人が動く等の他の物体が移動することによって引き起こされる。特に、１ＧＨｚ帯域内には好適なチャンネルも保証されたチャンネルさえも存在しない。

【００２０】直接通路以外の全ての伝送通路を排除するために高度に指向性のあるアンテナを使用することによって上述の問題を解決することは可能であろう。しかし、可搬型のコンピュータに固定されたそのようなアンテナを機械的に整列させる試みは商業的には魅力的では無い。図４は本発明による好適な実施例に基づくワイヤレスＬＡＮの一般的な配置を模式的に示す。複数のハブ８と移動トランシーバ９とが設けられている。ハブ８は導電体又は光ファイバケーブルの何れの形態でもよいバックボーン１０により相互接続されている。図４の点線により示されるように、バックボーン１０はループを構成する。所望であれば、バックボーン１０は多重通路伝送のコンピュータ７に、又、所望であればゲートウェイ１１を介して公衆電話回線網１２に接続可能である。一般的な構成では、各々のオフィス（又は構内の各々の建物の各々のオフィス）には、部屋内の移動トランシーバ９、又はその各々と通信するであろう単一のハブ８が設

けられる。バックボーン１０がカバーされる全領域にわたって延在しうるか、或いは領域は多ゲートウェイ及び多バックボーンを使用することによりカバーされうる。ハブ８内のトランシーバの有効範囲はその部屋内だけを実質的にカバーするように構成される。ハブ８の限定された伝送範囲は図４の破線により示されるように対応するセル１３を形成する。教育環境内におけるレクチャールームのような大きな部屋では、部屋の長さによってその部屋は２つのハブ８を設けられる必要があり、その場合一つの部屋内に二つの部分的に重なりあったセル１３が存在するであろう。

【００２１】図５に示されるように、ハブトランシーバ８には多数の構成部品ブロックが設けられる。これらは、ネットワークインターフェース２０、バッファメモリ２１、フレーム、フォーワードエラー補正（ＦＥＣ）及び変調器２３、ＩＦ（中間周波数）システム部２４、ｍｍ波受信機２５、ｍｍ波送信機２６、及びセル全体を照射するために放射パターンが十分に広いアンテナ１７の形を取る。アンテナ２７はこの結果を静的又は動的（電子的又は機械的ビーム操作により）に達成する。これらの部品は全て制御タイミング部２８に接続され操作される。更に、全てはＡＣ主要操作操作電源供給部２９により駆動される。

【００２２】移動トランシーバ９の同等な部分は図５中及び図６－９に１０だけ大きい参照符号により示される。移動トランシーバ９は電池駆動の電源供給部３９を有する。これは、特に受信機３５及び発信機３６内で低電力ガリウム砒素装置を使用することにより可能である。尚、アンテナ３７は、少なくとも伝送を移動トランシーバに又はから対応するハブ８に向けて部分的に方向付けるために制御タイミング部３８により電気的に操縦可能な操縦可能アンテナであることが好ましい。この目的のための好適なアンテナは、本出願人による”平面アンテナ”という名称のオーストラリア特許出願第ＰＬ９７３９号（代理人番号２３９０４５）に開示されており、ここに参考として挙げる。このアンテナはワイヤレス連結の信号ノイズ比を改善し、遅延信号を減衰し、それによって多重通路性能を改善する。

【００２３】トランシーバ９の一部のより詳細なブロック系統図が図６－９に示される。図６において、トランシーバ９（端末インタフェース３０及びバッファメモリ３１を除く）の一般的な構成が示されている。詳細の中間段階は受信機３５及び送信機３６と受信中間周波数システム３４及び受信復調器３３及び送信中間周波数システム３４及び送信変調器３２とに与えられる。変調の完全な詳細は図７に示され、復調は図８に示されている。図７において、伝送路フレーム、ＦＥＣ及び図５の変調器３２が詳細に示されている。図５のバッファメモリ３１から２値データの流れがＣＲＣ（サイクリック　リダンダンシイ　チェック）発生付加ブロック４０に供給される。このブロック４０又はパケットパターン発生部４１からの出力は選択的に１／２比のＴＣＭ（格子符号化変調）符号化部４２に入力される。符号化部４２の出力は次にＤｉビットインタリーバ４３に入力され、その出力は次にフレーム毎に差符号化を実行するＱＰＳＫ符号化部４４に入力される。ＱＰＳＫ符号化部４４及び同期ヘッダー発生部４５の出力はフレーム組立及びゼロバッド挿入ブロック４６において組み合わされ、六つの搬送波が中心周波数の両側に同時ではなく発生するようにフレームは組み立てられて四つのゼロバッドが挿入される。

【００２４】組み立てられたフレームは１６点の複合ＩＦＦＴを使用する逆高速フーリエ変換装置１７を通過する。結果としての信号は、４点巡回拡張と共に直列フレームを正確にシーケンスするためにフレーム直列化部及び巡回拡張ブロック４８を通過させられる。結果はディジタルアナログ変換器４９，５０を介して図５及び６の中間周波数段３４に送られる。

【００２５】図５及び６のフレーム化ＦＥＣ及び復調器３３の受信路において、図８に詳細に示されるように実質的に逆の手順が実行される。中間周波数段３４から受け取った信号はアナログディジタル変換器６０，６１を通過し、巡回抽出フレーム組立部６２に送られる。結果としての信号は実質的に復号化された信号を得るために高速フーリエ変換装置６３を通過させられる。この信号は同時にフレーム分解及びゼロバッド除去部６４及びメッセージの開始、終了及び記号タイミング信号を提供する同期計算検出部６５に送られる。これらは図５及び６の制御タイミング部３８に送られる。

【００２６】フレーム分解及びゼロバッド除去部６４の出力は、必要なフレーム毎のソフト決定差復調及び検出を実行する復調／検出部６６に送られる。結果としての出力は、デインタリーバ６７に送られそして再度ソフト決定復号器であるＴＣＭ復号化部に送られる。復号化部の出力は図５のバッファメモリ３１とＣＲＣ積算検査部６９との両方に送られる。この後者の装置は、もし復号化／符号化が伝送データを正確に回復しなかった場合に、図５及び６の制御タイミミング部３８のためのエラー信号を生成する。

【００２７】図９に移り、アンテナ３７から簡略的に示された双方向増幅器７１はフィルタ７２を介して映像阻止ミクサー７３に接続される。双方向増幅器７１の好適な形態は、本出願人による”双方向増幅器”という名称のオーストラリア特許出願第ＰＭ２４４５号（代理人番号２５０９８３）に開示されており、それをここに参考として挙げる。代わりに、双方向増幅器７１は、図示されるように図５及び６の制御タイミング部３８の制御下で適当に切り換えることによりアンテナ３７とフィルタ７２との間に接続される独立の発信増幅器と別の送信増幅器とを使用することによって実現可能である。

【００２８】映像阻止ミクサー７３は局部発振器部（ＬＯ）７４から５８ＧＨｚ信号を受信する。好適な形態において、第１の局部発振器（ＬＯ）は、５８ＧＨｚの周波数であり、２－３ＧＨｚの中間周波数帯域を生じる結果となる。図９に示される好適な実施例において、この信号は２９ＧＨｚ発振器の出力信号を倍にすることで得られる。図９に示されるように外部周波数弁別器を使用する、或いは安定内部共振器又はある形態の周波数／位相ロックドループを使用することにより、この発振器に周波数安定化のある形態を実行することも好ましい。

【００２９】映像阻止ミクサー７３は受信ＩＦシステム３４及び発信ＩＦシステム３４の両方に接続され、再び図５及び６の制御タイミング部３８の制御下において適当なスイッチを使用することによりそれらの間で分けられる。フィルタ７２の使用は映像周波数の付加的な阻止を提供する。図６－９により、変調の好適な形態は符号化だけではなく高速フーリエ変換及びその逆をも含む。トランシーバ３５，３６は一つ以上のモノリシック集積回路により好適に実現される。更に、移動トランシーバ９での電力消費を低減するため、制御タイミングストリーム３８は送信中又は受信中以外の各々のトランシーバ９の出力を低減させることができる。これはハブトランシーバ８により開始されるポーリングスキームによって決定される。例えば、ハブ８は各々の移動トランシーバ９と通信可能であり、発信されるべきデータが要求されているか、又はＬＡＮの他の部分にアクセスすることが要求されているかを順次調べる。様々なステーションのこのポーリングは、時分割多数アクセス、ＡＬＯＨＡ又はスロットＡＬＯＨＡ、時間トークン通過、許容要求スキーム又は他の適用可能な技術等の多くの標準技術の内の一つより構成することができる。

【００３０】ネットワークを構成する様々なトランシーバ８及び９からの伝送は、ネットワークのある部分は低速度の伝送のみを必要とし一方他の部分は非常に高速の伝送を必要とするので、同じビットレートである必要はない。この実施例は、両立可能なネットワーク内に適応されるべき様々な速度の伝送を可能とする。これはプリンタや低データ速度演算装置に使用される低コスト及び／又は低電力消費トランシーバ９を可能にする。

【００３１】上述のような妨害的な無線環境内で高速のビット伝送速度を得るために、少なくとも二つ（好ましくは三つ）の技術が同時に使用される。第１の技術は、各々のチャンネルが低ビットレートを有するが総体又は全体のビットレートが高くなるように、使用可能な帯域幅内で比較的多数の並列のサブチャンネルにわたって伝送することである。記号長さを増大することによるこの拡散は遅延時間の問題を解決し、よって記号間の干渉により生じる問題を減少させる。

【００３２】第２の技術は、フォーワードエラー補正（ＦＥＣ）のようなデータ信頼性監視及び／又は増補のある形態を有する小さなパケット内のデータの伝送を含む。パケットの長さは、データ信頼性増強方法及び環境の妨害性に依存する。十分に小さなパケットは、チャンネル特性の急速な時間的変化の問題を解決する。第３の技術は、本質的に更なるデータ信頼性増強である（以下に説明する）インタリーブである。この技術は、チャンネルの周波数応答における零により生じる問題の解決において多くのＦＥＣ法の性能を改善する。

【００３３】最も好適な環境において、集団変調（第１の技術）だけを使用することは適当な結果を生成するのに十分であり得る。しかし、そのような環境は、稀に生じるものであり、従って、実際は第２の技術が第１の技術に組み合わされて使用される。第２の技術の初期の形態は、自動繰り返し要求（ＡＲＱ）によるデータ信頼性増強である。選ぶことのできる最大許容パケット長さは、エラー無し伝送の実際の可能性を保証するものである。環境の妨害性が増大するにしたがい、チャンネル包囲又はフォーワードエラー補正（ＦＥＣ）のような冗長構成及び／又はデータ冗長及び／又は置換変調が使用されるべきである。必要であれば、チャンネル探査及び冗長技術の両方が使用される。

【００３４】これらの技術の第１に関し、多重通路伝送による一般的な時間遅延は、一般的な部屋の大きさからして５０ｎｓのオーダーである。１００Ｍｂｉｔ／ｓのオーダーの好適なビットレートにおいて、これはビット期間が遅延時間の２０％だけである１０ｎｓであることを示す。しかし、もし伝送が例えば１２のサブチャンネルに分割されるとすると、全体的に１００Ｍｂｉｔ／ｓのビットレートを達成するためには、これは各々のチャンネルが約８．３Ｍｂｉｔ／ｓのビットレートを有さなくてはならないことを意味する。もし１２ビットが符号化され記号として送られた場合、記号時間は遅延時間より大きい１２０ｎｓのオーダーとなる。サブチャンネルの最適な数の選択は環境に依存する。

【００３５】第２の技術に関し、減衰するチャンネルのため、サブチャンネルの全てがうまく伝送するとは期待されない。この理由により、データエラー補正が設けられる。これは多くの形態を持つ。第１は、その中で正確に受信されない情報のそれらの通路がリセットされる少なくとも選択されたデータの引き続いて起こる再伝送がされるようなエラーの検出に十分な冗長度である。再伝送は同じサブチャンネル又はチャンネルで行われる必要は無い。第２は、非相互作用補正に十分な冗長度を有するフォーワードエラー補正である。第３は、内蔵冗長度を有する多重トーン増幅シフトキーイングのような置換変調である。これらの技術は、受信されたビットの比較的小さな割合のエラーを復調器が補正することを可能にする。

【００３６】各々のサブチャンネルにおける変調の好適な型は、搬送波振幅及び／又は位相（ｍＱＡＭ）の多重

レベル変調である。変調の種類ｍＱＡＭは、振幅シフトキーイング（ＡＳＫ）、多重レベルＡＳＫ（ｍＡＳＫ）、置換変調、２値数位相シフトキーイング（ＢＰＳＫ），多重レベル位相シフトキーイング（ｍＰＳＫ）、振幅位相キーイング（ＡＰＫ）、多重レベルＡＰＫ（ｍＡＰＫ）等を含む。

【００３７】低ビットレート伝送を必要とするプリンタのような装置のためのトランシーバ９は、振幅シフトキーイング（ＡＳＫ）のような低スペクトル効率を与える技術を使用することができる。搬送波の集合のＡＳＫの変体は置換変調と呼ばれる。この方法において、伝送は伝送される記号が$\log_2 m$の２進数を符号化できるｍ－ａｒｙである。チャンネルに割り当てられたｍ個の記号のアルファベットがある。伝送される各々の記号は内蔵された冗長度を有し、もし記号の幾つかがチャンネルの対応する部分の劣悪な性質によりエラーとして受信された場合、どの許容された記号が伝送されたかの正確な決定が行われる。適当な直交性は、多数の既知の情報理論技術を使用することにより、又は適当な符号のためのコンピュータ検索により得られる。置換変調の高冗長度及び限定された帯域幅効率により、このシステムは（ｂｉｔｓ／Ｈｚで表される）高スペクトル効率を生じない。図示された実施例のシステムにとって、これは０．２５ｂｉｔ／Ｈｚ以下である。しかし、具体化は比較的簡単であり、例えば以下に説明する高性能の実施例と互換性があるプリンタ用の低ビットレートトランシーバ９は低コストで好適に使用される。

【００３８】多重搬送波法の他の実施例は、位相シフトキーイング（ＰＳＫ）を使用して各々の搬送波を位相変調することである。簡単な実施例において、これは二つの位相オプションが伝送される２値位相シフトキーイング（ＢＰＳＫ）又は四つのオプションが伝送される直角位相シフトキーイング（ＱＰＳＫ）である。必要に応じてより高い数が伝送される。

【００３９】フォーワードエラー補正が組み込まれたＢＰＳＫの実施例において、ビットレート”ｂ”で入ってくる２値データの流れは、限定はされないがリード－ソロモン又はたたみこみ符号化のような従来のフォーワードエラー補正構成を使用して符号化される。そのようなコーディングは、コードレートの逆数である計数”ｒ”によって伝送されるべきビットの数を増加する。ビットレートｂ．ｒで符号化された流れは”ｐ”の並行通路に分割され、ＢＳＫに使用される各々の通路は集合の別々の搬送波を変調し、無線連結に関してｐ／（ｂ．ｒ．）秒の有効な記号時間を与える。結果としての信号はチャンネル上を伝送され、チャンネルの周波数選択特性により幾つかのサブチャンネルではエラー無しで、又他では起こり得る実質的なエラーレートと共に他の装置により受信される。

【００４０】受信された搬送波は復調され、個々のビットの流れは可能性のあるエラー（主に悪いサブチャンネルから）と共に符号化されたデータの流れを形成するために組み合わされ（又は集合され）、それは（リード－ソロモン又はビテルビ復号器のような）装置によって復号化される。受信された信号におけるエラーはこの復号化処理によって普通は完全に補正される。

【００４１】また、受信された搬送波の振幅に基づき、各々のＢＰＳＫ変調の出力の正確さの信頼性として重み付けが与えられる。この重み付けは、どのビットがよりエラーと思われるかを決定するために、また伝送においてできるだけ多くのエラーを補正するために、装置の性能を高めるように符号化装置への付加的な入力として使用される。

【００４２】改善された帯域幅効率及び改善されたエラー補正能力を与えるため、組み合わされたコーディング及びトレリスコード変調（ＴＣＭ）のような変調構成を使用することが可能である。伝送される搬送波の各々に多重レベル位相シフトキーイング及び受信機の対応する復調器を使用することも可能である。これは改善された帯域幅効率を与え、したがって同じ互換性のある帯域幅のためのチャンネルを介して伝送されるより高いデータレートを可能にする。このオプションは、互換性のある手段によってではあるがより低いビットレートのトランシーバとして、より高いビットレートユニットが同じスペクトルを占有することを可能にする。増大されたスペクトル効率を得るには、ある程度のエラー性能の低下と共に変調器及び復調器のコストが増大された複雑となる。

【００４３】上述のように、個々のデータ要素の貢献を集合の総数より少ない搬送波に分配するＦＥＣのエラー補正性能を更に改善するために、連結データインタリーブスキームが使用可能である。連結データインタリーブスキームは、符号化されない入力データの与えられた要素に関連したこれらの搬送波のエラーの可能性の相互関連は最小とされるような方法で搬送波間の符号化されたデータを分配することによってこれを行う。普通は、これらの搬送波の間の最小周波数間隔を最大とすることに対応する。

【００４４】例えば５ビットの拘束長さと共の、１２搬送波集合体の搬送波のハーフレートトレリスコードＱＰＳＫ変調において、適当なインタリーブスキームは以下の通りである。

連続したエンコーダ出力ｄｉ－ｂｉｔｓにより変調された搬送波番号（１～１２）：１，３，５，７，９，１１，２，４，６，８，１０，１２，１，３，．．．

そのようなインタリーブスキームは実質的に従来の方法によってデマルチプレクサ、シフトレジスタ及びマルチプレクサによって一般的に具体化される。

【００４５】上記はシステムのエラーレート性能を改善するであろうが、全ての場合において全てのエラーを除

外しない。システム内に残ったエラーを無くすため、巡回冗長検査（ＣＲＣ）自動繰り返し要求（ＡＲＱ）のような付加的なエラー補正層が使用される。このエラー補正層は、エラーと思われるこれらの記号の再伝送を要求する。この再伝送は、同じ周波数のチャンネルで行われることもあり、又はいくらかの所定の量だけ全部の周波数チャンネルにシフトさせることが制御タイミング部に要求されることもあり、又はエラーの無い伝送の可能性を増加するためにアンテナの特性を極性が生じるように変えることもある。

【００４６】伝送チャンネルの高度の時間変化特性のため、伝送データは短い時間のパケット（一般的に１００マイクロ秒）に分割される。この短い時間の間伝送特性は一定であると仮定することができる。データのパケットの伝送の前に、エラーレートを減少させるためチャンネル選択技術を使用してもよい。一つのチャンネル選択技術はパケットの伝送に先立ってチャンネルを探ることである。必要であれば、特定のサブチャンネル又はチャンネルが減衰することがわかれば、これはデータレートを減少させる。

【００４７】図７及び８に示されるように、多重搬送波変調スキームを発生し復調する好適な方法は、復号データに関して高速で高速フーリエ変換（ＦＦＴｓ）及び逆高速フーリエ変換（ＩＦＦＴｓ）が可能な装置を使用する。そのような装置は、本出願人に対して許可された「変換処理回路」という名称のオーストラリア特許第６１０、９３４号に記載されており、その開示内容はここに参考として挙げる。図７及び８に示される例において、１６点の高速フーリエ変換が使用される。

【００４８】高速フーリエ変換と共に回路４８による巡回拡張、及び回路６２による巡回抽出の使用によって改善された性能を得ることができる。巡回拡張は、チャンネル遅延拡散効果及び復調器タイミングエラーによって生成されたサブチャンネルの直行性の減衰を減少することによるＦＦＴベースの集合変調構成の多重通路を増補するための技術である。復調器において、それは、ＦＦＴ出力フレームにそのフレームのコピーを付加し組み合わせを所望の長さに縮めることによって個々の多重搬送波記号の時間を拡張することよりなる。拡張の長さは、多重通路誘起中間記号干渉への許容とチャンネルスペクトル効率の減少との中間である。それはチャンネルインパルス応答が実質的なエネルギーを有する時間間隔に好適に対応する。

【００４９】抽出器及びフレーム組立器６２において、本質的に悪化されていない多重搬送波記号は、その端部が多重通路チャンネルの拡張されたインパルス応答により悪化される潜在的に歪んだ入来拡張記号から（巡回抽出によって）摘出される。この摘出された記号はＦＦＴを基にした復調処理に使用される。例えば、１６点ＦＦＴを使用する時、４点の巡回抽出長さが使用可能である。

【００５０】これらの処理は、ＦＦＴインタフェースのために要求されるフレーム組立／分解機構の僅かな拡張によって効率的に具体化される。関連した処理（より演算的に集中した）は、「テーパリング」又は「ウィンドイング」のものであり、それでは多重搬送波記号の振幅は、サブチャンネルの相互クロストークを周波数の数搬送波間隔分以上低減するために記号時間の一部の間で変化する。

【００５１】多重搬送波スキームを使用する時、全ての帯域を占有することは常に好ましいわけではなく、幾つかの搬送波は伝送される必要は無い。例えば、ＦＦＴ装置６３を使用するときには、所定の近接したチャンネル抑制／拒否のためのアナログ（再構成／耐エイリアシング）フィルタ選択性要求は、その高周波数ビンは変調器内でゼロフィルされ、変調器内で無視されるより大きな変換によって緩和することができる。これは、送信機において高い周波数（帯域外）の搬送波を発生しないで、それらの周波数において受信されたエネルギーを無視することに相当し、よってＦＦＴは（ダイナミックレンジの考慮に従って）帯域端選択性の重要な部分を与える。ゼロ挿入は、システム内のＤＣオフセットドリフトへの感受性を低減するように帯域中心搬送波（基本帯域におけるＤＣ）を除外するために使用される。例えば、１６点ＦＦＴ装置６３を使用するとき、１２の搬送波のみが操作可能に使用される。

【００５２】図６に示されるように、装置６５は受信機を入来データに同期させるように要求される。この装置は、例えばこの入ってくるデータを受信機のタイミング信号と比較し、記号とビット時間との差を計算し、この情報を同期又はゼロ差を達成するために適当な補正を行う制御タイミング部に送る。集合変調及びＦＦＴハードウェアの分割に釣り合った多重通路誤差を有する好適な同期スキームは、発生器４５により発生するメッセージヘッダーに存在する幾つかの搬送波相対的位相の計測と、これらをヘッダー伝送の最初の伝送される搬送波の既知の位相関係と比較することにより多重搬送波記号タイミング及び全局部発信周波数差を決定する。

【００５３】ＩＦシステム３４は図６に示され、送信機のためのＩ，Ｑアップ変換器及び受信機のためのＩ，Ｑダウン変換器を構成する。ＩＦシステムの第２のＬＯ部は帯域２－３ＧＨｚに同調され、これは基本帯域への及びからの信号の変換を可能にする。幾つかの実施例において、第１の部分発振器７４（図９）の周波数を変えることにより、及び他においてはＩＦシステム内の第２の部分発振器の周波数を変えることにより、搬送波周波数の同調を与えることが好ましい。発信及び受信ＩＦシステム内の構成部品を共通に使用することが可能である。

【００５４】前述は本送信機の幾つかの実施例を説明しているにすぎず、本発明の範囲から逸脱することなく変

形例を成すことが可能である。例えば、受信されるエラーレートの減少のために発信されるデータのインタリーブ及びビット反転は、ＦＦＴ変換の固有のビット反転を利用することによって達成可能である。また、アンテナ３７は受信を改善するために極性変化を利用してもよい。

【００５５】低ビットレートトランシーバ及び高ビットトランシーバの同時動作のための一つの構成は、例えば、利用可能なチャンネル（高ビット）の半分を低ビットレートトランシーバに割り当てることである。よって、低ビットトランシーバは利用可能な帯域幅の半分だけを使用し、ハブは同時に二つの低ビットレートトランシーバに低速度でデータを伝送できる。よって、同じハブのハードウェアが高ビットレート及び低ビットレートトランシーバの両方に使用できる。

【００５６】移動トランシーバ９は互いに所定のセル範囲内で直接伝送し会うことができるため、ＬＡＮはハブ８を含むことを必要としないことは当業者には明白である。そのようなＬＡＮはピールツーピール（ｐｅｅｒ　ｔｏ　ｐｅｅｒ）ＬＡＮと呼ばれている。同様に、ハブ８は電気ケーブル及び／又は光ファイバによって相互接続されているとして説明したが、無線又は赤外線連結により相互接続されてもよい。連結はバックボーン１０の一部を形成し、又はハブ間の通信連結を構成する。

【図面の簡単な説明】

【図１】反射によって生じる少なくとも１０ＧＨｚの無線周波数の多重通路伝送を示すオフィスの簡略平面図である。

【図２】多重通路伝送の可能性のために遅延された減少された強さの受信信号を示すインパルス伝送のための時間の関数としての受信された電力のグラフである。

【図３】特性自体が時間依存であり、伝送周波数の関数としての定常状態信号の受信された振幅のグラフである。

【図４】各々が対応するセル内で移動トランシーバと通信可能である複数のハブを有するローカルエリアネットワークを示す簡略線図である。

【図５】各々のハブ及び移動トランシーバ内の回路構成の簡略ブロック図である。

【図６】図５の移動トランシーバの一部を示すより詳細なブロック図である。

【図７】図６の移動トランシーバの伝送通路のフレーム、ＦＥＣ及び変調器部３２のより詳細なブロック図である。

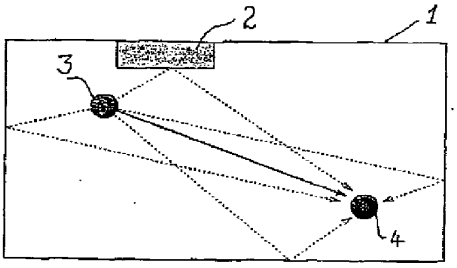
【図８】図６の移動トランシーバの伝送通路のフレーム、ＦＥＣ及び変調器部３２のより詳細なブロック図である。

【図９】図６の移動トランシーバのｍｍ波送信機３６及び受信機３５のより詳細なブロック図である。

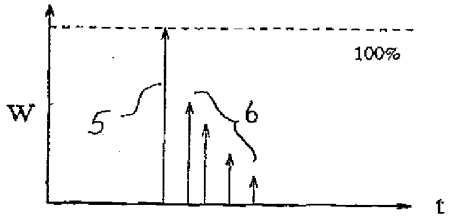
【符号の説明】

１　部屋
２　家具
３　送信機
４　受信機
５　非遅延信号
６　遅延信号
８　ハブ
９　移動トランシーバ
１０　バックボーン
１１　ホストコンピュータ
１２　公衆電話回線網
１３　セル
２０　ネットワークインタフェース
２１，３１　バッファメモリ
２２，３２　フレーム、ＦＥＣ及び変調システム
２３，３３　フレーム、ＦＥＣ及び復調システム
２４，３４　中間周波数部
２５，３５　ｍｍ波受信機
２６，３６　ｍｍ波送信機
２７　広帯域アンテナ
２８，３８　制御タイミング部
２９，３９　電源供給部
３０　端末インタフェース
３７　操縦可能アンテナ
４０　ＣＲＣ発生及び付加ブロック
４１　パケット端部及びパターン発生器
４２　レート１／２ＴＣＭエンコーダ
４３　ｄｉ－ｂｉｔインタリーバ
４４　差（フレーム毎）ＱＰＳＫエンコーダ
４５　同期ヘッダー発生器
４６　フレーム組立体及びゼロバッド挿入ブロック
４７　１６点復号ＩＦＦＴ
４８　フレーム直列化部及び４点巡回拡張器ブロック
４９，５０　ディジタルアナログ変換器
６０，６１　アナログデジタル変換器
６２　４点巡回抽出及びフレーム組立体
６３　１６点ＦＦＴ装置
６４　フレーム分解及びゼロパッド除去部
６５　同期計算器及び検出器
６６　復調器／検出器
６７　デインタリーバ
６８　ＴＣＭデコーダ
６９　ＣＲＣ積算器／検査器
７１　双方向増幅器
７２　フィルタ
７３　影像阻止ミクサー
７４　局部発信部

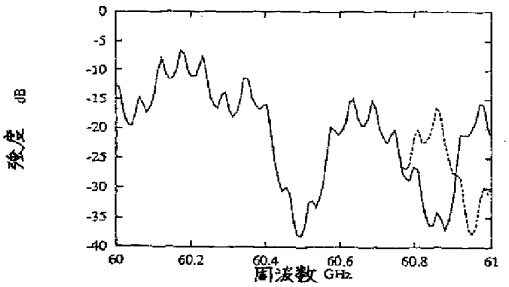
【図１】


2
1
3
4

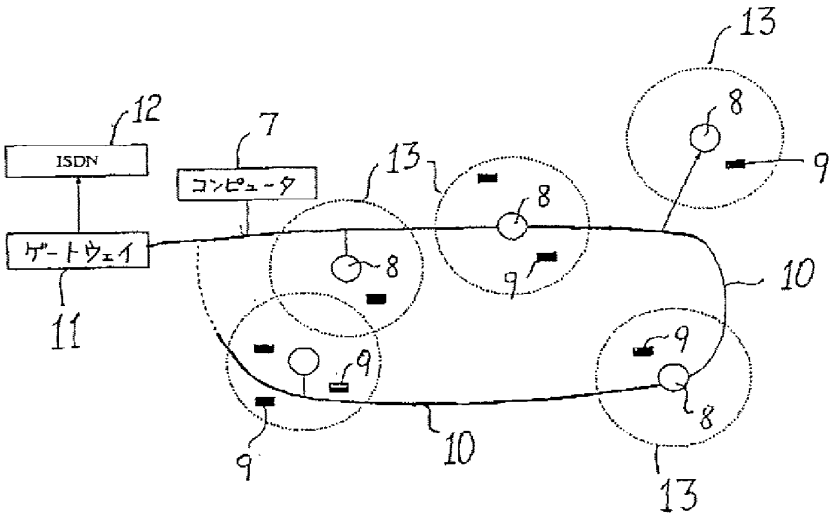
【図２】


100%
W
5
6
t

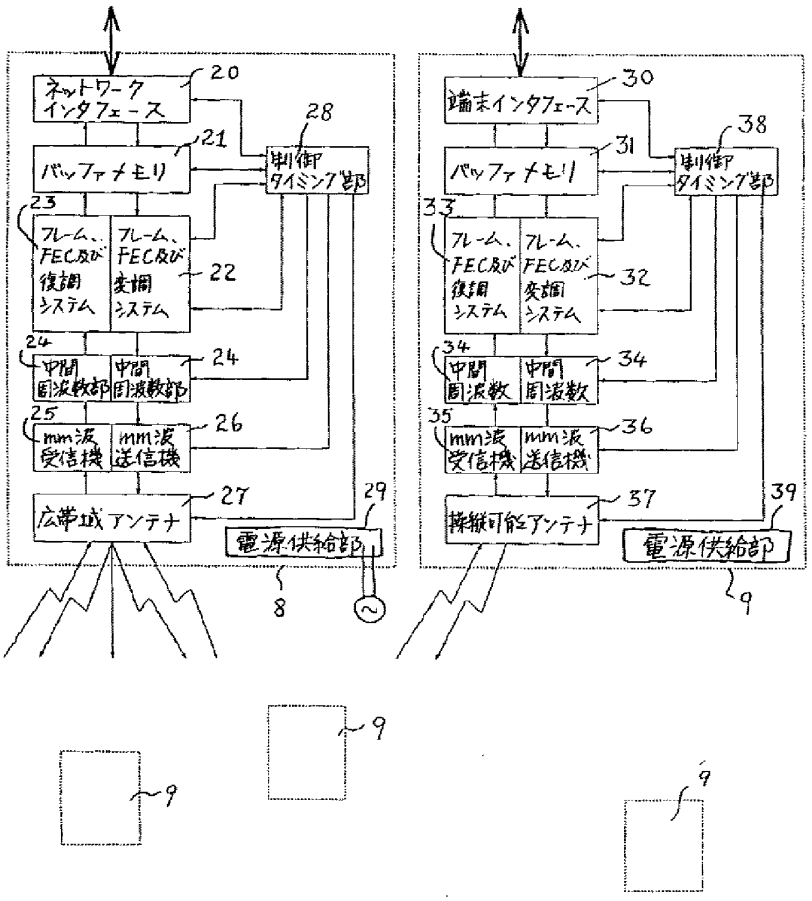
【図３】


0
-5
-10
-15
-20
-25
-30
-35
-40
強度 dB
60
60.2
60.4
60.6
60.8
61
周波数 GHz

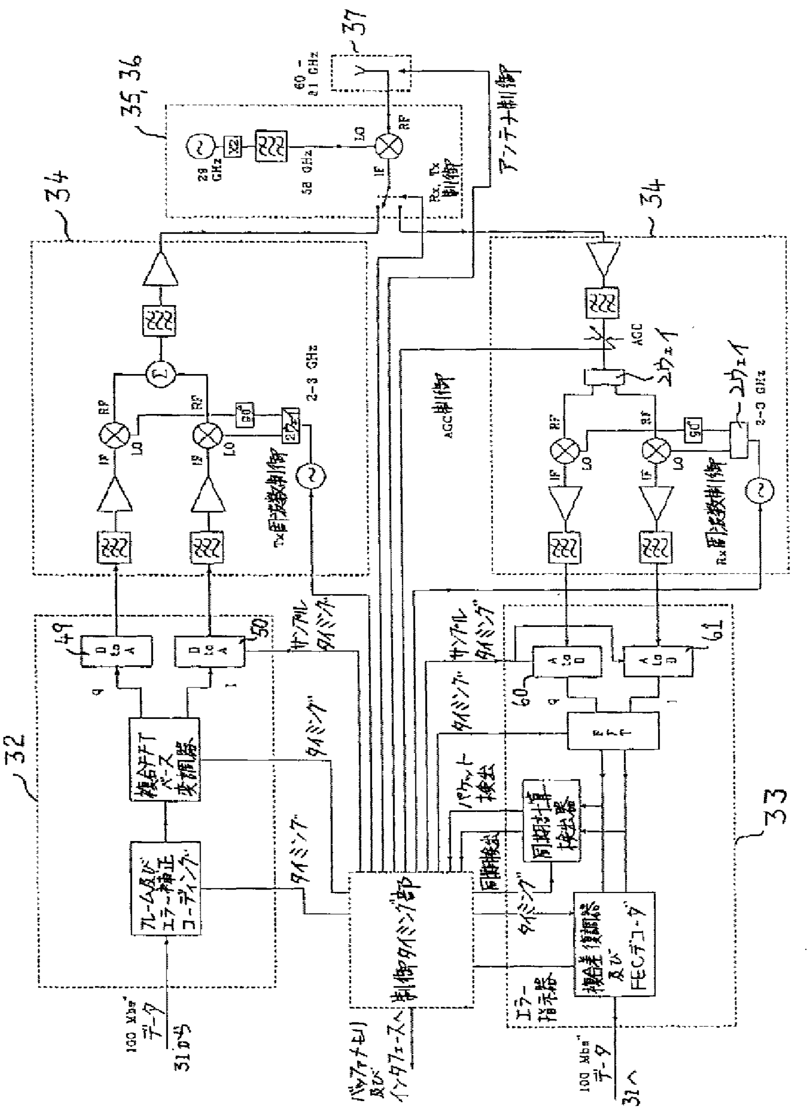
【図４】


12
ISDN
7
コンピュータ
ゲートウェイ
11
13
8
9
10

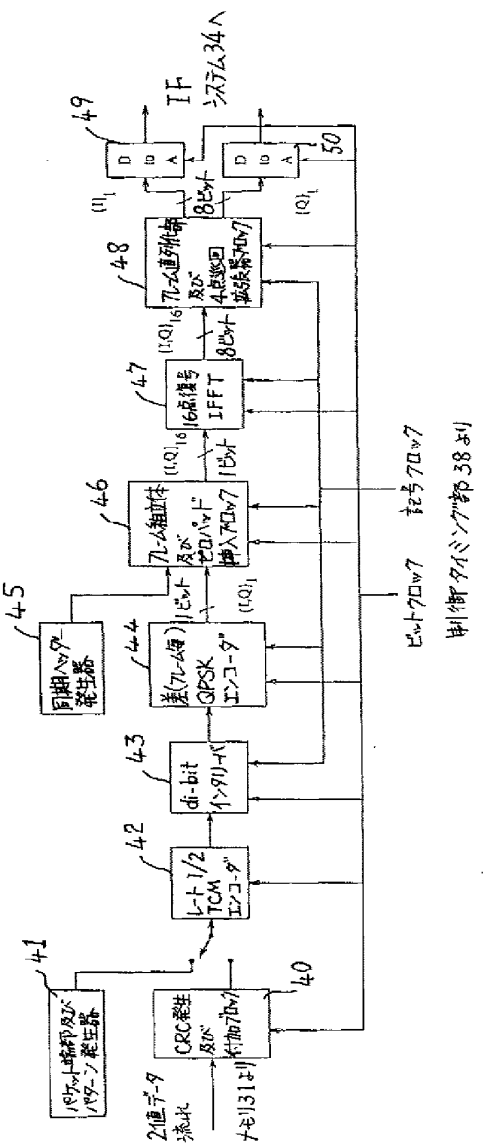
【図５】


ネットワーク インタフェース
20
バッファメモリ
21
制御 タイミング部
28
フレーム、FEC及び 復調 システム
23
フレーム、FEC及び 変調 システム
22
中間 周波数部
24
mm波 受信機
25
mm波 送信機
26
広帯域アンテナ
27
電源供給部
29
8
端末インタフェース
30
バッファメモリ
31
制御 タイミング部
38
フレーム、FEC及び 復調 システム
33
フレーム、FEC及び 変調 システム
32
中間 周波数
34
mm波 受信機
35
mm波 送信機
36
指向可能アンテナ
37
電源供給部
39
9

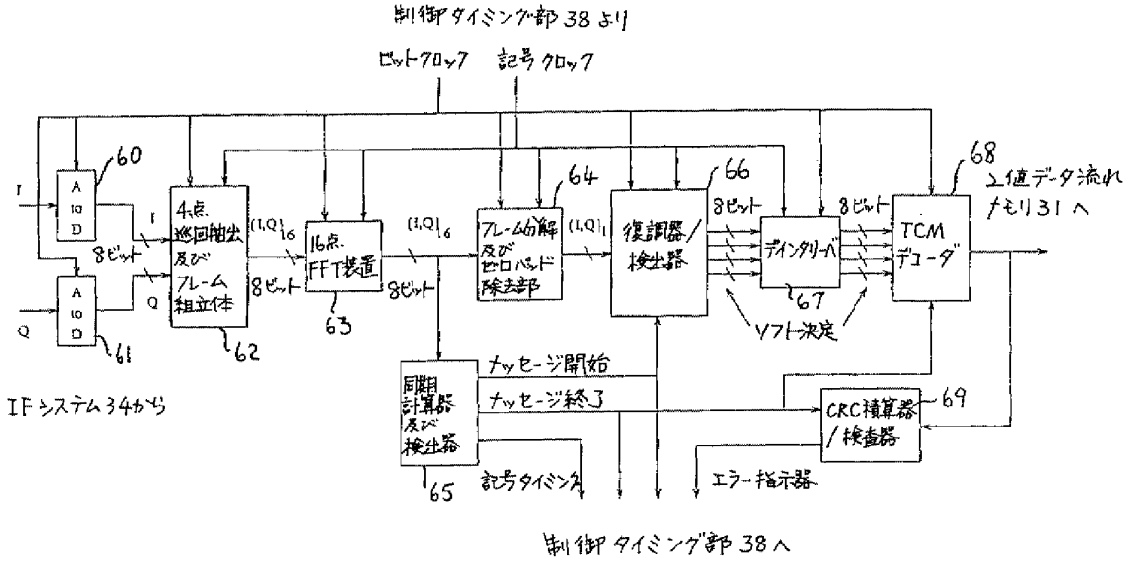
【図６】


32
33
34
35, 36
37
49
50
60
61
アンテナ制御
AGC制御
タイミング
サンプルタイミング
パケット検出
同期検出
60 - 61 GHz
58 GHz
29 GHz
2-3 GHz
2ウェイ
IF
LO
RF
AGC

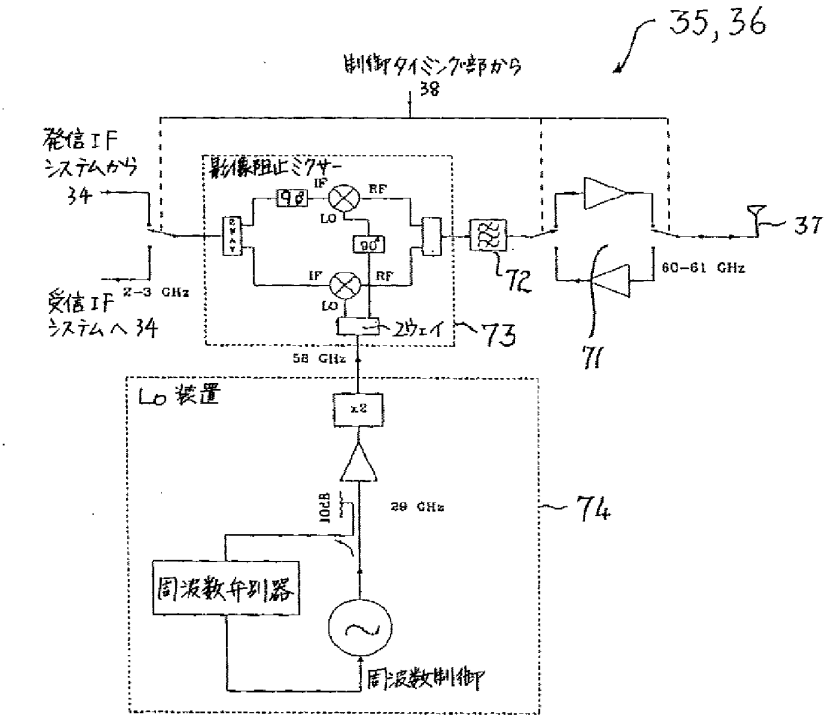
【図７】


IF
システム34へ
49
48
47
46
45
44
43
42
41
40
50
8ビット
1ビット
16点複素IFFT
ビットクロック
制御タイミング信号38より

【図８】


制御タイミング部38より
ビットクロック
記号クロック
I
Q
A to D
60
61
8ビット
4点巡回相関及びフレーム相立体
62
(I,Q)16
16点FFT装置
63
8ビット
フレーム分解及びゼロバンド除去部
64
(I,Q)1
復調器/検出器
66
ディンタリーバ
67
ソフト決定
TCMデコーダ
68
2値データ流れ
メモリ31へ
IFシステム34から
同期計算器及び検出器
65
メッセージ開始
メッセージ終了
記号タイミング
エラー指示器
CRC積算器/検査器
69
制御タイミング部38へ

【図９】


35,36
制御タイミング部から
38
発信IFシステムから34
影像阻止ミクサー
IF
RF
LO
90°
2ウェイ
73
72
37
60-61 GHz
71
受信IFシステムへ34
2-3 GHz
58 GHz
LO装置
x2
10dB
20 GHz
74
周波数並列器
周波数制御

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【公報種別】特許法第１７条の２の規定による補正の掲載
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　H04L　12/28
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　H04L　11/00　　310 B

【手続補正書】
【提出日】平成１２年１１月１６日（２０００．１１．１６）
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】変更
【補正内容】
【特許請求の範囲】
【請求項１】　無線周波数信号を送信及び受信するアンテナを含む無線周波数手段と、
入力データチャネルから入力データを受信し且つ前記無線周波数手段により伝送するために入力データを処理する、入力データを変調する変調手段を有する伝送信号処理手段と、
前記無線周波数手段により受信された信号を処理し且つ出力データチャネルへデータを出力する受信信号処理手段とを有する、周波数選択的フェージングと符号間干渉を受けやすい、閉じ込められたマルチパス伝送環境内での動作のためのトランシーバであって、
前記変調手段は、サブチャネルシンボルの周期が非直接伝送経路の内の重要な１つの時間遅延を表す所定の周期よりも長いように、前記入力データを複数の異なる周波数の、各々のサブチャネルがデータシンボルのシーケンスを担う、サブチャネルへ変調するように作用することを特徴とするトランシーバ。
【請求項２】　前記伝送信号処理手段は、前記変調手段へ送られた前記入力データに、データの信頼性の向上を供給する手段を更に有することを特徴とする請求項１記載のトランシーバ。
【請求項３】　前記伝送信号処理手段は、前記入力データ信頼性向上手段と前記変調手段との間に挿入された、前記データのブロックをインターリーブするための手段と更に有することを特徴とする請求項２記載のトランシーバ。
【請求項４】　前記データの前記ブロックは、ビットであることを特徴とする請求項３記載のトランシーバ。
【請求項５】　データの信頼性の向上を供給する前記手段は、フォワード誤り訂正を行うように作用することを特徴とする請求項２乃至４のうちいずれか一項記載のトランシーバ。
【請求項６】　前記変調手段は、前記サブチャネルシンボルの継続時間を拡張するように成された周期的拡張手段を更に有することを特徴とする請求項１乃至５のうちいずれか一項記載のトランシーバ。
【請求項７】　前記変調手段は、多値振幅位相シフトキーイング（ｍＡＳＫ）、パーミュテーション変調、２値位相シフトキーイング（ＢＰＳＫ）、多値位相シフトキーイング（ｍＰＳＫ）及び、多値振幅位相キーイング（ｍＡＰＫ）よりなる変調群から選択された変調を使用するように適用されることを特徴とする請求項１乃至６のうちいずれか一項記載のトランシーバ。
【請求項８】　前記受信信号処理手段は、前記複数のサブチャネルの受信されたシンボルを前記出力データチャネルに対する出力データへ復調するための復調手段を有することを特徴とする請求項１乃至７のうちいずれか一項記載のトランシーバ。
【請求項９】　前記復調手段は、拡張された継続時間のサブチャネルシンボルから、サブチャネルシンボルを抽出するようになされた周期的抽出手段を有することを特徴とする請求項６或は８のうちいずれか一項記載のトランシーバ。
【請求項１０】　前記トランシーバは、更に、
前記無線周波数手段と前記受信信号処理手段を入力信号に対して同期する同期手段と、
受信された信号をベースバンド周波数へ、及び、ベースバンド周波数から変換することを可能とする、動作周波数が制御可能な第２の発振器手段とを有することを特徴とする請求項１乃至９のうちいずれか一項記載のトランシーバ。
【請求項１１】　前記同期手段は、チャネルシンボルタイミング値と、前記トランシーバの前記動作周波数と第２のトランシーバの動作周波数の間の差を決定するよう

に作用することを特徴とする請求項１０記載のトランシーバ。

【請求項１２】　前記同期手段は、伝送の最初で、異なる周波数サブチャネルキャリアの少なくとも１つの対の相対的な位相の測定により、前記チャネルシンボルタイミングと前記差を決定し、且つ、前記測定された位相差と前記伝送されたサブチャネルキャリアの所定の位相関係とを比較するのに適用されることを特徴とする請求項１１記載のトランシーバ。

【請求項１３】　前記アンテナ手段を、データの伝送のための前記伝送信号処理手段と、データの受信のための前記受信信号処理手段へ、選択的に結合するための切り替え手段を更に有することを特徴とする請求項１乃至１２のうちいずれか一項記載のトランシーバ。

【請求項１４】　前記トランシーバは、１０ＧＨｚを超える無線周波数でデータを送信及び受信するように動作することを特徴とする請求項１乃至１３のうちいずれか一項記載のトランシーバ。

【請求項１５】　複数のデータ源と行き先を構成するためにともに結合された複数のハブトランシーバと、
各移動トランシーバは請求項１乃至１４のうちいずれか一項記載のトランシーバを含み、各移動トランシーバはデータ処理手段に接続されている複数の移動トランシーバを有する無線ＬＡＮであって、各前記データ処理手段間、各前記データ処理手段と対応する前記トランシーバ間で、データは伝送又は受信されるために通過し、各前記トランシーバは、閉じ込められたマルチパス環境内で、前記ハブ受信器の１つへ、無線伝送により、データの送受信動作のために適用される、無線ＬＡＮ。

【請求項１６】　各移動トランシーバは請求項１乃至１４のうちいずれか一項記載のトランシーバを含み、閉じ込められたマルチパス環境内で、その間で、無線伝送により、データの送受信動作のために適用され、各前記トランシーバはデータ処理手段に接続された、複数の移動トランシーバを有するピアツーピア無線ＬＡＮであって、各前記データ処理手段と対応する前記トランシーバの間で、データが伝送又は受信されるために通過するピアツーピア無線ＬＡＮ。

【請求項１７】　無線周波数信号を送信するアンテナを含む無線周波数手段と、
入力データチャネルから入力データを受信し且つ前記無線周波数手段により伝送するために入力データを処理する、入力データを変調する変調手段を有する伝送信号処理手段とを有する、周波数選択的フェージングと符号間干渉を受けやすい、閉じ込められたマルチパス伝送環境内での動作のための送信器であって、
前記変調手段は、サブチャネルシンボルの周期が非直接伝送経路の内の重要な１つの時間遅延を表す所定の周期よりも長いように、前記入力データを複数の異なる周波数の、各々のサブチャネルがデータシンボルのシーケンスを担う、サブチャネルへ変調するように作用することを特徴とする送信器。

【請求項１８】　前記伝送信号処理手段は、前記変調手段へ送られた前記入力データに、データの信頼性の向上を供給する手段を更に有することを特徴とする請求項１７記載の送信器。

【請求項１９】　前記伝送信号処理手段は、前記入力データ信頼性向上手段と前記変調手段との間に挿入された、前記データのブロックをインターリーブするための手段と更に有することを特徴とする請求項１８記載の送信器。

【請求項２０】　前記データの前記ブロックは、ビットであることを特徴とする請求項１９記載の送信器。

【請求項２１】　データの信頼性の向上を供給する前記手段は、フォワード誤り訂正を行うように作用することを特徴とする請求項１８乃至２０のうちいずれか一項記載の送信器。

【請求項２２】　前記変調手段は、前記サブチャネルシンボルの継続時間を拡張するように成された周期的拡張手段を更に有することを特徴とする請求項１７乃至２１のうちいずれか一項記載の送信器。

【請求項２３】　前記変調手段は、多値振幅位相シフトキーイング（ｍＡＳＫ）、バーミュテーション変調、２値位相シフトキーイング（ＢＰＳＫ）、多値位相シフトキーイング（ｍＰＳＫ）及び、多値振幅位相キーイング（ｍＡＰＫ）よりなる変調群から選択された変調を使用するように適用されることを特徴とする請求項１７乃至２２のうちいずれか一項記載の送信器。

【請求項２４】　前記受信信号処理手段は、前記複数のサブチャネルの受信されたシンボルを前記出力データチャネルに対する出力データへ復調するための復調手段を有することを特徴とする請求項１７乃至２３のうちいずれか一項記載の送信器。

【請求項２５】　前記復調手段は、拡張された継続時間のサブチャネルシンボルから、サブチャネルシンボルを抽出するようになされた周期的抽出手段を有することを特徴とする請求項２２或は２４のうちいずれか一項記載の送信器。

【請求項２６】　前記送信器は、更に、前記無線周波数手段と前記受信信号処理手段を入力信号に対して同期する同期手段と、
受信された信号をベースバンド周波数へ、及び、ベースバンド周波数から変換することを可能とする、動作周波数が制御可能な第２の発振器手段とを有することを特徴とする請求項１７乃至２５のうちいずれか一項記載の送信器。

【請求項２７】　前記同期手段は、チャネルシンボルタイミング値と、前記トランシーバの前記動作周波数と第２のトランシーバの動作周波数の間の差を決定するように作用することを特徴とする請求項２６記載の送信器。

【請求項２８】　前記同期手段は、伝送の最初で、異なる周波数サブチャネルキャリアの少なくとも１つの対の相対的な位相の測定により、前記チャネルシンボルタイミングと前記差を決定し、且つ、前記測定された位相差と前記伝送されたサブチャネルキャリアの所定の位相関係とを比較するのに適用されることを特徴とする請求項２７記載の送信器。

【請求項２９】　前記アンテナ手段を、データの伝送のための前記伝送信号処理手段と、データの受信のための前記受信信号処理手段へ、選択的に結合するための切り替え手段を更に有することを特徴とする請求項１７乃至２８のうちいずれか一項記載の送信器。

【請求項３０】　前記トランシーバは、１０ＧＨｚを超える無線周波数でデータを送信するように動作することを特徴とする請求項１７乃至２９のうちいずれか一項記載の送信器。

【請求項３１】　入力データチャネルから入力データを受信するステップと、
前記入力データを変調するステップと、
その変調されたデータを伝送するするステップとを有する、周波数選択的フェージングと符号間干渉を受けやすい、閉じ込められたマルチパス伝送環境内での無線周波数波を使用してデータを伝送する方法であって、
変調ステップは、サブチャネルシンボルの周期が非直接伝送経路の内の重要な１つの時間遅延を表す所定の周期よりも長いように、前記入力データを複数の異なる周波数の、各々のサブチャネルがデータシンボルのシーケンスを担う、サブチャネルへ変調することを特徴とする方法。

【請求項３２】　前記データへデータの信頼性の向上を与えるステップを更に有することを特徴とする請求項３１記載の方法。

【請求項３３】　前記向上されたデータのブロックをインターリーブするステップを更に有することを特徴とする請求項３２記載の方法。

【請求項３４】　前記データの前記ブロックは、ビットであることを特徴とする請求項３３記載の方法。

【請求項３５】　前記データの信頼性の向上は、フォワード誤り訂正であることを特徴とする請求項３２乃至３４のうちいずれか一項記載の方法。

【請求項３６】　前記サブチャネルシンボルの継続時間を拡張する更なるステップを特徴とする請求項３１乃至３５のうちいずれか一項記載の方法。

【請求項３７】　前記変調は、多値振幅位相シフトキーイング（ｍＡＳＫ）、パーミュテーション変調、２値位相シフトキーイング（ＢＰＳＫ）、多値位相シフトキーイング（ｍＰＳＫ）及び、多値振幅位相キーイング（ｍＡＰＫ）よりなる変調群からであることを特徴とする請求項３１乃至３６のうちいずれか一項記載の方法。

【請求項３８】　前記複数のサブチャネルの受信されたシンボルを出力データチャネルに対する出力データへ復調する更なるステップを特徴とする請求項３１乃至３７のうちいずれか一項記載の方法。

【請求項３９】　前記サブチャネルシンボルの継続時間を短縮する更なるステップを特徴とする請求項３８記載の方法。

【請求項４０】　同期手段を使用して、前記無線周波数手段と前記受信信号処理手段を入力信号に対して、同期するステップと、
第２の発振器手段を使用して、受信された信号をベースバンド周波数へ、及び、ベースバンド周波数から変換するステップとを更に有し、前記第２の発振器手段の動作周波数は制御可能であることを特徴とする請求項３１乃至３９のうちいずれか一項記載の方法。

【請求項４１】　前記同期手段は、チャネルシンボルタイミング値と、第1のトランシーバの前記動作周波数と第２のトランシーバの動作周波数の間の差を決定するように作用することを特徴とする請求項４０記載の方法。

【請求項４２】　伝送の最初で、異なる周波数サブチャネルキャリアの少なくとも１つの対の相対的な位相の測定により、前記チャネルシンボルタイミングと前記差が決定され、且つ、前記測定された位相差と前記伝送されたサブチャネルキャリアの所定の位相関係を比較することを特徴とする請求項４１記載の方法。

【請求項４３】　前記アンテナ手段を、データの伝送のための前記伝送信号処理手段と、データの受信のための前記受信信号処理手段へ、選択的に結合する更なるステップを特徴とする請求項３１乃至４２のうちいずれか一項記載の方法。

【請求項４４】　前記伝送するステップは、１０ＧＨｚを超える無線周波数で行われることを特徴とする請求項３１乃至４３のうちいずれか一項記載の方法。

PATENT ABSTRACTS OF JAPAN

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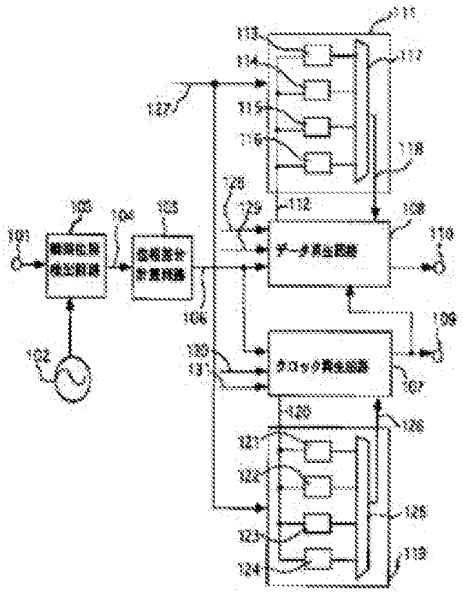
(54) DEMODULATION CIRCUIT AND DEMODULATING METHOD

(57)Abstract:
PURPOSE: To receive and demodulate the radio waves from plural transmission stations by a TDMA communication without errors by performing a parameter correction based on the storage value of a parameter error in communication.

CONSTITUTION: An inputted modulated wave is supplied to an instantaneous phase detection circuit 103, the output 104 is inputted in a phase difference calculation circuit 105 and the output 106 is inputted in a clock regeneration circuit 107 and a data reproduction circuit 108. The output 112 of the reproduction circuit 108 is a frequency error corrected value signal and is supplied to the register 113 to 116 within a frequency error storage circuit 111. Corresponding to time slot numbers, respectively, a frequency error correction signal 128 is latched to one register selected by a selection signal 127 at the time of a fall. The reproduction circuit 108 starts the data reproduction by using a frequency error correction storage output 118 at first and the corrected value is updated for a period when the control signal 128 is '1'.



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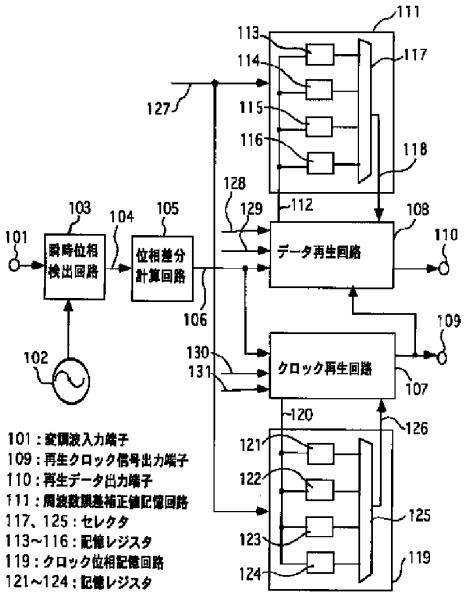
最終頁に続く

(54)【発明の名称】　復調回路及び復調方法

(57)【要約】

【目的】　ＴＤＭＡ通信における、変調された受信信号を精度よく復調することができる復調回路及び復調方法を提供する。

【構成】　復調におけるデータの判定を行なうに際し、各タイムスロット毎にパラメータの補正値を記憶する記憶回路１１１、１１９を設け、この補正値を用いてデータ再生、クロック再生を行なうようにした。



発明に係る復調回路図

【特許請求の範囲】
【請求項１】　時分割多重方式で送られて来る複数の送信局からの電波を受信して検波及び判定する復調回路において、
時分割された各時間帯毎に受信した信号の検波を行なう検波回路と、
時分割された各時間帯毎に前記受信信号のパラメータ誤差を記憶する記憶回路と、
通信の開始時にはパラメータ誤差無しの点からパラメータ補正を行い、通信中は前記記憶回路に記憶されている前記パラメータ誤差の記憶値を基にパラメータ補正を行なって判定する判定回路とを具えてなることを特徴とする復調回路。
【請求項２】　時分割多重方式で送られて来る複数の送信局からの電波を受信して検波及び判定する復調回路において、
時分割された各時間帯毎に受信した信号の検波を行なう検波回路と、
時分割された各時間帯番号毎に前記受信信号のパラメータ誤差を記憶する記憶回路と、
各時間帯番号毎に、通信の開始時にはパラメータ誤差無しの点からパラメータ補正を行い、通信中は前記記憶回路に記憶された時間帯番号に対応するパラメータ誤差の記憶値を基にパラメータ補正を行なって、判定する判定回路とを具えてなる復調回路。
【請求項３】　時分割多重方式で送られて来る複数の送信局からの電波を受信して復調する復調回路において、
時分割された各時間帯毎に受信した信号の検波を行なう検波回路と、
時分割された各時間帯毎に前記受信信号のクロック位相を記憶する記憶回路と、
通信の開始時には所定の位相から位相補正を行い、通信中は前記記憶回路に記憶されている前記クロック位相の記憶値を基にクロック補正を行なって出力するクロック再生回路と、
前記クロック再生回路からの出力に同期して前記検波回路からの出力を判定するデータ再生回路とを具えてなることを特徴とする復調回路。
【請求項４】　時分割多重方式で送られて来る複数の送信局からの電波を受信して復調する復調回路において、
時分割された各時間帯毎に受信した信号の検波を行なう検波回路と、
時分割された各時間帯番号毎に前記受信信号のクロック位相を記憶する記憶回路と、
各時間帯番号毎に、通信の開始時には所定の位相から位相補正を行い、通信中は前記記憶回路に記憶された時間帯番号に対応するクロック位相の記憶値を基に位相補正を行なって出力するクロック再生回路と、
前記クロック再生回路からの出力に同期して前記検波回路からの出力を判定するデータ再生回路とを具えてなる復調回路。
【請求項５】　時分割多重方式で送られて来る複数の送信局からの電波を受信して復調する復調方法において、
時分割された各時間帯毎に受信した信号の検波を行ない、
時分割された各時間帯毎に前記受信信号のパラメータを記憶し、
各時間帯毎に通信の開始時には前記パラメータの補正を所定の値から高速で行い、
各時間帯毎に通信中は前記記憶回路に記憶されたパラメータの記憶値を基にパラメータの補正を低速で行い、
前記検波の結果を前記補正されたパラメータに基づいて判定することを特徴とする復調方法。
【請求項６】　時分割多重方式で送られて来る複数の送信局からの電波を受信して復調する復調方法において、
時分割された各時間帯番号毎に受信した信号の検波を行ない、
時分割された各時間帯番号毎に前記受信信号のパラメータを記憶し、
各時間帯番号毎に通信の開始時にはパラメータの補正を所定の値から高速で行い、
通信中は前記記憶回路に記憶された各時間帯番号に対応するパラメータの記憶値を基にパラメータの補正を行ない、
各時間帯番号に対応して前記検波の結果を前記補正されたパラメータに基づいて判定することを特徴とする復調方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、ＴＤＭＡ（Ｔｉｍｅ Ｄｉｖｉｓｉｏｎ Ｍｕｌｔｉｐｌｅ Ａｃｃｅｓｓ；時分割多重）方式で送られて来る複数の送信局からの電波を受信し復調する復調回路及び復調方法に関するものである。
【０００２】
【従来の技術】従来のこの種の復調回路について、π／４シフトＱＰＳＫで変調された図２（ａ）に示すようなＴＤＭＡ信号が受信された場合を例にとり説明する。ここで、π／４シフトＱＰＳＫ変調方式は、「ディジタル移動通信用線形変調方式の提案」、電子通信学会総合全国大会、Ｎｏ２３８４、１９８５年3月２７日～３０日、１０－９７頁に示されるように、入力データの符号列（ＸＫ、ＹＫ）が（１、１）のときはその前のシンボルの位相から－３π／４、（０、１）のときはその前のシンボルの位相から＋３π／４、（０、０）のときは同様に＋π／４、（１、０）のときは同様に－π／４だけ位相変化をする。また、「ディジタルコードレス電話用π／４シフトＱＰＳＫ遅延検波回路」、電子情報通信学会春季大会、Ｎｏ．Ｂ－３４４、１９９２年3月２４日～２７日、２－３４４頁に示されるように、復調構成の

小型化や低消費電力化を実現できるπ／４シフトＱＰＳＫ方式の遅延検波回路も提案されている。以下では、まず、π／４シフトＱＰＳＫ信号を検波するための遅延検波回路について、図３に従って説明する。

【０００３】図３において、入力端子１には、π／４シフトＱＰＳＫで変調された搬送波（変調波）が入力され、この変調波が瞬時位相検出回路３に与えられる。例えば、この変調波周波数１．２ＭＨｚ等の受信機中間周波である。発振器２は、入力端子１に入力された変調波の周波数にほぼ等しい周波数を有するキャリアを発生して瞬時位相検出回路３に与える。瞬時位相検出回路３は、例えばイクスクルーシブオア回路やＤ型フリップフロップ回路等の位相検出回路とアナログローパスフィルタやアナログ／ディジタル変換器等で構成されているものであり、変調波と発振器２のキャリアとの瞬時位相差を表すディジタルデータである瞬時位相データ４を得て位相差分計算回路５に与えるものである。なお、アナログローパスフィルタ及びアナログ／ディジタル変換器部分を、特公平１－３８２４４号公報に開示された移動平均検出装置に置き換えた瞬時位相検出回路３も存在する。位相差分計算回路５は、ベースバンド遅延検波を行なうものであり、入力された瞬時位相データ４と、１シンボル時間だけ遅延された瞬時位相データ４とを減算してディジタルデータ（位相差分信号）６を得て検波を完了する。判定回路として、クロック再生回路７は、検波出力である位相差分信号６に基づいて、タイミングクロック信号を再生するものであり、また、データ再生回路８は、タイミングクロック信号に同期してこの位相差分信号６を処理してデータを判定するものである。再生されたクロック信号及びデータはそれぞれ出力端子９及び１０を介して次段の回路に与えられる。図４は、位相差分信号６をディジタル／アナログ変換した後、オシロスコープに表わしたアイパターンを示すものである。上述したクロック再生回路７は、アイパタンの目の開いたタイミングＴｎでデータ再生回路８がデータ判定ができるように、タイミングクロック信号を再生するものである。

【０００４】

【発明が解決しようとする課題】ＴＤＭＡ通信の場合、各バースト通信は、通信の開始時には、送信・受信間の周波数に差があると、受信符号が誤るので、急速に周波数誤差の補正を行なう必要がある。また、受信側で再生したデータのクロック位相を受信データのクロック位相に急速に合わせないと、同様に受信符号を誤ってしまう。また、各送信局の間で送信周波数にずれがあって、送信されるＴＤＭＡ信号の各時間帯間で、即ち各タイムスロット間で周波数が異なると、受信符号を誤るという問題があった。例えば、図２（ｂ）に示すＴＤＭＡ信号を受信するものとする。図２は縦軸を周波数軸とみなして模式的にＴＤＭＡ信号を表わしたもので、（１）、（２）、（３）、（４）はタイムスロットを示す。図２（ｂ）のタイムスロット（１）の受信に続いてタイムスロット（２）を受信したとき、タイムスロット（２）では、図４に示したアイパタンが全体的に上の方にずれる。このため、図３に示したデータ再生回路８の判定結果が誤ってしまう結果になる。

【０００５】更に、例えばタイムスロット番号（１）と、タイムスロット番号（２）との間の切れ目を図５のように詳細に見てみる。図５においてＲＸＤは、受信されたデータで、図の左側部分はタイムスロット番号（１）、右側部分はタイムスロット番号（２）の部分である。ここで、タイムスロット番号（１）とタイムスロット番号（２）との間には、実際にはガードビットが置かれているが、理解しやすくするために、ここではガードビットを考えない。同図において、ＲＸＣはデータのクロックとして再生されるべきもので、タイムスロット（１）とタイムスロット（２）の切りかわる瞬時には、クロックの位相が急変しているが、図３のクロック再生回路７では、このようなクロック位相の急変に追従することはできない。本発明は、ＴＤＭＡ通信で送られて来る複数の送信局からの電波を誤りなく受信し復調する復調回路及び復調方法を提供する事を目的とする。

【０００６】

【課題を解決するための手段】そこで、本発明は、ＴＤＭＡ方式で送られてくる複数の送信局からの電波を受信して遅延検波する復調回路において、ＴＤＭＡ信号の各タイムスロット番号毎に受信信号のパラメータである周波数の誤差を記憶する回路と前記ＴＤＭＡ信号のタイムスロット番号毎に受信信号の他のパラメータであるクロック位相を記憶する回路を持ち、各タイムスロット番号毎に通信の開始時には、周波数誤差無しの点から高速周波数補正をまた、クロック任意の位相から高速位相補正を行い各タイムスロット番号毎に通信中は各タイムスロットの開始直前に前回と同一タイムスロット番号の最後の周波数誤差と位相を用い、その周波数誤差及び位相から周波数誤差補正及び位相補正を行なう様にしたものである。

【０００７】

【作用】以上のように本発明によれば、各タイムスロット番号毎に受信信号のパラメータ補正を一端高速で行なった後は、各タイムスロット番号毎に記憶回路に記憶された周波数や位相等のパラメータの値を用いてその補正を行なっているので、低速で補正を行なうことができ受信信号を誤りなく復調することができるのである。

【０００８】

【実施例】図１はこの発明の実施例を示す回路図であって、以下図面を用いて説明する。図１に示されるように、変調波入力端子１０１は、瞬時位相検出回路１０３に接続され、入力された変調波を瞬時位相検出回路１０３へ入力する。発振器１０２は、入力端子１０１の変調

波の周波数にほぼ等しい周波数の信号を出力するもので、同様に瞬時位相検出回路１０３に入力される。瞬時位相検出回路１０３の出力１０４は、位相差分計算回路１０５に入力され、その出力１０６は、クロック再生回路１０７及びデータ再生回路１０８に入力される。クロック再生回路１０７の出力は、再生クロック信号出力端子１０９に接続され、再生クロックとして出力されると共にデータ再生回路１０８にも入力される。データ再生回路１０８の第１の出力は、再生データであり、再生データ出力端子１１０に接続される。データ再生回路１０８の第２の出力１１２は、周波数誤差補正値信号で、位相差分信号の縦軸のずれ分をある一定時間Ｔ０内で平均をとったものであり、この信号１１２は、周波数誤差記憶回路１１１内のレジスタ１１３～１１６に接続され、タイムスロット番号にそれぞれ対応して、タイムスロット選択信号１２７で選択された１１３～１１６の内１つのレジスタに、周波数誤差補正制御信号１２８が立ち下がる時に出力されラッチされる。この周波数誤差補正制御信号１２８は’１’のとき周波数誤差補正を行なうものであり、この信号の立上りでタイムスロット選択信号１２７で選択される１１３～１１６の内１つのレジスタの内容をセレクタ１１７を介してデータ再生回路１０８にロードする。データ再生回路１０８は、この周波数誤差補正記憶出力１１８を最初に用い、データ再生を開始し制御信号１２８が’１’の期間中補正値は更新される。通信中は、以上の様に補正値の記憶回路１１１へのセーブ、再生回路１０８へのロードが行なわれるが、通信の開始時には、周波数誤差がまだ解っていないので、急速に周波数誤差の補正を行なう必要がある。その為に周波数誤差高速補正制御信号１２９をデータ再生回路１０８に与える。この制御信号が’１’になるとデータ再生回路１０８は、初期値として周波数誤差０の点から高速誤差補正を開始し、’０’になったところで補正値を用いた低速誤差補正に切り換わる。この高速／低速の違いは、位相差分信号のずれ分をある一定期間中（時間Ｔ０）平均をとったときのＴ０時間の短／長であるが、Ｔ０を短くとると、フィルタ効果（雑音成分が除かれ、実際の誤差値に近くなる。）は小さいが、収束時間は遅くなる。一方、Ｔ０を長くするとフィルタ効果は大きくなるが、収束時間は遅くなる。

【０００９】周波数誤差は自局の発信器と相手方の発信器の周波数誤差であり、ほとんど一定の誤差値で時間と共に大きく変化するものではないため、低速で周波数誤差補正をしたほうがより正確な誤差値を求められ、精度よく復調することができる。尚、これらの制御方法を図６のタイムチャートに示す。図６に示されるように、ＴＤＭＡ信号は、Ｇ、ＰＲ、ＵＷ、Ｄで構成される。Ｇはガードビットであり、隣接する各タイムスロット間で相互に衝突しないよう、各タイムスロット間にガード時間を設けるためのものである。ＰＲはプリアンブルビットであり、通信開始時に信号受信に必要なビット同期確立のための固定パターンである。ＵＷはユニークワードであり、フレーム同期信号でこの固定パターンを検出できたかどうかで同期確立を確認する。Ｄはデータである。タイムスロット選択信号１２７は、各タイムすロットを選ぶための信号で、各タイムスロットの始めと終わりのガードビット期間中に変化させる。周波数誤差補正制御信号１２８は、タイムスロット選択信号１２７が変化した後プリアンブルビットの立ち上がり時に立ち上げ、タイムスロット選択信号１２７が変化する前のデータビットの最終で立ち下げる。周波数誤差高速補正制御信号１２９は、通信の開始時に周波数誤差補正信号１２８と同時に立ち上げ、プリアンブルビット中’１’に設定する。また、通信中には前回のタイムスロットで周波数誤差は既に計算されているため、前回の最終誤差値をタイムスロットの開始時に用いることができ、高速補正を行なう必要はなくなる。

【００１０】次にクロック再生回路１０７の第２の出力１２０は、クロック位相記憶信号であり、この信号１２０は、クロック位相記憶回路１１９内のレジスタ１２１～１２４に接続され、タイムスロット番号にそれぞれ対応して、タイムスロット選択信号１２７で選択された１２１～１２４の内の１つレジスタに、クロック再生制御信号１３０の立ち下がり時出力されラッチされる。このクロック再生制御信号１３０は’１’の時クロック再生を行なうものであり、またこの信号１３０の立上り時にタイムスロット制御１２７で選択される１２１～１２４の内１つのレジスタの内容をセレクタ１２５を通してクロック再生回路１０７にロードする。クロック再生回路１０７は、このクロック位相記憶出力１２６の示す位相からスタートし、クロック再生を行なう。通信中は、以上の様にクロックの位相情報をクロック再生制御信号１３０の立ち下がり、立上りによってクロック位相記憶回路１１９へのセーブ、またはクロック位相記憶回路１１９からのロードを行なうが、通信の開始時には、クロックの位相がまだ解っていないので、急速に位相を合わせる必要がある。その為にクロック高速再生制御信号１３１をクロック再生回路１０７に入力する。この制御信号１３１により通信の開始時には、任意のクロック位相から高速に、クロック再生回路１０７は位相を補正しクロックを再生する。また、この制御信号１３１が’０’になるとクロック再生回路１０７は、低速の位相補正に切り換わる。尚、これらの制御方法を、図６と同様に、図７のタイムチャートに示す。以上のようにこの実施例によれば、ＴＤＭＡの各タイムスロット毎に周波数誤差と受信データのクロック位相を記憶する回路を設け、通信開始時には、周波数誤差なし、及び任意のクロック位相から高速の補正を行い、また、通信中には各タイムスロットの開始時に前回の同一タイムスロットの最終周波数誤差及びクロック位相情報をロードして、低速の補正を

行い、また各タイムスロットの終了時には、最終の周波数誤差及び位相情報を記憶回路にセーブするようにした事により、ＴＤＭＡ通信の受信を精度良く復調する事ができる。

【００１１】

【発明の効果】以上、詳細に説明したように本発明によれば、各タイムスロット番号毎に記憶回路に記憶されたパラメータの値を用いてその補正を行なっているので、低速で補正を行なうことができ受信信号を誤りなく復調することができるのである。

【図面の簡単な説明】

【図１】本発明の実施例を説明するための復調回路図。

【図２】ＴＤＭＡ信号の説明図。

【図３】従来の復調回路図。

【図４】位相差分信号をＤ／Ａ変換したアイパターン図。

【図５】タイムスロット番号間のクロックのタイムチャート。

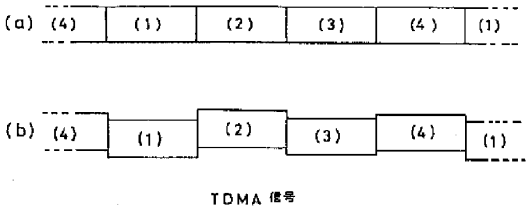
【図６】本発明の実施例を説明するための、制御方法を示すタイムチャート。

【図７】本発明の実施例を説明するための、制御方法を示すタイムチャート。

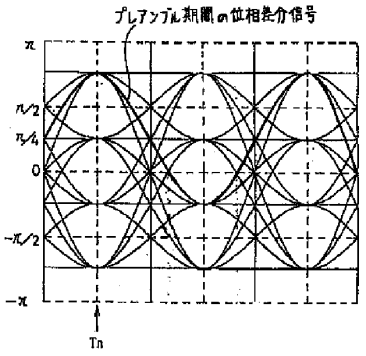
【符号の説明】

１０１	変調波入力端子
１０３	瞬時位相検出回路
１０５	位相差分計算回路
１０７	クロック再生回路
１０８	データ再生回路
１０９	再生クロック信号出力端子
１１０	再生データ出力端子
１１１	周波数誤差補正値記憶回路
１１９	クロック位相記憶回路

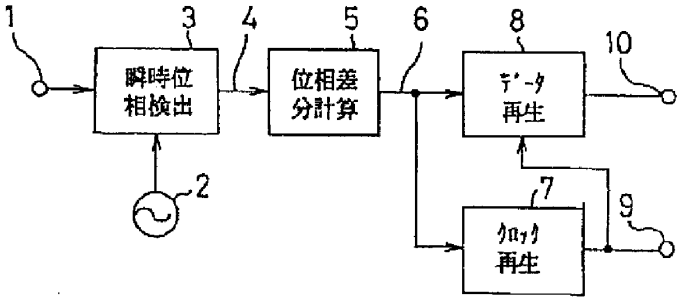
【図２】



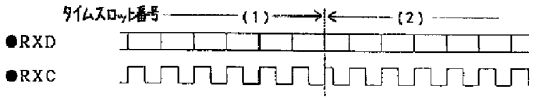
【図４】



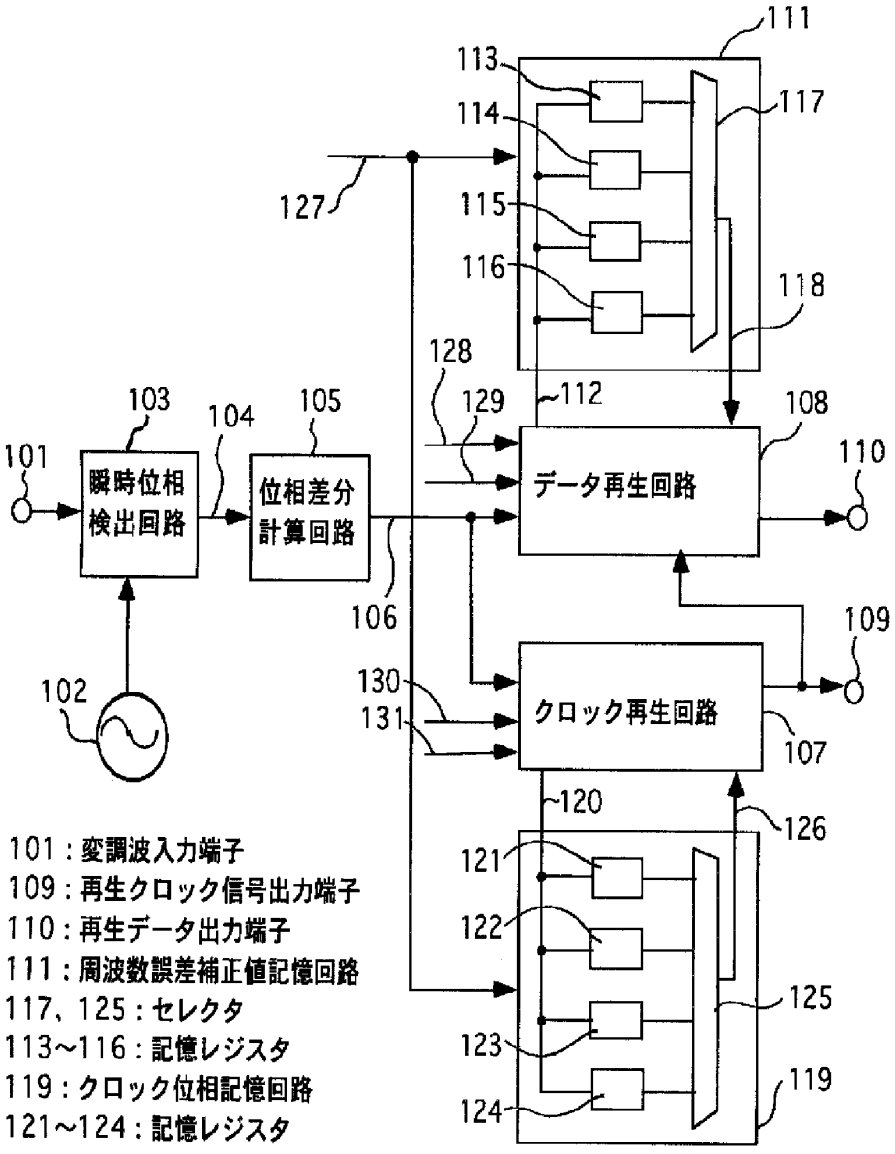
【図３】



【図５】



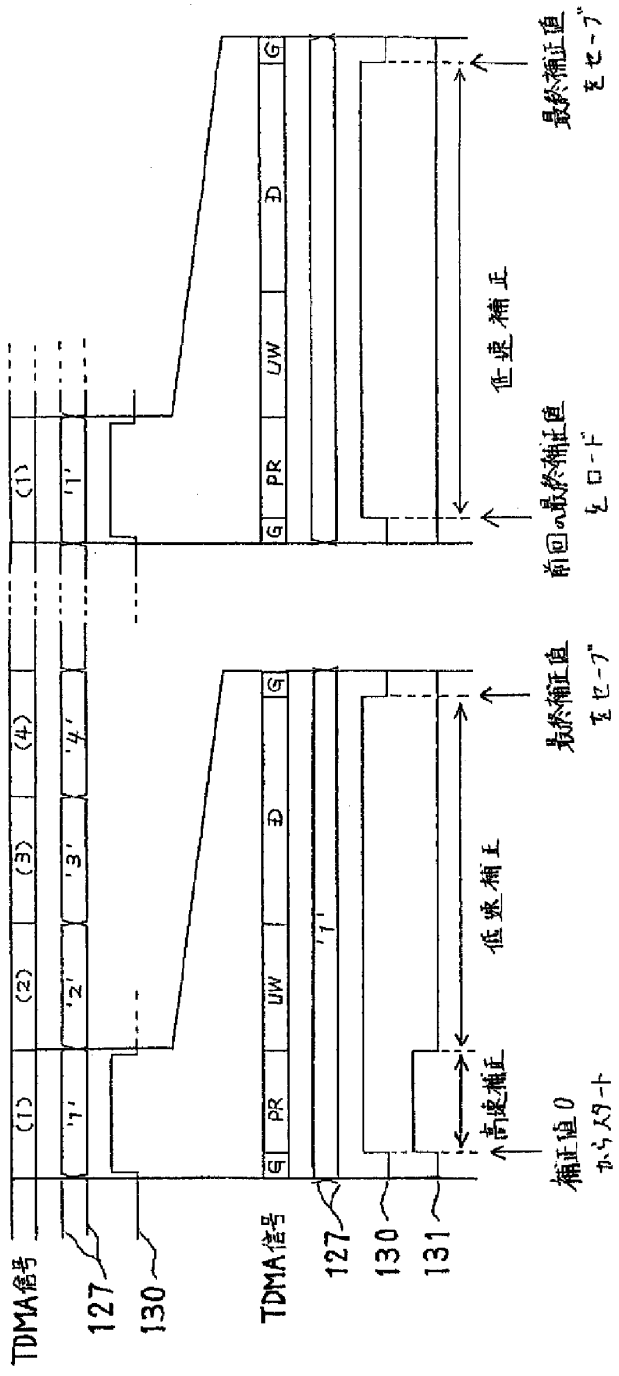
【図1】



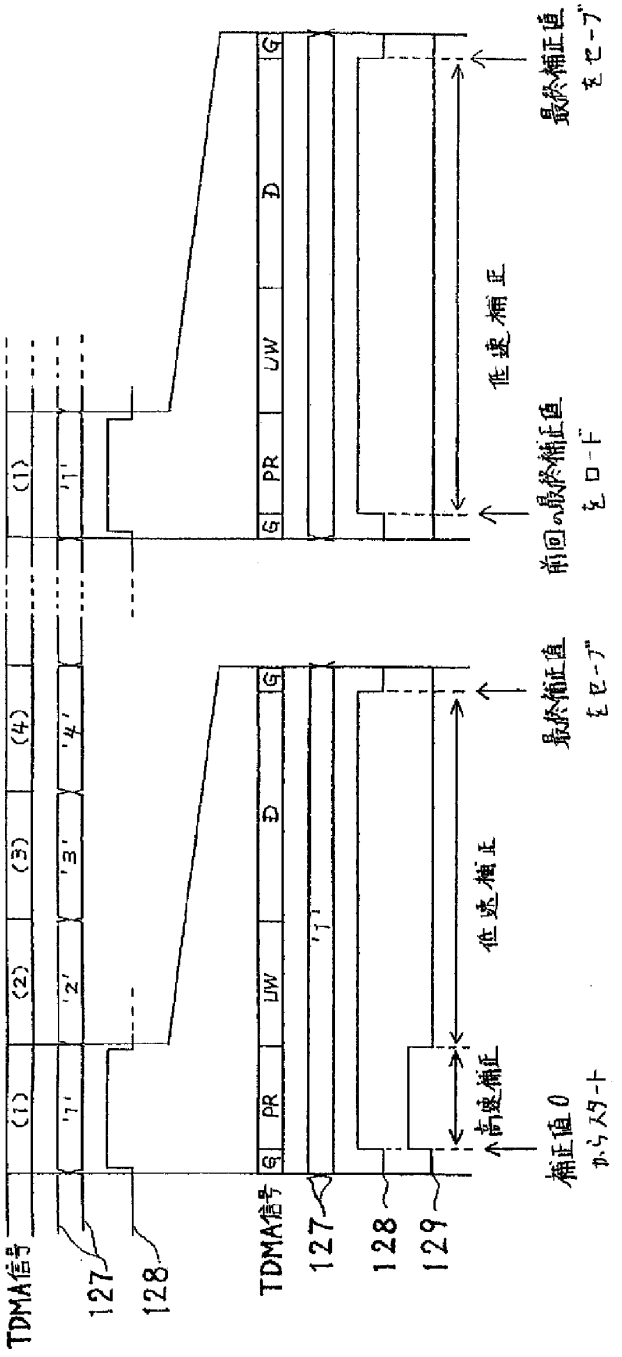
101：変調波入力端子
109：再生クロック信号出力端子
110：再生データ出力端子
111：周波数誤差補正値記憶回路
117、125：セレクタ
113～116：記憶レジスタ
119：クロック位相記憶回路
121～124：記憶レジスタ

発明に係る復調回路図

【図6】


TDMA信号
127
130
TDMA信号
127
130
131
(1)
'1'
(2)
'2'
(3)
'3'
(4)
'4'
G
PR
UW
D
高速補正
低速補正
補正値0
からスタート
最終補正値
セット
前回の最終補正値
セット
低速補正
最終補正値
セット

【図7】


TDMA信号
127
128
TDMA信号
127
128
129
(1)
(2)
(3)
(4)
'1'
'2'
'3'
'4'
G
PR
UW
D
高速補正
位速補正
補正値0
からスタート
最終補正値
セーブ"
前回の最終補正値
ロード"

フロントページの続き

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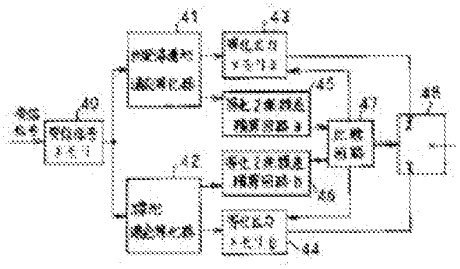
(54) ADAPTIVE EQUALIZER AND ADAPTIVE DIVERISTY EQUALIZER

(57)Abstract:
PURPOSE: To obtain an adaptive equalizer in which operating quantity is not remarkably increased and normalized delay time can be prevented from being deteriorated compared with bit error rate characteristic in one symbol and also, characteristic equal to or larger than that of a conventional equalizer even when Eb/No is small is provided.
CONSTITUTION: This equalizer is equipped with a decision feedback type adaptive equalizer 41 and a linear adaptive equalizer 42 which update the tap coefficient of an equalization filter part according to tap coefficient update algorithm, a comparator 47 which compares a value decided by respective equalized error of each equalizer, and a means 48 which selects either the equalized output of the decision feedback type adaptive equalizer or that of the linear adaptive equalizer, and sets it as the final equalized output. The difference of equalization characteristic of each equalizer is compared, and the output with better equalization characteristic is set as the final equalized output.



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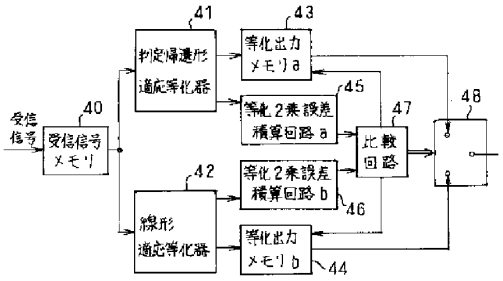
(54)【発明の名称】　適応等化器および適応ダイバーシチ等化器

(57)【要約】　（修正有）

【目的】　演算量が大幅に増えること無く、正規化遅延時間が１シンボルの時のビット誤り率特性にくらべて劣化することなく、また、Ｅｂ／Ｎｏが小さいときにも従来の適応等化器と同等以上の特性を持つ適応等化器を得る。

【構成】　タップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する判定帰還形適応等化器４１及び線形適応等化器４２と、各等化器それぞれの等化誤差より定める値を比較する比較回路４７と、その結果に基づいて、判定帰還形適応等化器の等化出力または、線形適応等化器の等化出力のいずれかを選択し、最終的な等化出力とする手段を備え、各等化器の等化特性の差を比較し、等化特性の良い方の出力を最終的な等化出力とする。



【特許請求の範囲】
【請求項１】　フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する判定帰還形適応等化器部と、
タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する線形適応等化器部と、
上記判定帰還形適応等化器部の等化誤差より定める値と、上記線形適応等化器部の等化誤差より定める値を比較する比較回路と、
上記比較回路の結果に基づいて、上記判定帰還形適応等化器部の等化出力または、上記線形適応等化器部の等化出力のいずれかを選択し、最終的な等化出力とする手段を備えたことを特徴とする適応等化器。
【請求項２】　フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止する判定帰還形適応等化器部と、
タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止する線形適応等化器部と、
上記判定帰還形適応等化器部の等化誤差より定める値と、上記線形適応等化器部の等化誤差より定める値を比較する比較回路と、
上記比較回路の結果に基づいて、上記判定帰還形適応等化器部の等化出力または、上記線形適応等化器の等化出力のいずれかを選択し、最終的な等化出力とするとともに、上記判定帰還形適応等化器部または、上記線形適応等化器部の動作を停止する手段を備えたことを特徴とする適応等化器。
【請求項３】　フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止および再開する判定帰還形適応等化器部と、
タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する線形適応等化器部と、
上記判定帰還形適応等化器部にて、既知信号系列に対応する受信信号を等化する際の等化誤差からしきい値を定めるしきい値設定回路と、
上記線形適応等化器部にて、ランダム信号系列に対応する受信信号を等化する際の等化誤差より定まる値と上記しきい値を比較する第一の比較回路と、
上記線形適応等化器部より定まる値が上記しきい値より少なくとも小さい場合には、線形適応等化器部の等化出力を最終的な等化出力とするとともに、判定帰還形適応等化器部のランダム信号系列に対する等化を停止する手段と、
上記線形適応等化器部より定まる値が上記しきい値より少なくとも大きい場合には、判定帰還形適応等化器部にて既知信号系列以外に対する受信信号の等化を行なう手段と、
上記線形適応等化器部より定まる値が上記しきい値より少なくとも大きい場合には、上記判定帰還形適応等化器部による既知信号系列以外に対する受信信号の等化誤差より定めた値と、上記線形適応等化器部より定まる値を比較する第二の比較回路と、
上記線形適応等化器部より定まる値が上記しきい値より少なくとも大きい場合には、上記第二の比較回路の結果に基づいて、上記判定帰還形適応等化器部の等化出力または、上記線形適応等化器部の等化出力のいずれかを選択し、最終的な等化出力とする手段を備えたことを特徴とする適応等化器。
【請求項４】　フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィル多部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止および再開する判定帰還形適応等化器部と、
タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止および再開する線形適応等化器部と、
上記判定帰還形適応等化器部と上記線形適応等化器部の等化処理を任意のデータで一旦打ち切り、両等化器のタップ係数をリセット、再トレーニングを行なった後に再び等化処理を行なう手段と、
等化処理を一旦打ち切るまでの上記判定帰還形適応等化器部の等化誤差より定める値と、上記線形適応等化器部の等化誤差より定める値を比較する比較回路と、
上記比較回路の結果に基づいて、上記判定帰還形適応等化器部の等化出力または、上記線形適応等化器部の等化出力のいずれかを選択し、最終的な等化出力とする手段と、
上記比較回路の結果に基づいて、上記判定帰還形適応等

化器部の等化出力または、上記線形適応等化器部の等化出力のいずれかを上記再トレーニング時に参照信号とする手段を備えたことを特徴とする適応等化器。

【請求項５】　フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する判定帰還形適応等化器部と、

タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する線形適応等化器部と、

伝送路の多重路伝搬特性を検出する遅延測定回路と、上記遅延測定回路での測定結果に基づいて、上記判定帰還形適応等化器部または、上記線形適応等化器部を動作させる手段を備えたことを特徴とする適応等化器。

【請求項６】　複数のアンテナと、複数の受信波を検波する複数の検波回路と、

検波後の各信号をそれぞれの入力とする、フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する複数の判定帰還形適応等化器部と、

上記検波後の各信号をそれぞれの入力とする、タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する複数の線形適応等化器部と、上記各適応等化器部の等化誤差より定める値を比較する比較回路と、

上記比較回路の結果に基づいて、上記複数の判定帰還形適応等化器部の等化出力または、上記複数の線形適応等化器部の等化出力のうちの一つを選択し、最終的な等化出力とする手段を備えたことを特徴とする適応ダイバーシチ等化器。

【請求項７】　複数のアンテナと、複数の受信波を検波する複数の検波回路と、

検波後の各信号をそれぞれの入力とする、フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止する複数の判定帰還形適応等化器部と、

上記検波後の各信号をそれぞれの入力とする、タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止する複数の線形適応等化器部と、

上記各適応等化器部の等化誤差より定める値を比較する比較回路と、

上記比較回路の結果に基づいて、上記複数の判定帰還形適応等化器部の等化出力または、上記複数の線形適応等化器部の等化出力のうちの一つを選択し、最終的な等化出力とするとともに、選択されなかった判定帰還形適応等化器部または、線形適応等化器部の動作を停止する手段を備えたことを特徴とする適応ダイバーシチ等化器。

【請求項８】　複数のアンテナと、複数の受信波を検波する複数の検波回路と、

検波後の各信号をそれぞれの入力とする、フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止および再開する複数の判定帰還形適応等化器部と、

上記検波後の各信号をそれぞれの入力とする、タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する複数の線形適応等化器部と、上記複数の判定帰還形適応等化器部にて、既知信号系列に対応する受信信号を等化する際の等化誤差からしきい値を定めるしきい値設定回路と、

上記複数の線形適応等化器部にて、ランダム信号系列に対応する受信信号を等化する際の等化誤差より定まる値と上記しきい値を比較する第一の比較回路と、

上記複数の線形適応等化器部より定まる値が上記しきい値より少なくとも小さい場合には、複数の線形適応等化器部の等化出力の中の一つを選択し、最終的な等化出力とするとともに、複数の判定帰還形適応等化器部のランダム信号系列に対する等化を停止する手段と、

上記線形適応等化器部より定まる値が上記しきい値より少なくとも大きい場合には、上記複数の判定帰還形適応等化器部にて、複数の受信信号における既知信号系列以外に対する等化を行なう手段と、

上記線形適応等化器部より定まる値が上記しきい値より少なくとも大きい場合には、上記複数の判定帰還形適応等化器部による既知信号系列以外に対する受信信号の等化誤差より定めた値と、上記複数の線形適応等化器部より定まる値を比較する第二の比較回路と、

上記線形適応等化器部より定まる値が上記しきい値より少なくとも大きい場合には、上記第二の比較回路の結果に基づいて、上記複数の判定帰還形適応等化器部の等化出力および上記複数の線形適応等化器部の等化出力の中

の一つを選択し、最終的な等化出力とする手段を備えたことを特徴とする適応ダイバーシチ等化器。

【請求項９】　複数のアンテナと、複数の受信波を検波する複数の検波回路と、

検波後の各信号をそれぞれの入力とする、フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止および再開する複数の判定帰還形適応等化器部と、

上記検波後の各信号をそれぞれの入力とする、タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新し、また、外部制御信号により動作を停止および再開する複数の線形適応等化器部と、

上記複数の判定帰還形適応等化器部と上記複数の線形適応等化器部の等化処理を任意のデータで一旦打ち切り、全ての等化器のタップ係数をリセット、再トレーニングを行なった後に再び等化処理を行なう手段と、

等化処理を一旦打ち切るまでの上記複数の判定帰還形適応等化器部の等化誤差より定める値と、上記複数の線形適応等化器部の等化誤差より定める値を比較する比較回路と、

上記比較回路の結果に基づいて、上記複数の判定帰還形適応等化器部の等化出力または、上記複数の線形適応等化器部の等化出力の中の一つを選択し、最終的な等化出力とする手段と、

上記選択された等化出力を上記再トレーニング時に参照信号とする手段を備えたことを特徴とする適応ダイバーシチ等化器。

【請求項１０】　複数のアンテナと、複数の受信波を検波する複数の検波回路と、

検波後の各信号をそれぞれの入力とする、フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部とを備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する複数の判定帰還形適応等化器部と、

上記検波後の各信号をそれぞれの入力とする、タップ付き遅延回路を有する等化フィルタ部と、データ判定部と、タップ係数演算部を備え、タップ係数演算部ではタップ係数更新アルゴリズムに従い等化フィルタ部のタップ係数を更新する複数の線形適応等化器部と、検波後の各信号をそれぞれの入力とし、伝送路の多重路伝搬特性を検出する複数の遅延測定回路と、各適応等化器部の等化誤差より定める値を比較する比較回路と、

上記各遅延測定回路の出力結果と比較回路の結果に基づいて、上記複数の判定帰還形適応等化器部の等化出力または、上記複数の線形適応等化器部の等化出力のうちの一つを選択し、最終的な等化出力とする手段を備えたことを特徴とする適応ダイバーシチ等化器。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】高速ディジタル移動体通信では、周波数選択性フェージングによる波形歪が伝送特性に大きな劣化をもたらす。この発明はこの伝送特性の劣化を抑える目的で使用する適応等化器および適応ダイバーシチ等化器に関するものである。

【０００２】

【従来の技術】最初に適応等化器の従来の構成と動作について示す。移動体通信のような伝送路の速い変動に追従し、等化器の初期設定が短時間のトレーニングプロセスで行えるベースバンド波形適応等化器の種類の一つとして、例えば、中嶋、三瓶：“判定帰還形適応等化器による陸上移動通信の周波数選択性フェージング補償特性”，電子情報通信学会論文誌　Ｂ－ＩＩ．Ｖｏｌ．Ｊ７２－Ｂ－ＩＩ．Ｎｏ．１０　ｐｐ．５１３－５２３（１９８９．１０）に記載されているような判定帰還形適応等化器が知られている。また、同等化器における特性の向上、演算量の削減および同等化器を含む受信機の消費電力の低減を目的としたものとして、例えば特開平３－２４４２２０号公報に記載された自動等化器、また、特開平３－２４２０１５号公報に記載された等化器、特開平４－７７０１９号公報に記載されたディジタル通信制御装置などがある。

【０００３】図１５は上記文献に示された判定帰還形適応等化器を示すブロック図である。図において、１はタップ間隔が一定遅延時間Ｔｐ秒でタップ数がＬ個であるフィードフォワード部のトランスバーサルフィルタ（ＦＦ部）、２はタップ間隔が一定遅延時間Ｔ秒でタップ数が（Ｍ－Ｌ）個であるフィードバック部のトランスバーサルフィルタ（ＦＢ部）、３はＦＦ部１の出力データとＦＢ部２の出力データを加算する加算器、４は加算器３の出力信号系列をＴ秒毎に識別し硬判定を行う判定器、５は加算器３の出力と、判定器４の出力信号系列または既知信号系列の差を求める加算器、６はＦＦ部１、ＦＢ部２のタップ係数をＴ秒毎に定めるタップ係数更新回路、７はＦＢ部２の入力信号系列を判定器４の出力信号系列と既知信号系列とに切り替えるスイッチ回路、８は適応等化器の受信信号入力端子、９は参照信号系列入力端子、１０は判定帰還形適応等化器の出力信号端子である。

【０００４】図１６は、移動体通信等に用いられる信号のバーストフォーマットの一例を示す図である。１１は適応等化器のトレーニングや、フレーム同期をとるために用いるユニークワード（以下ＵＷと記す）、１２はラ

ンダムデータ部である。

【０００５】図１７は、特開平３－２４４２２０号公報に示された従来の等化器を示すブロック図である。図において、１３はシンボル間隔自動等化器、１４は分数間隔自動等化器、１５は出力選択スイッチ、１６は出力選択スイッチ１５を制御するスイッチ制御部である。

【０００６】図１８は、特開平３－２４２０１５号公報に示された従来の等化器を示すブロック図である。図において、１７はＩチャネルおよびＱチャネルの受信ベースバンド信号を記憶する受信信号メモリ、１８は受信信号メモリ１７よりＵＷ１１やランダムデータ１２に対応する受信信号を読み出し、等化処理を行う等化処理部、１９は所定量の等化出力信号を蓄積し、受信データとして出力する等化出力メモリ、２０は受信信号メモリ１７、等化処理部１８、等化出力メモリ１９を制御する制御部である。

【０００７】図２０は、特開平４－７７０１９号公報に示された等化器を含むディジタル通信制御装置を示すブロック図である。図において、２１は受信信号であるＳＩを信号Ｓ１、信号Ｓ２に分配する入力信号分配器、２２は入力信号分配器２１より出力される第１の信号Ｓ１をＵＷ１１期間より長い時間だけ遅延される遅延器、２３は適応自動等化器、２４は遅延器２２の出力と適応自動等化器２３との間の接続、切断を行う切り換えスイッチＳＷａ、２５は遅延検波器、２６は遅延検波器２５から出力される復調データのうち、UWを含まないデータを適応自動等化器２３で等化処理に要する時間だけ遅延させる事が可能な遅延器、２７は遅延検波器２５によって復調されたUWを既知のUWと比較することでUW期間に存在する符号誤り率を数える符号誤り率測定器、２８は遅延器２２、切り換えスイッチＳＷａ２４、適応自動等化器２３、で構成される第１の復調器、２９は遅延検波器２５、遅延器２６で構成される第２の復調器、３０は符号誤り率測定器２７から出力される制御信号に基いて第１の復調器２８と第２の復調器２９の出力を切り替える切り換えスイッチＳＷｂである。

【０００８】次に、従来の等化器の動作について説明する。図１５に示した判定帰還形適応等化器では、復調器によりベースバンドに変換された受信信号に対して、各バースト先頭の図１６に示したＵＷ１１を用いて伝送路の特性を推定しタップ係数を収束させる。（トレーニングモード）。このとき、ＦＢ部２の入力信号系列および加算器５の入力信号系列は判定誤りのないデータとしＵＷ１１の既知信号系列より定めた参照信号系列である。次いでランダムデータ部１２について等化を行なう（トラッキングモード）。このとき、判定器４では、加算器３の出力信号系列をＴ秒毎に識別し硬判定を行い、ＦＢ部２の入力信号系列および加算器５の入力信号系列は、判定器４の出力信号系列となる。

【０００９】タップ係数更新回路６では、判定帰還形適応等化器の入力信号系列と、ＵＷ１１の既知信号系列より定まる参照信号系列または判定器４の出力信号系列より定められた加算器５の出力信号系列を用い、カルマンフィルタアルゴリズム（ＲＬＳアルゴリズム）等のタップ係数更新アルゴリズムに従い、１シンボル毎にＦＦ部１、ＦＢ部２のタップ係数を更新する。

【００１０】上記タップ係数更新アルゴリズムについて、カルマンフィルタアルゴリズム（ＲＬＳアルゴリズム）の例を取り、簡単に説明する。時刻ｔ＝ｎＴ（ｎ＝０，１，２，・・・・）における等化器への入力信号ベクトルをX_M（ｎ）、タップ係数をC_M（ｎ）、等化器出力をＩ（ｎ）、希望出力をｄ（ｎ）、誤差信号をｅ（ｎ）とする。ここでX_M（ｎ）、C_M（ｎ）、Ｉ（ｎ）、ｄ（ｎ）は、同相、直交チャネルを示す複素数となる。また、判定帰還形適応等化器のＦＦ部１のタップ数をＬ、総タップ数をＭとするとこれらの関係は次式となる。

【００１１】

【数１】

$$X_M(n) = [y_1^*(n),\ y_2^*(n),\ \cdots,\ y_L^*(n),\ d_1^*(n),\ d_2^*(n),\ \cdots,\ d_{M-L}^*(n)]^* \quad (1)$$

$$C_M(n) = [C_1^*(n),\ C_2^*(n),\ \cdots,\ C_M^*(n)] \quad (2)$$

$$I(n) = C_M^*(n-1)\ X_M(n) \quad (3)$$

$$e(n/n-1) = d(n) - I(n) = d(n) - C_M^*(n-1)\ X_M(n) \quad (4)$$

【００１２】ここで＊は、複素共役転置行列（又は、ベクトル）を表わす。ｙ（ｎ）は、ＦＦ部の受信入力信号、ｄ（ｎ）は、ＦＢ部入力信号であり、トレーニングモードでは、既知信号系列トラッキングモードでは、判定器４にて式３の結果を硬判定した出力信号系列となる。また、誤差信号ｅ（ｎ）は、加算器５の出力である。そして、次式で表される評価関数εを最小にするタップ係数C_M（ｎ）が求める値となる。

【0013】　【数2】

$$\varepsilon = \sum_{i=1}^{n} \lambda^{n-i}\ e^{*}(i/n)\ e(i/n) \qquad (5)$$

【0014】ここでλは忘却係数（0＜λ≦1）を表す。式5を最小にするC_M（n）は以下となる。　【0015】

【数3】

$$C_M(n) = R^{-1}(n)\ D(n) \qquad (6)$$

$$P^{-1}(n) = R(n) = \sum_{i=1}^{n} \lambda^{n-i}\ X_M(i)\ X_M^{*}(i) + \delta \lambda^{n}\ I$$

$$\delta：正定数 \qquad (7)$$

$$D(n) = \sum_{i=1}^{n} \lambda^{n-i}\ X_M(i)\ d^{*}(i) \qquad (8)$$

【0016】さらに、時刻t＝（n－1）Tの時のC_M（n－1）、P（n－1）から、時刻t＝nTの時のC_M（n）を漸化的に求めるアルゴリズムは、以下のようになる。　【0017】

【数4】

$$K(n) = P(n-1)\ X_M(n) \Big/ [\lambda + X_M^{*}(n)\ P(n-1)\ X_M(n)] \qquad (9)$$

$$P(n) = P(n-1) - K(n)\ X_M^{*}(n)\ P(n-1) \qquad (10)$$

$$C_M(n) = C_M(n-1) + K(n)\ e^{*}(n/n-1) \qquad (11)$$

$$P(0) = \delta^{-1} I,\ C_M(0) = 0 \qquad (12)$$

【0018】ここで、K（n）はカルマンゲイン、P（n）は、タップ係数の推定誤差共分散行列、Iは単位行列である。なお、このタップ係数更新アルゴリズムについては、S・ヘイキン著、武部幹訳：“適応フィルタ入門”，第5章，現代工学社（1987），またはJ．G．PROAKIS：“DIGITAL COMMUNICATION”，6．8章，McGRAW－HILL（1983）に詳しく示されている。

【0019】図17に示した等化器の動作について説明する。ここで、シンボル間隔自動等化器13は図15に示した判定帰還形適応等化器において、FF部のタップ間隔を1シンボル、すなわちT秒としたもの、分数間隔自動等化器14もまた、図15に示した判定帰還形適応等化器において、FF部のタップ間隔を（M／N）シンボルすなわち（M／N）T秒（M、Nは整数、M＜N）としたものである。また、このシンボル間隔自動等化器13と分数間隔自動等化器14は両方とも判定帰還部のない線形等化器の場合もある。まず、受信信号はシンボル間隔自動等化器13と分数間隔自動等化器14の両方に供給される。シンボル間隔自動等化器13および分数間隔自動等化器14の出力は、出力選択スイッチ15によって選択され出力されるものである。スイッチ制御部16は、例えば受信局が送信局の遠方にある場合のようにマルチパス遅延時間が大きい場合、すなわち直接波と遅延波の時間差が大きい場合には、シンボル間隔自動等化器13の出力を選択するように出力選択スイッチ15を設定し、例えば、受信局が送信局の近郊にある場合のように、マルチパス遅延時間が小さい場合には分数間隔自動等化器14の出力を選択するように出力選択スイッチ15を制御するものである。この出力選択スイッチ15の切り替え制御の具体的方法としては、例えば、図15の判定帰還形適応等化器における加算器3の出力のアイパターンの開きを、シンボル間隔自動等化器13と分数間隔自動等化器14とで調べ、開きが大きい方を選択する方法、また、両等化器のアイパターンの分散をしらべ分散が小さい方を選択する方法、また、両等化器の出力に対して誤り訂正を行う手段を設け、その訂正の程度を比較することにより出力選択スイッチ15の切り替え

制御を行う方法等が特開平３－２４４２２０号公報に記載されている。

【００２０】図１８に示した等化器の動作について図１９を参照して説明する。等化処理部１８は、ＵＷ１１に対する処理で設定したタップ係数に基づきランダムデータ１２についての等化処理を行うが、１バースト信号の途中で等化処理を一旦打ち切る。制御部２０は等化処理されて等化出力メモリ１９に記憶された信号系列を正しいものと仮定し、この信号系列を再トレーニングのための既知信号系列とみなして等化処理部に再トレーニングを行わせる。すなわち、受信信号メモリ１７の読み出しポインタをそのトレーニング系列の長さだけ前に戻し、等化処理部１８は等化出力メモリ１９から読み出した既知信号系列を基に、受信信号メモリ１７から読み出されたランダムデータの一部を用いて再トレーニングを行う。なお、この再トレーニングでは等化処理部１８はリセットされるが、すでに設定されているタップ係数については初期状態に戻さず、等化処理を打ち切る直前の状態を保持することにより、再トレーニングにより設定されるタップ係数を高速に収束させることが可能となる。また、１バースト信号の途中で等化処理を一旦打ち切るタイミングは、ＵＷの長さ、要求される信号処理速度および追従特性との関係に基づいて決定される。以下同様に、１バースト信号の最後まで再トレーニング操作を繰り返す。したがって、従来では１バースト信号の最初だけ等化器をリセットしトレーニング処理を行っていたが、ランダムデータの等化処理の過程においても周期的リセットし、タップ係数の再設定を行うことにより追従特性を高めることができる。

【００２１】図２０に示したディジタル通信制御装置の動作について説明する。ベースバンドの入力信号ＳＩは、既にディジタル信号化されていて、入力信号分配器２１によって２つの同様な内容を持った信号に分配される。ここで２つの分配された信号をそれぞれＳ１，Ｓ２とする。第１の信号Ｓ１は遅延器２２に入力され、第２の信号Ｓ２は遅延検波器２５に入力される。遅延検波器２５では、遅延検波復調方式を用い、復調する信号に対し、１シンボル前の信号を基準位相信号とし、例えば、前の信号との位相差がπ／２以下であれば“０”、位相差がπ／２以上異なれば“１”を出力する等の動作を行い、バーストの先頭に位置するＵＷ１１に対応する受信信号から順次復調する。一方、遅延検波器２５から出力される信号のうちＵＷ１１だけが符号誤り率測定器２７に入力され符号誤り率が測定される共に、遅延検波器２５から出力された信号のうちＵＷ信号を除くデータが遅延器２６に入力される。遅延器２２に入力された第１の信号Ｓ１は、第２の復調器２９の遅延検波器２５で当該信号のＵＷ１１が復調され、さらに符号誤り率測定が終了するまでに要するだけの時間遅延され、符号誤り率測定器２７で任意のしきい値によって決定されているフラグによって制御される切り換えスイッチＳＷａ２４を介して適応自動等化器２３に入力される。ここでフラグが立たない時は、常に信号Ｓ１は、適応自動等化器２３に入力されることなく、また適応自動等化器２３も、またその動作を停止している。また、遅延器２６に入力された遅延検波器２５からのＵＷを除く信号は、遅延器２２から出力された信号が切り換えスイッチＳＷａ２４を通過して適応自動等化器２３に入力し等化処理が終了するまでの時間だけ遅延される。以上の結果、同じ内容の信号を復調した信号が、同じ時刻に第１の復調器２８の出力端と第２の復調器２９の出力端に現れることになり、とちらかの復調結果がフラグによって制御されるスイッチＳＷｂ３０を介して択一的に出力される。

【００２２】このように、適応自動等化器を有しない復調器によって復調されたトレーニング信号を監視することにより、マルチパスの状態を把握し、適応自動等化器を有する復調器にバースト単位で切り替えることが可能となる。その結果、受信側での情報の信頼性（通話品質など）を悪化させずに通信が可能となる。また、消費電力の非常に大きな自動等化器の動作を制御することが可能となった結果、復調器での消費電力が激減でき、移動体などに搭載・携帯される電話などの限られた電源容量を有効に使用することが可能となる。

【００２３】次に従来の適応ダイバーシチ等化器について示す。等化器とダイバーシチを組み合わせた適応ダイバーシチ等化器の一つとして、例えば、東、鈴木：“移動無線における適応等化後選択ダイバーシチの平均ＢＥＲ特性”，１９９０年電子情報通信学会秋季全国大会Ｂ－２７９（１９９０．９）に記載されているようなものが知られている。

【００２４】図２１は上記文献に示された適応ダイバーシチ等化器を示すブロック図である。図において、１０１はアンテナａ、１０２はアンテナｂ、１０３はアンテナａ１０１より出力される受信信号を検波しベースバンド信号に変換する検波回路ａ、１０４はアンテナｂ１０２より出力される受信信号を検波しベースバンド信号に変換する検波回路ｂ、１０５は検波回路ａ１０３の出力を等化する判定帰還形適応等化器ａ、１０６は検波回路ｂ１０４の出力を等化する判定帰還形適応等化器ｂ、１０７は判定帰還形適応等化器ａ、および判定帰還形適応等化器ｂの等化誤差を比較する比較回路、１０８は比較回路１０７の出力信号に従い、判定帰還形適応等化器ａの出力または判定帰還形適応等化器ｂの出力を選択し最終的な等化出力結果とする選択回路である。

【００２５】次に従来の適応ダイバーシチ等化器の動作について説明する。図２１に示した適応ダイバーシチ等化器では、アンテナａ１０１、およびアンテナｂ１０２より出力される受信信号はそれぞれ検波回路ａ１０３および検波回路ｂ１０４によりベースバンド信号に変換され、検波回路ａ１０３の出力信号は判定帰還形適応等化

器ａ１０５の入力信号、また、検波回路ｂ１０４の出力信号は判定帰還形適応等化器ｂ１０６の入力信号となる。判定帰還形適応等化器ａ１０５および判定帰還形適応等化器ｂ１０６では、図１５に示す等化器の動作の項で示したように各バースト先頭の図１６に示したＵＷ１１を用いて伝送路の特性を推定しタップ係数を収束させる。次いでランダムデータ部１２について等化を行うとともに等化誤差の平均値を算出し、その結果を比較回路１０７に出力する。比較回路１０７では判定帰還形適応等化器ａ１０５の等化誤差の平均値および判定帰還形適応等化器ｂ１０６の等化誤差の平均値を比較し等化誤差の平均値が小さい方の出力を選択する信号を選択回路１０８に出力する。選択回路１０８では、比較回路１０７の出力に従い、判定帰還形適応等化器ａ１０５または判定帰還形適応等化器ｂ１０６の出力を最終的な等化出力として出力する。

【００２６】

【発明が解決しようとする課題】従来の適応等化器は以上のような構成になっているために、以下に記すような課題があった。

【００２７】周波数選択性フェージング下において、遅延波の正規化遅延時間が１シンボルより小さい場合には、遅延波による符号間干渉は、数シンボルに渡るが、ＦＢ部のタップ数が少ないため、遅延波の正規化遅延時間が１シンボルの時のビット誤り率特性にくらべて大幅に劣化するという問題点があった。また、これを改善するためにＦＢ部のタップ数を多くすると、等化器のタップ数が増えるため、演算量が増えると共に今度は、伝送路への追従性が悪くなりビット誤り率特性が劣化するという課題があった。

【００２８】図２２は、図１７に示した従来の等化器の正規化遅延時間に対するビット誤り率特性の１例である。この図で示すようにシンボル間隔自動等化器および分数間隔自動等化器のビット誤り率は、遅延波の正規化遅延時間が１シンボルより小さい場合には、遅延波の正規化遅延時間が１シンボルの時のビット誤り率特性にくらべて大幅に劣化する。

【００２９】図２３は、図２０に示した従来のディジタル通信制御装置の、遅延波の正規化遅延時間に対するビット誤り率特性の１例である。この図より、このディジタル通信制御装置では先に述べたように遅延検波器と等化器の出力を切り替えることによって、遅延波の正規化遅延時間が１シンボルより小さい場合の特性が改善されることがわかる。しかし、逆に遅延波の正規化遅延時間が、０．２シンボルより大きいときには、この装置全体のビット誤り率特性は、等化器単体のビット誤り率より劣化するという課題があった。また、遅延検波器のＵＷ部分の誤り率を測定し、等化器を作動させるかどうかを決定するため、Ｅｂ／Ｎｏ（１ビット当たりの信号電力対雑音密度比）が小さい場合には、遅延波が無い場合でも、雑音によって遅延検波器のＵＷ部分の誤り率が劣化し、常に等化器が作動するという課題があった。

【００３０】また、数＋ｋｂｐｓ以上の高速ディジタル移動体通信では、先に述べたカルマンフィルタを適応アルゴリズムを用いても十分な追従特性が得られないことがある。そこで、高速な伝送路の変動に対する追従性を高め、ビット誤り率を改善するものとして、従来例でのべた図１８に示された等化器等が考案されている。しかし、図２４に示す同等化器の誤り率特性の例のようにＥｂ／Ｎｏ（信号対雑音電力比）が小さい場合にはビット誤り率が劣化するという課題があった。

【００３１】この発明は、かかる課題を解決するためになされたもので、演算量が大幅に増えること無く、遅延波の正規化遅延時間が１シンボルより小さい場合や、遅延波が無い場合でも、正規化遅延時間が１シンボルの時のビット誤り率特性にくらべて劣化することなく、また、Ｅｂ／Ｎｏが小さいときにも従来の適応等化器と同等以上の特性を持つ適応等化器を得ることを目的としている。また、遅延波が無い場合や遅延波の正規化遅延時間が小さい場合に、従来の適応等化器より演算量が低減する適応等化器を得ることを目的としてる。

【００３２】また、従来の適応ダイバーシチ等化器は以上のような構成になっているために、従来の適応等化器と同様に以下に記すような課題があった。

【００３３】周波数選択性フェージング下において、遅延波の正規化遅延時間が１シンボルより小さい場合には、遅延波による符号間干渉は、数シンボルに渡るが、ＦＢ部のタップ数が少ないため、遅延波の正規化遅延時間が１シンボルの時のビット誤り率特性にくらべて大幅に劣化するという問題点があった。また、これを改善するためにＦＢ部のタップ数を多くすると、等化器のタップ数が増えるため、演算量が増えると共に今度は、伝送路への追従性が悪くなりビット誤り率特性が劣化するという課題があった。

【００３４】この発明は、かかる課題を解決するためになされたもので、演算量が大幅に増えること無く、遅延波の正規化遅延時間が１シンボルより小さい場合や、遅延波が無い場合でも、正規化遅延時間が１シンボルの時のビット誤り率特性にくらべて劣化することなく、また、Ｅｂ／Ｎｏが小さいときにも従来の適応ダイバーシチ等化器と同等以上の特性を持つ適応ダイバーシチ等化器を得ることを目的としている。また、遅延波が無い場合や遅延波の正規化遅延時間が小さい場合に、従来の適応ダイバーシチ等化器より演算量が低減するダイバーシチ等化器を得ることを目的としている。

【００３５】

【課題を解決するための手段】上記の目的を達成するために、請求項１に係わる発明の適応等化器は、フィードフォワード部（ＦＦ部）とフィードバック部（ＦＢ部）にタップ付き遅延回路を有する等化フィルタ部と、デー