LXT914

Flexible Quad Ethernet Repeater

General Description

The LXT914 is an integrated multi-port repeater designed for mixed-media networks. It provides all the active circuitry required for the repeater function in a single CMOS device. It includes one Attachment Unit Interface (AUI) port and four 10BASE-T transceivers. The AUI port is mode selectable: DTE mode allows connection of an external transceiver (10BASE2, 10BASE5, 10BASE-T or FOIRL) or a drop cable. MAU mode creates a MAU output allowing direct connection to another DTE interface. The 10BASE-T transceivers are entirely self-contained with internal filters which simplify the design work required for FCC-compliant EMI performance.

An inter-repeater backplane interface allows 128 or more 10BASE-T ports to be cascaded together. In addition, a serial port provides information for network management.

The LXT914 requires only a single 5-volt power supply due to an advanced CMOS fabrication process.

Applications

- · LAN Repeaters
- · Integrated Repeaters
- Switched Repeater Clusters

Features

- Four integrated 10BASE-T transceivers and one AUI transceiver on a single chip
- Programmable DTE/MAU interface on AUI port
- Seven integrated LED drivers with four unique operational modes
- · On-chip transmit and receive filtering
- Automatic partitioning of faulty ports, enabled on an individual port basis
- Automatic polarity detection and correction
- Programmable squelch level allows extended range in low-noise environments
- Synchronous or asynchronous inter-repeater backplane supports "hot swapping"
- Inter-repeater backplane allows cascaded repeaters, linking 128 or more 10BASE-T ports
- Serial port for selecting programmable options
- 68-pin PLCC (Commercial or Extended temp range)
- 100-pin PQFP (Commercial temp range)

LXT914 Block Diagram

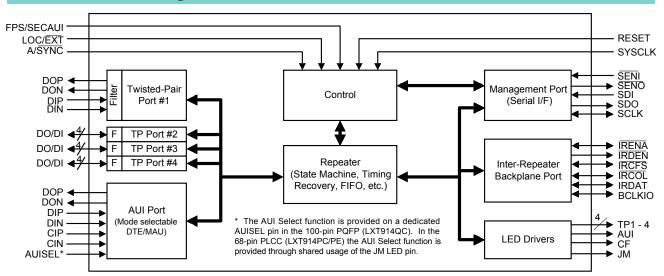




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LXT914 PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT914 Pin Assignments

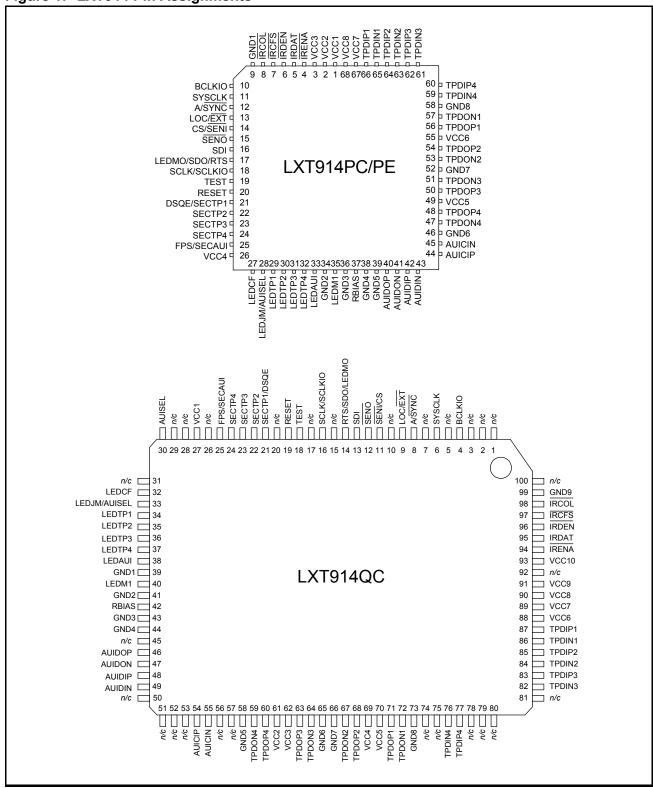




Table 1: LXT914 Power, Ground and Clock Signal Descriptions

		. 51151, 5	. 54110	and Clock Signal Descriptions
Pir	า #	Symbol	I/O	Description
PLCC	PQFP	Cymbol	"0	Description
1	27	VCC1		Power Supply Inputs. These pins each require a +5 VDC power supply. The
2	61	VCC2		various pins may be supplied from a single power source, but special de-cou-
3	62	VCC3		pling requirements may apply. Each VCC input must be within ±0.3 V of every other VCC input.
26	69	VCC4	_	omer vee input.
49	70	VCC5	_	
55	88	VCC6	_	
67	89	VCC7	_	
68	90	VCC8		
	91	VCC9	_	
	93	VCC10		
9	39	GND1	_	Ground. These pins provide ground return paths for the various power supply
34	41	GND2	_	pins.
36	43	GND3		
38	44	GND4		
39	58	GND5		
46	65	GND6		
52	66	GND7		
58	73	GND8		
_	99	GND9	_	
37	42	RBIAS	_	Bias. This pin provides bias current for the internal circuitry. The 100 μA bias current is provided through an external 12.4 $k\Omega$ resistor to ground.
10	4	BCLKIO	I/O	Backplane Clock. This 10 MHz clock synchronizes multiple repeaters on a common backplane. In the synchronous mode, BCLKIO must be supplied to all repeaters from a common external source. In the asynchronous mode, BCLKIO is supplied only when a repeater is outputting data to the bus. Each repeater outputs its internally recovered clock when it takes control of the bus. Other repeaters on the backplane then sync to BCLKIO for the duration of the transmission.
11	6	SYSCLK	I	System Clock. The required 20 MHz system clock is input at this pin. Clock must have a 40-60 duty cycle with < 10 ns rise time.

Table 2: LXT914 Inter-Repeater Backplane Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
4	94	IRENA	I/O	Inter-Repeater Backplane Enable. This pin allows individual LXT914 repeaters to take control of the Inter-Repeater Backplane (IRB) data bus (IRDAT). The $\overline{\text{IRENA}}$ bus must be pulled up locally by a 330 Ω resistor.
5	95	IRDAT	I/O	IRB Data. This pin is used to pass data between multiple repeaters on the IRB. The IRDAT bus must be pulled up locally by a 330 Ω resistor. ¹
6	96	IRDEN	О	IRB Driver Enable. The IRDEN pin is used to enable external bus drivers which may be required in synchronous systems with large backplanes. This is an active Low signal, maintained for the duration of the data transmission. IRDEN must be pulled up locally by a 330 Ω resistor.
7	97	<u>IRCFS</u>	I/O	IRB Collision Flag Sense (IRCFS) and IRB Collision (IRCOL). These two pins
8	98	IRCOL	I/O	are used for collision signalling between multiple LXT914 devices on the Inter-Repeater Backplane (IRB). Both the \overline{IRCFS} bus and the \overline{IRCOL} bus must be pulled up globally with 330 Ω resistors. (IRCFS requires a precision resistor [±1%].) ²

^{1.} $\overline{\text{IRENA}}$ and $\overline{\text{IRDAT}}$ can be buffered between boards in multi-board configurations. Where buffering is used, a 330 Ω pull-up resistor can be used on each signal, on each board. Where no buffering is used, the total impedance should be no less than 330 Ω

Table 3: LXT914 Mode Select and Control Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
12	8	A/SYNC	I	Backplane Sync Mode Select. This pin selects the backplane sync mode. When this pin is left floating an internal pull-up defaults to the Asynchronous mode (A/SYNC High). In the asynchronous mode 12 or more LXT914s can be connected on the backplane, and an external 10 MHz backplane clock source is not required. When the synchronous mode is selected (A/SYNC tied Low), 32 or more LXT914s can be connected to the backplane and an external 10 MHz backplane clock source is required.
13	9	LOC/EXT	I	Management Mode Select. This pin selects the management mode. When this pin is left floating, an internal pull-up defaults to the Local management mode (LOC/EXT High). In the Local mode, setup parameters are downloaded from an EEPROM during initialization. Once initialized with the setup parameters, the repeater functions independently.
28	33	LEDJM/ AUISEL	I/O	LED Driver or DTE/MAU Select. At reset, this pin selects the mode of the AUI port. If left floating, an internal pull-down device forces the AUI port to DTE mode. If pulled High with an external resistor, the port changes to a MAU, in which case the functions of the LEDJM pin are disabled and the default LED mode (Refer to Table 7) is not available.
_	30	AUISEL	I	DTE/MAU Select. This pin changes the mode of the AUI port independent of the condition at reset. This function is available only in the 100-pin PQFP package.
17 35	14 40	LEDM0 LEDM1	I/O I/O	LED Mode 0 & 1 Select. These two pins select one of four possible LED modes of operation. The Functional Description section describes the four modes.



^{2.} IRCFS and IRCOL cannot be buffered. In multi-board configurations, the total impedance on IRCOL should be no smaller than 330 Ω IRCFS should be pulled up only once, by a single 330 Ω , 1% resistor.

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