



# Technical Feasibility Sending Common Mode Power on the Signal Pa

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# Presentation Overview

**Two parts**

**Part 1 - High Level Overview**

**No Questions please**

**Part 2 - Technical Detail**

**250 hrs of investigation**

**90 Slides**

**Questions OK**

# Criteria for Technical feasibility

- 1. Signal Integrity, 10 Mbps**
  - 2. Signal Integrity, 100 Mbps**
  - 3. Effects on Magnetics**
  - 4. Operational characteristics**
- Isolation is important but common to all solutions – will not be addressed here**

# Criteria 1 - details

- **Signal Integrity, 100 Mbit/s**

**Differential Signal 0-Pk**

**Amplitude Symmetry**

**Rise/Fall Time**

**Duty Cycle Distortion**

**Transmit Jitter**

**Overshoot**

**Differential Input Impedance**

**Common Mode Rejection**

# Criteria 2 - details

- **Signal Integrity, 10 Mbit/s**

Peak Differential Output Voltage on TD(Transmit Data)

Harmonic Content, All Ones

Output Waveform vs Template

Start of TP\_IDL(End of 10Base-T Packet) waveform vs Template

Link Test Pulse vs Template

TD circuit Differential Output Impedance

Transmitter added Jitter

TD common mode output voltage

TD common mode rejection

RD(Received Data) Signal Acceptance

Receiver Jitter Acceptance

Receiver Added Jitter

RD Differential Input Impedance

RD Common Mode Rejection

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