

**(12) United States Patent**  
**Aoi**

**(10) Patent No.: US 6,287,973 B2**  
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**(54) METHOD FOR FORMING INTERCONNECTION STRUCTURE**

**(75) Inventor: Nobuo Aoi, Hyogo (JP)**

**(73) Assignee: Matsushita Electric Industrial Co., Ltd., Osaka (JP)**

**(\*) Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

**(21) Appl. No.: 09/756,242**

**(22) Filed: Jan. 9, 2001**

**Related U.S. Application Data**

**(63)** Continuation of application No. 09/274,114, filed on Mar. 23, 1999, now Pat. No. 6,197,696.

**(30) Foreign Application Priority Data**

- Mar. 26, 1998 (JP) ..... 10-079371
- (51) Int. Cl.<sup>7</sup>** ..... **H01L 21/311; H01L 21/3065**
- (52) U.S. Cl.** ..... **438/700; 438/706; 438/723; 438/725**
- (58) Field of Search** ..... **438/700, 706, 438/723, 725**

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**(57) ABSTRACT**

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film is masked with the third insulating film and dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films are masked with the mask pattern and the second insulating film, respectively, and dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.

**8 Claims, 37 Drawing Sheets**

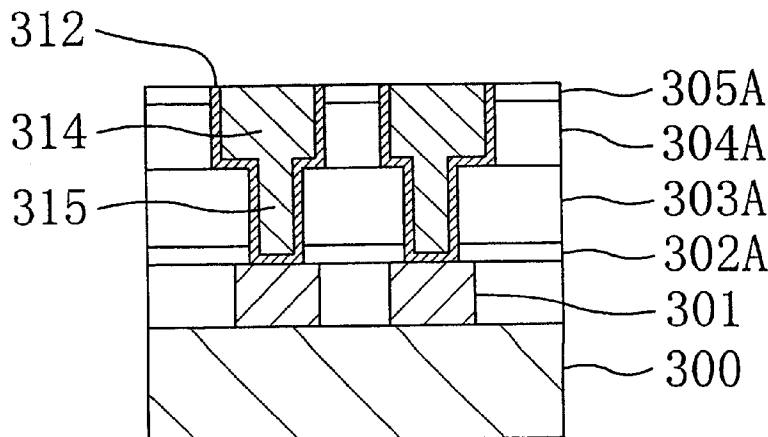


Fig. 1 (a)

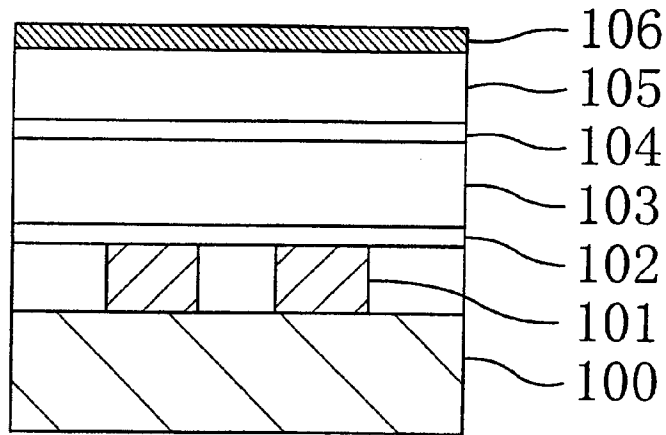


Fig. 1 (b)

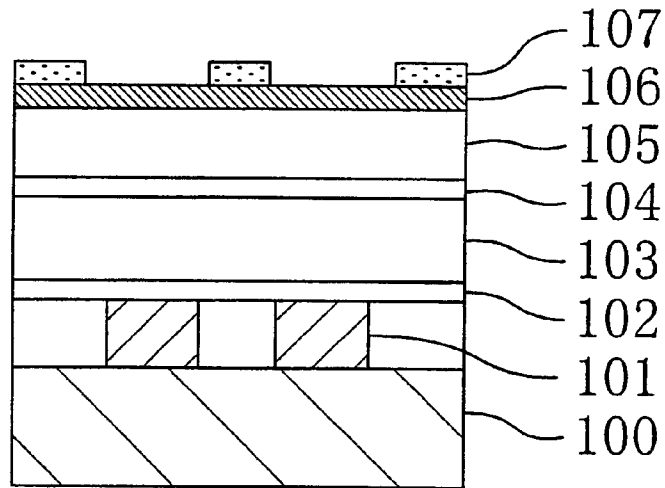


Fig. 1 (c)

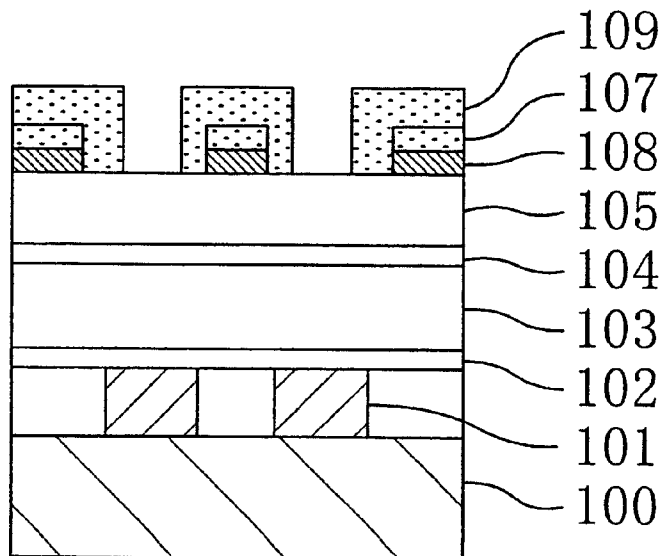


Fig. 2(a)

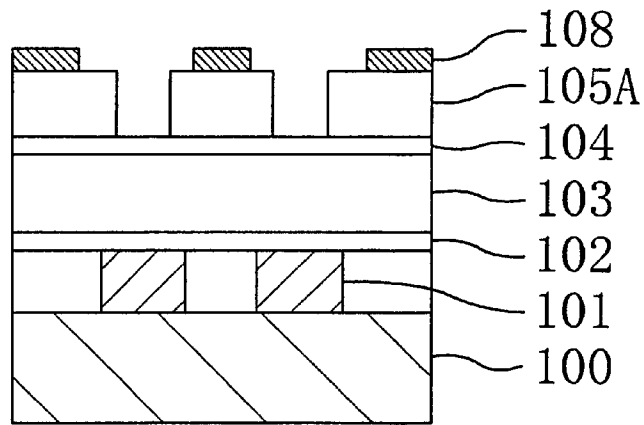


Fig. 2(b)

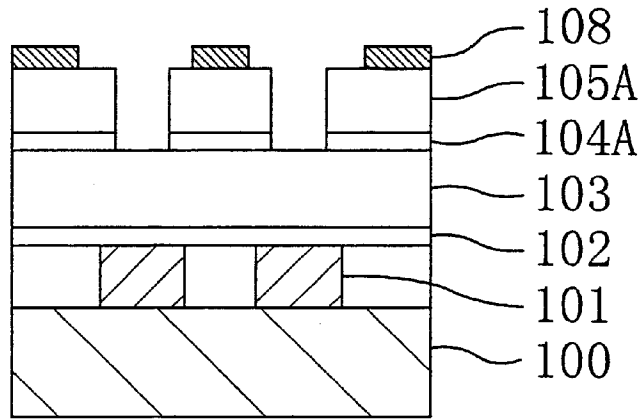


Fig. 2(c)

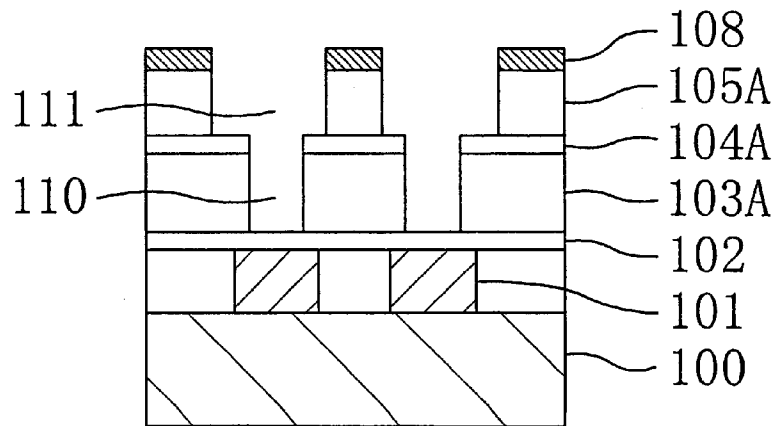


Fig. 3 (a)

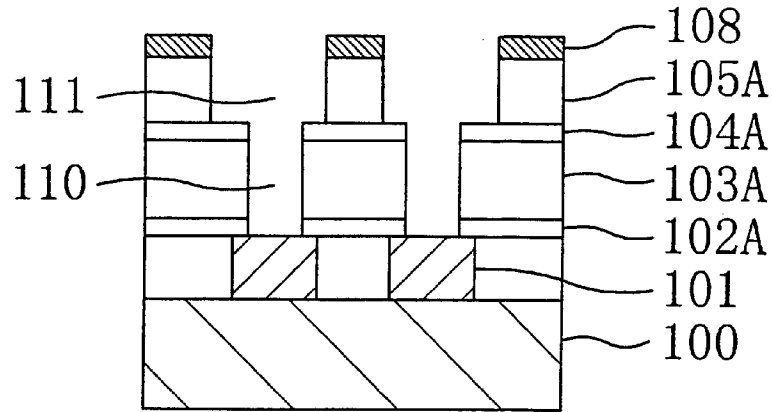


Fig. 3 (b)

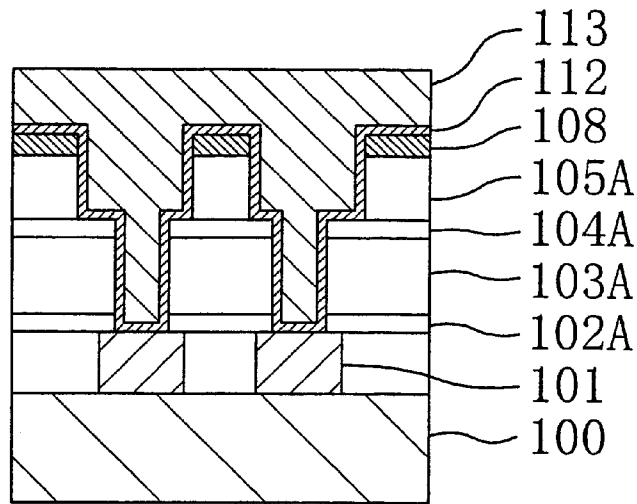


Fig. 3 (c)

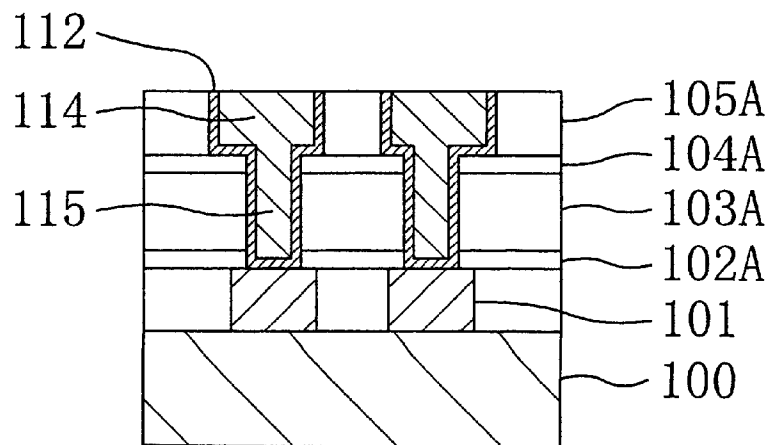


Fig. 4(a)

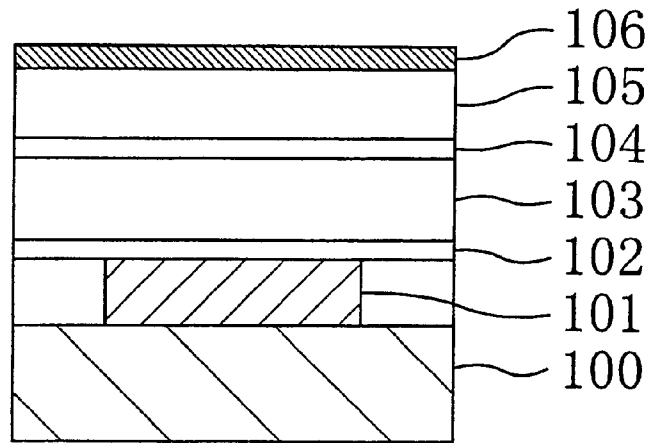


Fig. 4(b)

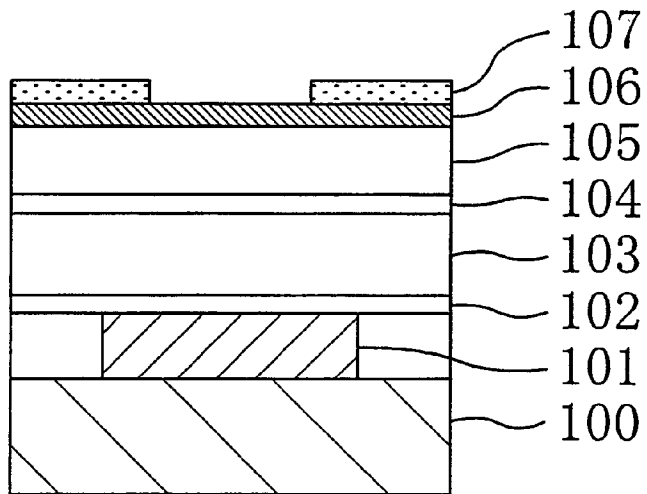
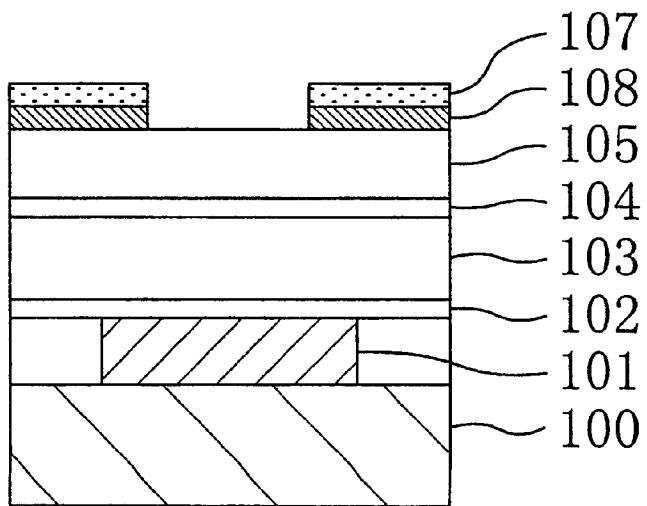


Fig. 4(c)



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