

FILE HISTORY

US 6,197,696

PATENT: 6,197,696

INVENTORS: Aoi, Nobuo

TITLE: Method for forming interconnection  
structure

APPLICATION NO: US1999274114A

FILED: 23 MAR 1999

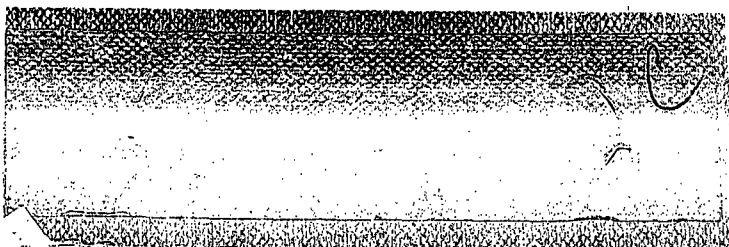
ISSUED: 06 MAR 2001

COMPILED: 12 MAY 2015

09/27/114



438	700	ISSUE CLASSIFICATION
Class	Subclass	



PATENT NUMBER  
**6197696**

6197696

### U.S. UTILITY PATENT APPLICATION

*Dwd* O.I.P.E. PATENT DATE  
 SCANNED *TNE* Q.A. *KB* MAR 06 2001

SECTOR	CLASS <i>438</i>	SUBCLASS <i>700</i>	ART UNIT <i>1765 1765</i>	EXAMINER <i>Umez-Eronini</i>
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PREPARED AND APPROVED FOR ISSUE

ISSUING CLASSIFICATION					
ORIGINAL		CROSS REFERENCE(S)			
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)		
<i>438</i>	<i>700</i>	<i>706</i>			
INTERNATIONAL CLASSIFICATION					
<i>H01L</i>	<i>21/311</i>				

Continued on Issue Slip Inside File Jacket

*1-31-01* Formal Drawings (*37* shts) set *L* *3/23/99*

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg. <i>37</i>	Figs. Drwg. <i>108</i>	Print Fig. <i>36</i>	Total Claims <i>15</i>	Print Claim for O.G. <i>1</i>
<input type="checkbox"/> a) The term of this patent subsequent to _____ (date) has been disclaimed.	<i>Lynette T. Umez-Eronini</i> <i>10/6/2000</i> (Assistant Examiner) (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> b) The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	<i>Benjamin L. Utech</i> BENJAMIN L. UTECH SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 1700 <i>10/11/00</i> (Primary Examiner) (Date)			<i>10-10-00</i> <b>ISSUE FEE</b> <i>2000</i> Amount Due <i>\$1240<sup>00</sup></i> Date Paid <i>1-9-01</i>	
<input type="checkbox"/> c) The terminal _____ months of this patent have been disclaimed.	<i>[Signature]</i> (Legal Instruments Examiner) (Date)			<b>ISSUE BATCH NUMBER</b> <i>753</i>	

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Form PTO-436A (Rev. 6/98)

ISSUE FEE IN FILE

(LABEL AREA)

Formal Drawings (*37* shts) set *L*

(FACE)

6,197,696

**METHOD FOR FORMING INTERCONNECTION STRUCTURE**

**Transaction History**

<b>Date</b>	<b>Transaction Description</b>
03-23-1999	Workflow - Drawings Finished
03-23-1999	Workflow - Drawings Matched with File at Contractor
03-23-1999	Workflow - Drawings Received at Contractor
03-29-1999	Initial Exam Team nn
04-09-1999	IFW Scan & PACR Auto Security Review
04-14-1999	Application Dispatched from OIPE
05-11-1999	Case Docketed to Examiner in GAU
06-25-1999	Request for Foreign Priority (Priority Papers May Be Included)
08-09-1999	Information Disclosure Statement (IDS) Filed
08-09-1999	Information Disclosure Statement (IDS) Filed
02-09-2000	Information Disclosure Statement (IDS) Filed
02-09-2000	Information Disclosure Statement (IDS) Filed
10-05-2000	Case Docketed to Examiner in GAU
10-10-2000	Mail Notice of Allowance
10-10-2000	Notice of Allowance Data Verification Completed
11-29-2000	Workflow - File Sent to Contractor
01-09-2001	Issue Fee Payment Verified
01-31-2001	Workflow - Complete WF Records for Drawings
02-04-2001	Application Is Considered Ready for Issue
02-15-2001	Issue Notification Mailed
03-06-2001	Recordation of Patent Grant Mailed



# PATENT APPLICATION



09274114

APR 07 1999

## CONTENTS

	Received (Incl. C. of M.) or Date Mailed	Date received (Incl. C. of M.) or Date Mailed
1. Application <input checked="" type="checkbox"/> papers.		
2. Priority Paper 6-25-99		
3. IDS 8.9.99		
4. IDS / Prior Art 2-9-00		
5. Allowance 10-10-00		
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POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	PTM	67814	4/1/99
O.I.P.E. CLASSIFIER			5 4-7-99
FORMALITY REVIEW	DB	70014	4/13/99

INDEX OF CLAIMS

- ✓ ..... Rejected
- = ..... Allowed
- (Through numeral)... Canceled
- ÷ ..... Restricted
- N ..... Non-elected
- I ..... Interference
- A ..... Appeal
- O ..... Objected

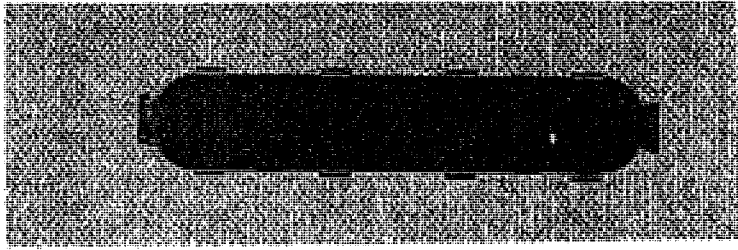
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If more than 150 claims or 10 actions  
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SEARCHED			
Class	Sub.	Date	Exmr.
438	700	<del>L.J.M.E</del> 10/6/2008	L.J.M.E
↓	706	↓	↓

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	Date	Exmr.
EAST	10/6/2008	L.J.M.E

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.



US006197696B1

(12) **United States Patent**  
**Aoi**

(10) **Patent No.:** **US 6,197,696 B1**  
(45) **Date of Patent:** **Mar. 6, 2001**

(54) **METHOD FOR FORMING INTERCONNECTION STRUCTURE**

- (75) Inventor: **Nobuo Aoi, Hyogo (JP)**
- (73) Assignee: **Matsushita Electric Industrial Co., Ltd., Osaka (JP)**
- (\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

- (21) Appl. No.: **09/274,114**
- (22) Filed: **Mar. 23, 1999**
- (30) **Foreign Application Priority Data**  
Mar. 26, 1998 (JP) ..... 10-079371
- (51) **Int. Cl.<sup>7</sup>** ..... **H01L 21/311**
- (52) **U.S. Cl.** ..... **438/700; 438/706**
- (58) **Field of Search** ..... **438/700, 706**

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9-64034	3/1997	(JP)	H01L/21/3205
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European Search Report dated Jul. 1, 1999.

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*Primary Examiner*—Benjamin L. Utech  
*Assistant Examiner*—Lynette T. Umez-Eronini  
(74) *Attorney, Agent, or Firm*—Eric J. Robinson; Nixon Peabody LLP

(57) **ABSTRACT**

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film is masked with the third insulating film and dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films are masked with the mask pattern and the second insulating film, respectively, and dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.

**15 Claims, 37 Drawing Sheets**

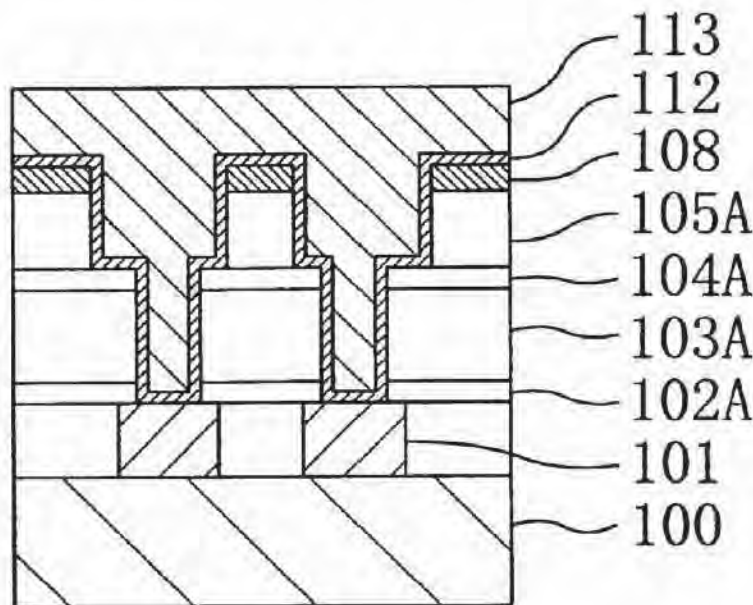


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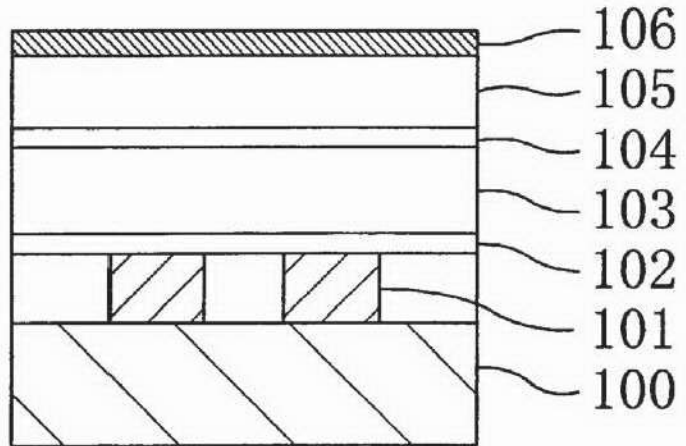


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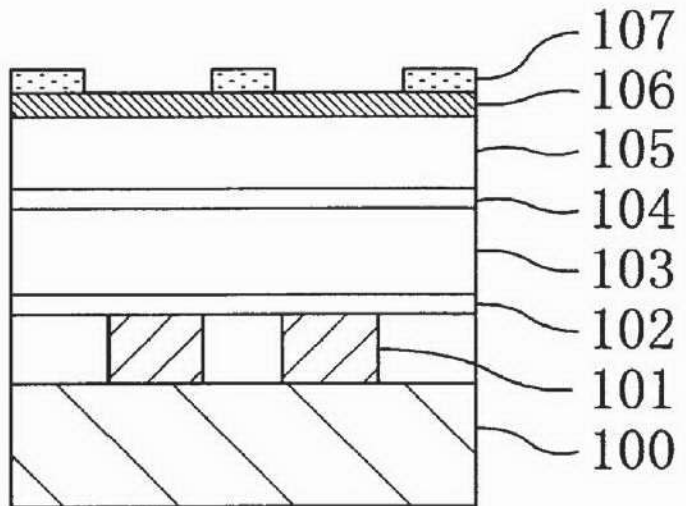


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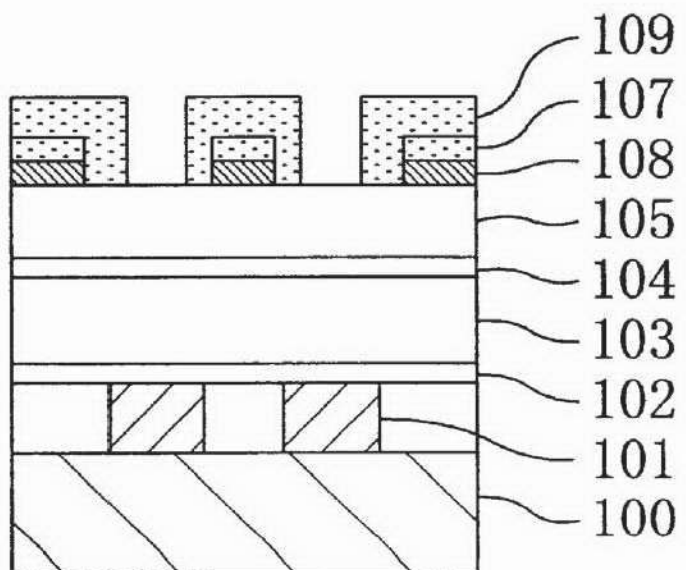


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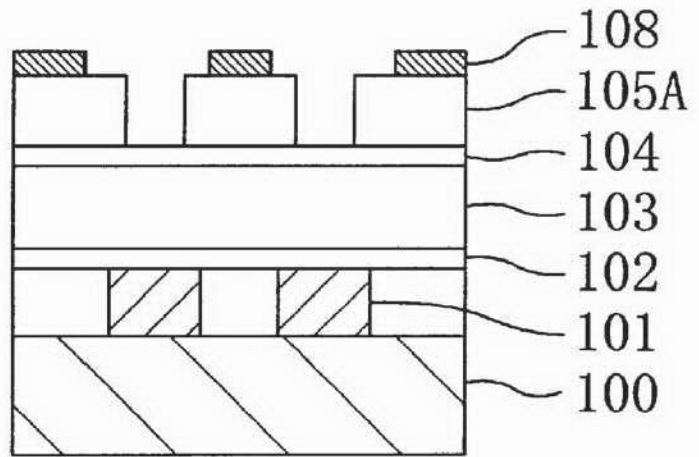


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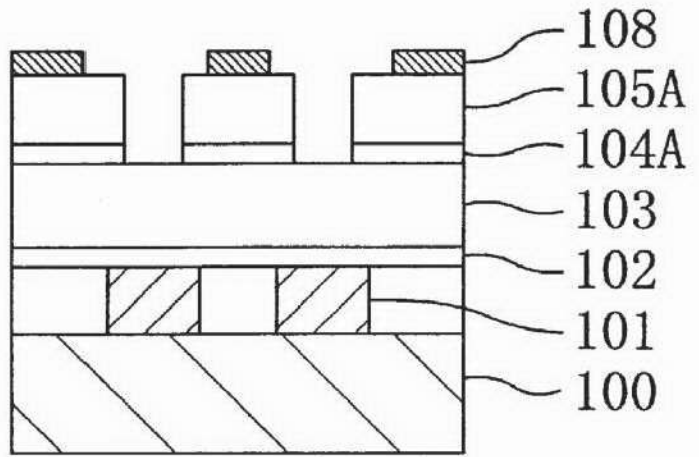


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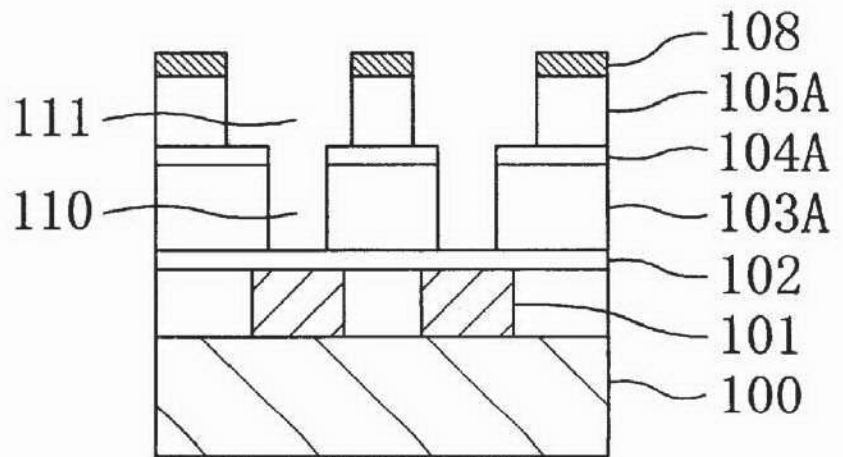


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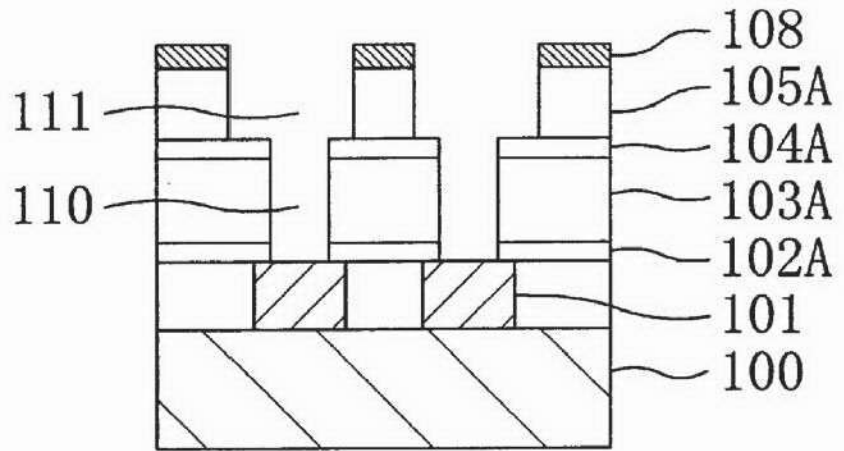


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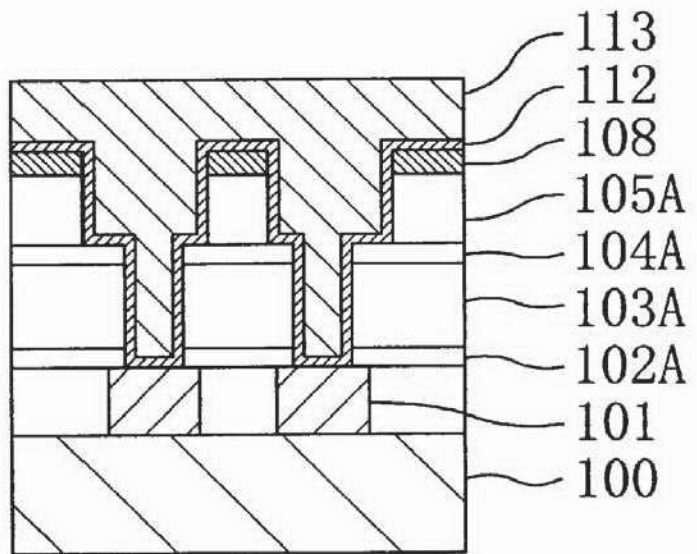


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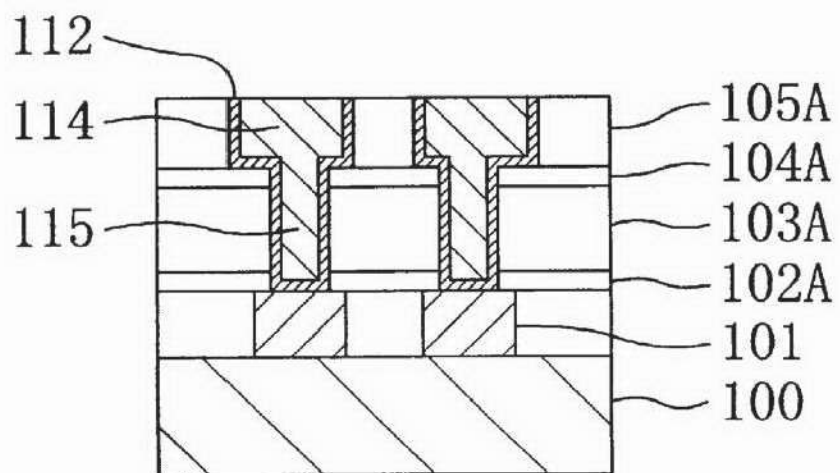


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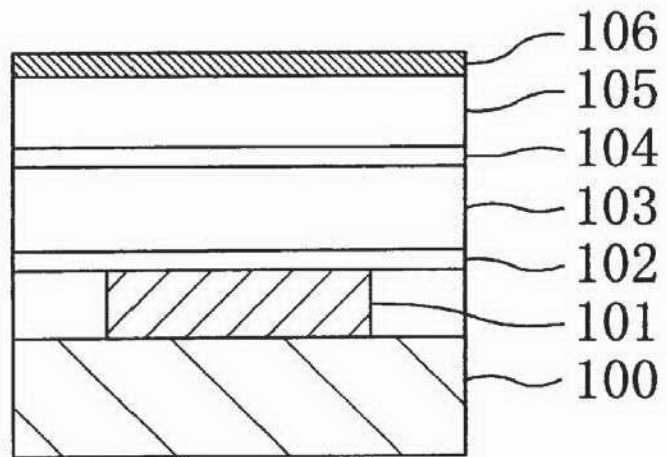


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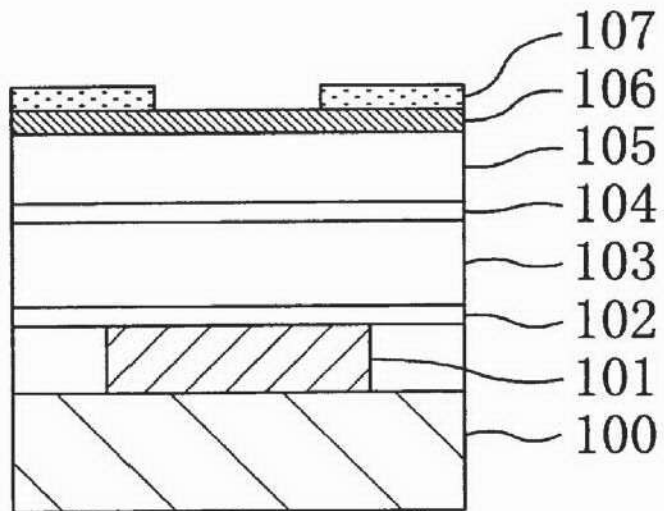


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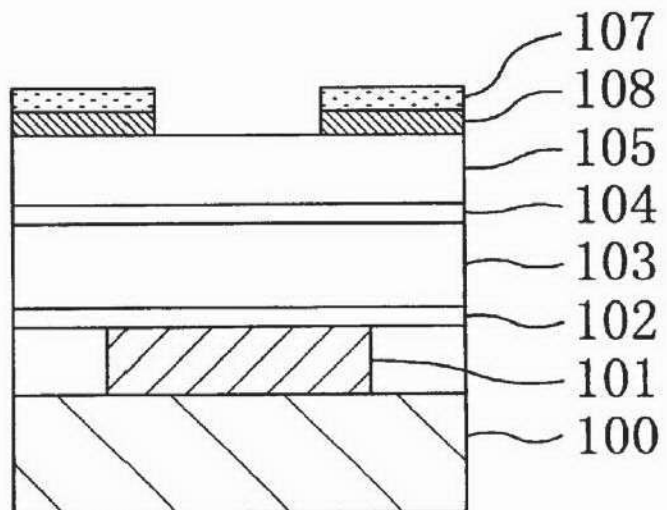


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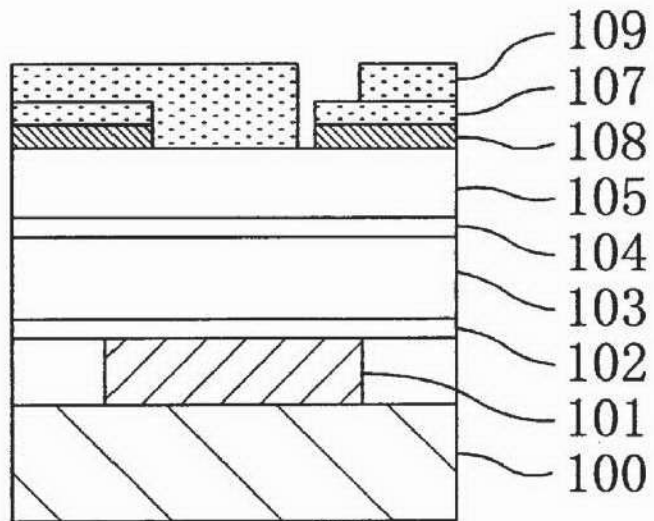


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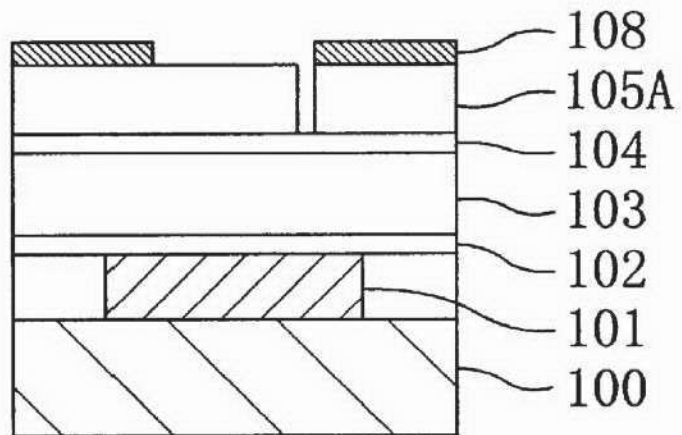


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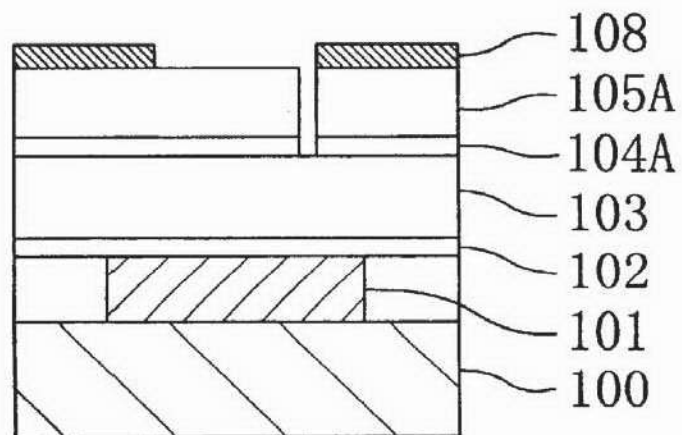




Fig. 6(a)

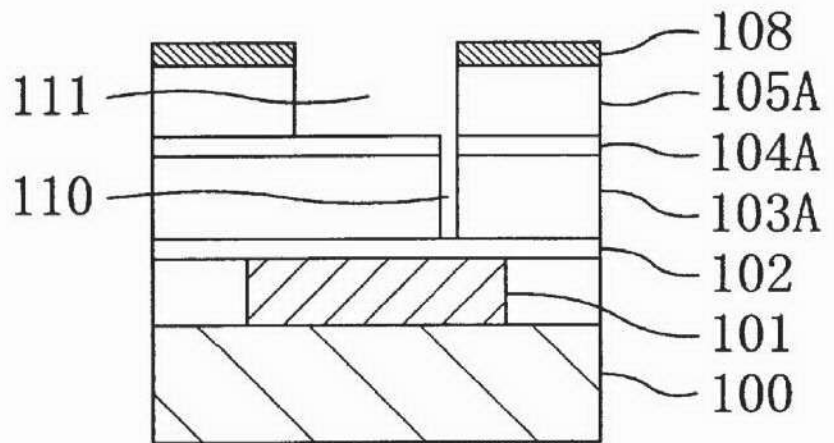


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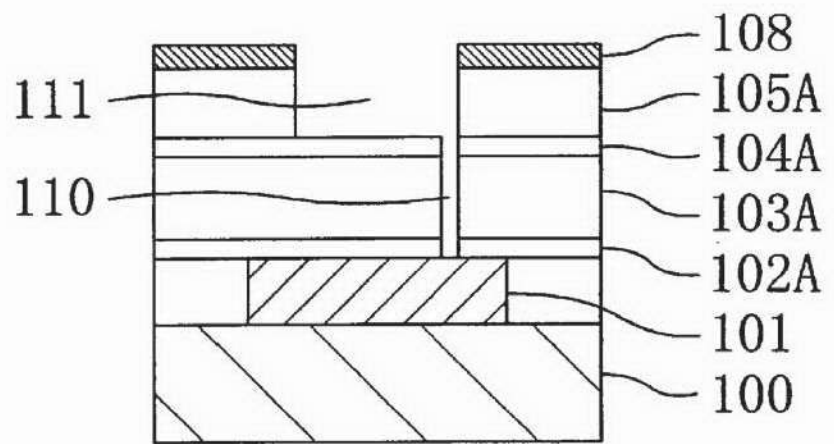


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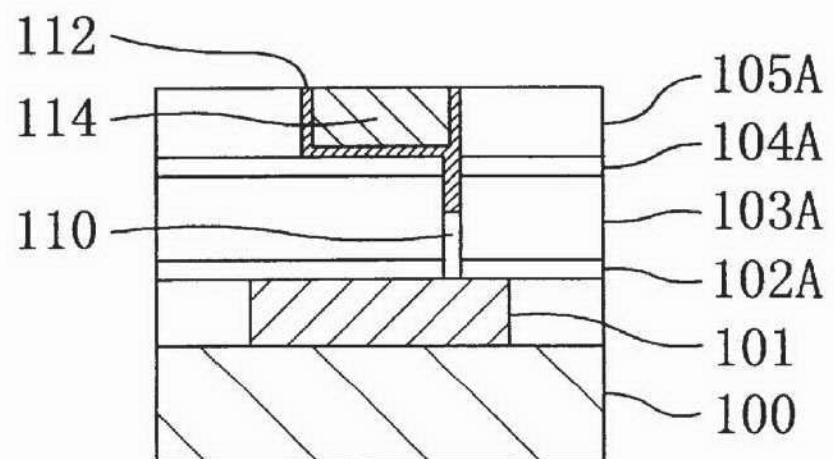


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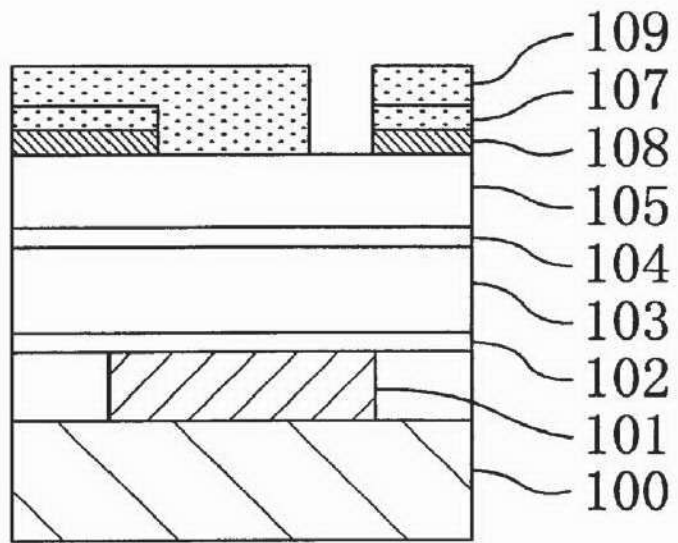


Fig. 7(b)

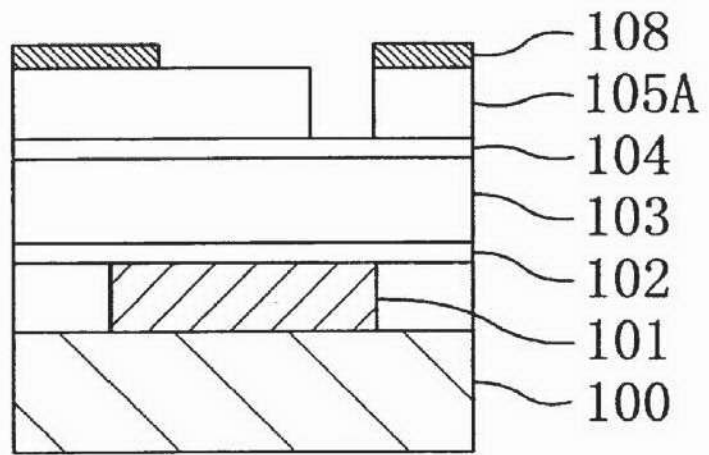


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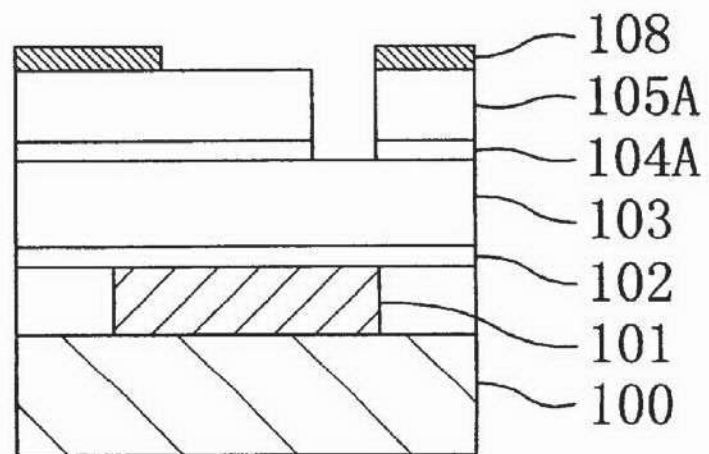


Fig. 8(a)

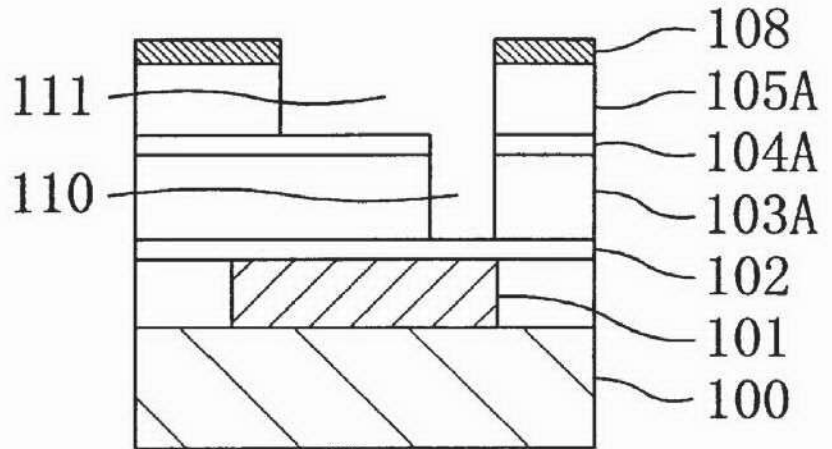


Fig. 8(b)

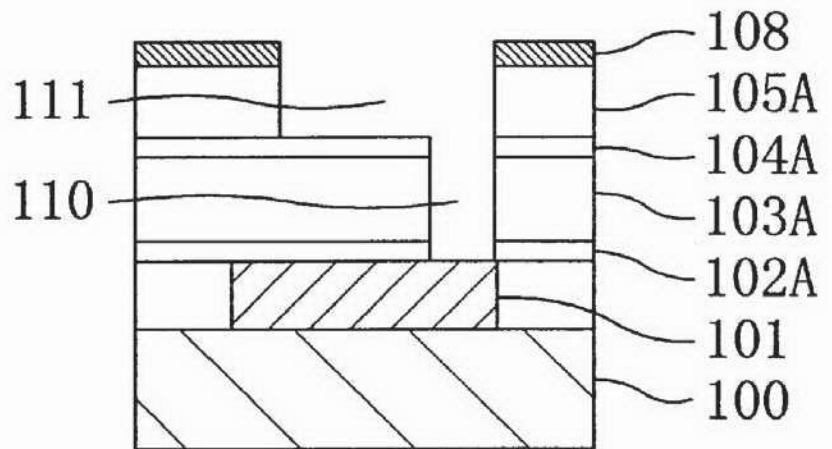


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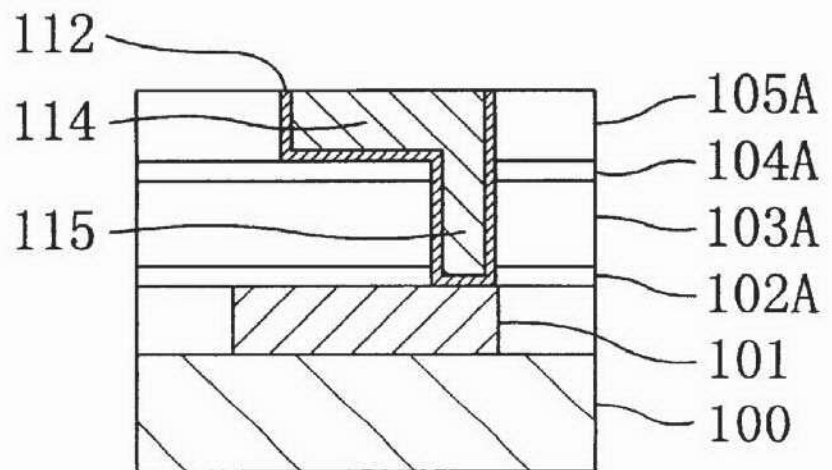


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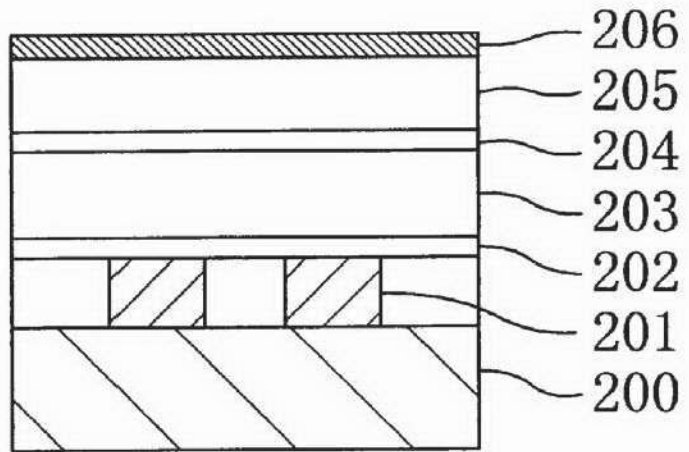


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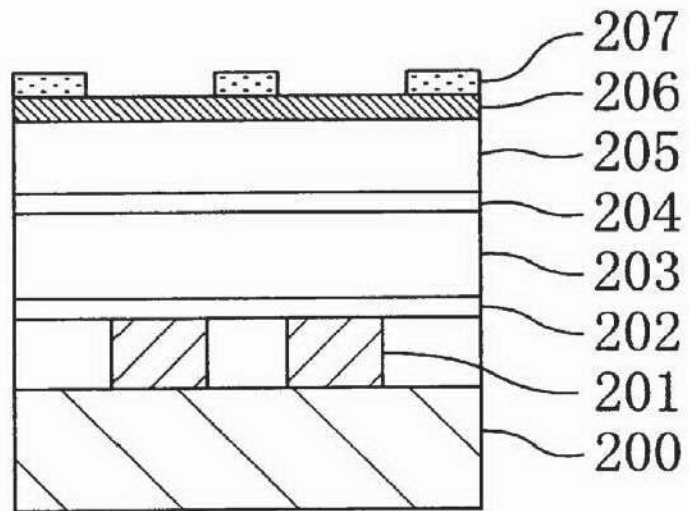


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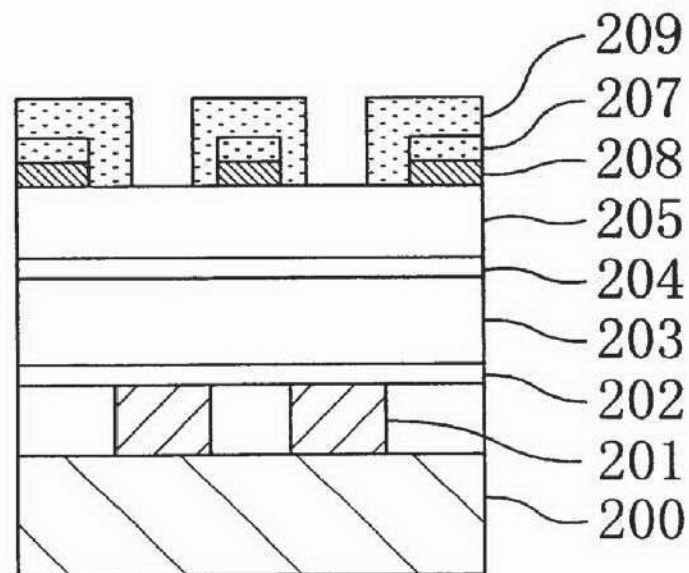


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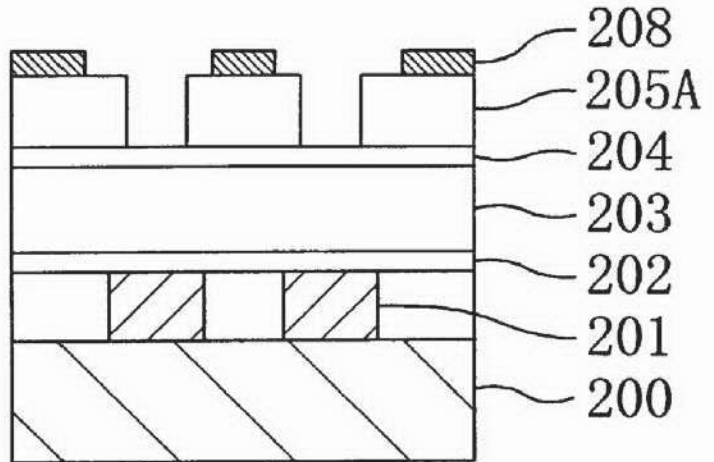


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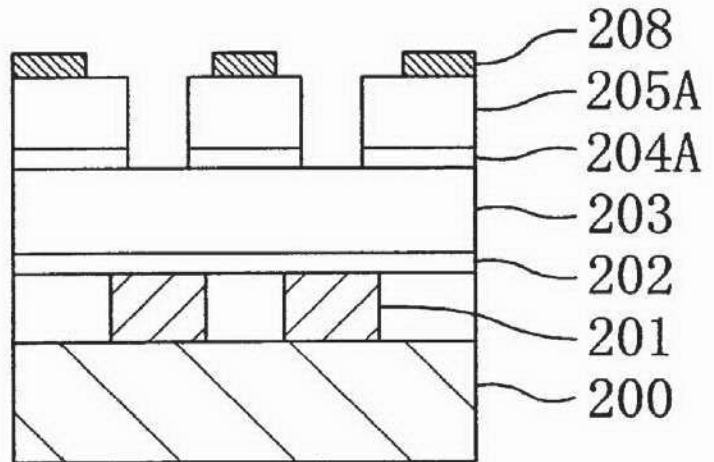


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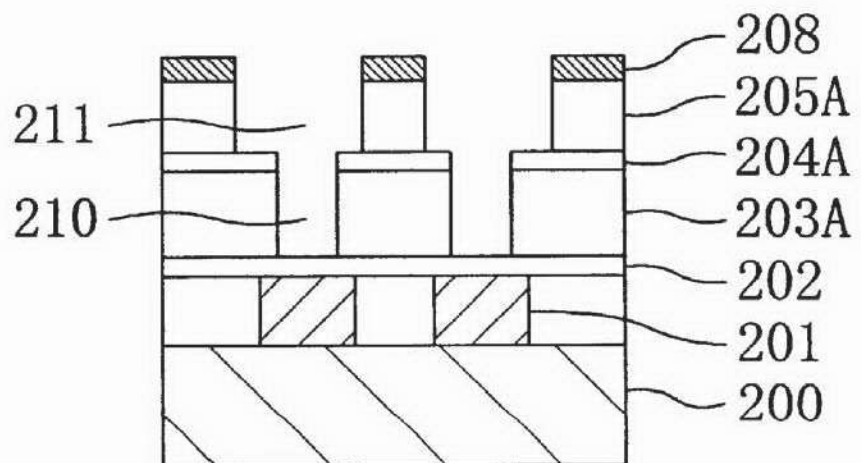


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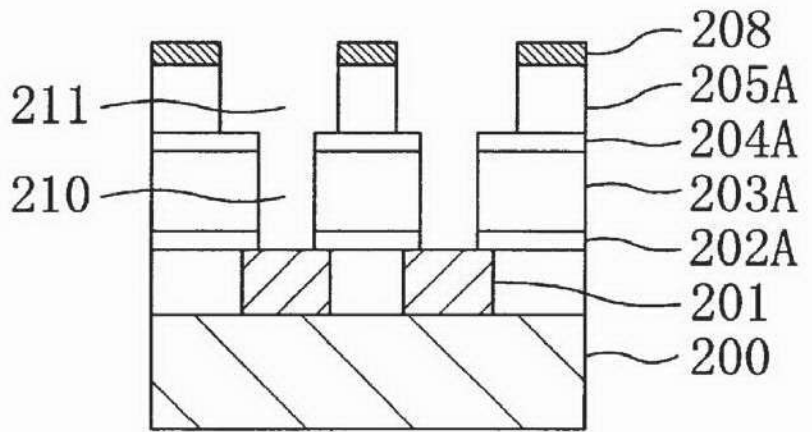


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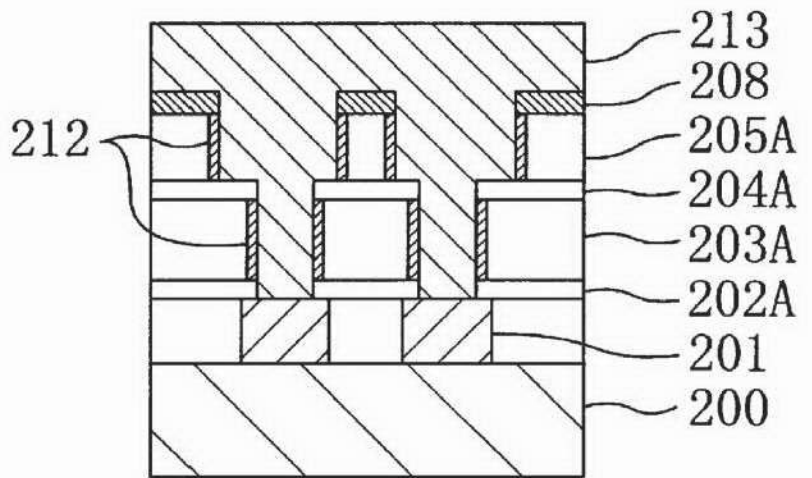


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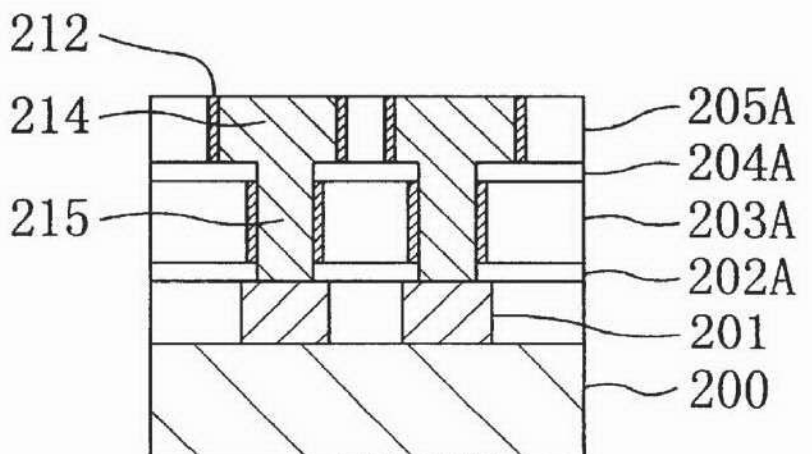


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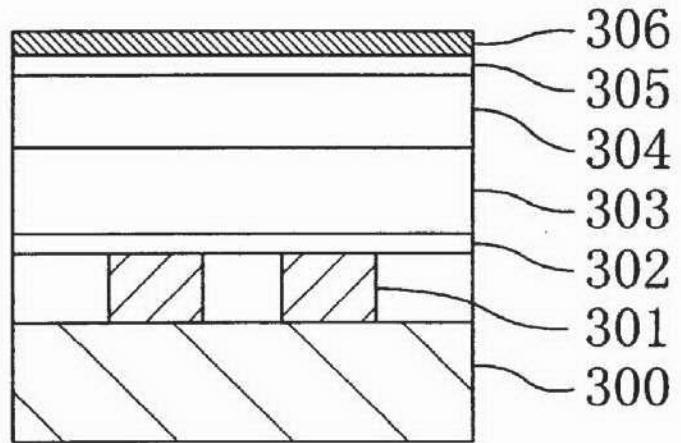


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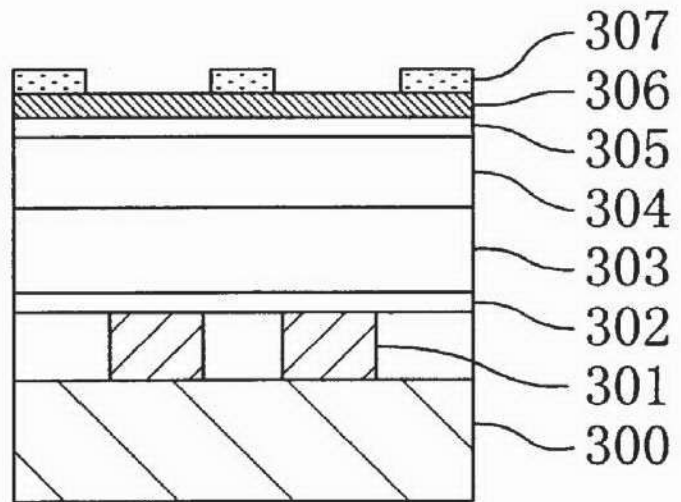


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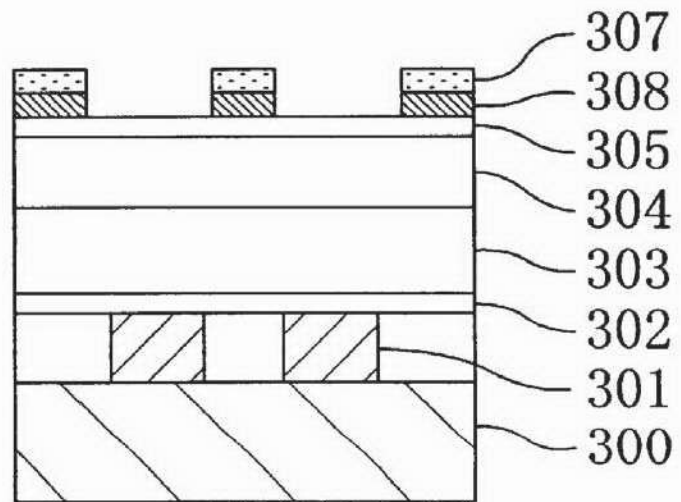


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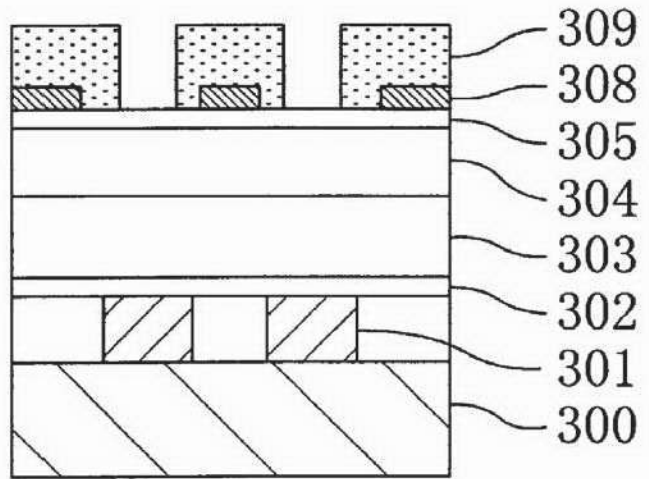


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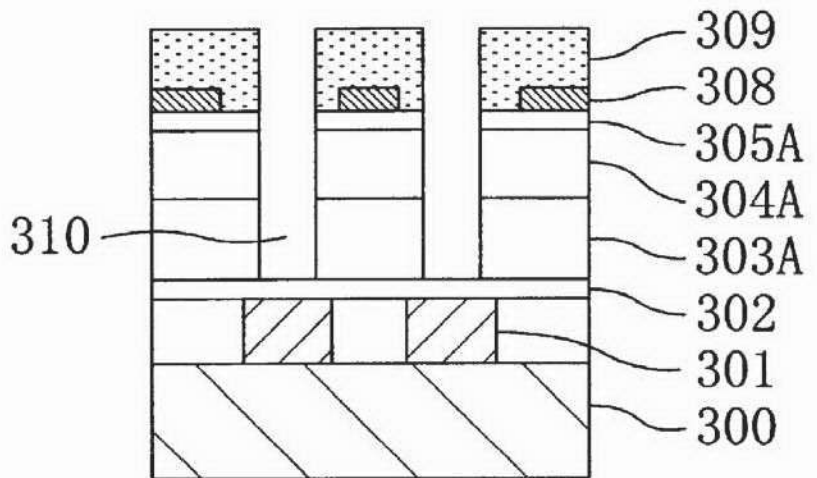


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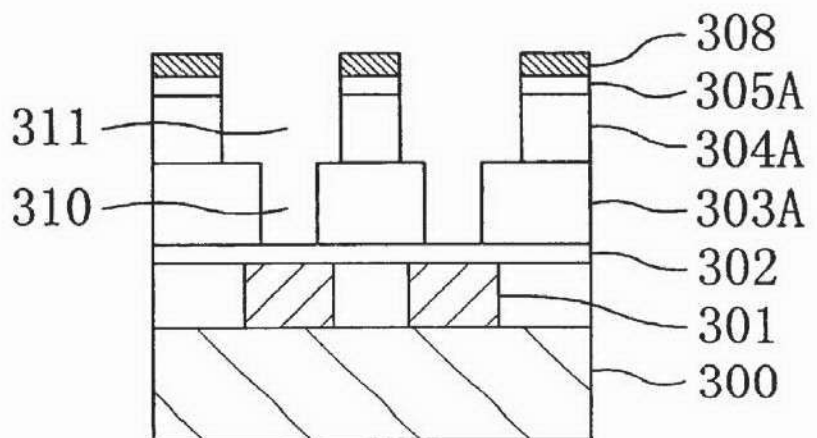




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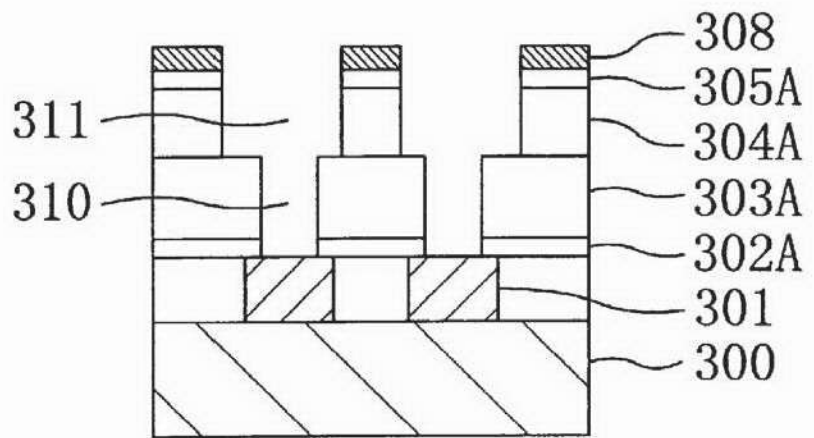


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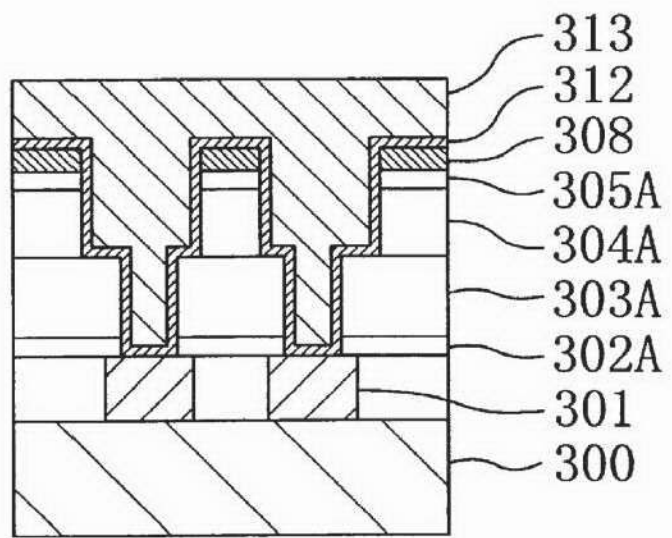


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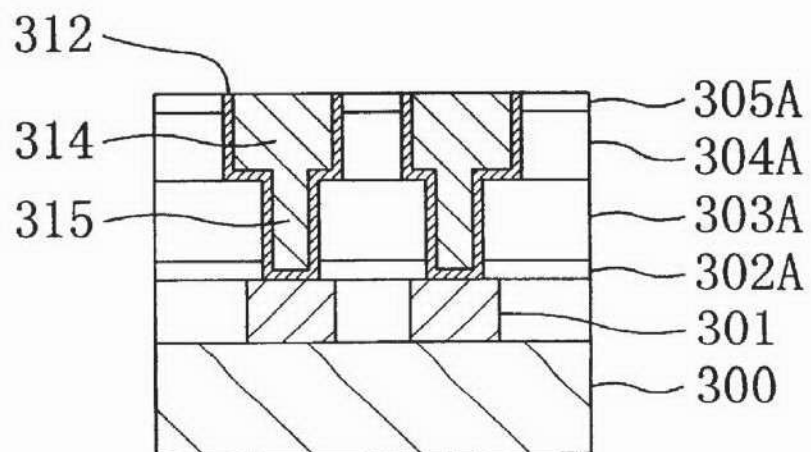


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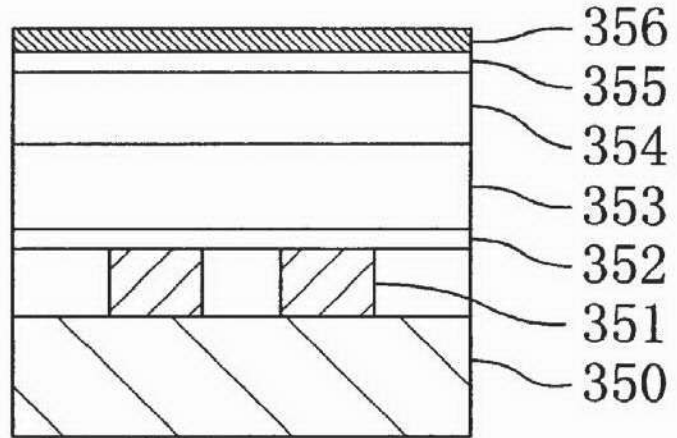


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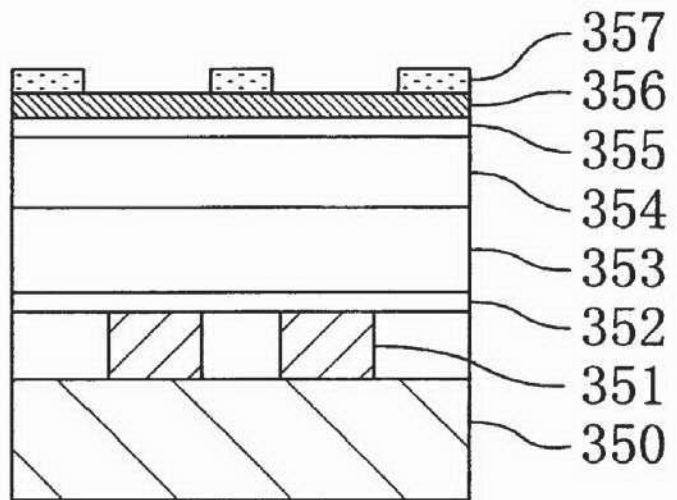


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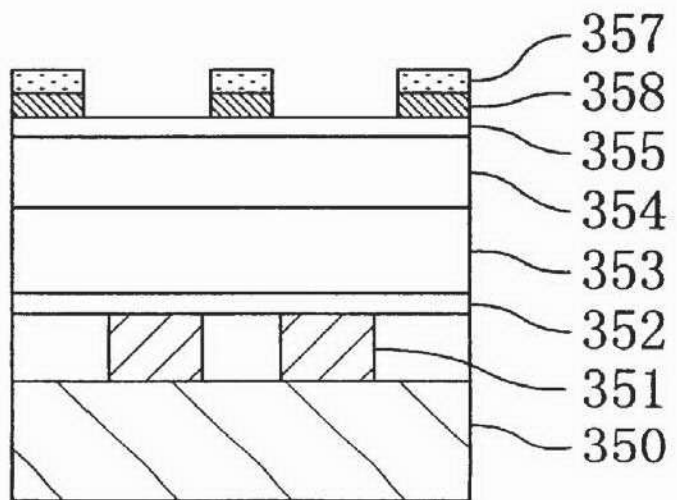


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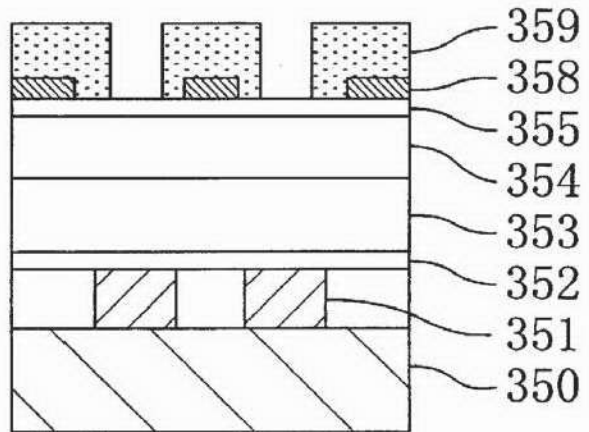


Fig. 16(b)

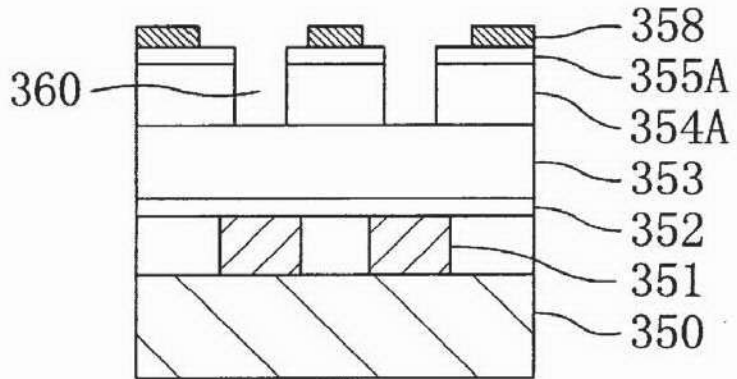


Fig. 16(c)

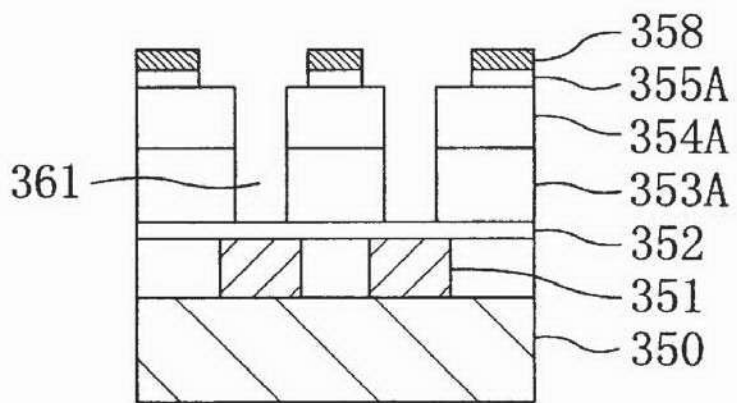


Fig. 16(d)

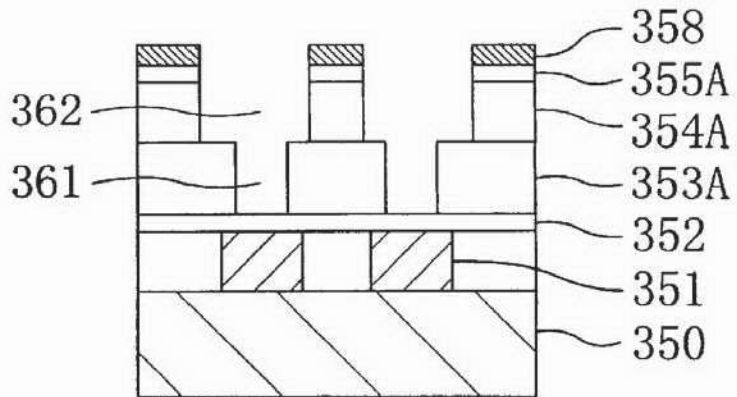


Fig. 17(a)

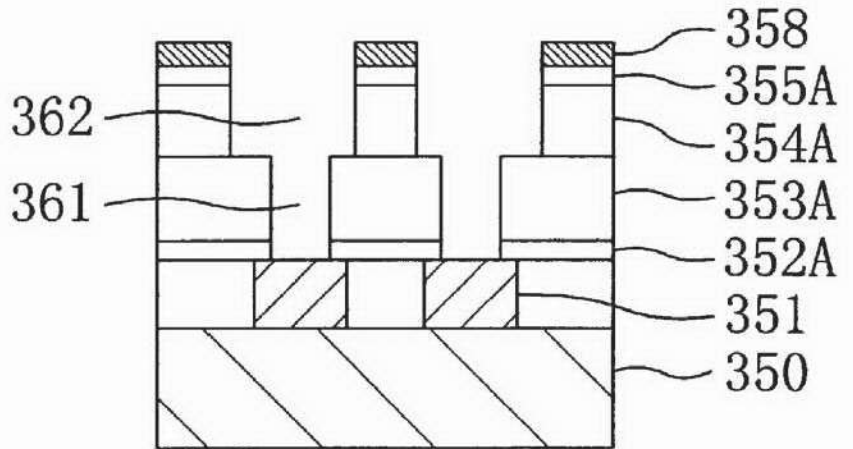


Fig. 17(b)

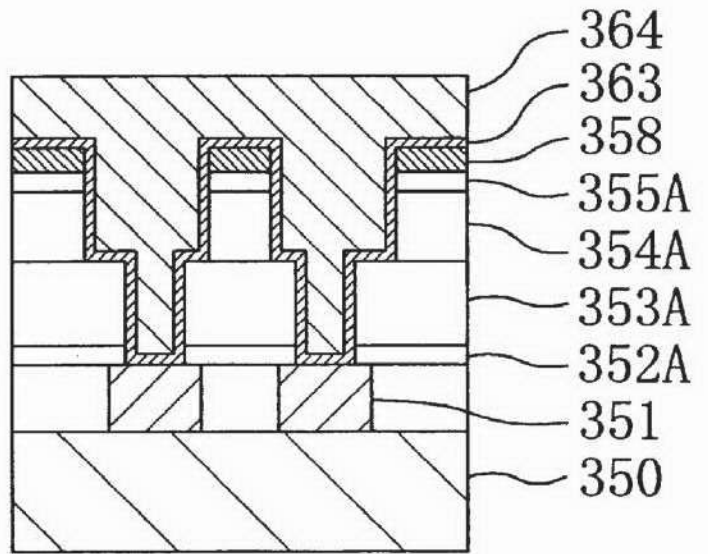


Fig. 17(c)

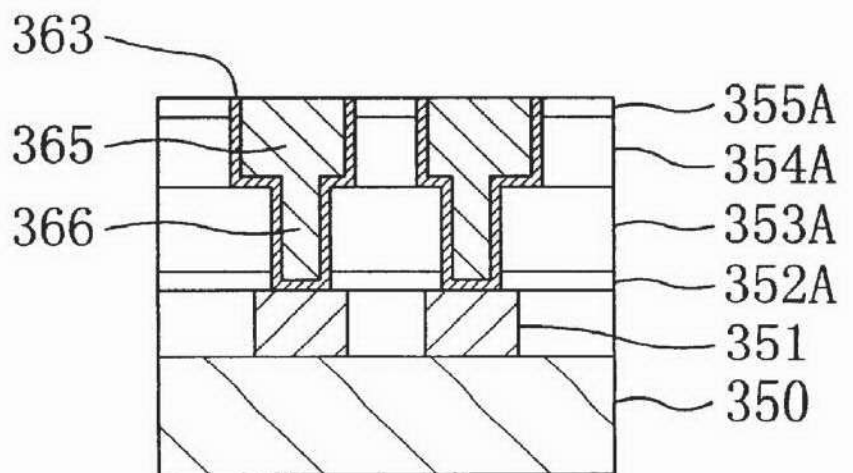


Fig. 18(a)

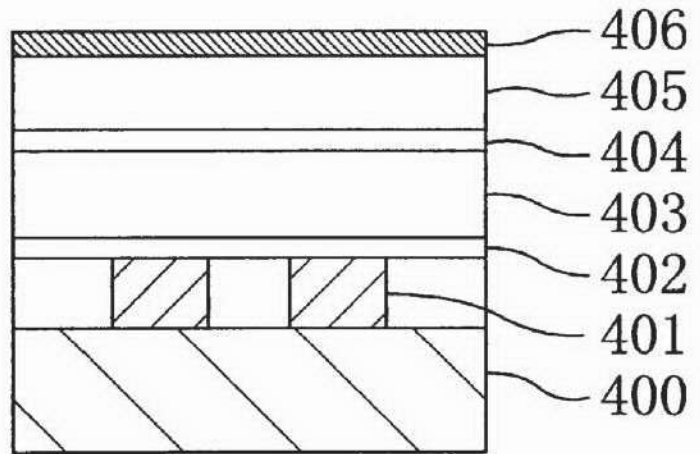


Fig. 18(b)

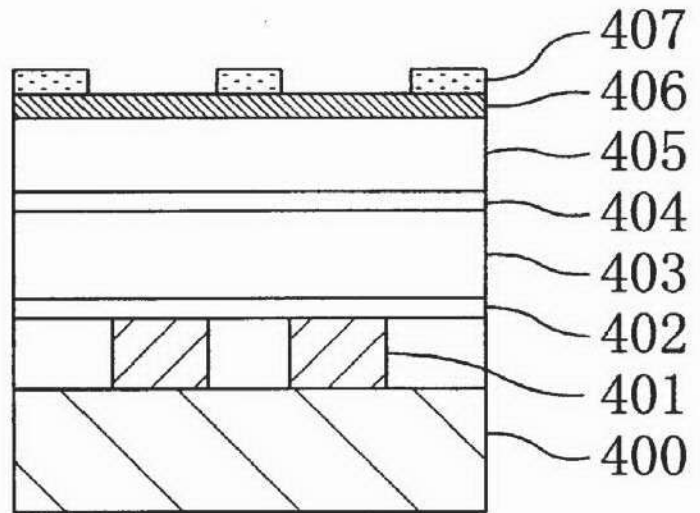


Fig. 18(c)

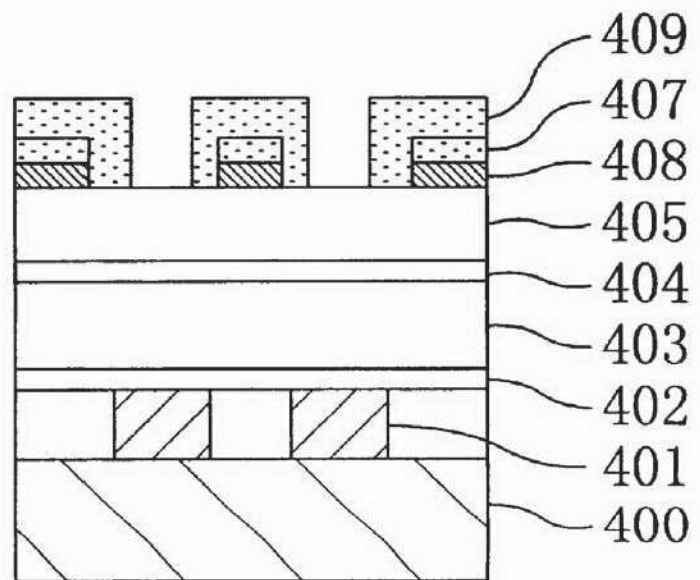


Fig. 19(a)

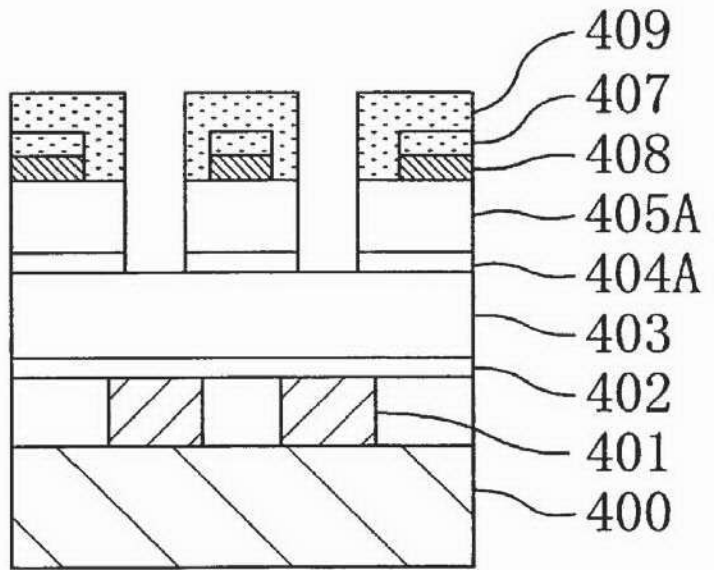


Fig. 19(b)

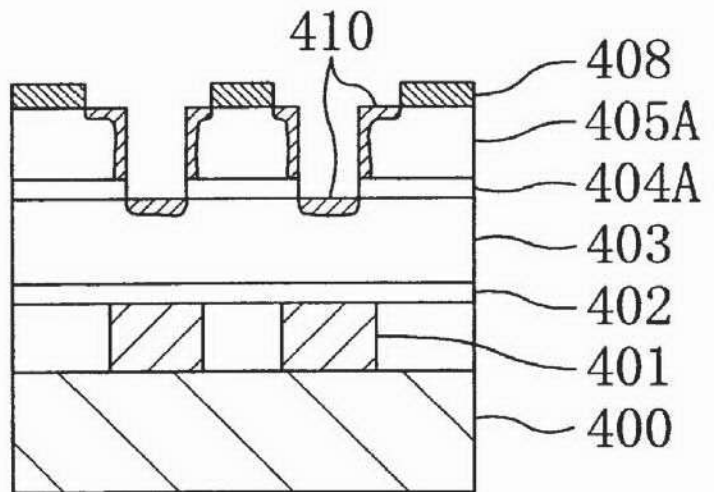


Fig. 19(c)

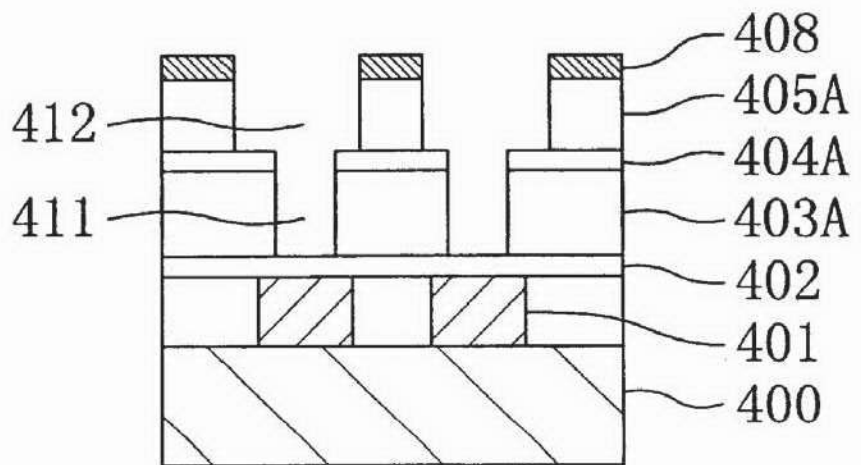


Fig. 20 (a)

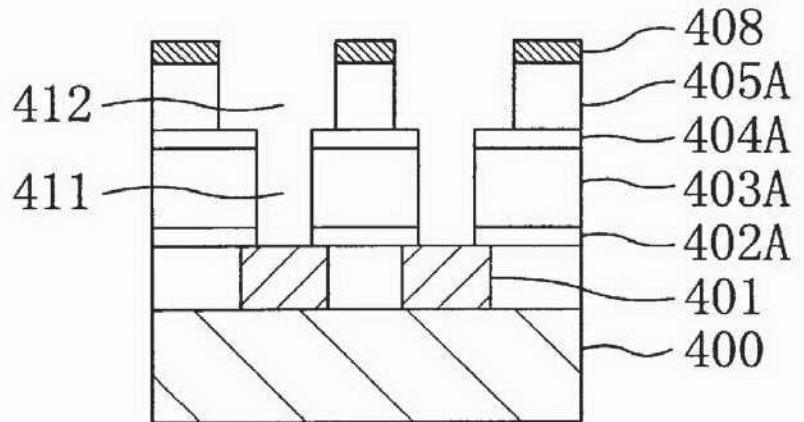


Fig. 20 (b)

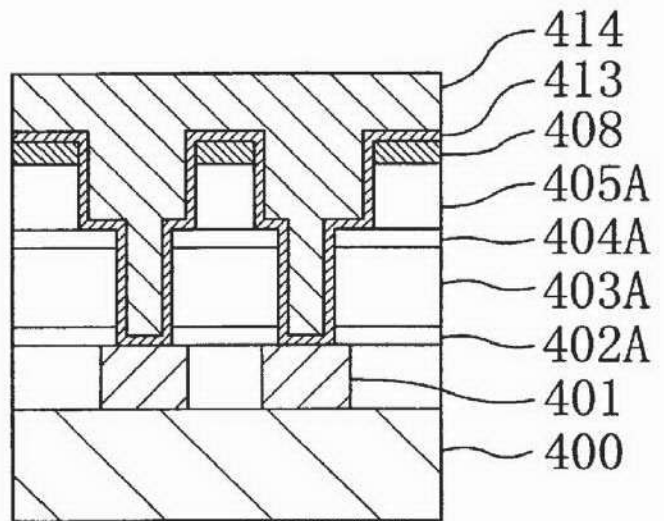


Fig. 20 (c)

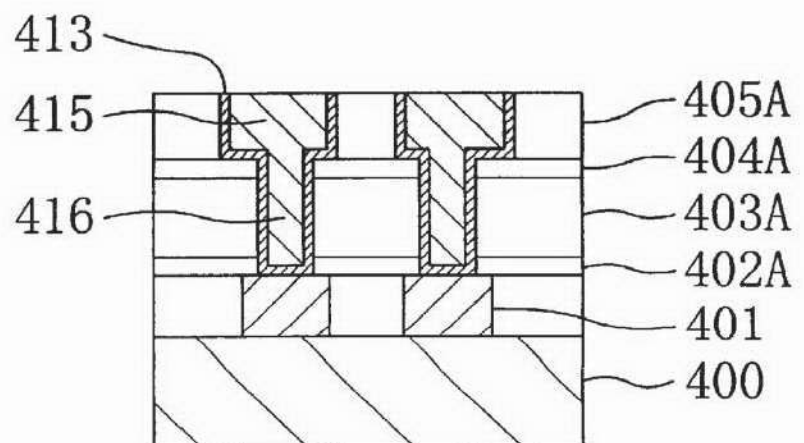


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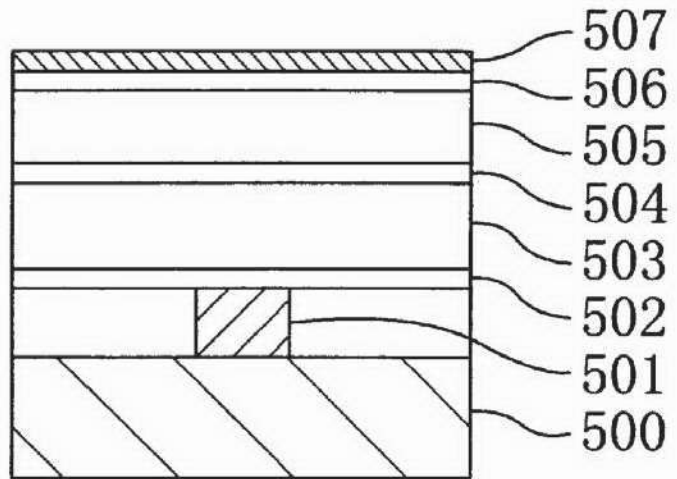


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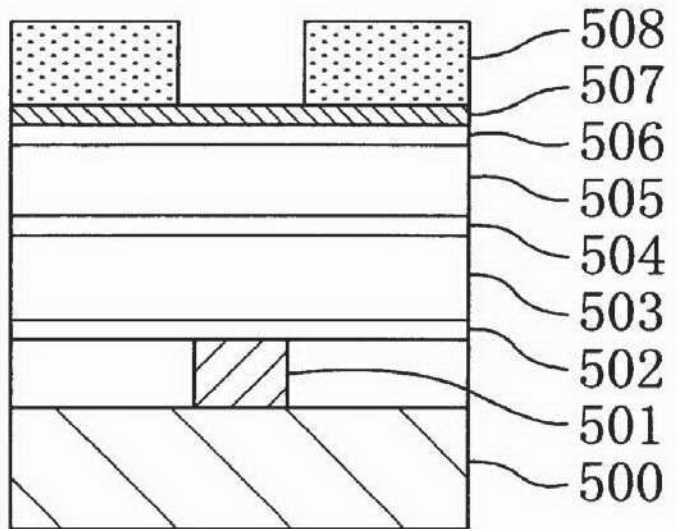


Fig. 21 (c)

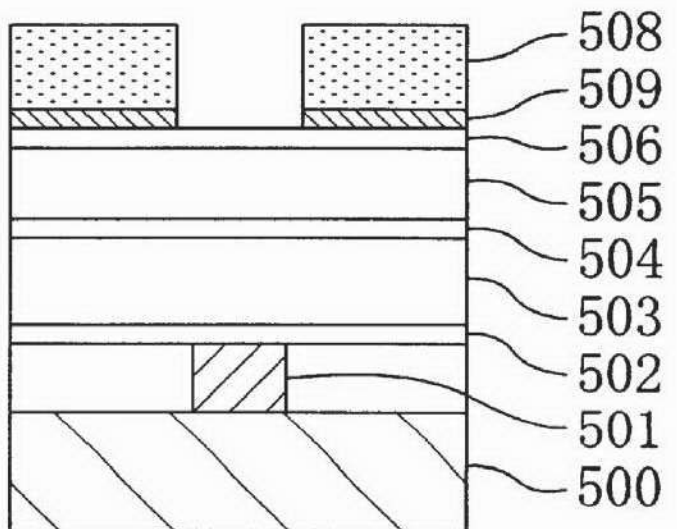




Fig. 22 (a)

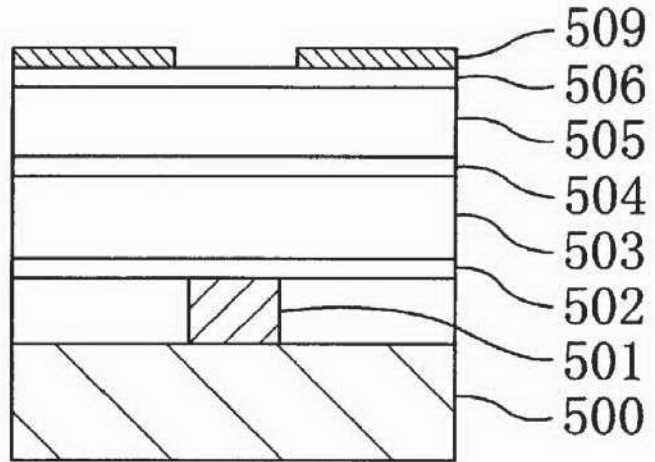


Fig. 22 (b)

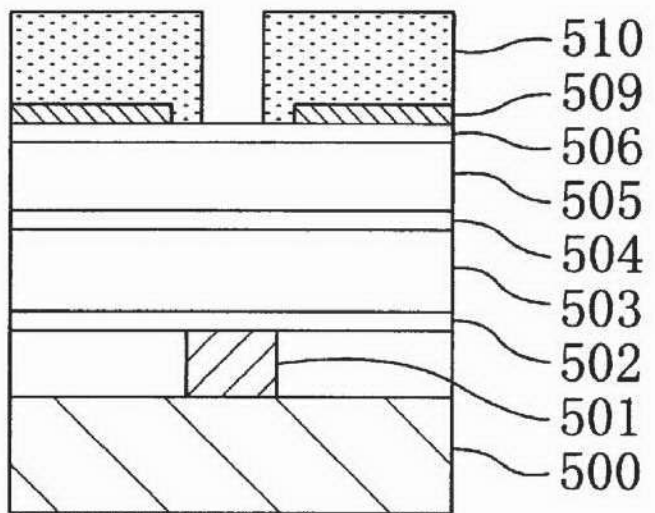


Fig. 22 (c)

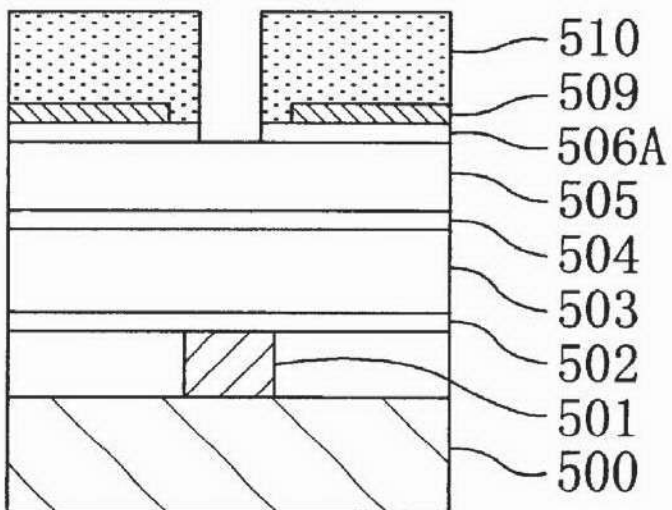


Fig. 23(a)

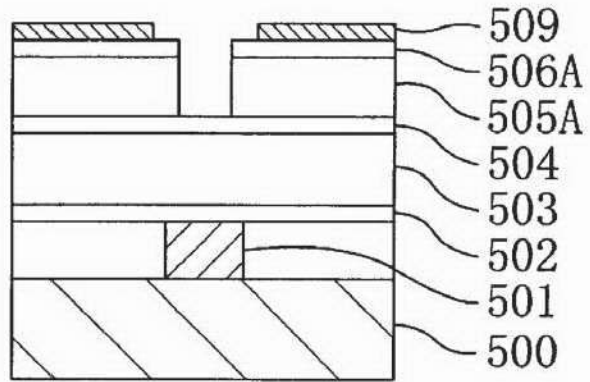


Fig. 23(b)

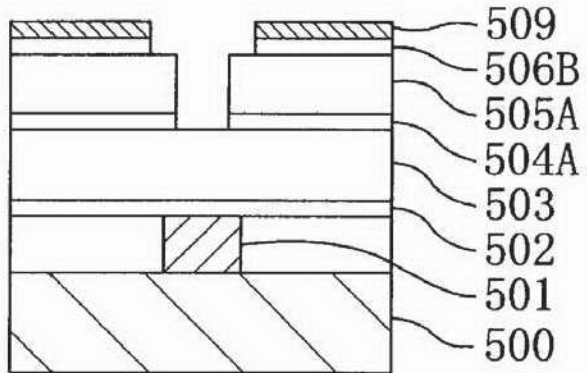


Fig. 23(c)

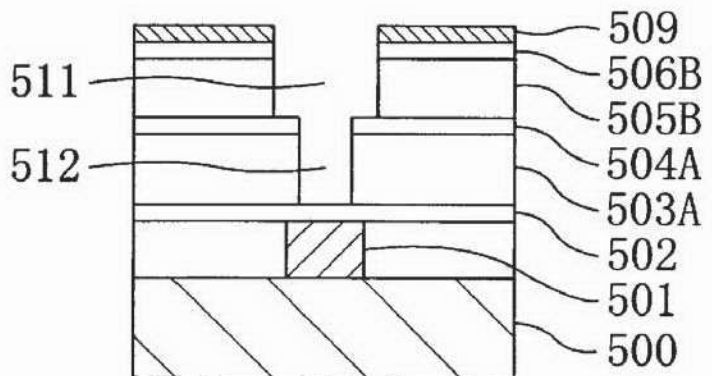


Fig. 23(d)

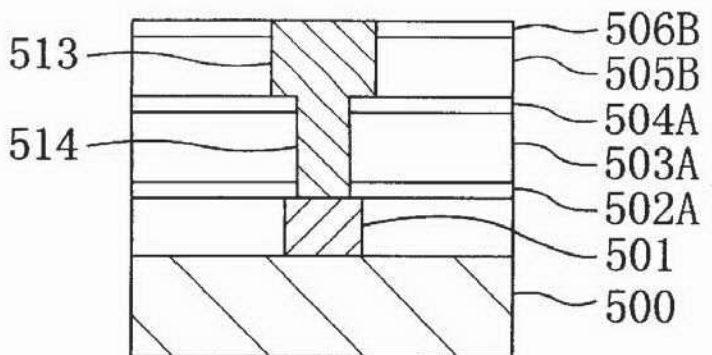


Fig. 24(a)

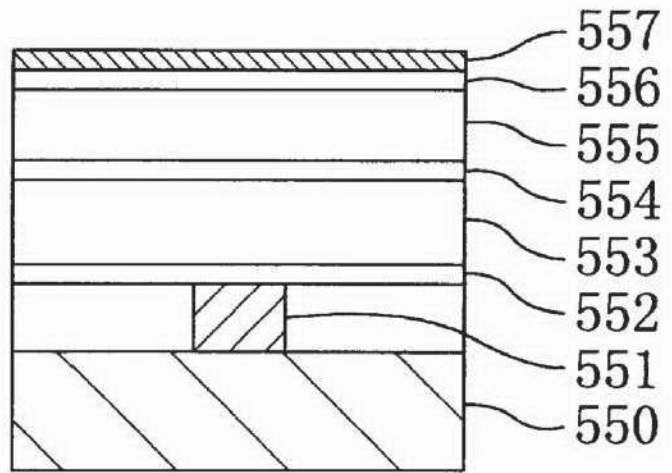


Fig. 24(b)

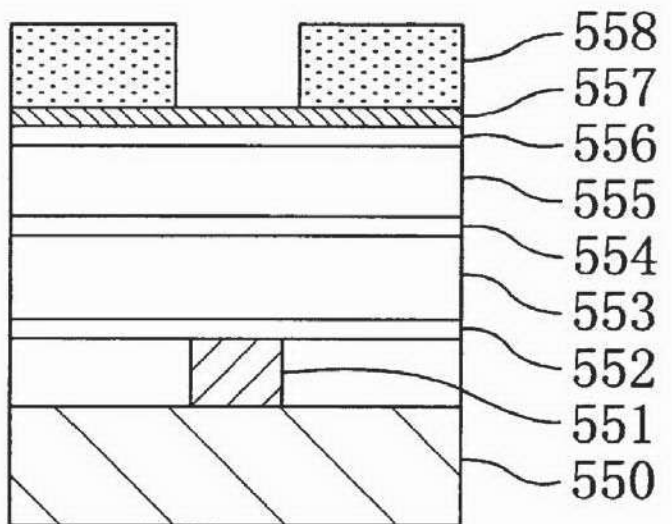


Fig. 24(c)

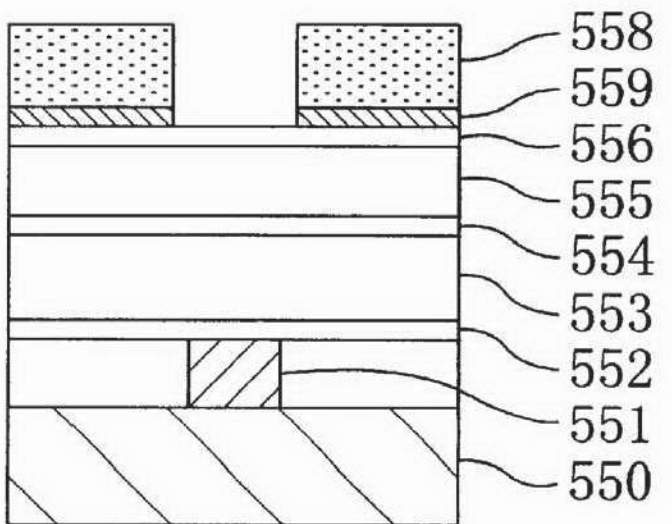


Fig. 25 (a)

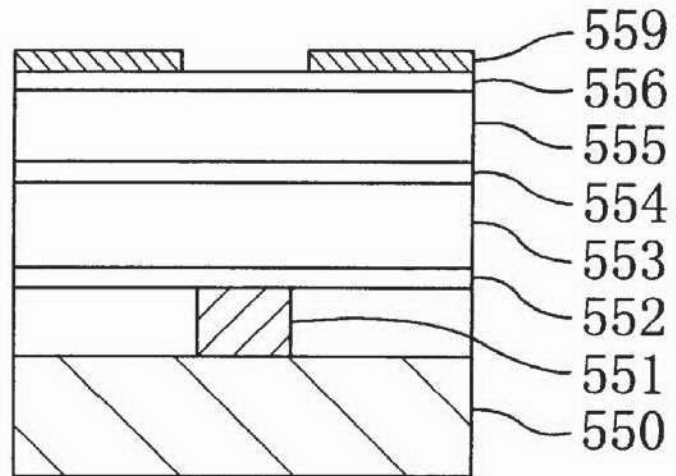


Fig. 25 (b)

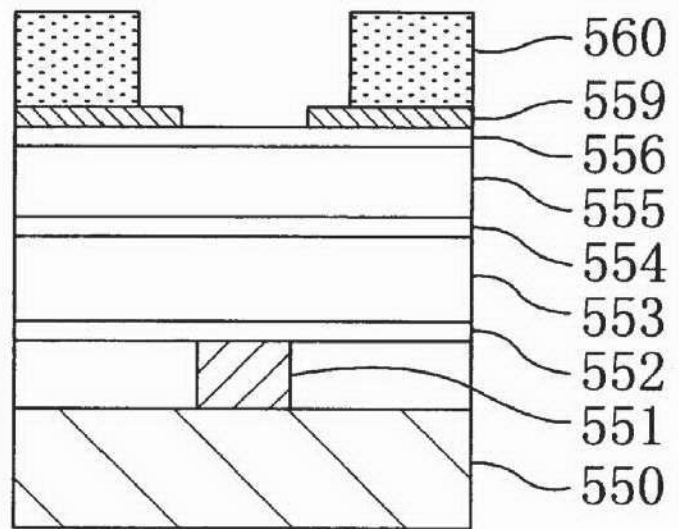


Fig. 25 (c)

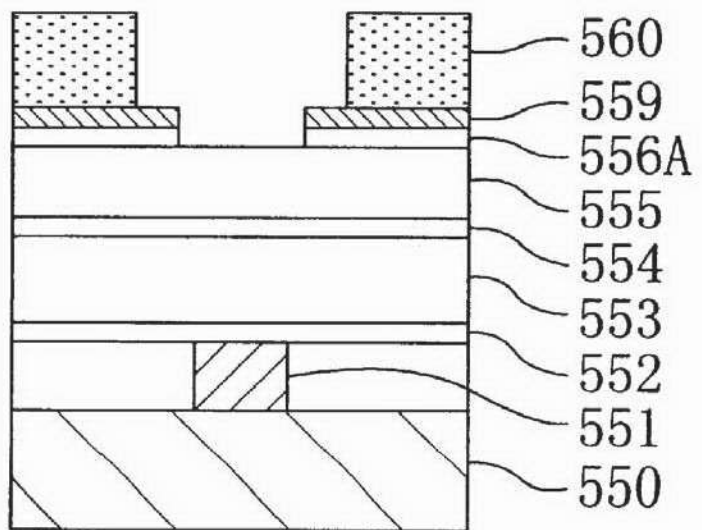


Fig. 26 (a)

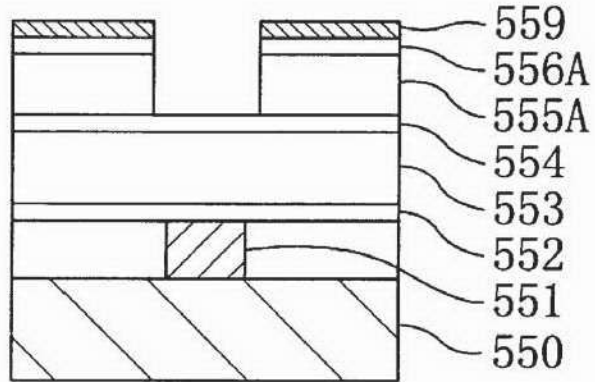


Fig. 26 (b)

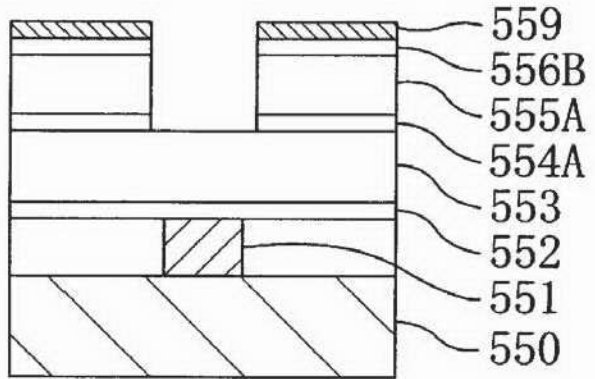


Fig. 26 (c)

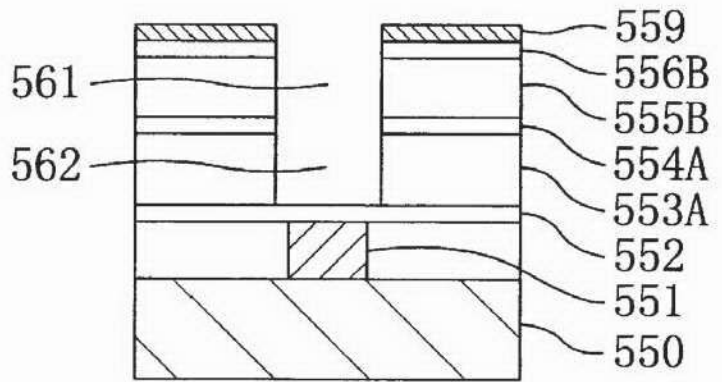


Fig. 26 (d)

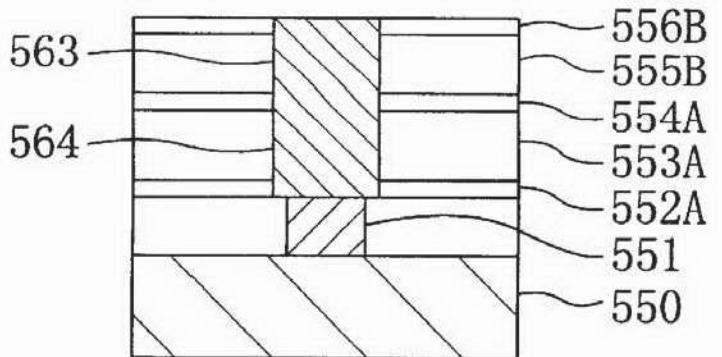


Fig. 27 (a)

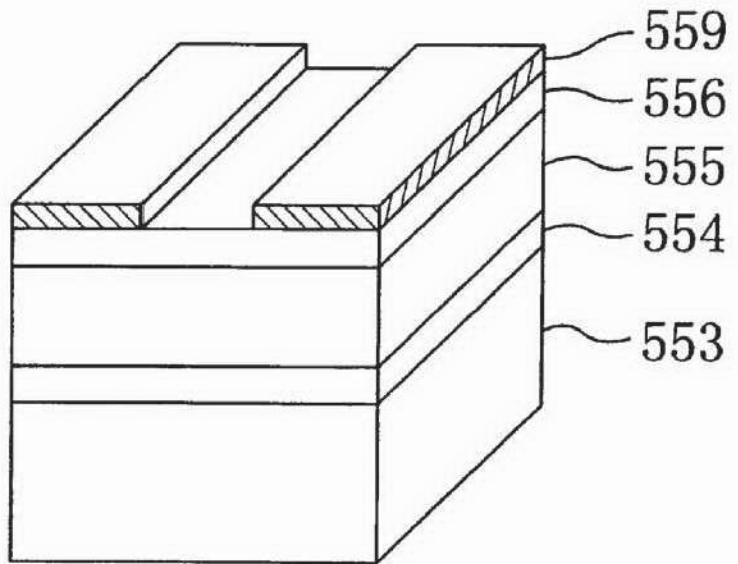


Fig. 27 (b)

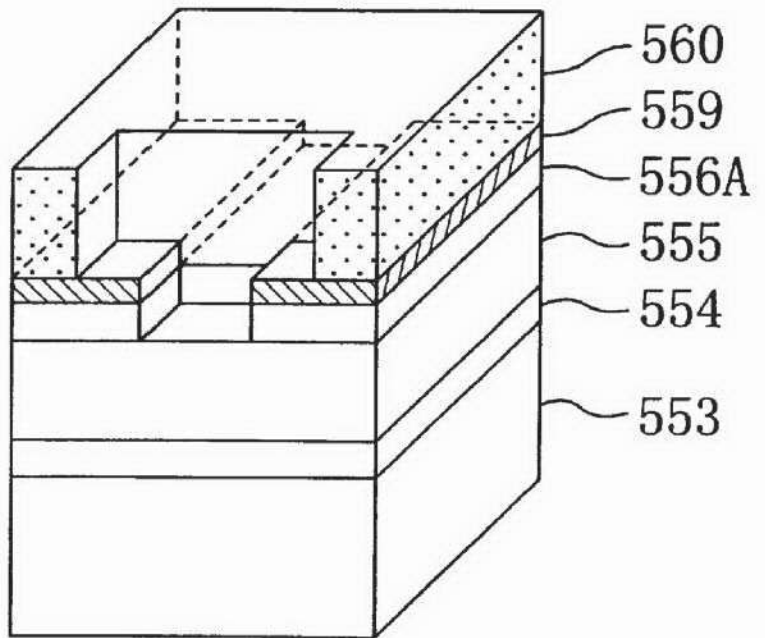


Fig. 28 (a)

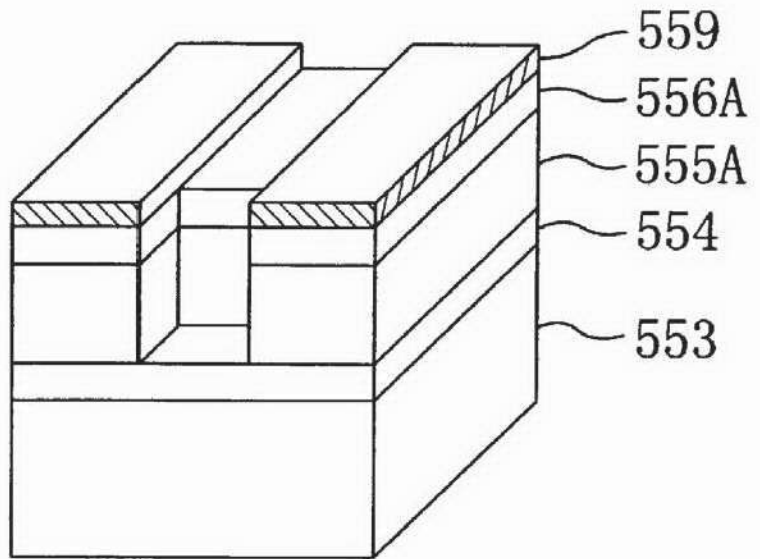


Fig. 28 (b)

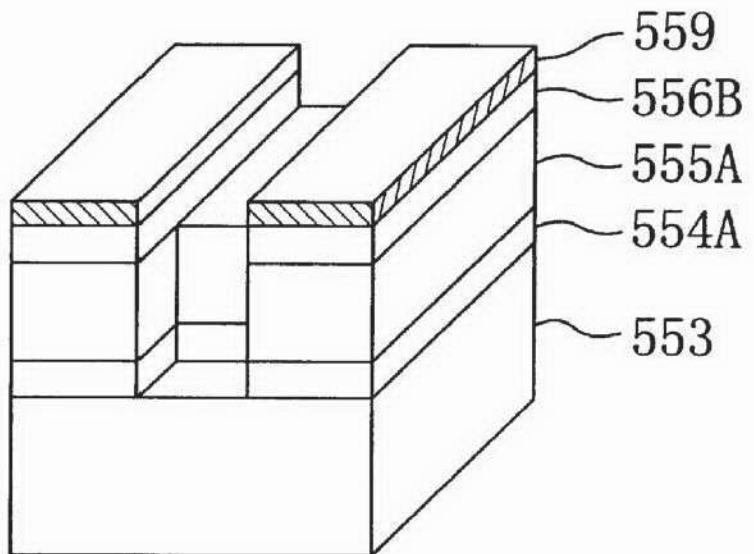


Fig. 29 (a)

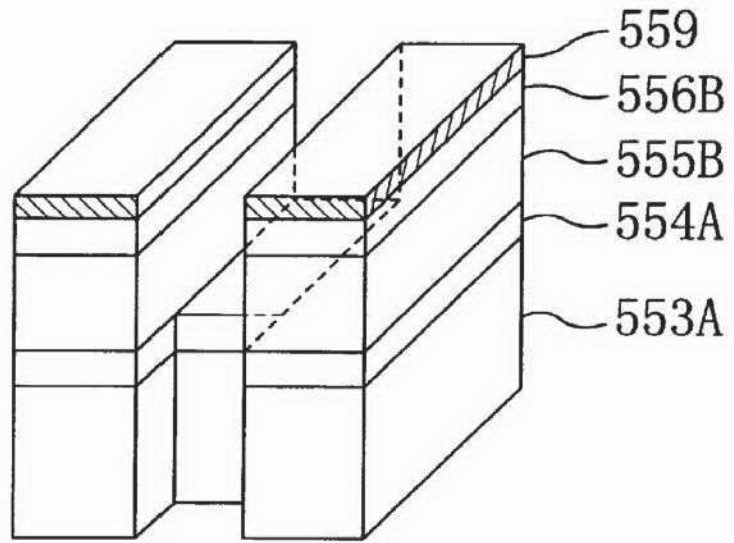


Fig. 29 (b)

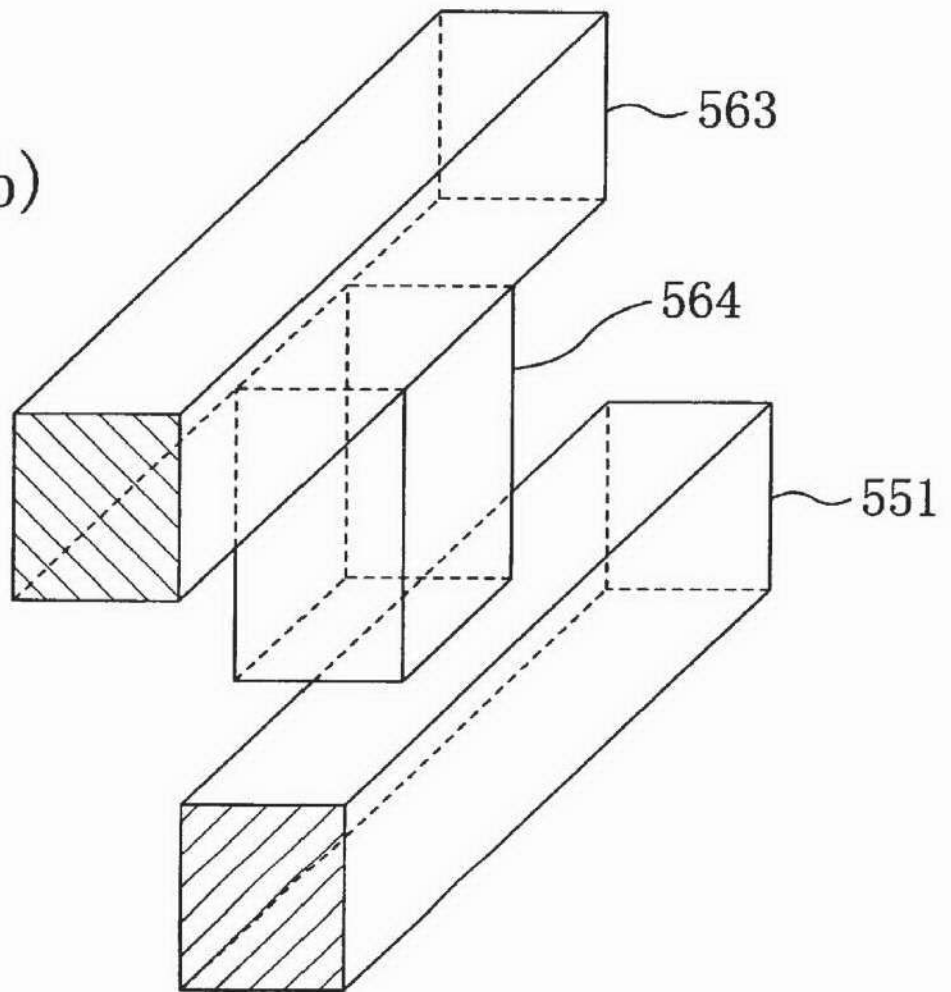




Fig. 30 (a)

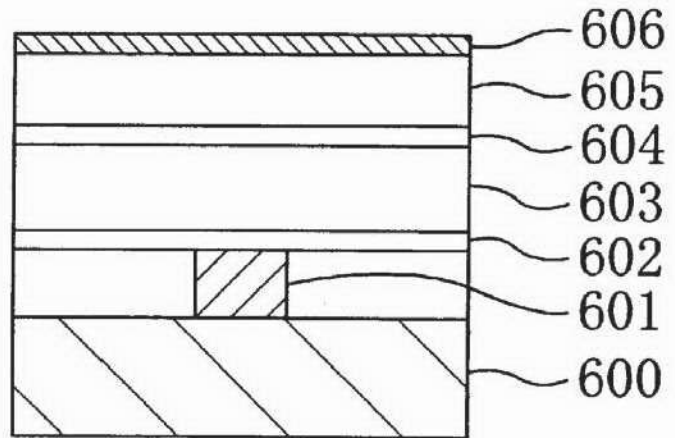


Fig. 30 (b)

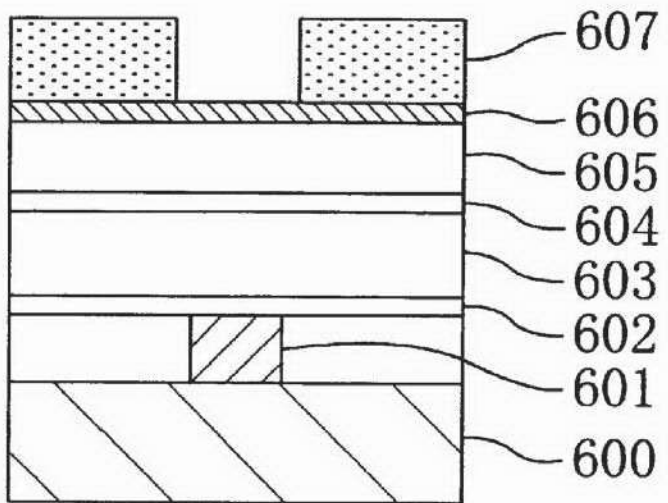


Fig. 30 (c)

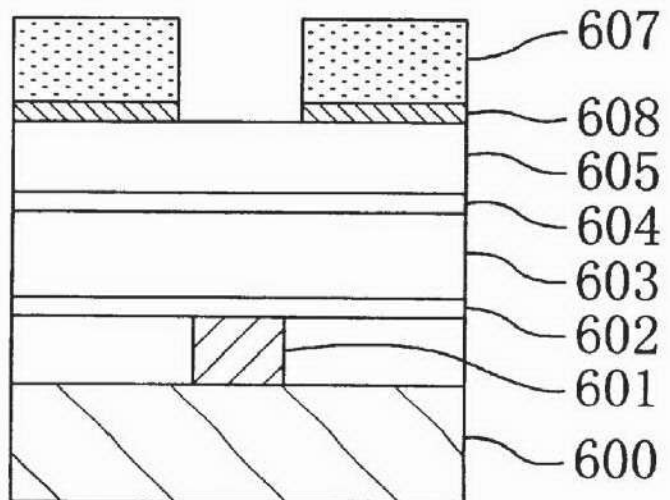


Fig. 31 (a)

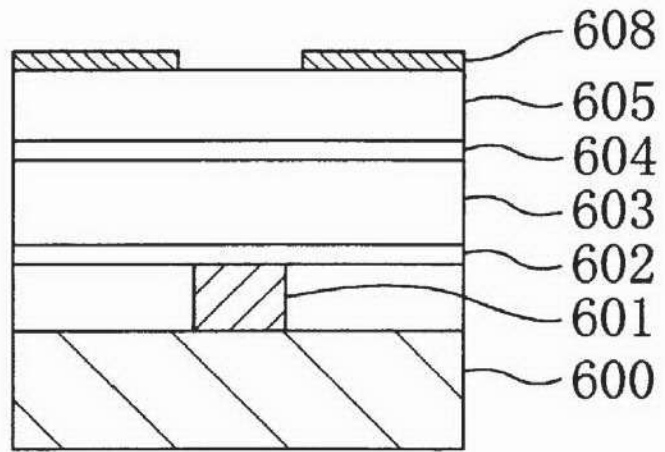


Fig. 31 (b)

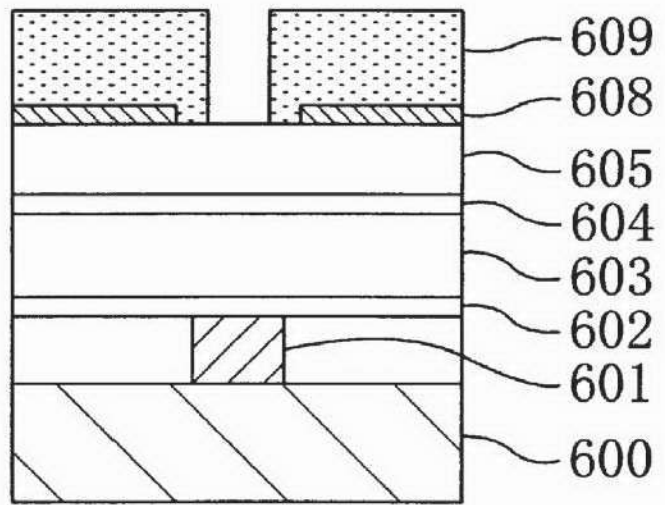


Fig. 31 (c)

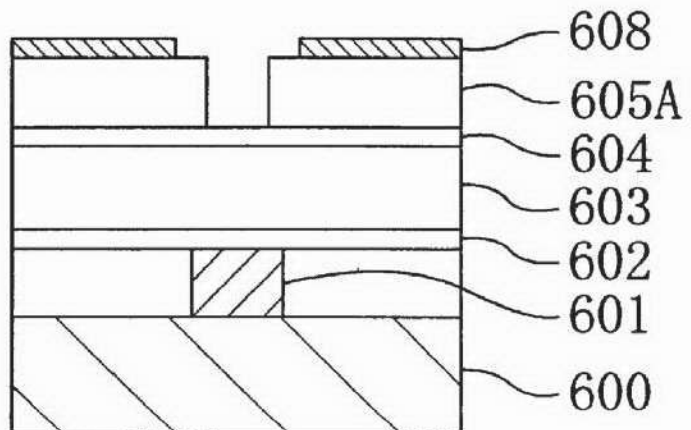


Fig. 32 (a)

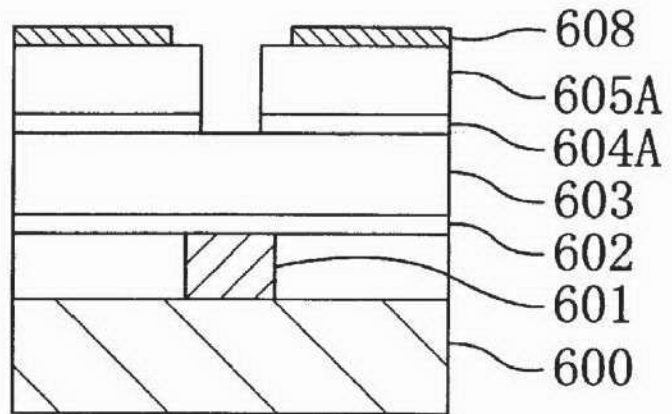


Fig. 32 (b)

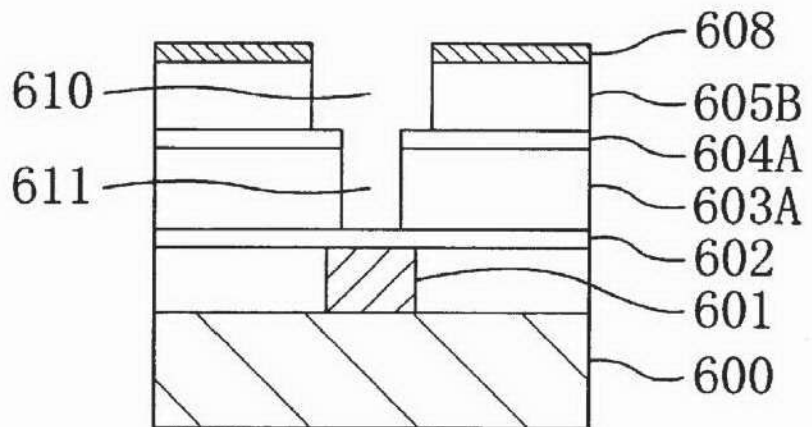


Fig. 32 (c)

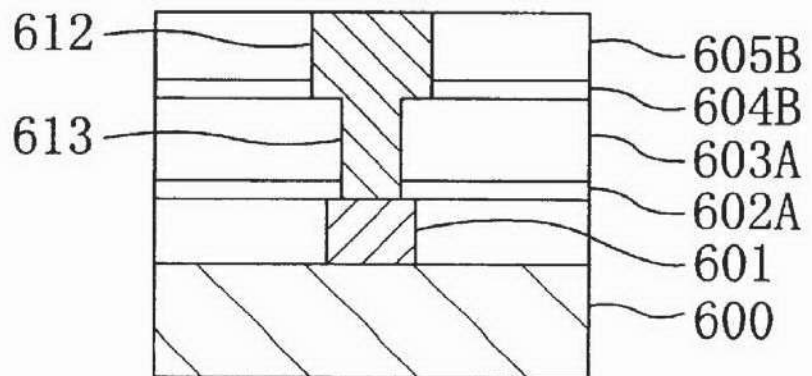


Fig. 33 (a)

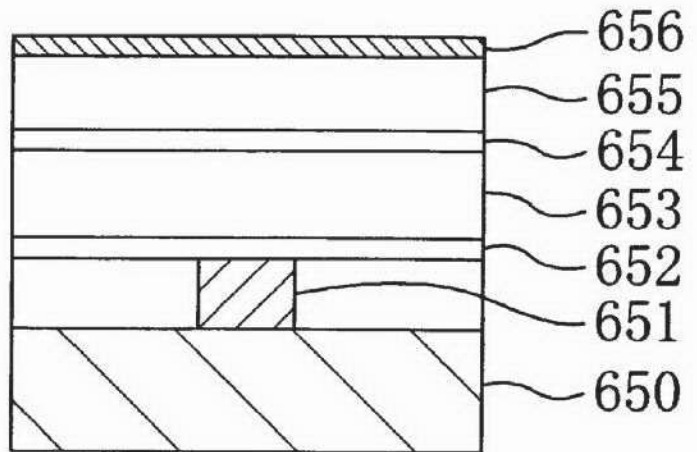


Fig. 33 (b)

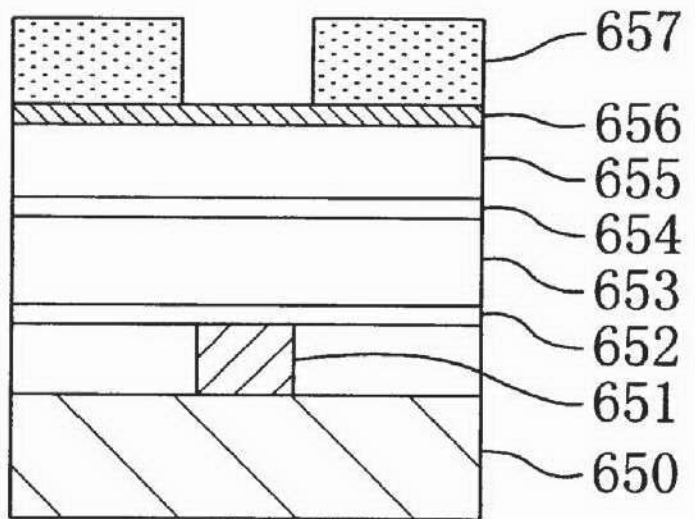


Fig. 33 (c)

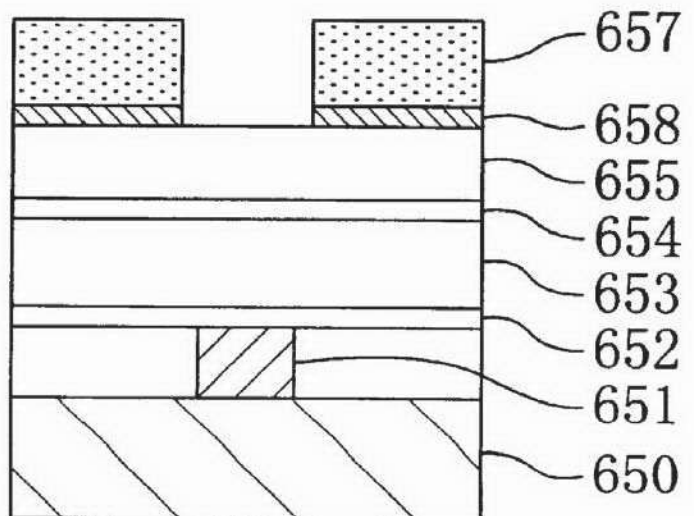


Fig. 34(a)

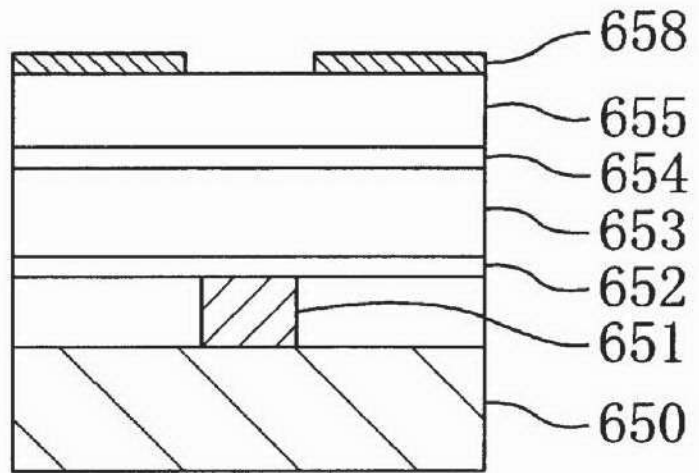


Fig. 34(b)

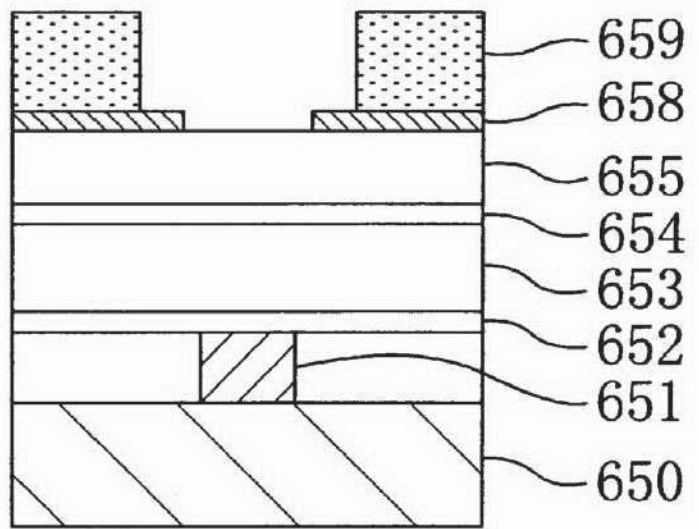


Fig. 34(c)

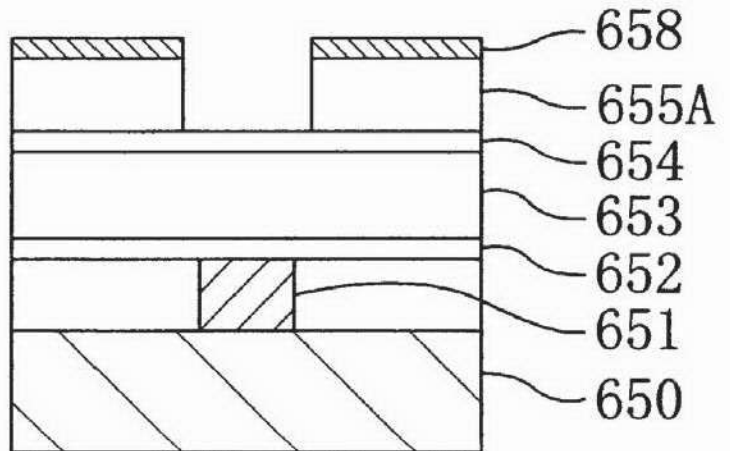


Fig. 35 (a)

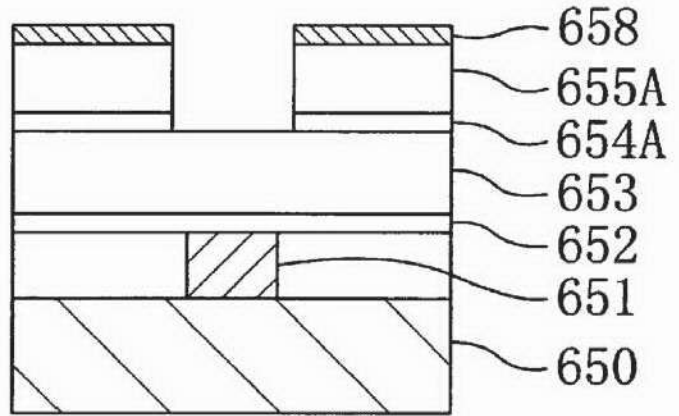


Fig. 35 (b)

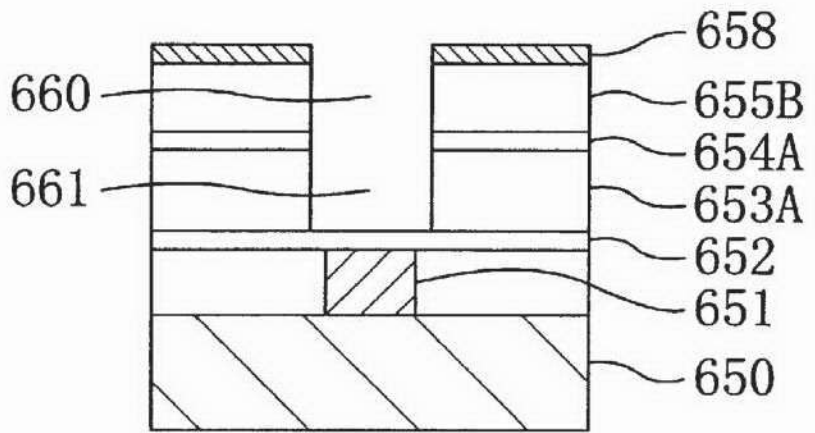


Fig. 35 (c)

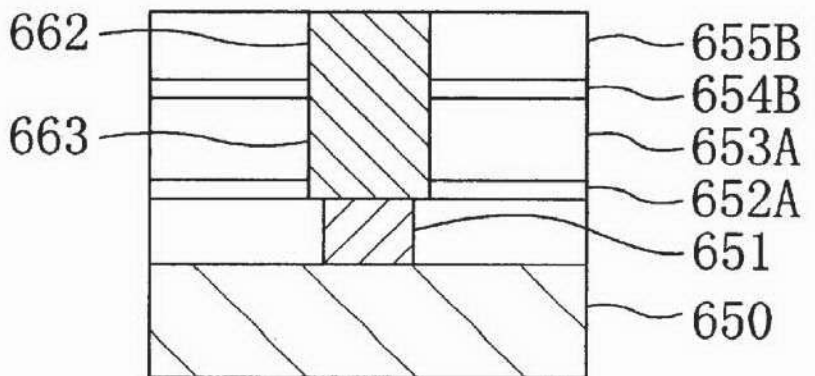


Fig. 36

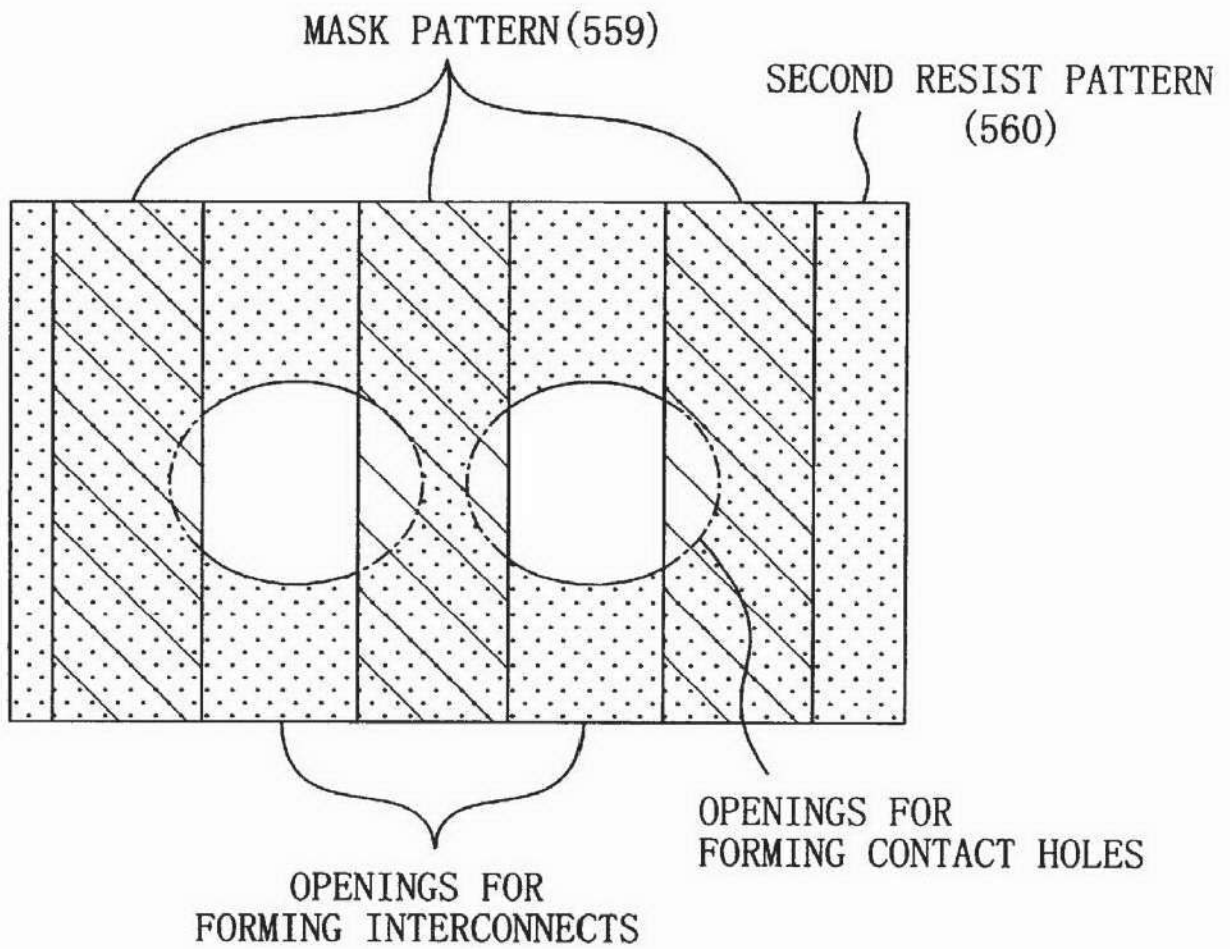


Fig. 37 (a)

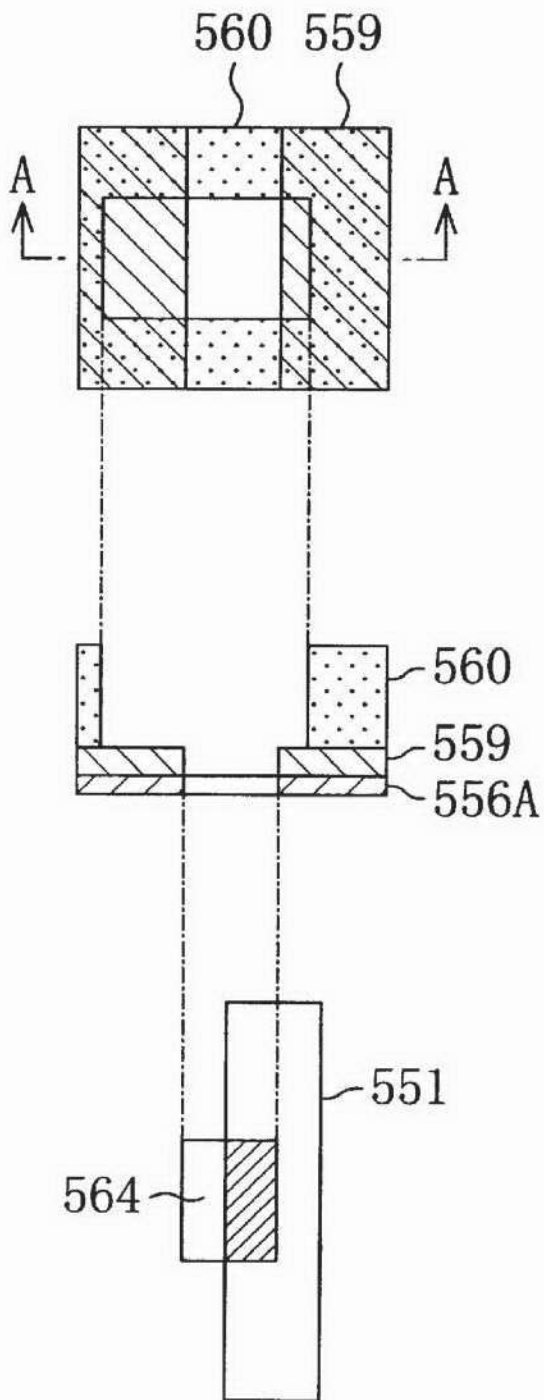
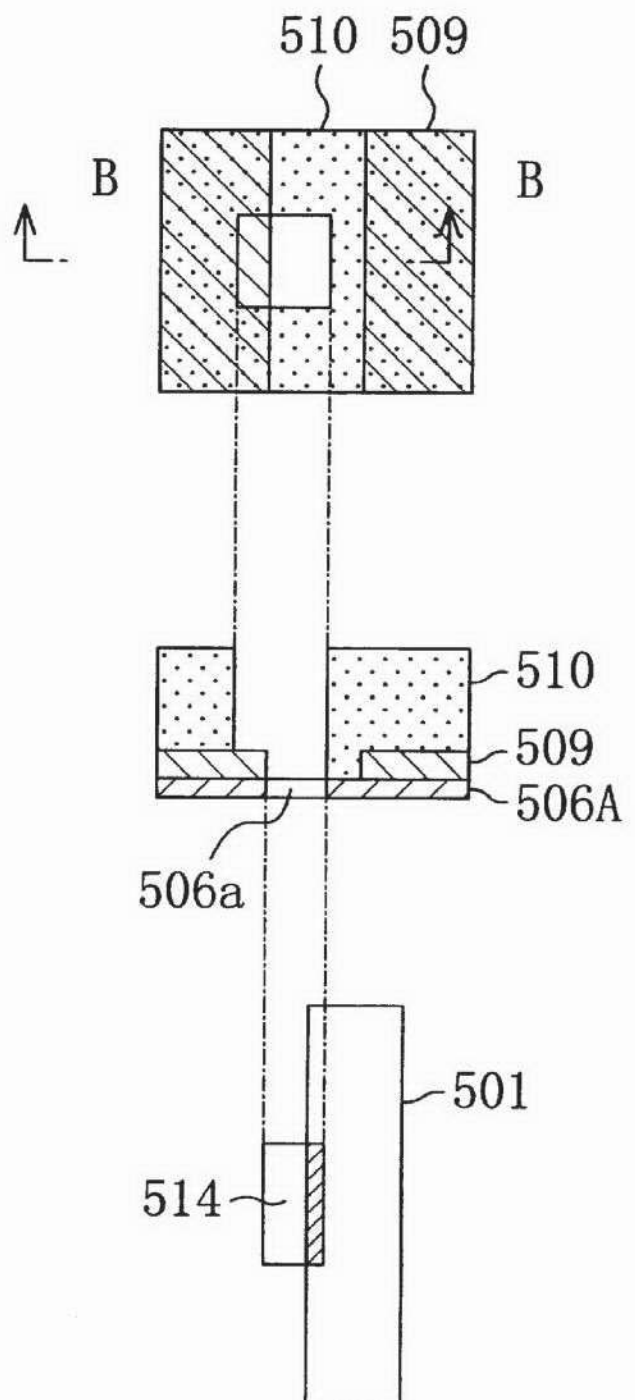


Fig. 37 (b)





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## METHOD FOR FORMING INTERCONNECTION STRUCTURE

### BACKGROUND OF THE INVENTION

The present invention relates to a method for forming an interconnection structure in a semiconductor integrated circuit.

As the number of devices, integrated within a single semiconductor integrated circuit, has been tremendously increasing these days, wiring delay has also been increasing noticeably. This is because the larger the number of devices integrated, the larger line-to-line capacitance (i.e., parasitic capacitance between metal interconnects), thus interfering with the performance improvement of a semiconductor integrated circuit. The wiring delay is so-called "RC delay", which is proportional to the product of the resistance of metal interconnection and the line-to-line capacitance.

In other words, to reduce the wiring delay, either the resistance of metal interconnection or the line-to-line capacitance should be reduced.

In order to reduce the interconnection resistance, IBM Corp., Motorola, Inc., etc. have reported semiconductor integrated circuits using copper, not aluminum alloy, as a material for metal interconnects. A copper material has a specific resistance about two-thirds as high as that of an aluminum alloy material. Accordingly, in accordance with simple calculation, the wiring delay involved with the use of a copper material for metal interconnects can be about two-thirds of that involved with the use of an aluminum alloy material therefor. That is to say, the operating speed can be increased by about 1.5 times.

However, the number of devices, integrated within a single semiconductor integrated circuit, is expected to further increase by leaps and bounds from now on, thus increasing the wiring delay considerably. Therefore, it is concerned that even the use of copper as an alternate metal interconnection material would not be able to catch up with such drastic increase. Also, the specific resistance of copper as a metal interconnection material is just a little bit higher than, but almost equal to, that of gold or silver. Accordingly, even if gold or silver is used instead of copper as a metal interconnection material, the wiring delay can be reduced only slightly.

Under these circumstances, not only reducing interconnection resistance but also suppressing line-to-line capacitance play a key role in further increasing the number of devices that can be integrated within a single semiconductor integrated circuit. And the relative dielectric constant of an interlevel insulating film should be reduced to suppress the line-to-line capacitance. A silicon dioxide film has heretofore been used as a typical material for an interlevel insulating film. The relative dielectric constant of a silicon dioxide film is, however, about 4 to about 4.5. Thus, it would be difficult to apply a silicon dioxide film to a semiconductor integrated circuit incorporating an even larger number of devices.

In order to solve such a problem, fluorine-doped silicon dioxide film, low-dielectric-constant spin-on-glass (SOG) film, organic polymer film and so on have been proposed as alternate interlevel insulating films with respective relative dielectric constants smaller than that of a silicon dioxide film.

The relative dielectric constant of a fluorine-doped silicon dioxide film is about 3.3 to about 3.7, which is about 20 percent lower than that of a conventional silicon dioxide

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film. Nevertheless, a fluorine-doped silicon dioxide film is highly hygroscopic, and easily absorbs water in the air, resulting in various problems in practice. For example, when the fluorine-doped silicon dioxide film absorbs water, SiOH groups, having a high relative dielectric constant, are introduced into the film. As a result, the relative dielectric constant of the fluorine-doped silicon dioxide film adversely increases, or the SiOH groups react with the water during a heat treatment to release H<sub>2</sub>O gas. In addition, fluorine free radicals, contained in the fluorine-doped silicon dioxide film, segregate near the surface thereof during a heat treatment and react with Ti, contained in a TiN layer formed thereon as an adhesion layer, to form a TiF film, which easily peels off.

An HSQ (hydrogen silsesquioxane) film, composed of Si, O and H atoms, is an exemplary low-dielectric-constant SOG film. In the HSQ film, the number of the H atoms is about two-thirds of that of the O atoms. However, the HSQ film releases a larger amount of water than a conventional silicon dioxide film. Accordingly, since it is difficult to form a buried interconnection line in the HSQ film, a patterned metal film should be formed as metal interconnects on the HSQ film.

Also, since the HSQ film cannot adhere so strongly to metal interconnects, a CVD oxide film should be formed between the metal interconnects and the HSQ film to improve the adhesion therebetween. However, in such a case, if the CVD oxide film is formed on the metal interconnects, then the substantial line-to-line capacitance is equal to the serial capacitance formed by the HSQ and CVD films. This is because the CVD oxide film with a high dielectric constant exists between the metal interconnects. Accordingly, the resulting line-to-line capacitance is larger as compared with using the HSQ film alone.

An organic polymer film, as well as the low-dielectric-constant SOG film, cannot adhere strongly to metal interconnects, either. Accordingly, a CVD oxide film should be formed as an adhesion layer between the metal interconnects and the organic polymer film, too.

Moreover, an etch rate, at which an organic polymer film is etched, is approximately equal to an ash rate, at which a resist pattern is ashed with oxygen plasma. Accordingly, a usual resist application process is not applicable in such a situation, because the organic polymer film is likely to be damaged during ashing and removing the resist pattern. Therefore, a proposed alternate process includes: forming a CVD oxide film on an organic polymer film; forming a resist film on the CVD oxide film; and then etching the resist film using the CVD oxide film as an etch stopper, or a protective film.

However, during the step of forming the CVD oxide film on the organic polymer film, the surface of the organic polymer film is exposed to a reactive gas containing oxygen. Accordingly, the organic polymer film reacts with oxygen to take in polar groups such as carbonyl groups and ketone groups. As a result, the relative dielectric constant of the organic polymer film disadvantageously increases.

Also, in forming inlaid copper interconnects in the organic polymer film, a TiN adhesion layer, for example, should be formed around wiring grooves formed in the organic polymer film, because the organic polymer film cannot adhere strongly to the metal interconnects. However, since the TiN film has a high resistance, the effective cross-sectional area of the metal interconnects decreases. Consequently, the intended effect attainable by the use of the copper lines, i.e., reduction in resistance, would be lost.

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## SUMMARY OF THE INVENTION

An object of the present invention is providing a method for forming an interconnection structure in which an insulating film with a low dielectric constant can be formed by an ordinary resist application process.

A first method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the thin film; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; g) forming a second resist pattern, having a plurality of openings for forming contact holes, on the third insulating film; h) dry-etching the third insulating film under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left; i) dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes; j) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the first method of the present invention, the third insulating film is dry-etched under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film and removing the first and second resist patterns in the step h). Accordingly, it is not necessary to perform the step of ashing and removing the first and second resist patterns with oxygen plasma. In other words, since it is possible to prevent the third insulating film from being damaged during ashing and removing a resist pattern, a low-dielectric-constant insulating film, which would otherwise be damaged easily by oxygen plasma, may be used as the third insulating film. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In addition, the second insulating film can be used as an etch stopper while the wiring grooves are formed by dry-etching the third insulating film using the mask pattern as a mask in the step j). Accordingly, the depth of each wiring groove can be equalized with the thickness of the third

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insulating film. That is to say, the depth of the wiring grooves can be defined by self-alignment.

Moreover, the composition of the second insulating film is different from that of the third insulating film. Thus, the second insulating film can be used as an etch stopper while the wiring grooves are formed by dry-etching the third insulating film using the mask pattern as a mask in the step j).

In one embodiment of the present invention, the first method preferably further includes the step of forming a metal adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes between the steps j) and k).

In such an embodiment, the adhesion between the upper-level metal interconnects and the third insulating film and between the contacts and the first insulating film can be improved.

In another embodiment of the present invention, the third insulating film is preferably mainly composed of an organic component.

In such an embodiment, the conditions employed in the step h), i.e., that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, are realized with much more certainty.

In this embodiment, the step c) preferably includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin.

Then, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the third insulating film with a lot more certainty.

In another embodiment, the first insulating film is also preferably mainly composed of an organic component.

Then, the conditions employed in the step i), i.e., that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, are realized with much more certainty. At the same time, the conditions employed in the step j), i.e., that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, are also realized with much more certainty.

In an embodiment where the first and third insulating films are both mainly composed of organic components, the first method preferably further includes the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process using a reactive gas containing nitrogen between the steps j) and k).

In such a case, the adhesion between the upper-level metal interconnects and the third insulating film mainly composed of an organic component, and between the contacts and the first insulating film mainly composed of an organic component can be improved substantially without fail.

In the embodiment where the first insulating film is mainly composed of an organic component, the step a) preferably includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin.

In such a case, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the first insulating film with a lot more certainty.



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A second method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the thin film; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; g) forming a second resist pattern, having a plurality of openings for forming contact holes, on the third insulating film; h) dry-etching the third insulating film using the first and second resist patterns as a mask under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes; i) dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films and the first and second resist patterns are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes; j) removing the first and second resist patterns; k) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and l) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the second method of the present invention, even if a damaged layer is formed in respective parts of the first and third insulating films that are exposed inside the openings for forming contact holes in the second insulating film during the step j) of removing the first and second resist patterns, the damaged layer can be removed without fail in the next step k). In this step, the third and first insulating films are dry-etched using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively. Accordingly, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, the third insulating film is preferably a low-dielectric-constant SOG film with a siloxane skeleton.

In such an embodiment, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

A third method for forming an interconnection structure according to the present invention includes the steps of: a)

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forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film; e) forming a thin film over the fourth insulating film; f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves; g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes; i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes; j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes; k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes; l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the third method of the present invention, the fourth insulating film exists on the third insulating film during the removal of the first resist pattern in the step h). Accordingly, even if the first resist pattern is removed by oxygen plasma, the third insulating film is not damaged. Also, the second insulating film exists on the first insulating film during dry-etching the third insulating film in the step j). Accordingly, the first insulating film is not damaged, either. Thus, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma or dry etching, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, at least one of the first and third insulating films is preferably mainly composed of an organic component.

In such an embodiment, the relative dielectric constant of the interlevel insulating film can be reduced.

In another embodiment of the present invention, a size of the openings of the second resist pattern for forming contact holes is preferably larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

In such an embodiment, even if the openings of the second resist pattern for forming contact holes have misaligned with the openings of the mask pattern for forming wiring grooves, the openings of the patterned fourth insu-

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lating film for forming contact holes can be formed to be self-aligned with the openings of the mask pattern for forming wiring grooves. This is because the openings of the patterned fourth insulating film for forming contact holes are formed in respective regions where the openings of the second resist pattern for forming contact holes overlap with corresponding openings of the mask pattern for forming wiring grooves. As a result, the connection between the contacts and the upper-level metal interconnects is ensured.

A fourth method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes; h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes; i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes; j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the fourth method of the present invention, the second insulating film exists on the first insulating film during dry-etching the third insulating film in the step h). Accordingly, the first insulating film is not damaged. Thus, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma or dry etching, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, at least one of the first and third insulating films is preferably mainly composed of an organic component.

In such an embodiment, the relative dielectric constant of the interlevel insulating film can be reduced.

In another embodiment of the present invention, a size of the openings of the second resist pattern for forming contact holes is preferably larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

In such an embodiment, even if the openings of the second resist pattern for forming contact holes have misaligned with the openings of the mask pattern for forming wiring grooves, the openings of the patterned third insulating film for forming contact holes can be formed to be self-aligned with the openings of the mask pattern for

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forming wiring grooves. This is because the openings of the patterned third insulating film for forming contact holes are formed in respective regions where the openings of the second resist pattern for forming contact holes overlap with corresponding openings of the mask pattern for forming wiring grooves. As a result, the connection between the contacts and the upper-level metal interconnects is ensured.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1(a) through 1(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the first embodiment of the present invention.

FIGS. 2(a) through 2(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

FIGS. 3(a) through 3(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

FIGS. 4(a) through 4(c) are cross-sectional views illustrating problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. 5(a) through 5(c) are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. 6(a) through 6(c) are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. 7(a) through 7(c) are cross-sectional views illustrating measures to solve the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. 8(a) through 8(c) are cross-sectional views illustrating the measures to solve the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. 9(a) through 9(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the second embodiment of the present invention.

FIGS. 10(a) through 10(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

FIGS. 11(a) through 11(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

FIGS. 12(a) through 12(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the third embodiment of the present invention.

FIGS. 13(a) through 13(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

FIGS. 14(a) through 14(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

FIGS. 15(a) through 15(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to a modified example of the third embodiment.



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FIGS. 16(a) through 16(d) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the modified example of the third embodiment.

FIGS. 17(a) through 17(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the modified example of the third embodiment.

FIGS. 18(a) through 18(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the fourth embodiment of the present invention.

FIGS. 19(a) through 19(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fourth embodiment.

FIGS. 20(a) through 20(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fourth embodiment.

FIGS. 21(a) through 21(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the fifth embodiment of the present invention.

FIGS. 22(a) through 22(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fifth embodiment.

FIGS. 23(a) through 23(d) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fifth embodiment.

FIGS. 24(a) through 24(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to a modified example of the fifth embodiment.

FIGS. 25(a) through 25(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. 26(a) through 26(d) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. 27(a) and 27(b) are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. 28(a) and 28(b) are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. 29(a) and 29(b) are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. 30(a) through 30(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the sixth embodiment of the present invention.

FIGS. 31(a) through 31(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the sixth embodiment.

FIGS. 32(a) through 32(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the sixth embodiment.

FIGS. 33(a) through 33(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to a modified example of the sixth embodiment.

FIGS. 34(a) through 34(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the sixth embodiment.

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FIGS. 35(a) through 35(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the sixth embodiment.

FIG. 36 is a plan view illustrating a positional relationship between the openings of a mask pattern for forming wiring grooves and the openings of a second resist pattern for forming contact holes in the modified example of the fifth embodiment.

FIG. 37(a) illustrates respective positional relationships between the mask pattern and the second resist pattern and between a first metal interconnect and an associated contact in the modified example of the fifth embodiment; and

FIG. 37(b) illustrates respective positional relationships between the mask pattern and the second resist pattern and between a first metal interconnect and an associated contact in the fifth embodiment.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

### EMBODIMENT 1

Hereinafter, an exemplary method for forming an interconnection structure according to the first embodiment of the present invention will be described with reference to FIGS. 1(a) through 1(c), FIGS. 2(a) through 2(c) and FIGS. 3(a) through 3(c).

First, as shown in FIG. 1(a), a silicon nitride film 102 is formed over first metal interconnects 101 formed on a semiconductor substrate 100. The silicon nitride film 102 is formed to be 50 nm thick, for example, and used to protect the first metal interconnects 101 during a subsequent etching process step. Thereafter, a first organic film 103 (first insulating film), mainly composed of an organic component, is formed to be 1  $\mu$ m thick, for example, on the silicon nitride film 102. Next, an organic-containing silicon dioxide film 104 (second insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the first organic film 103. Then, a second organic film 105 (third insulating film), mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film 104. And a titanium nitride film 106 is formed to be 50 nm thick, for example, on the second organic film 105.

The first and second organic films 103 and 105 may be deposited by any arbitrary technique. For example, these films 103 and 105 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films 103 and 105.

Moreover, the first organic film 103 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin and organic silane such as hexamethyl disiloxane, arylalkoxy silane or alkylalkoxy silane. In such a case, an organic/inorganic hybrid film can be obtained.

Similarly, the organic-containing silicon dioxide film 104 may also be deposited by any arbitrary technique. For instance, the film 104 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. In such a case, an organic-containing silicon dioxide film 104, having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide, can be obtained.

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It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **103** and **105** and the organic-containing silicon dioxide film **104**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **106**.

Next, as shown in FIG. 1(b), a first resist pattern **107**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **106**. Thereafter, the titanium nitride film **106** is dry-etched using the first resist pattern **107** as a mask, thereby forming a mask pattern **108** out of the titanium nitride film **106** as shown in FIG. 1(c).

Subsequently, a second resist pattern **109**, having openings for forming contact holes, is formed by lithography on the second organic film **105** without removing the first resist pattern **107**. Then, the second organic film **105** is dry-etched, thereby forming a patterned second organic film **105A** having the openings for forming contact holes as shown in FIG. 2(a). In this case, since the second organic film **105** and the first and second resist patterns **107** and **109** are all mainly composed of organic components, the second organic film **105** is etched at a substantially equal rate to that of the first and second resist patterns **107** and **109**. Thus, when the second organic film **105** is dry-etched, the first and second resist patterns **107** and **109** are also removed simultaneously.

It should be noted that part of the second resist pattern **109** may be left in the process step of dry-etching the second organic film **105**. This is because the residual second resist pattern **109** can be removed during a subsequent process step of forming wiring grooves **111** in the patterned second organic film **105A** (see FIG. 2(c)).

Then, the organic-containing silicon dioxide film **104** is dry-etched using the patterned second organic film **105A** as a mask, thereby forming a patterned organic-containing silicon dioxide film **104A** having the openings for forming contact holes as shown in FIG. 2(b). In this process step, by selecting such etching conditions that the organic-containing silicon dioxide film **104** is etched at a rate higher than that of the patterned second organic film **105A**, it is possible to prevent the patterned second organic film **105A** from being erroneously etched.

Next, the patterned second organic film **105A** is dry-etched using the mask pattern **108** as a mask, thereby forming the wiring grooves **111** in the patterned second organic film **105A** as shown in FIG. 2(c). At the same time, the first organic film **103** is also dry-etched using the patterned organic-containing silicon dioxide film **104A** as a mask, thereby forming a patterned first organic film **103A** having the contact holes as shown in FIG. 2(c).

Subsequently, the silicon nitride film **102** is dry-etched using the patterned organic-containing silicon dioxide film **104A** as a mask, thereby forming a patterned silicon nitride film **102A** and exposing the first metal interconnects **101** within the contact holes **110** as shown in FIG. 3(a).

Then, as shown in FIG. 3(b), an adhesion layer **112**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **110** and the wiring grooves **111**. Thereafter, a metal film **113** is deposited over the entire surface of the substrate to completely fill in the contact holes **110** and the wiring grooves **111**. In this embodiment, the metal film **113** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **113** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

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Finally, as shown in FIG. 3(c), respective portions of the adhesion layer **112**, the metal film **113** and the mask pattern **108**, which are deposited on the patterned second organic film **105A**, are removed by a CMP technique, for example. As a result, second metal interconnects **114** and contacts **115**, connecting the first and second metal interconnects **101** and **114**, are formed out of the metal film **113**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **114** through the same process steps as those described above.

In the first embodiment, the organic-containing silicon dioxide film **104** is formed by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Accordingly, the film **104** has a structure in which a phenyl group (i.e., an exemplary organic group), bonded to a silicon atom, is introduced into silicon dioxide. Thus, the film **104** can be processed as well as a conventional CVD oxide film, and the relative dielectric constant of the film **104** is as low as that of the conventional CVD oxide film. In addition, the film **104** can adhere strongly to organic film, oxide film and metal film.

After the mask pattern **108** has been formed out of the titanium nitride film **106**, the second resist pattern **109** is formed without removing the first resist pattern **107**, and the first and second resist patterns **107** and **109** are removed while the second organic film **105** is dry-etched. Thus, it is no longer necessary to ash and remove the first and second resist patterns **107** and **109** with oxygen plasma. That is to say, it is possible to prevent the second organic film **105** from being damaged during the step of ashing and removing a resist pattern. Accordingly, although the second organic film **105** with a low relative dielectric constant is used as an interlevel insulating film, an ordinary resist application process is applicable to this embodiment.

Moreover, the wiring grooves **111** are formed by dry-etching the patterned second organic film **105A** using the mask pattern **108** as a mask and using the patterned organic-containing silicon dioxide film **104A** as an etch stopper. Accordingly, the depth of the wiring grooves **111** matches with the thickness of the second organic film **105**. That is to say, the depth of the wiring grooves **111** can be defined by self-alignment.

Hereinafter, problems caused by the misalignment of the second resist pattern **109** with the first resist pattern **107** and the measured taken to solve the problems will be described.

First, it will be described with reference to FIGS. 4(a) through 4(c), FIGS. 5(a) through 5(c) and FIGS. 6(a) through 6(c) what problems are caused if the second resist pattern **109** has misaligned.

As in the first embodiment, a silicon nitride film **102** is first formed to be 50 nm thick, for example, over first metal interconnects **101** formed on a semiconductor substrate **100** as shown in FIG. 4(a). Thereafter, a first organic film **103**, mainly composed of an organic component, is formed to be 1  $\mu\text{m}$  thick, for example, on the silicon nitride film **102**.

Next, an organic-containing silicon dioxide film **104**, containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the first organic film **103**. Then, a second organic film **105**, mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film **104**. And a titanium nitride film **106** is formed to be 50 nm thick, for example, on the second organic film **105**.

Next, as shown in FIG. 4(b), a first resist pattern **107**, having openings for forming wiring grooves, is formed on



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the titanium nitride film 106. Thereafter, the titanium nitride film 106 is dry-etched using the first resist pattern 107 as a mask, thereby forming a mask pattern 108 out of the titanium nitride film 106 as shown in FIG. 4(c).

Subsequently, a second resist pattern 109, having openings for forming contact holes, is formed on the second organic film 105 without removing the first resist pattern 107. As can be seen if FIGS. 5(a) and 1(c) are compared with each other, the second resist pattern 109 has misaligned with the first resist pattern 107 in this case.

Then, the second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the openings for forming contact holes as shown in FIG. 5(a). As in the first embodiment, since the second organic film 105 and the first and second resist patterns 107 and 109 are all mainly composed of organic components, the first and second resist patterns 107 and 109 are removed simultaneously with the dry-etching of the second organic film 105. In this case, since the second resist pattern 109 has misaligned with the first resist pattern 107, the diameter of the openings for forming contact holes, which are provided in the second organic film 105A, is smaller than desired.

Then, the organic-containing silicon dioxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic-containing silicon dioxide film 104A having the openings for forming contact holes as shown in FIG. 5(c).

Next, the patterned second organic film 105A is dry-etched using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in FIG. 6(a). At the same time, the first organic film 103 is also dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes 110 as shown in FIG. 6(a). Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes 110 as shown in FIG. 6(b).

Then, an adhesion layer 112, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer 112, the metal film and the mask pattern 108, which are deposited on the patterned second organic film 105A, are removed by a CMP technique, for example. As a result, second metal interconnects 114 are certainly formed. However, since the diameter of the contact holes 110 is smaller than desired, the contact holes 110 cannot be completely filled in with the metal film, and the first and second metal interconnects 101 and 112 cannot be connected to each other, resulting in a contact failure.

Next, it will be described with reference to FIGS. 7(a) through 7(c) and FIGS. 8(a) through 8(c) what measures should be taken to solve the problems caused by the misalignment of the second resist pattern 109.

First, a second resist pattern 109, having openings for forming contact holes, is formed through the same process steps as those described with reference to FIGS. 4(a) through 4(c) and FIG. 5(a). In this case, the second resist pattern 109 has also misaligned with the first resist pattern 107 (see FIG. 5(a)).

Thus, as shown in FIG. 7(a), the first resist pattern 107 and the mask pattern 108 are dry-etched using the second

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resist pattern 109 as a mask. In this manner, portions of the first resist pattern 107, not overlapping with the second resist pattern 109, are removed and each opening of the mask pattern 108 is expanded to be equal to or larger than each opening for forming wiring grooves or each opening for forming contact holes. As a result, the pattern for the openings of the second resist pattern for forming contact holes 109 can be transferred to the first resist pattern 107 and the mask pattern 108.

Then, the second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the openings for forming contact holes as shown in FIG. 7(b). In this case, since the second organic film 105 and the first and second resist patterns 107 and 109 are all mainly composed of organic components, the first and second resist patterns 107 and 109 are removed simultaneously with the dry-etching of the second organic film 105.

Then, the organic-containing silicon dioxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic-containing silicon dioxide film 104A having the openings for forming contact holes as shown in FIG. 7(c).

As described above, the second resist pattern 109 has misaligned with the first resist pattern 107. However, in this case, the pattern for the openings of the second resist pattern for forming contact holes 109 has been successfully transferred to the first resist pattern 107 and the mask pattern 108. Thus, the diameter of the openings for forming contact holes, which have been formed in the patterned second organic film 105A and the patterned organic-containing silicon dioxide film 104A, is a predetermined size.

Next, the patterned second organic film 105A is dry-etched using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in FIG. 8(a). At the same time, the first organic film 103 is also dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes 110 as shown in FIG. 8(a). Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes 110 as shown in FIG. 8(b).

Then, an adhesion layer 112, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer 112, the metal film and the mask pattern 108, which are deposited on the patterned second organic film 105A, are removed by a CMP technique, for example. As a result, second metal interconnects 114 and contacts 115 are formed out of the titanium nitride film 112 and the metal film as shown in FIG. 8(c).

## EMBODIMENT 2

Next, an exemplary method for forming an interconnection structure according to the second embodiment of the present invention will be described with reference to FIGS. 9(a) through 9(c), FIGS. 10(a) through 10(c) and FIGS. 11(a) through 11(c).

First, as shown in FIG. 9(a), a silicon nitride film 202 is formed to be 50 nm thick, for example, over first metal interconnects 201 formed on a semiconductor substrate 200. Thereafter, a first organic film 203 (first insulating film),

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mainly composed of an organic component, is formed to be 1  $\mu\text{m}$  thick, for example, on the silicon nitride film 202. Next, an organic-containing silicon dioxide film 204 (second insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the first organic film 203. Then, a second organic film 205 (third insulating film), mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film 204. And a titanium nitride film 206 is formed to be 50 nm thick, for example, on the second organic film 205.

The first and second organic films 203 and 205 may be deposited by any arbitrary technique. For example, these films 203 and 205 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films 203 and 205.

Similarly, the organic-containing silicon dioxide film 204 may also be deposited by any arbitrary technique. For instance, the film 204 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films 203 and 205 and the organic-containing silicon dioxide film 204, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 206.

Next, as shown in FIG. 9(b), a first resist pattern 207, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 206. Thereafter, the titanium nitride film 206 is dry-etched using the first resist pattern 207 as a mask, thereby forming a mask pattern 208 out of the titanium nitride film 206 as shown in FIG. 9(c).

Subsequently, a second resist pattern 209, having openings for forming contact holes, is formed by lithography on the second organic film 205 without removing the first resist pattern 207. Then, the second organic film 205 is dry-etched, thereby forming a patterned second organic film 205A having the openings for forming contact holes as shown in FIG. 10(a). In this case, since the second organic film 205 and the first and second resist patterns 207 and 209 are all mainly composed of organic components, the second organic film 205 is etched at a rate substantially equal to that of the first and second resist patterns 207 and 209. Accordingly, when the second organic film 205 is dry-etched, the first and second resist patterns 207 and 209 are also removed simultaneously.

If the second resist pattern 209 may have been misaligned with the first resist pattern 207, then the first resist pattern 207 and the mask pattern 208 should be dry-etched using the second resist pattern 209 as a mask. In this manner, parts of the first resist pattern 207, not overlapping with the second resist pattern 209, are removed and the openings of the mask pattern 208 are expanded to be equal to or larger than the openings for forming wiring grooves and contact holes as described in the first embodiment.

Then, the organic-containing silicon dioxide film 204 is dry-etched using the patterned second organic film 205A as a mask, thereby forming a patterned organic-containing silicon dioxide film 204A having the openings for forming contact holes as shown in FIG. 10(b). Next, the patterned second organic film 205A is dry-etched using the mask pattern 208 as a mask, thereby forming the wiring grooves

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211 in the patterned second organic film 205A as shown in FIG. 10(c). At the same time, the first organic film 203 is also dry-etched using the patterned organic-containing silicon dioxide film 204A as a mask, thereby forming a patterned first organic film 203A having the contact holes 210 as also shown in FIG. 10(c).

Subsequently, the silicon nitride film 202 is dry-etched using the patterned organic-containing silicon dioxide film 204A as a mask, thereby forming a patterned silicon nitride film 202A and exposing the first metal interconnects 201 within the contact holes 210 as shown in FIG. 11(a).

Then, the patterned first and second organic films 203A and 205A are subjected to plasma processing using ammonium gas. As a result, as shown in FIG. 11(b), an adhesion layer 212, including amino and amide groups, is deposited on the wall faces of the patterned first organic film 203A exposed inside the contact holes 210 and on the wall faces of the patterned second organic film 205A exposed inside the wiring grooves 211. Thereafter, a metal film 213 is deposited over the entire surface of the substrate to completely fill in the contact holes 210 and the wiring grooves 211. In this embodiment, the metal film 213 may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 213 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in FIG. 11(c), respective portions of the metal film 213 and the mask pattern 208, which are deposited on the patterned second organic film 205A, are removed by a CMP technique, for example. As a result, second metal interconnects 214 and contacts 215 are formed out of the metal film 213.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 214 through the same process steps as those described above.

### EMBODIMENT 3

Next, an exemplary method for forming an interconnection structure according to the third embodiment of the present invention will be described with reference to FIGS. 12(a) through 12(c), FIGS. 13(a) through 13(c) and FIGS. 14(a) through 14(c).

First, as shown in FIG. 12(a), a silicon nitride film 302 is formed over first metal interconnects 301 formed on a semiconductor substrate 300. The silicon nitride film 302 is formed to be 50 nm thick, for example, and to protect the first metal interconnects 301 during a subsequent etching process step. Thereafter, a first organic-containing silicon dioxide film 303 (first insulating film), containing an organic component in silicon dioxide, is formed to be 1  $\mu\text{m}$  thick, for example, on the silicon nitride film 302. Next, a low-dielectric-constant SOG film 304 (second insulating film), having a siloxane skeleton, is deposited to be 400 nm thick, for example, on the first organic-containing silicon dioxide film 303. Then, a second organic-containing silicon dioxide film 305 (third insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the low-dielectric-constant SOG film 304. And a titanium nitride film 306 is formed to be 50 nm thick, for example, on the second organic-containing silicon dioxide film 305.

The first and second organic-containing silicon dioxide films 303 and 305 may be deposited by any arbitrary technique. For example, these films 303 and 305 may be



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deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Also, an HSQ film may be used as the low-dielectric-constant SOG film 304 with a siloxane skeleton.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic-containing silicon dioxide films 303 and 305 and the low-dielectric-constant SOG film 304, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 306.

Next, as shown in FIG. 12(b), a first resist pattern 307, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 306. Thereafter, the titanium nitride film 306 is dry-etched using the first resist pattern 307 as a mask, thereby forming a mask pattern 308 out of the titanium nitride film 306 as shown in FIG. 12(c).

Subsequently, as shown in FIG. 13(a), the first resist pattern 307 is removed and then a second resist pattern 309, having openings for forming contact holes, is formed on the second organic-containing silicon dioxide film 305. Then, the second organic-containing silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic-containing silicon dioxide film 303 are sequentially dry-etched using the second resist pattern 309 as a mask. As a result, a patterned second organic-containing silicon dioxide film 305A, a patterned low-dielectric-constant SOG film 304A and a patterned first organic-containing silicon dioxide film 303A having contact holes 310 are formed as shown in FIG. 13(b).

Next, as shown in FIG. 13(c), the second resist pattern 309 is removed and the patterned second organic-containing silicon dioxide film 305A is dry-etched using the mask pattern 308 as a mask, thereby forming openings for forming wiring grooves in the patterned second organic-containing silicon dioxide film 305A. Thereafter, the patterned low-dielectric-constant SOG film 304A is dry-etched using the mask pattern 308 and the patterned second organic-containing silicon dioxide film 305A having the openings for wiring grooves as a mask, thereby forming the wiring grooves 311. In forming the wiring grooves 311, by selecting such etching conditions that the first organic-containing silicon dioxide film 303A is etched at a rate sufficiently lower than that of the low-dielectric-constant SOG film 304A, sufficient selectivity can be secured for the patterned first organic-containing silicon dioxide film 303A. Accordingly, the depth of the wiring grooves 311 can be determined univalently at the sum of the thicknesses of the second organic-containing silicon dioxide film 305 and the low-dielectric-constant SOG film 304.

If the second resist pattern 309 may have been misaligned with the first resist pattern 307, the mask pattern 308 should be dry-etched using the second resist pattern 309 as a mask before the second organic-containing silicon dioxide film 305 is dry-etched using the second resist pattern 309 as a mask. That is to say, if the mask pattern 308 is partially exposed inside the openings of the second resist pattern 309 for forming contact holes because of the misalignment of the second resist pattern 309 with the first resist pattern 307, then the mask pattern 308 is dry-etched using the second resist pattern 309 as a mask. In this manner, the openings of the mask pattern 308 are expanded to include the openings for forming wiring grooves and contact holes.

Subsequently, the silicon nitride film 302 is dry-etched using the patterned first organic-containing silicon dioxide film 303A as a mask, thereby forming a patterned silicon nitride film 302A and exposing the first metal interconnects 301 within the contact holes 310 as shown in FIG. 14(a).

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Then, as shown in FIG. 14(b), an adhesion layer 312, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 310 and the wiring grooves 311. Thereafter, a metal film 313 is deposited over the entire surface of the substrate to completely fill in the contact holes 310 and the wiring grooves 311. In this embodiment, the metal film 313 may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 313 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in FIG. 14(c), respective portions of the adhesion layer 312, the metal film 313 and the mask pattern 308, which are deposited on the patterned second organic-containing silicon dioxide film 305A, are removed by a CMP technique, for example. As a result, second metal interconnects 314 and contacts 315, connecting the first and second metal interconnects 301 and 314, are formed out of the metal film 313.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 314 through the same process steps as those described above.

In the third embodiment, while the first resist pattern 307 is ashed and removed with oxygen plasma, the low-dielectric-constant SOG film 304 is not exposed to the oxygen plasma, because the second organic-containing silicon dioxide film 305 exists on the low-dielectric-constant SOG film 304.

Also, in this embodiment, after the second organic-containing silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic-containing silicon dioxide film 303 have been sequentially dry-etched using the second resist pattern 309 as a mask, the second resist pattern 309 is ashed and removed with oxygen plasma. Accordingly, the regions of the patterned low-dielectric-constant SOG film 304A, which are exposed inside the openings for forming contact holes, are exposed to oxygen plasma and damaged. However, the damaged layer, formed in the patterned low-dielectric-constant SOG film 304A, can be removed when the wiring grooves 311 are formed in the patterned low-dielectric-constant SOG film 304A, and does not have harmful effects on subsequent process steps.

Accordingly, the low-dielectric-constant SOG film 304 may be made of a material degradable with oxygen plasma. For example, in general, if an HSQ film is exposed to oxygen plasma, the Si—H bonds thereof are oxidized and the content of water and the relative dielectric constant thereof both increase to deteriorate the reliability and performance of the device. However, according to the third embodiment, the patterned low-dielectric-constant SOG film 304A, in which the wiring grooves 311 have already been formed, is not affected by oxygen plasma. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

#### MODIFIED EXAMPLE OF EMBODIMENT 3

Next, an exemplary method for forming an interconnection structure according to a modified example of the third embodiment of the present invention will be described with reference to FIGS. 15(a) through 15(c), FIGS. 16(a) through 16(c) and FIGS. 17(a) through 17(c).

First, as shown in FIG. 15(a), a silicon nitride film 352 is formed over first metal interconnects 351 formed on a

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semiconductor substrate **350**. The silicon nitride film **352** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **351** during a subsequent etching process step. Thereafter, a first silicon dioxide film **353** (first insulating film) is formed to be 1  $\mu\text{m}$  thick, for example, on the silicon nitride film **352**. Next, an organic film **354** (second insulating film) is deposited to be 400 nm thick, for example, on the first silicon dioxide film **353**. Then, a second silicon dioxide film **355** (third insulating film) is formed to be 50 nm thick, for example, on the organic film **354**. And a titanium nitride film **356** is formed to be 50 nm thick, for example, on the second silicon dioxide film **355**.

The first and second silicon dioxide films **353** and **355** may be deposited by any arbitrary technique. For example, these films **353** and **355** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

It should be noted that a thin film showing high etch selectivity with respect to the first and second silicon dioxide films **353** and **355** and the organic film **354**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **356**.

Next, as shown in FIG. 15(b), a first resist pattern **357**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **356**. Thereafter, the titanium nitride film **356** is dry-etched using the first resist pattern **357** as a mask, thereby forming a mask pattern **358** out of the titanium nitride film **356** as shown in FIG. 15(c).

Subsequently, as shown in FIG. 16(a), the first resist pattern **357** is removed and then a second resist pattern **359**, having openings for forming contact holes, is formed on the second silicon dioxide film **355**. Then, the second silicon dioxide film **355** and the organic film **354** are sequentially dry-etched using the second resist pattern **359** as a mask, thereby forming a patterned second silicon dioxide film **355A** and a patterned organic film **354A** having openings **360** for forming contact holes as shown in FIG. 16(b). In this case, the second resist pattern **359** is removed during the step of etching the organic film **354**.

Next, as shown in FIG. 16(c), the first silicon dioxide film **353** is dry-etched using the patterned second silicon dioxide film **355A** and the patterned organic film **354A** as a mask, thereby forming a patterned first silicon dioxide film **353A** having contact holes **361**. In this etching process step, the mask pattern **358** is transferred to the patterned second silicon dioxide film **355A**. Accordingly, openings for forming wiring grooves are formed in the patterned second silicon dioxide film **355A**.

Thereafter, as shown in FIG. 16(d), the patterned organic film **354A** is dry-etched using the mask pattern **358** and the patterned second silicon dioxide film **355A** having the openings for forming wiring grooves as a mask, thereby forming the wiring grooves **362**. In forming the wiring grooves **362**, by selecting such etching conditions that the first silicon dioxide film **353A** is etched at a rate sufficiently lower than that of the organic film **354A**, sufficient selectivity can be secured for the patterned first silicon dioxide film **353A**. Accordingly, the depth of the wiring grooves **362** can be determined univalently at the sum of the thicknesses of the second silicon dioxide film **355** and the organic film **354**.

If the second resist pattern **359** may have been misaligned with the first resist pattern **357**, then the mask pattern **358** should be dry-etched using the second resist pattern **359** as a mask before the second silicon dioxide film **355** is dry-etched using the second resist pattern **359** as a mask. That is

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to say, if the mask pattern **358** is partially exposed inside the openings of the second resist pattern **359** for forming contact holes because of the misalignment of the second resist pattern **359** with the first resist pattern **357**, then the mask pattern **358** is dry-etched using the second resist pattern **359** as a mask. In this manner, the openings of the mask pattern **358** are expanded to include the openings for forming wiring grooves and contact holes.

Subsequently, the silicon nitride film **352** is dry-etched using the patterned first silicon dioxide film **353A** as a mask, thereby forming a patterned silicon nitride film **352A** and exposing the first metal interconnects **351** within the contact holes **361** as shown in FIG. 17(a).

Then, as shown in FIG. 17(b), an adhesion layer **363**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **361** and the wiring grooves **362**. Thereafter, a metal film **364** is deposited over the entire surface of the substrate to completely fill in the contact holes **361** and the wiring grooves **362**. In this embodiment, the metal film **364** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **364** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in FIG. 17(c), respective portions of the adhesion layer **363**, the metal film **364** and the mask pattern **358**, which are deposited on the patterned second silicon dioxide film **355A**, are removed by a CMP technique, for example. As a result, second metal interconnects **365** and contacts **366**, connecting the first and second metal interconnects **351** and **365**, are formed out of the metal film **364**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **365** through the same process steps as those described above.

In this modified example of the third embodiment, while the first resist pattern **357** is ashed and removed by oxygen plasma, the organic film **354** is not exposed to the oxygen plasma, because the second silicon dioxide film **355** exists on the organic film **354**.

Also, in this example, the second resist pattern **359** is removed while the second silicon dioxide film **355** and the organic film **354** are dry-etched using the second resist pattern **359** as a mask. Accordingly, since there is no need to ash and remove the second resist pattern **359** with oxygen plasma, the organic film **354** is not exposed to oxygen plasma.

#### EMBODIMENT 4

Next, an exemplary method for forming an interconnection structure according to the fourth embodiment of the present invention will be described with reference to FIGS. 18(a) through 18(c), FIGS. 19(a) through 19(c) and FIGS. 20(a) through 20(c).

First, as shown in FIG. 18(a), a silicon nitride film **402** is formed over first metal interconnects **401** formed on a semiconductor substrate **400**. The silicon nitride film **402** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **401** during a subsequent etching process step. Thereafter, a first low-dielectric-constant SOG film **403** (first insulating film), having a siloxane skeleton, is formed to be 1  $\mu\text{m}$  thick, for example, on the silicon nitride film **402**. Next, an organic-containing silicon dioxide film **404** (second insulating film), containing an organic component in silicon dioxide, is deposited to be 50 nm thick, for



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example, on the first low-dielectric-constant SOG film **403**. Then, a second low-dielectric-constant SOG film **405** (third insulating film), having a siloxane skeleton, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film **404**. And a titanium nitride film **406** is formed to be 50 nm thick, for example, on the second low-dielectric-constant SOG film **405**.

The first and second low-dielectric-constant SOG films **403** and **405** may be HSQ films, for example. The organic-containing silicon dioxide film **404** may be deposited by any arbitrary technique. For example, the film **404** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Then, an organic-containing silicon dioxide film **404**, having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide, can be obtained.

It should be noted that a thin film showing high etch selectivity with respect to the first and second low-dielectric-constant SOG films **403** and **405** and the organic-containing silicon dioxide film **404**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **406**.

Next, as shown in FIG. **18(b)**, a first resist pattern **407**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **406**. Thereafter, the titanium nitride film **406** is dry-etched using the first resist pattern **407** as a mask, thereby forming a mask pattern **408** out of the titanium nitride film **406** as shown in FIG. **18(c)**.

Subsequently, a second resist pattern **409**, having openings for forming contact holes, is formed by lithography on the second low-dielectric-constant SOG film **405** without removing the first resist pattern **407**. Then, the second low-dielectric-constant SOG film **405** and the organic-containing silicon dioxide film **404** are sequentially dry-etched using the second resist pattern **409** as a mask, thereby forming a patterned second low-dielectric-constant SOG film **405A** and a patterned organic-containing silicon dioxide film **404A** as shown in FIG. **19(a)**.

Next, the first and second resist patterns **407** and **409** are ashed and removed with oxygen plasma. As a result, a damaged layer **410** is unintentionally formed in respective portions of the patterned second low-dielectric-constant SOG film **405A** and the first low-dielectric-constant SOG film **403**, which are exposed inside the openings for forming contact holes, as shown in FIG. **19(b)**.

Then, the patterned second low-dielectric-constant SOG film **405A** is dry-etched using the mask pattern **408** as a mask, thereby forming wiring grooves **412** in the patterned second low-dielectric-constant SOG film **405A** as shown in FIG. **19(c)**. At the same time, the first low-dielectric-constant SOG film **403** is dry-etched using the patterned organic-containing silicon dioxide film **404A** as a mask, thereby forming a patterned first low-dielectric-constant SOG film **403A** having contact holes **411** as shown in FIG. **19(c)**. By performing this dry-etching process step, the damaged layer **410** can be removed from the patterned second low-dielectric-constant SOG films **405A** and the first low-dielectric-constant SOG film **403**.

Subsequently, the silicon nitride film **402** is dry-etched using the patterned organic-containing silicon dioxide film **404A** as a mask, thereby forming a patterned silicon nitride film **402A** and exposing the first metal interconnects **401** within the contact holes **411** as shown in FIG. **20(a)**.

Then, as shown in FIG. **20(b)**, an adhesion layer **413**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **411** and the

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wiring grooves **412**. Thereafter, a metal film **414** is deposited over the entire surface of the substrate to completely fill in the contact holes **411** and the wiring grooves **412**. In this embodiment, the metal film **414** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **414** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in FIG. **20(c)**, respective portions of the adhesion layer **413**, the metal film **414** and the mask pattern **408**, which are deposited on the patterned second low-dielectric-constant SOG film **405A**, are removed by a CMP technique, for example. As a result, second metal interconnects **415** and contacts **416**, connecting the first and second metal interconnects **401** and **415**, are formed out of the metal film **414**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **415** through the same process steps as those described above.

In the fourth embodiment, while the first and second resist patterns **407** and **409** are ashed and removed with oxygen plasma, a damaged layer **410** is formed in the first low-dielectric-constant SOG film **403** and the patterned second low-dielectric-constant SOG film **405A**. But the damaged layer **410** can be removed while the contact holes **411** and the wiring grooves **412** are formed.

Accordingly, the first and second low-dielectric-constant SOG films **403** and **405** may be made of a material degradable with oxygen plasma. For example, in general, if an HSQ film is exposed to oxygen plasma, Si—H bonds thereof are oxidized and the content of water and the relative dielectric constant thereof both increase to deteriorate the reliability and performance of the device. However, according to the fourth embodiment, the patterned first low-dielectric-constant SOG film **403A**, in which the contact holes **411** have already been formed, and the patterned second low-dielectric-constant SOG film **405A**, in which the wiring grooves **412** have already been formed, are not affected by oxygen plasma any more. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

#### EMBODIMENT 5

Next, an exemplary method for forming an interconnection structure according to the fifth embodiment of the present invention will be described with reference to FIGS. **21(a)** through **21(c)**, FIGS. **22(a)** through **22(c)** and FIGS. **23(a)** through **23(d)**.

First, as shown in FIG. **21(a)**, a silicon nitride film **502** is formed over first metal interconnects **501** formed on a semiconductor substrate **500**. The silicon nitride film **502** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **501** during a subsequent etching process step. Thereafter, a first organic film **503** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **502**. Then, a first silicon dioxide film **504** (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film **503**. Subsequently, a second organic film **505** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the first silicon dioxide film **504**. Next, a second silicon dioxide film **506** (fourth insulating film) is deposited to be 200 nm thick, for example, on the

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second organic film **505**. And a titanium nitride film **507** (thin film) is deposited to be 50 nm thick, for example, on the second silicon dioxide film **506**.

The first and second organic films **503** and **505** may be deposited by any arbitrary technique. For example, these films **503** and **505** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **503** and **505**. More specifically, the organic films **503** and **505** may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The first and second silicon dioxide films **504** and **506** may also be deposited by any arbitrary technique. For example, these films **504** and **506** may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **503** and **505** and the first and second silicon dioxide films **504** and **506**, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **507**.

Next, as shown in FIG. **21(b)**, a first resist pattern **508**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **507**. Thereafter, the titanium nitride film **507** is dry-etched using the first resist pattern **508** as a mask, thereby forming a mask pattern **509**, having openings for forming wiring grooves, out of the titanium nitride film **507** as shown in FIG. **21(c)**.

Subsequently, as shown in FIG. **22(a)**, the first resist pattern **508** is removed by oxygen plasma, for example. In this case, even if the first resist pattern **508** is ashed and removed using oxygen plasma, the quality of the second organic film **505** does not degrade, because the second silicon dioxide film **506** exists on the second organic film **505** mainly composed of an organic component.

Then, as shown in FIG. **22(b)**, a second resist pattern **510**, having openings for forming contact holes, is formed by lithography on the mask pattern **509**. Thereafter, the second silicon dioxide film **506** is dry-etched using the second resist pattern **510** and the mask pattern **509** as a mask, thereby forming a patterned second silicon dioxide film **506A** having openings for forming contact holes as shown in FIG. **22(c)**.

Next, the second organic film **505** is dry-etched using the patterned second silicon dioxide film **506A** as a mask, thereby forming a patterned second organic film **505A** having openings for forming contact holes as shown in FIG. **23(a)**. In this case, the second organic film **505** and the second resist pattern **510** are both mainly composed of organic components, the second organic film **505** is etched at a substantially equal rate to that of the second resist pattern **510**. Thus, when the second organic film **505** is dry-etched, the second resist pattern **510** is also removed simultaneously. The patterned second silicon dioxide film **506A** functions as an etch stopper during dry-etching the second resist pattern **510**.

It should be noted that part of the second resist pattern **510** may be left in the process step of dry-etching the second organic film **505**. This is because the residual second resist pattern **510** can be removed during a subsequent process step of dry-etching the first organic film **503** (see FIG. **23(c)**).

Thereafter, the patterned second silicon dioxide film **506A** and the first silicon dioxide film **504** are dry-etched using the

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mask pattern **509** and the patterned second organic film **505A** as respective masks, thereby forming a patterned second silicon dioxide film **506B** having openings for forming wiring grooves and a patterned first silicon dioxide film **504A** having openings for forming contact holes as shown in FIG. **23(b)**.

Then, the patterned second organic film **505A** and the first organic film **503** are dry-etched using the mask pattern **509** and the patterned first silicon dioxide film **504A** as respective masks, thereby forming a patterned second organic film **505B** having wiring grooves **511** and a patterned first organic film **503A** having contact holes **512** as shown in FIG. **23(c)**.

Subsequently, the silicon nitride film **502** is dry-etched using the patterned first silicon dioxide film **504A** as a mask, thereby forming a patterned silicon nitride film **502A** (see FIG. **23(d)**) and exposing the first metal interconnects **501** within the contact holes **512**. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **512** and the wiring grooves **511** as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes **512** and the wiring grooves **511**. In this embodiment, the metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern **509**, which are deposited on the patterned second silicon dioxide film **506B**, are removed by a CMP technique, for example. As a result, second metal interconnects **513** and contacts **514**, connecting the first and second metal interconnects **501** and **513** together, are formed as shown in FIG. **23(d)**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **513** through the same process steps as those described above.

In the fifth embodiment, while the first resist pattern **508** is being removed by oxygen plasma, for example, the quality of the second organic film **505** does not degrade. This is because the second silicon dioxide film **506** exists on the second organic film **505**, which is likely to be damaged by oxygen plasma.

Also, in this embodiment, the first silicon dioxide film **504** functions as an etch stopper during dry-etching the second organic film **505**. Accordingly, it is possible to prevent the quality of the first organic film **503** from being degraded.

#### MODIFIED EXAMPLE OF EMBODIMENT 5

Next, a method for forming an interconnection structure according to a modified example of the fifth embodiment will be described with reference to FIGS. **24(a)** through **24(c)**, FIGS. **25(a)** through **25(c)**, FIGS. **26(a)** through **26(d)**, FIGS. **27(a)** and **27(b)**, FIGS. **28(a)** and **28(b)** and FIGS. **29(a)** and **29(b)**.

First, as shown in FIG. **24(a)**, a silicon nitride film **552** is formed over first metal interconnects **551** formed on a semiconductor substrate **550**. The silicon nitride film **552** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **551** during a subsequent etching process step. Thereafter, a first organic film **553** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon



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nitride film 552. Then, a first silicon dioxide film 554 (second insulating film) is formed to be 100 nm thick, for example, on the first organic film 553. Subsequently, a second organic film 555 (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the first silicon dioxide film 554. Next, a second silicon dioxide film 556 (fourth insulating film) is deposited to be 200 nm thick, for example, on the second organic film 555. And a titanium nitride film 557 is deposited to be 50 nm thick, for example, on the second silicon dioxide film 556.

The first and second organic films 553 and 555 and the first and second silicon dioxide films 554 and 556 may be deposited by any arbitrary technique as in the fifth embodiment. Also, a thin film showing high etch selectivity with respect to the first and second organic films 553 and 555 and the first and second silicon dioxide films 554 and 556 may be used instead of the titanium nitride film 557.

Next, as shown in FIG. 24(b), a first resist pattern 558, having openings for forming wiring grooves, is formed on the titanium nitride film 557. Thereafter, the titanium nitride film 557 is dry-etched using the first resist pattern 558 as a mask, thereby forming a mask pattern 559, having openings for forming wiring grooves, out of the titanium nitride film 557 as shown in FIG. 24(c).

Subsequently, as shown in FIGS. 25(a) and 27(a), the first resist pattern 558 is removed. Then, a second resist pattern 560, having openings for forming contact holes, is formed on the mask pattern 559 as shown in FIG. 25(b). In this modified example of the fifth embodiment, the sizes of the openings of the second resist pattern 560 for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to wiring grooves for forming second metal interconnects. The reason thereof will be described later.

Then, the second silicon dioxide film 556 is dry-etched using the second resist pattern 560 and the mask pattern 559 as a mask, thereby forming a patterned second silicon dioxide film 556A having openings for forming contact holes as shown in FIGS. 25(c) and 27(b).

As described above, the sizes of the openings of the second resist pattern 560 for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to wiring grooves for forming second metal interconnects. Accordingly, even if the openings of the second resist pattern 560 for forming contact holes have misaligned with the openings of the mask pattern 559 for forming wiring grooves, the openings of the patterned second silicon dioxide film 556A for forming contact holes can be formed to be self-aligned with the openings of the mask pattern 559 for forming wiring grooves. This is because the openings of the patterned second silicon dioxide film 556A for forming contact holes are formed in respective regions where the openings of the second resist pattern 560 for forming contact holes overlap with corresponding openings of the mask pattern 559 for forming wiring grooves.

In addition, the size of the openings of the second resist pattern 560 for forming contact holes is also extended in the direction parallel to the wiring grooves for forming second metal interconnects. Thus, the contact area between contacts 564 to be formed later and second metal interconnects 563 (see FIG. 26(d)) expands. As a result, the contacts 564 can connect the first and second metal interconnects 551 and 563 together with a lot more certainty.

Next, the second organic film 555 is dry-etched using the patterned second silicon dioxide film 556A as a mask,

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thereby forming a patterned second organic film 555A having openings for forming contact holes as shown in FIGS. 26(a) and 28(a). In this case, the second organic film 555 and the second resist pattern 560 are both mainly composed of organic components, the second organic film 555 is etched at a substantially equal rate to that of the second resist pattern 560. Thus, when the second organic film 555 is dry-etched, the second resist pattern 560 is also removed simultaneously. It should be noted that part of the second resist pattern 560 may be left in the process step of dry-etching the second organic film 555. This is because the residual second resist pattern 560 can be removed during a subsequent process step of dry-etching the first organic film 553 (see FIG. 26(c)).

Thereafter, the patterned second silicon dioxide film 556A and the first silicon dioxide film 554 are dry-etched using the mask pattern 559 and the patterned second organic film 555A as respective masks, thereby forming a patterned second silicon dioxide film 556B having wiring grooves and a patterned first silicon dioxide film 554A having openings for forming contact holes as shown in FIGS. 26(b) and 28(b). Then, the patterned second organic film 555A is dry-etched using the mask pattern 559 and the patterned second silicon dioxide film 556B as a mask, and the first organic film 553 is dry-etched using the patterned first silicon dioxide film 554A as a mask, thereby forming a patterned second organic film 555B having wiring grooves 561 and a patterned first organic film 553A having contact holes 562 as shown in FIGS. 26(c) and 29(a).

Subsequently, the silicon nitride film 552 is dry-etched using the patterned first silicon dioxide film 554A as a mask, thereby forming a patterned silicon nitride film 552A (see FIG. 26(d)) having contact holes, and exposing the first metal interconnects 551 within the contact holes 562. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 562 and the wiring grooves 561 as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 562 and the wiring grooves 561. Finally, respective portions of the adhesion layer, the metal film and the mask pattern 559, which are deposited on the patterned second silicon dioxide film 556B, are removed by a CMP technique, for example. As a result, second metal interconnects 563 and contacts 564, connecting the first and second metal interconnects 551 and 563 together, are formed as shown in FIGS. 26(d) and 29(b).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 563 through the same process steps as those described above.

According to this modified example of the fifth embodiment, the sizes of the openings of the second resist pattern 560 for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming the second metal interconnects. Thus, even if the openings of the second resist pattern 560 for forming contact holes have misaligned with the openings of the mask pattern 559 for forming wiring grooves, the openings of the patterned second silicon dioxide film 556A for forming contact holes can be formed to be self-aligned with the openings of the mask pattern 559 for forming wiring grooves. This is because the openings of the patterned second silicon dioxide film 556A for forming contact holes are formed in respective regions where the openings of the second resist pattern 560 for forming contact holes overlap with corresponding open-

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ings of the mask pattern 559 for forming wiring grooves. Accordingly, the connection between the contacts 564 and the second metal interconnects 563 is ensured.

In addition, the size of the openings of the second resist pattern 560 for forming contact holes is also extended in the direction parallel to the wiring grooves for forming the second metal interconnects. Thus, the contact area between contacts 564 and the second metal interconnects 563 expands. As a result, the contacts 564 can connect the first and second metal interconnects 551 and 563 together with a lot more certainty.

FIG. 36 illustrates a positional relationship between the openings of the mask pattern 559 for forming wiring grooves and those of the second resist pattern 560 for forming contact holes in this modified example of the fifth embodiment. As shown in FIG. 36, the size of the openings of the second resist pattern 560 for forming contact holes are larger than the designed size.

FIG. 37(a) illustrates respective positional relationships between the mask pattern 559 and the second resist pattern 560 and between a first metal interconnect 551 and a contact 564 in this modified example of the fifth embodiment. Specifically, the upper part of FIG. 37(a) illustrates a positional relationship between an opening of the mask pattern 559 for forming a wiring groove and an associated opening of the second resist pattern 560 for forming a contact hole. The middle part of FIG. 37(a) illustrates the cross section of the upper part taken along the line A—A. And the lower part of FIG. 37(a) illustrates a positional relationship between a first metal interconnect 551 and an associated contact 564. FIG. 37(b) illustrates respective positional relationships between the mask pattern 509 and the second resist pattern 510 and between a first metal interconnect 501 and a contact 514 in the fifth embodiment. Specifically, the upper part of FIG. 37(b) illustrates a positional relationship between an opening of the mask pattern 509 for forming a wiring groove and an associated opening of the second resist pattern 510 for forming a contact hole. The middle part of FIG. 37(b) illustrates the cross section of the upper part taken along the line B—B. And the lower part of FIG. 37(b) illustrates a positional relationship between a first metal interconnect 501 and an associated contact 514.

Setting the size of an opening of the second resist pattern 510 for forming a contact hole at the designed size thereof as in the fifth embodiment, if the opening of the second resist pattern 510 for forming a contact hole has misaligned with an associated opening of the mask pattern 509 for forming a wiring groove, then the contact area (indicated by hatching) between the contact 514 and the first metal interconnect 501 greatly decreases as can be seen from FIG. 37(b). In contrast, setting the size of an opening of the second resist pattern 560 for forming a contact hole larger than the designed size thereof as in this modified example of the fifth embodiment, even if the opening of the second resist pattern 560 for forming a contact hole has misaligned with an associated opening of the mask pattern 559 for forming a wiring groove, the contact area (indicated by hatching) between the contact 564 and the first metal interconnect 551 does not decrease so much as can be seen from FIG. 37(a).

#### EMBODIMENT 6

Next, an exemplary method for forming an interconnection structure according to the sixth embodiment of the present invention will be described with reference to FIGS. 30(a) through 30(c), FIGS. 31(a) through 31(c) and FIGS. 32(a) through 32(c).

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First, as shown in FIG. 30(a), a silicon nitride film 602 is formed over first metal interconnects 601 formed on a semiconductor substrate 600. The silicon nitride film 602 is formed to be 50 nm thick, for example, and to protect the first metal interconnects 601 during a subsequent etching process step. Thereafter, a first organic film 603 (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film 602. Then, a silicon dioxide film 604 (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film 603. Subsequently, a second organic film 605 (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the silicon dioxide film 604. And a titanium nitride film 606 (thin film) is deposited to be 50 nm thick, for example, on the second organic film 605.

The first and second organic films 603 and 605 may be deposited by any arbitrary technique. For example, these films 603 and 605 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films 603 and 605. More specifically, the organic films 603 and 605 may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The silicon dioxide film 604 may also be deposited by any arbitrary technique. For example, the film 604 may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films 603 and 605 and the silicon dioxide film 604, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 606.

Next, as shown in FIG. 30(b), a first resist pattern 607, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 606. Thereafter, the titanium nitride film 606 is dry-etched using the first resist pattern 607 as a mask, thereby forming a mask pattern 608, having openings for forming wiring grooves, out of the titanium nitride film 606 as shown in FIG. 30(c).

Subsequently, as shown in FIG. 31(a), the first resist pattern 607 is removed using an organic parting agent, for example. In such a case, since the second organic film 605 is not exposed to oxygen plasma, the quality of the second organic film 605 does not degrade.

Then, as shown in FIG. 31(b), a second resist pattern 609, having openings for forming contact holes, is formed by lithography on the mask pattern 608. Then, the second organic film 605 is dry-etched using the second resist pattern 609 and the mask pattern 608 as a mask, thereby forming a patterned second organic film 605A having openings for forming contact holes as shown in FIG. 31(c). In this case, the second organic film 605 and the second resist pattern 609 are both mainly composed of organic components, the second organic film 605 is etched at a substantially equal rate to that of the second resist pattern 609. Thus, when the second organic film 605 is dry-etched, the second resist pattern 609 is also removed simultaneously.

It should be noted that part of the second resist pattern 609 may be left in the process step of dry-etching the second organic film 605. This is because the residual second resist pattern 609 can be removed during a subsequent process step of dry-etching the first organic film 603 (see FIG. 32(b)).



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Thereafter, the silicon dioxide film 604 is dry-etched using the patterned second organic film 605A as a mask, thereby forming a patterned silicon dioxide film 604A having openings for forming contact holes as shown in FIG. 32(a).

Then, the patterned second organic film 605A and the first organic film 603 are dry-etched using the mask pattern 608 and the patterned silicon dioxide film 604A as respective masks, thereby forming a patterned second organic film 605B having wiring grooves 610 and a patterned first organic film 603A having contact holes 611 as shown in FIG. 32(b).

Subsequently, the patterned silicon dioxide film 604A and the silicon nitride film 602 are dry-etched using the mask pattern 608 and the patterned first organic film 603A as respective masks, thereby forming a patterned silicon dioxide film 604B having wiring grooves (see FIG. 32(c)) and a patterned silicon nitride film 602A having the contact holes (see FIG. 32(c)), and exposing the first metal interconnects 601 within the contact holes 611. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 611 and the wiring grooves 610 as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 611 and the wiring grooves 610. In this embodiment, the metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern 608, which are deposited on the patterned second organic film 605B, are removed by a CMP technique, for example. As a result, second metal interconnects 612 and contacts 613, connecting the first and second metal interconnects 601 and 612 together, are formed as shown in FIG. 32(c).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 612 through the same process steps as those described above.

In the sixth embodiment, a patterned second organic film 605B, having wiring grooves 610, and a patterned first organic film 603A, having contact holes 611, are formed by a single dry-etching process using the mask pattern 608, having the openings for forming wiring grooves, and the patterned silicon dioxide film 604A as respective masks. That is to say, the wiring grooves 610 and the contact holes 611 can be formed during the same etching process step. Accordingly, a dual damascene structure can be formed with the increase in number of process steps suppressed.

Also, in the sixth embodiment, since the first resist pattern 607 is removed by an organic parting agent, for example, the quality of the second organic film 605 does not degrade.

Furthermore, in this embodiment, the silicon dioxide film 604 functions as an etch stopper during dry-etching the second organic film 605. Accordingly, it is possible to prevent the quality of the first organic film 603 from being degraded.

#### MODIFIED EXAMPLE OF EMBODIMENT 6

Next, a method for forming an interconnection structure according to a modified example of the sixth embodiment will be described with reference to FIGS. 33(a) through 33(c), FIGS. 34(a) through 34(c) and FIGS. 35(a) through 35(c).

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First, as shown in FIG. 33(a), a silicon nitride film 652 is formed over first metal interconnects 651 formed on a semiconductor substrate 650. The silicon nitride film 652 is formed to be 50 nm thick, for example, and to protect the first metal interconnects 651 during a subsequent etching process step. Thereafter, a first organic film 653 (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film 652. Then, a silicon dioxide film 654 (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film 653. Subsequently, a second organic film 655 (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the silicon dioxide film 654. And a titanium nitride film 656 (thin film) is deposited to be 50 nm thick, for example, on the second organic film 655.

The first and second organic films 653 and 655 may be deposited by any arbitrary technique. For example, these films 653 and 655 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films 653 and 655. More specifically, the organic films 653 and 655 may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The silicon dioxide film 654 may also be deposited by any arbitrary technique. For example, the film 654 may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films 653 and 655 and the silicon dioxide film 654, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 656.

Next, as shown in FIG. 33(b), a first resist pattern 657, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 656. Thereafter, the titanium nitride film 656 is dry-etched using the first resist pattern 657 as a mask, thereby forming a mask pattern 658, having openings for forming wiring grooves, out of the titanium nitride film 656 as shown in FIG. 33(c).

Subsequently, as shown in FIG. 34(a), the first resist pattern 657 is removed by an organic parting agent, for example. In such a case, since the second organic film 655 is not exposed to oxygen plasma, the quality of the second organic film 655 does not degrade.

Then, as shown in FIG. 34(b), a second resist pattern 659, having openings for forming contact holes, is formed by lithography on the mask pattern 658. In this modified example of the sixth embodiment, the sizes of the openings of the second resist pattern 659 for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming second metal interconnects. The reason thereof will be described later.

Next, the second organic film 655 is dry-etched using the second resist pattern 659 and the mask pattern 658 as a mask, thereby forming a patterned second organic film 655A having openings for forming contact holes as shown in FIG. 34(c). In this case, the second organic film 655 and the second resist pattern 659 are both mainly composed of organic components, the second organic film 655 is etched at a substantially equal rate to that of the second resist pattern 659. Thus, when the second organic film 655 is dry-etched, the second resist pattern 659 is also removed

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simultaneously. It should be noted that part of the second resist pattern 659 may be left in the process step of dry-etching the second organic film 655. This is because the residual second resist pattern 659 can be removed during a subsequent process step of dry-etching the first organic film 653 (see FIG. 35(b)).

Thereafter, the silicon dioxide film 654 is dry-etched using the patterned second organic film 655A as a mask, thereby forming a patterned second silicon dioxide film 654A having openings for forming contact holes as shown in FIG. 35(a).

Then, the patterned second organic film 655A and the first organic film 653 are dry-etched using the mask pattern 658 and the patterned silicon dioxide film 654A as respective masks, thereby forming a patterned second organic film 655B having wiring grooves 660 and a patterned first organic film 653A having contact holes 661 as shown in FIG. 35(b).

Subsequently, the patterned silicon dioxide film 654A and the silicon nitride film 652 are dry-etched using the mask pattern 658 and the patterned first organic film 653A as respective masks, thereby forming a patterned silicon dioxide film 654B having wiring grooves (see FIG. 35(c)) and a patterned silicon nitride film 652A having the contact holes (see FIG. 35(c)), and exposing the first metal interconnects 651 within the contact holes 661. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 661 and the wiring grooves 660 as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 661 and the wiring grooves 660. In this embodiment, the metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern 658, which are deposited on the patterned second organic film 655B, are removed by a CMP technique, for example. As a result, second metal interconnects 662 and contacts 663, connecting the first and second metal interconnects 651 and 662 together, are formed as shown in FIG. 35(c).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 662 through the same process steps as those described above.

In this modified example of the sixth embodiment, the sizes of the openings of the second resist pattern 659 for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming the second metal interconnects. Accordingly, even if the openings of the second resist pattern 659 for forming contact holes have misaligned with the openings of the mask pattern 658 for forming wiring grooves, the openings of the patterned second organic film 655A for forming contact holes can be formed to be self-aligned with the openings of the mask pattern 658 for forming wiring grooves. This is because the openings of the patterned second organic film 655A for forming contact holes are formed in respective regions where the openings of the second resist pattern 659 for forming contact holes overlap with corresponding openings of the mask pattern 658 for forming wiring grooves. Accordingly, the connection between the contacts 663 and the second metal interconnects 662 is ensured.

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In addition, the size of the openings of the second resist pattern 659 for forming contact holes is also extended in the direction parallel to the wiring grooves for forming second metal interconnects. Thus, the contact area between the contacts 663 and the second metal interconnects 662 expands.

As a result, the contacts 663 can connect the first and second metal interconnects 651 and 662 together with a lot more certainty.

What is claimed is:

1. A method for forming an interconnection structure, comprising the steps of:

- a) forming a first insulating film over lower-level metal interconnects;
  - b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;
  - c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;
  - d) forming a thin film over the third insulating film;
  - e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;
  - f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;
  - g) forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;
  - h) dry-etching the third insulating film under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left;
  - i) dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;
  - j) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and
  - k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.
2. The method of claim 1, further comprising the step of forming a metal adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes between the steps j) and k).
3. The method of claim 1, wherein the third insulating film is mainly composed of an organic component.



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4. The method of claim 3, wherein the step c) includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin.

5. The method of claim 3, wherein the first insulating film is mainly composed of an organic component.

6. The method of claim 5, further comprising the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process using a reactive gas containing nitrogen between the steps j) and k).

7. The method of claim 3, wherein the step a) includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin.

8. A method for forming an interconnection structure, comprising the steps of:

- a) forming a first insulating film over lower-level metal interconnects;
- b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;
- c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;
- d) forming a thin film over the third insulating film;
- e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;
- f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;
- g) forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;
- h) dry-etching the third insulating film using the first and second resist patterns as a mask under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes;
- i) dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films and the first and second resist patterns are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;
- j) removing the first and second resist patterns;
- k) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and
- l) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

9. The method of claim 8, wherein the third insulating film is a low-dielectric-constant SOG film with a siloxane skeleton.

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10. A method for forming an interconnection structure, comprising the steps of:

- a) forming a first insulating film over lower-level metal interconnects;
- b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;
- c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;
- d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film;
- e) forming a thin film over the fourth insulating film;
- f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;
- g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;
- h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;
- i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes;
- j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;
- k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes;
- l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and
- m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

11. The method of claim 10, wherein at least one of the first and third insulating films is mainly composed of an organic component.

12. The method of claim 10, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

13. A method for forming an interconnection structure, comprising the steps of:

- a) forming a first insulating film over lower-level metal interconnects;
- b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;
- c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

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- d) forming a thin film over the third insulating film;
- e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;
- f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;
- g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;
- h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;
- i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes;

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- j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and
  - k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.
- 14.** The method of claim **13**, wherein at least one of the first and third insulating films is mainly composed of an organic component.
- 15.** The method of claim **13**, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

\* \* \* \* \*

SERIAL NUMBER 09/274,114	FILING DATE 03/23/99	CLASS 216	GROUP ART UNIT 1763	ATTORNEY DOCKET NO. 0819-226
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APPLICANT

NOBUO AOI, HYOGO, JAPAN.

\*\*CONTINUING DOMESTIC DATA\*\*\*\*\*none  
VERIFIED

*L.J.M-E*

\*\*371 (NAT'L STAGE) DATA\*\*\*\*\*none  
VERIFIED

*L.J.M-E*

\*\*FOREIGN APPLICATIONS\*\*\*\*\*

VERIFIED JAPAN 10-079371 03/26/98

*L.J.M-E*

IF REQUIRED, FOREIGN FILING LICENSE GRANTED 04/13/99

Foreign Priority claimed 35 USC 119 (a-d) conditions met	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> no <input type="checkbox"/> Yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	STATE OR COUNTRY JPX	SHEETS DRAWING 37	TOTAL CLAIMS 15	INDEPENDENT CLAIMS 4
Verified and Acknowledged	<i>L.J.M-E</i> Examiner's Initials	Initials			

ADDRESS  
GERALD J FERGUSON JR  
SIXBEY FRIEDMAN LEEDOM & FERGUSON  
3180 GREENSBORO DRIVE  
SUITE 800  
MCLEAN VA 22102

TITLE  
METHOD FOR FORMING INTERCONNECTION STRUCTURE

FILING FEE RECEIVED \$838	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit
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PATENT APPLICATION SERIAL NO. \_\_\_\_\_

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE  
FEE RECORD SHEET

04/01/1999 PALLEN 00000052 09274114

01 FC:101	760.00 OP
02 FC:102	78.00 OP

PTO-1556  
(5/87)

\*U.S. GPO: 1998-433-214/80404

Please type a plus sign (+) inside this box →


+

PTO/SB/05 (1/98)

Approved for use through 09/30/2000. OMB 0651-0032

Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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<b>UTILITY PATENT APPLICATION TRANSMITTAL</b>  <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>		Attorney Docket No. <b>0819-226</b>
		First Inventor or Application Identifier: <b>Nobuo AOI</b>
		Title: <b>METHOD FOR FORMING INTERCONNECTION STRUCTURE</b>
		Express Mail Label No.
<b>APPLICATION ELEMENTS</b> <small>See MPEP chapter 600 concerning utility patent application contents.</small>		<b>ADDRESS TO:</b> Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
1. <input checked="" type="checkbox"/> Fee Transmittal Form (e.g., PTO/SB/17) <small>(Submit an original, and a duplicate for fee processing)</small> 2. <input checked="" type="checkbox"/> Specification <span style="float: right;">Total Pages [91]</span> <small>(preferred arrangement set forth below)</small> - Descriptive title of the invention - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure 3. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) <span style="float: right;">Total Sheets [37]</span> 4. <input checked="" type="checkbox"/> Oath or Declaration <span style="float: right;">Total Pages [2]</span> a. <input checked="" type="checkbox"/> Newly executed (original or copy) b. <input type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) <small>(for continuation/divisional with Box 17 completed)</small> [Note Box 5 below] i. <input type="checkbox"/> <b>DELETION OF INVENTOR(S)</b> Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 5. <input type="checkbox"/> Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.		6. <input type="checkbox"/> Microfiche Computer Program (Appendix) 7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies  <hr/> <b>ACCOMPANYING APPLICATION PARTS</b> 8. <input checked="" type="checkbox"/> Assignment Papers (cover sheet & document(s)) 9. <input type="checkbox"/> 37 CFR 3.73(b) Statement <input type="checkbox"/> Power of Attorney <small>(when there is an assignee)</small> 10. <input type="checkbox"/> English Translation Document (if applicable) 11. <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Copies of IDS <small>(IDS)/PTO-1449 Citations</small> 12. <input type="checkbox"/> Preliminary Amendment 13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <small>(Should be specifically itemized)</small> 14. <input type="checkbox"/> *Small Entity <input type="checkbox"/> Statement filed in prior application, Statement(s) Status still proper and desired <small>(PTO/SB/09-12)</small> 15. <input type="checkbox"/> Certified Copy of Priority Document <small>(if foreign priority is claimed)</small> 16. <input type="checkbox"/> Other:  <small>*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.</small>
17. If a <b>CONTINUING APPLICATION</b> , check appropriate box, and supply the requisite information below and in a preliminary amendment: <input type="checkbox"/> Continuation <input type="checkbox"/> Divisional <input type="checkbox"/> Continuation-in-part (CIP) of prior application No. _____ Prior application information: Examiner: _____ Group/Art Unit: _____		
<b>18. CORRESPONDENCE ADDRESS</b>		
<input type="checkbox"/> Customer Number or Bar Code Label <span style="float: right;">or <input checked="" type="checkbox"/> Correspondence address below</span> <small>(Insert Customer No. or Attach bar code label here)</small>		
Name: Eric J. Robinson Firm: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C. Address: 8180 Greensboro Drive, Suite 800 City: McLean State: VA Zip Code: 22102 Country: U.S.A. Telephone (703) 790-9110 FAX (703) 883-0370		
Name: Eric J. Robinson		Registration No. 38,285
Signature 		Date: March 23, 1999

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

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JCS30 U.S. PTO  
09/274114  
03/23/99

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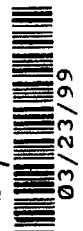
PTO/SB/05 (1/98)

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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<b>UTILITY PATENT APPLICATION TRANSMITTAL</b>	Attorney Docket No. <b>0819-226</b> First Inventor or Application Identifier: <b>Nobuo AOI</b> Title: <b>METHOD FOR FORMING INTERCONNECTION STRUCTURE</b> Express Mail Label No.
(Only for new nonprovisional applications under 37 CFR 1.53(b))	
<b>APPLICATION ELEMENTS</b> <i>See MPEP chapter 600 concerning utility patent application contents.</i>	<b>ADDRESS TO:</b> Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
1. <input checked="" type="checkbox"/> Fee Transmittal Form (e.g., PTO/SB/17) <i>(Submit an original, and a duplicate for fee processing)</i> 2. <input checked="" type="checkbox"/> Specification <span style="float: right;">Total Pages [91]</span> <i>(preferred arrangement set forth below)</i> - Descriptive title of the invention - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the invention - Brief Summary of the invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure <span style="float: right;">Total Sheets [37]</span> 3. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) <span style="float: right;">Total Pages [2]</span> 4. <input checked="" type="checkbox"/> Oath or Declaration a. <input checked="" type="checkbox"/> Newly executed (original or copy) b. <input type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) <i>(for continuation/divisional with Box 17 completed)</i> [Note Box 5 below] i. <input type="checkbox"/> <b>DELETION OF INVENTOR(S)</b> Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 5. <input type="checkbox"/> Incorporation By Reference <i>(useable if Box 4b is checked)</i> The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.	6. <input type="checkbox"/> Microfiche Computer Program <i>(Appendix)</i> 7. Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, all necessary)</i> a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies <hr/> <b>ACCOMPANYING APPLICATION PARTS</b> 8. <input checked="" type="checkbox"/> Assignment Papers (cover sheet & document(s)) 9. <input type="checkbox"/> 37 CFR 3.73(b) Statement <span style="float: right;">[ ] Power of Attorney</span> <i>(when there is an assignee)</i> 10. <input type="checkbox"/> English Translation Document <i>(if applicable)</i> 11. <input type="checkbox"/> Information Disclosure Statement <span style="float: right;">[ ] Copies of IDS</span> (IDS)/PTO-1449 <span style="float: right;">Citations</span> 12. <input type="checkbox"/> Preliminary Amendment 13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i> 14. <input type="checkbox"/> *Small Entity <span style="float: right;">[ ] Statement filed in prior application,</span> Statement(s) <span style="float: right;">Status still proper and desired</span> (PTO/SB/09-12) 15. <input type="checkbox"/> Certified Copy of Priority Document <i>(if foreign priority is claimed)</i> 16. <input type="checkbox"/> Other:  *A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.
17. If a <b>CONTINUING APPLICATION</b> , check appropriate box, and supply the requisite information below and in a preliminary amendment: <input type="checkbox"/> Continuation <input type="checkbox"/> Divisional <input type="checkbox"/> Continuation-in-part (CIP) of prior application No. _____ Prior application information: Examiner: _____ Group/Art Unit: _____	
<b>18. CORRESPONDENCE ADDRESS</b>	
<input type="checkbox"/> Customer Number or Bar Code Label <span style="float: right;">or <input checked="" type="checkbox"/> Correspondence address below</span> <i>(Insert Customer No. or Attach bar code label here)</i>	
Name: Eric J. Robinson Firm: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C. Address: 8180 Greensboro Drive, Suite 800 City: McLean State: VA Zip Code: 22102 Country: U.S.A. Telephone (703) 790-9110 FAX (703) 883-0370	
Name: Eric J. Robinson <span style="float: right;">Registration No. 38,285</span>	
Signature: <span style="float: right;">Date: March 23, 1999</span>	

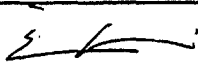


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<h1 style="margin: 0;">FEE TRANSMITTAL</h1> <p style="font-size: small; margin-top: 10px;">Patent fees are subject to annual revision on October 1. These are the fees effective October 1, 1997. Small Entity payments <u>must</u> be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.</p>		Complete If Known					
		Application Number					
		Filing Date		March 23, 1999			
		First Named Inventor		Nobuo AOI			
		Examiner Name					
Group Art Unit							
TOTAL AMOUNT OF PAYMENT		\$878.00	Attorney Docket Number		0819-228		
METHOD OF PAYMENT (check one)		FEE CALCULATION (continued)					
		3. ADDITIONAL FEES					
		Large Entity		Small Entity			
1. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge indicated fees and credit any over payments to: Deposit Account No. 19-2380 Deposit Account Name: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, PC  <input checked="" type="checkbox"/> Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17  <input type="checkbox"/> Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance  2. <input checked="" type="checkbox"/> Payment Enclosed: <input checked="" type="checkbox"/> Check <input type="checkbox"/> Money Order <input type="checkbox"/> Other		Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid
		105	130	205	65	Surcharge-late filing fee or oath	
	127	50	227	25	Surcharge-late provisional filing fee or cover sheet		
	139	130	139	130	Non-English specification		
	147	2,520	147	2,520	For filing a request for reexamination		
	112	920*	112	920*	Requesting publication of SIR prior to Examiner action		
	113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action		
	115	110	215	55	Ext for reply within first month		
	116	380	216	190	Ext for reply within second mth		
	117	870	217	435	Ext for reply within third mth		
	118	1,380	218	680	Ext for reply within fourth mth		
	128	1,850	228	925	Ext for reply within fifth month		
	119	300	219	150	Notice of Appeal		
	120	300	220	150	Filing brief in support of appeal		
	121	260	221	130	Request for Oral Hearing		
	138	1,510	138	1,510	Petition to institute public use proceeding		
	140	110	240	55	Petition to revive-unavoidable		
	141	1,210	241	605	Petition to revive-unintentional		
	142	1,210	242	605	Utility issue fee (or reissue)		
	143	430	243	215	Design issue fee		
	144	580	244	290	Plant issue fee		
	122	130	122	130	Petitions to the Commissioner		
	123	50	123	50	Petitions related to provisional applications		
	126	240	126	240	Submission of IDS		
	561	40	561	40	Recording each patent assignment per property (times number of properties)	\$40.00	
	146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))		
	149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))		
					Other _____		
					Other _____		
					*Reduced by Basic Filing Fee Paid		
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SUBTOTAL (1)							

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<h2 style="margin: 0;">FEE TRANSMITTAL</h2> <p style="font-size: small; margin: 5px 0;">Patent fees are subject to annual revision on October 1. These are the fees effective October 1, 1997. Small Entity payments <u>must</u> be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.</p>		Complete If Known					
		Application Number					
		Filing Date		March 23, 1999			
		First Named Inventor		Nobuo AOI			
		Examiner Name					
Group Art Unit							
TOTAL AMOUNT OF PAYMENT		\$878.00	Attorney Docket Number		0819-226		
METHOD OF PAYMENT (check one)		3. ADDITIONAL FEES					
		Large Entity		Small Entity			
1. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge indicated fees and credit any over payments to: Deposit Account No. 19-2380 Deposit Account Name: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, PC  <input checked="" type="checkbox"/> Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17  <input type="checkbox"/> Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance  2. <input checked="" type="checkbox"/> Payment Enclosed: <input checked="" type="checkbox"/> Check <input type="checkbox"/> Money Order <input type="checkbox"/> Other		Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid
		105	130	205	65	Surcharge-late filing fee or oath	
		127	50	227	25	Surcharge-late provisional filing fee or cover sheet	
		139	130	139	130	Non-English specification	
		147	2,520	147	2,520	For filing a request for reexamination	
		112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
		113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
		115	110	215	55	Ext for reply within first month	
		116	380	216	190	Ext for reply within second mth	
		117	870	217	435	Ext for reply within third mth	
		118	1,380	218	680	Ext for reply within fourth mth	
		128	1,850	226	925	Ext for reply within fifth month	
		119	300	219	150	Notice of Appeal	
		120	300	220	150	Filing brief in support of appeal	
		121	260	221	130	Request for Oral Hearing	
		138	1,510	138	1,510	Petition to institute public use proceeding	
		140	110	240	55	Petition to revive-unavoidable	
		141	1,210	241	605	Petition to revive-unintentional	
		142	1,210	242	605	Utility issue fee (or reissue)	
		143	430	243	215	Design issue fee	
		144	580	244	290	Plant issue fee	
		122	130	122	130	Petitions to the Commissioner	
		123	50	123	50	Petitions related to provisional applications	
		126	240	126	240	Submission of IDS	
		581	40	581	40	Recording each patent assignment per property (times number of properties)	\$40.00
		146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))	
		149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	
						Other _____	
						Other _____	
						*Reduced by Basic Filing Fee Paid	
SUBTOTAL (1)			\$760.00	SUBTOTAL (3)			\$40.00
2. EXTRA CLAIM FEES		Extra Claims Fee from Below		Fee Paid			
Total Claims		15	- 20** = 0	X \$18.00 =			
Independent Claims		4	- 3** = 1	X \$78.00 =		\$78.00	
Multiple Dependent Claims							
**or number previously paid, if greater. For Reissues, see below							
Large Entity		Small Entity		Fee Description			
Fee Code	Fee (\$)	Fee Code	Fee (\$)				
103	18	203	9	Claims in excess of 20			
102	78	202	39	Independent claims in excess of 3			
104	260	204	130	Multiple dependent claim			
109	78	209	39	**Reissue independent claims over original patent			
110	18	210	9	**Reissue claims in excess of 20 and over original patent			
SUBTOTAL (2)				\$78.00			
SUBMITTED BY				Complete (if applicable)			
Typed or Printed Name		Eric J. Robinson		Reg. Number		38,285	
Signature				Date		March 23, 1999	
				Deposit Account		19-2380	
				User ID			

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## METHOD FOR FORMING INTERCONNECTION STRUCTURE

### BACKGROUND OF THE INVENTION

5 The present invention relates to a method for forming an interconnection structure in a semiconductor integrated circuit.

As the number of devices, integrated within a single semiconductor integrated circuit, has been tremendously increasing these days, wiring delay has also been increasing noticeably. This is because the larger the number of devices integrated, the larger line-to-line capacitance (i.e., parasitic capacitance between metal interconnects), thus interfering with the performance improvement of a semiconductor integrated circuit. The wiring delay is so-called "RC delay", which is proportional to the product of the resistance of metal interconnection and the line-to-line capacitance.

In other words, to reduce the wiring delay, either the resistance of metal interconnection or the line-to-line capacitance should be reduced.

20 In order to reduce the interconnection resistance, IBM Corp., Motorola, Inc., etc. have reported semiconductor integrated circuits using copper, not aluminum alloy, as a material for metal interconnects. A copper material has a specific resistance about two-thirds as high as that of an aluminum alloy material. Accordingly, in accordance with

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simple calculation, the wiring delay involved with the use of a copper material for metal interconnects can be about two-thirds of that involved with the use of an aluminum alloy material therefor. That is to say, the operating speed can be  
5 increased by about 1.5 times.

However, the number of devices, integrated within a single semiconductor integrated circuit, is expected to further increase by leaps and bounds from now on, thus increasing the wiring delay considerably. Therefore, it is concerned that  
10 even the use of copper as an alternate metal interconnection material would not be able to catch up with such drastic increase. Also, the specific resistance of copper as a metal interconnection material is just a little bit higher than, but almost equal to, that of gold or silver. Accordingly,  
15 even if gold or silver is used instead of copper as a metal interconnection material, the wiring delay can be reduced only slightly.

Under these circumstances, not only reducing interconnection resistance but also suppressing line-to-line capacitance play a key role in further increasing the number of  
20 devices that can be integrated within a single semiconductor integrated circuit. And the relative dielectric constant of an interlevel insulating film should be reduced to suppress the line-to-line capacitance. A silicon dioxide film has  
25 heretofore been used as a typical material for an interlevel

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insulating film. The relative dielectric constant of a silicon dioxide film is, however, about 4 to about 4.5. Thus, it would be difficult to apply a silicon dioxide film to a semiconductor integrated circuit incorporating an even larger number of devices.

In order to solve such a problem, fluorine-doped silicon dioxide film, low-dielectric-constant spin-on-glass (SOG) film, organic polymer film and so on have been proposed as alternate interlevel insulating films with respective relative dielectric constants smaller than that of a silicon dioxide film.

The relative dielectric constant of a fluorine-doped silicon dioxide film is about 3.3 to about 3.7, which is about 20 percent lower than that of a conventional silicon dioxide film. Nevertheless, a fluorine-doped silicon dioxide film is highly hygroscopic, and easily absorbs water in the air, resulting in various problems in practice. For example, when the fluorine-doped silicon dioxide film absorbs water, SiOH groups, having a high relative dielectric constant, are introduced into the film. As a result, the relative dielectric constant of the fluorine-doped silicon dioxide film adversely increases, or the SiOH groups react with the water during a heat treatment to release H<sub>2</sub>O gas. In addition, fluorine free radicals, contained in the fluorine-doped silicon dioxide film, segregate near the surface thereof during a



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nects, either. Accordingly, a CVD oxide film should be formed as an adhesion layer between the metal interconnects and the organic polymer film, too.

Moreover, an etch rate, at which an organic polymer film is etched, is approximately equal to an ash rate, at which a resist pattern is ashed with oxygen plasma. Accordingly, a usual resist application process is not applicable in such a situation, because the organic polymer film is likely to be damaged during ashing and removing the resist pattern. Therefore, a proposed alternate process includes: forming a CVD oxide film on an organic polymer film; forming a resist film on the CVD oxide film; and then etching the resist film using the CVD oxide film as an etch stopper, or a protective film.

However, during the step of forming the CVD oxide film on the organic polymer film, the surface of the organic polymer film is exposed to a reactive gas containing oxygen. Accordingly, the organic polymer film reacts with oxygen to take in polar groups such as carbonyl groups and ketone groups. As a result, the relative dielectric constant of the organic polymer film disadvantageously increases.

Also, in forming inlaid copper interconnects in the organic polymer film, a TiN adhesion layer, for example, should be formed around wiring grooves formed in the organic polymer film, because the organic polymer film cannot adhere strongly

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to the metal interconnects. However, since the TiN film has a high resistance, the effective cross-sectional area of the metal interconnects decreases. Consequently, the intended effect attainable by the use of the copper lines, i.e., re-  
5 duction in resistance, would be lost.

#### SUMMARY OF THE INVENTION

An object of the present invention is providing a method for forming an interconnection structure in which an insulat-  
10 ing film with a low dielectric constant can be formed by an ordinary resist application process.

A first method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal inter-  
15 connects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming  
20 a thin film over the third insulating film; e) forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the thin film; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for  
25 forming wiring grooves; g) forming a second resist pattern,

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having a plurality of openings for forming contact holes, on the third insulating film; h) dry-etching the third insulating film under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left; i) dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes; j) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts con-

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In this embodiment, the step c) preferably includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin.

Then, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the third insulating film with a lot more certainty.

In another embodiment, the first insulating film is also preferably mainly composed of an organic component.

Then, the conditions employed in the step i), i.e., that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, are realized with much more certainty. At the same time, the conditions employed in the step j), i.e., that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, are also realized with much more certainty.

In an embodiment where the first and third insulating films are both mainly composed of organic components, the first method preferably further includes the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process using a reactive gas containing nitrogen between the steps j) and k).

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In such a case, the adhesion between the upper-level metal interconnects and the third insulating film mainly composed of an organic component, and between the contacts and the first insulating film mainly composed of an organic component can be improved substantially without fail.

In the embodiment where the first insulating film is mainly composed of an organic component, the step a) preferably includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin.

In such a case, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the first insulating film with a lot more certainty.

A second method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the thin film; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for

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forming wiring grooves; g) forming a second resist pattern, having a plurality of openings for forming contact holes, on the third insulating film; h) dry-etching the third insulating film using the first and second resist patterns as a mask  
5 under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes;  
10 i) dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films and the first and second resist patterns are etched at a relatively  
15 low rate, thereby patterning the second insulating film to have the openings for forming contact holes; j) removing the first and second resist patterns; k) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under  
20 such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and l) filling  
25 in the wiring grooves and the contact holes with a metal film,

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thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the second method of the present invention, even if a  
5 damaged layer is formed in respective parts of the first and third insulating films that are exposed inside the openings for forming contact holes in the second insulating film during the step j) of removing the first and second resist patterns, the damaged layer can be removed without fail in the next step  
10 k). In this step, the third and first insulating films are dry-etched using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second  
15 insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively. Accordingly, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma, can be used as the first  
20 and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, the third insulating film is preferably a low-dielectric-constant SOG film  
25 with a siloxane skeleton.

In such an embodiment, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

A third method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film; e) forming a thin film over the fourth insulating film; f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves; g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes; i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for



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Accordingly, the first insulating film is not damaged, either. Thus, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma or dry etching, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, at least one of the first and third insulating films is preferably mainly composed of an organic component.

In such an embodiment, the relative dielectric constant of the interlevel insulating film can be reduced.

In another embodiment of the present invention, a size of the openings of the second resist pattern for forming contact holes is preferably larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

In such an embodiment, even if the openings of the second resist pattern for forming contact holes have misaligned with the openings of the mask pattern for forming wiring grooves, the openings of the patterned fourth insulating film for forming contact holes can be formed to be self-aligned with the openings of the mask pattern for forming wiring grooves. This is because the openings of the patterned fourth insulating film for forming contact holes are formed in respective re-

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gions where the openings of the second resist pattern for forming contact holes overlap with corresponding openings of the mask pattern for forming wiring grooves. As a result, the connection between the contacts and the upper-level metal interconnects is ensured.

A fourth method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes; h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming

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contact holes; i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes; j) dry-etching the patterned third  
5 insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and k) filling in the wiring grooves  
10 and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the fourth method of the present invention, the second insulating film exists on the first insulating film during  
15 dry-etching the third insulating film in the step h). Accordingly, the first insulating film is not damaged. Thus, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma or dry etching, can be used as the first and third insulating films. As a result,  
20 an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, at least one of the first and third insulating films is preferably mainly composed of an organic component.

25 In such an embodiment, the relative dielectric constant

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of the interlevel insulating film can be reduced.

In another embodiment of the present invention, a size of the openings of the second resist pattern for forming contact holes is preferably larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

In such an embodiment, even if the openings of the second resist pattern for forming contact holes have misaligned with the openings of the mask pattern for forming wiring grooves, the openings of the patterned third insulating film for forming contact holes can be formed to be self-aligned with the openings of the mask pattern for forming wiring grooves. This is because the openings of the patterned third insulating film for forming contact holes are formed in respective regions where the openings of the second resist pattern for forming contact holes overlap with corresponding openings of the mask pattern for forming wiring grooves. As a result, the connection between the contacts and the upper-level metal interconnects is ensured.

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#### BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a) through 1(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the first embodiment of the present invention.

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Figures 2(a) through 2(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

Figures 3(a) through 3(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

Figures 4(a) through 4(c) are cross-sectional views illustrating problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

Figures 5(a) through 5(c) are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

Figures 6(a) through 6(c) are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

Figures 7(a) through 7(c) are cross-sectional views illustrating measures to solve the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

Figures 8(a) through 8(c) are cross-sectional views illustrating the measures to solve the problems caused by the

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misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

5 Figures 9(a) through 9(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the second embodiment of the present invention.

10 Figures 10(a) through 10(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

Figures 11(a) through 11(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

15 Figures 12(a) through 12(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the third embodiment of the present invention.

20 Figures 13(a) through 13(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

Figures 14(a) through 14(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

25 Figures 15(a) through 15(c) are cross-sectional views illustrating respective process steps for forming an inter-





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illustrating respective process steps for forming the inter-connection structure of the fifth embodiment.

Figures 23(a) through 23(d) are cross-sectional views illustrating respective process steps for forming the inter-connection structure of the fifth embodiment.

Figures 24(a) through 24(c) are cross-sectional views illustrating respective process steps for forming an inter-connection structure according to a modified example of the fifth embodiment.

Figures 25(a) through 25(c) are cross-sectional views illustrating respective process steps for forming the inter-connection structure in the modified example of the fifth embodiment.

Figures 26(a) through 26(d) are cross-sectional views illustrating respective process steps for forming the inter-connection structure in the modified example of the fifth embodiment.

Figures 27(a) and 27(b) are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

Figures 28(a) and 28(b) are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

Figures 29(a) and 29(b) are perspective views illustrating respective process steps for forming the interconnection

structure in the modified example of the fifth embodiment.

5 Figures 30(a) through 30(c) are cross-sectional views illustrating respective process steps for forming an inter-connection structure according to the sixth embodiment of the present invention.

Figures 31(a) through 31(c) are cross-sectional views illustrating respective process steps for forming the inter-connection structure of the sixth embodiment.

10 Figures 32(a) through 32(c) are cross-sectional views illustrating respective process steps for forming the inter-connection structure of the sixth embodiment.

15 Figures 33(a) through 33(c) are cross-sectional views illustrating respective process steps for forming an inter-connection structure according to a modified example of the sixth embodiment.

Figures 34(a) through 34(c) are cross-sectional views illustrating respective process steps for forming the inter-connection structure in the modified example of the sixth embodiment.

20 Figures 35(a) through 35(c) are cross-sectional views illustrating respective process steps for forming the inter-connection structure in the modified example of the sixth embodiment.

25 Figure 36 is a plan view illustrating a positional relationship between the openings of a mask pattern for forming

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wiring grooves and the openings of a second resist pattern for forming contact holes in the modified example of the fifth embodiment.

Figure 37(a) illustrates respective positional relationships between the mask pattern and the second resist pattern and between a first metal interconnect and an associated contact in the modified example of the fifth embodiment;

Figure 37(b) illustrates respective positional relationships between the mask pattern and the second resist pattern and between a first metal interconnect and an associated contact in the fifth embodiment.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

##### EMBODIMENT 1

Hereinafter, an exemplary method for forming an interconnection structure according to the first embodiment of the present invention will be described with reference to Figures 1(a) through 1(c), Figures 2(a) through 2(c) and Figures 3(a) through 3(c).

First, as shown in Figure 1(a), a silicon nitride film 102 is formed over first metal interconnects 101 formed on a semiconductor substrate 100. The silicon nitride film 102 is formed to be 50 nm thick, for example, and used to protect the first metal interconnects 101 during a subsequent etching process step. Thereafter, a first organic film 103 (first in-

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instance, the film 104 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. In such a case, an organic-containing silicon dioxide film 104, having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide, can be obtained.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films 103 and 105 and the organic-containing silicon dioxide film 104, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 106.

Next, as shown in Figure 1(b), a first resist pattern 107, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 106. Thereafter, the titanium nitride film 106 is dry-etched using the first resist pattern 107 as a mask, thereby forming a mask pattern 108 out of the titanium nitride film 106 as shown in Figure 1(c).

Subsequently, a second resist pattern 109, having openings for forming contact holes, is formed by lithography on the second organic film 105 without removing the first resist pattern 107. Then, the second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the openings for forming contact holes as shown in Figure 2(a). In this case, since the second organic film 105 and the first

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105A as shown in Figure 2(c). At the same time, the first organic film 103 is also dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact  
5 holes as shown in Figure 2(c).

Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101  
10 within the contact holes 110 as shown in Figure 3(a).

Then, as shown in Figure 3(b), an adhesion layer 112, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film 113 is deposited  
15 over the entire surface of the substrate to completely fill in the contact holes 110 and the wiring grooves 111. In this embodiment, the metal film 113 may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the  
20 metal film 113 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure 3(c), respective portions of the adhesion layer 112, the metal film 113 and the mask pattern 108, which are deposited on the patterned second organic  
25 film 105A, are removed by a CMP technique, for example. As a





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100 as shown in Figure 4(a). Thereafter, a first organic film 103, mainly composed of an organic component, is formed to be 1 $\mu$ m thick, for example, on the silicon nitride film 102.

Next, an organic-containing silicon dioxide film 104, 5 containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the first organic film 103. Then, a second organic film 105, mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film 104. And a 10 titanium nitride film 106 is formed to be 50 nm thick, for example, on the second organic film 105.

Next, as shown in Figure 4(b), a first resist pattern 107, having openings for forming wiring grooves, is formed on the titanium nitride film 106. Thereafter, the titanium ni- 15 tride film 106 is dry-etched using the first resist pattern 107 as a mask, thereby forming a mask pattern 108 out of the titanium nitride film 106 as shown in Figure 4(c).

Subsequently, a second resist pattern 109, having openings for forming contact holes, is formed on the second or- 20 ganic film 105 without removing the first resist pattern 107. As can be seen if Figures 5(a) and 1(c) are compared with each other, the second resist pattern 109 has misaligned with the first resist pattern 107 in this case.

Then, the second organic film 105 is dry-etched, thereby 25 forming a patterned second organic film 105A having the open-

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ings for forming contact holes as shown in Figure 5(a). As in the first embodiment, since the second organic film 105 and the first and second resist patterns 107 and 109 are all mainly composed of organic components, the first and second resist patterns 107 and 109 are removed simultaneously with the dry-etching of the second organic film 105. In this case, since the second resist pattern 109 has misaligned with the first resist pattern 107, the diameter of the openings for forming contact holes, which are provided in the second organic film 105A, is smaller than desired.

Then, the organic-containing silicon dioxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic-containing silicon dioxide film 104A having the openings for forming contact holes as shown in Figure 5(c).

Next, the patterned second organic film 105A is dry-etched using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in Figure 6(a). At the same time, the first organic film 103 is also dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes 110 as shown in Figure 6(a). Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby form-

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ing a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes 110 as shown in Figure 6(b).

Then, an adhesion layer 112, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer 112, the metal film and the mask pattern 108, which are deposited on the patterned second organic film 105A, are removed by a CMP technique, for example. As a result, second metal interconnects 114 are certainly formed. However, since the diameter of the contact holes 110 is smaller than desired, the contact holes 110 cannot be completely filled in with the metal film, and the first and second metal interconnects 101 and 112 cannot be connected to each other, resulting in a contact failure.

Next, it will be described with reference to Figures 7(a) through 7(c) and Figures 8(a) through 8(c) what measures should be taken to solve the problems caused by the misalignment of the second resist pattern 109.

First, a second resist pattern 109, having openings for forming contact holes, is formed through the same process steps as those described with reference to Figures 4(a) through 4(c) and Figure 5(a). In this case, the second re-



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sist pattern 109 has also misaligned with the first resist pattern 107 (see Figure 5(a)).

Thus, as shown in Figure 7(a), the first resist pattern 107 and the mask pattern 108 are dry-etched using the second resist pattern 109 as a mask. In this manner, portions of the first resist pattern 107, not overlapping with the second resist pattern 109, are removed and each opening of the mask pattern 108 is expanded to be equal to or larger than each opening for forming wiring grooves or each opening for forming contact holes. As a result, the pattern for the openings of the second resist pattern for forming contact holes 109 can be transferred to the first resist pattern 107 and the mask pattern 108.

Then, the second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the openings for forming contact holes as shown in Figure 7(b). In this case, since the second organic film 105 and the first and second resist patterns 107 and 109 are all mainly composed of organic components, the first and second resist patterns 107 and 109 are removed simultaneously with the dry-etching of the second organic film 105.

Then, the organic-containing silicon dioxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic-containing silicon dioxide film 104A having the openings for forming contact

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holes as shown in Figure 7(c).

As described above, the second resist pattern 109 has misaligned with the first resist pattern 107. However, in this case, the pattern for the openings of the second resist pattern for forming contact holes 109 has been successfully transferred to the first resist pattern 107 and the mask pattern 108. Thus, the diameter of the openings for forming contact holes, which have been formed in the patterned second organic film 105A and the patterned organic-containing silicon dioxide film 104A, is a predetermined size.

Next, the patterned second organic film 105A is dry-etched using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in Figure 8(a). At the same time, the first organic film 103 is also dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes 110 as shown in Figure 8(a). Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes 110 as shown in Figure 8(b).

Then, an adhesion layer 112, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall

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faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer 112, the metal film and the mask pattern 108, which are  
5 deposited on the patterned second organic film 105A, are removed by a CMP technique, for example. As a result, second metal interconnects 114 and contacts 115 are formed out of the titanium nitride film 112 and the metal film as shown in Figure 8(c).

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EMBODIMENT 2

Next, an exemplary method for forming an interconnection structure according to the second embodiment of the present invention will be described with reference to Figures 9(a) through 9(c), Figures 10(a) through 10(c) and Figures 11(a) through 11(c).  
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First, as shown in Figure 9(a), a silicon nitride film 202 is formed to be 50 nm thick, for example, over first metal interconnects 201 formed on a semiconductor substrate  
20 200. Thereafter, a first organic film 203 (first insulating film), mainly composed of an organic component, is formed to be 1 $\mu$ m thick, for example, on the silicon nitride film 202. Next, an organic-containing silicon dioxide film 204 (second insulating film), containing an organic component in silicon  
25 dioxide, is formed to be 50 nm thick, for example, on the fir-

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st organic film 203. Then, a second organic film 205 (third insulating film), mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film 204. And a titanium nitride film 206 is formed to be 50 nm thick, for example, on the second organic film 205.

The first and second organic films 203 and 205 may be deposited by any arbitrary technique. For example, these films 203 and 205 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films 203 and 205.

Similarly, the organic-containing silicon dioxide film 204 may also be deposited by any arbitrary technique. For instance, the film 204 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films 203 and 205 and the organic-containing silicon dioxide film 204, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 206.

Next, as shown in Figure 9(b), a first resist pattern 207, having openings for forming wiring grooves, is formed by

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lithography on the titanium nitride film 206. Thereafter, the titanium nitride film 206 is dry-etched using the first resist pattern 207 as a mask, thereby forming a mask pattern 208 out of the titanium nitride film 206 as shown in Figure 9(c).

5       Subsequently, a second resist pattern 209, having openings for forming contact holes, is formed by lithography on the second organic film 205 without removing the first resist pattern 207. Then, the second organic film 205 is dry-etched, thereby forming a patterned second organic film 205A having  
10 the openings for forming contact holes as shown in Figure 10(a). In this case, since the second organic film 205 and the first and second resist patterns 207 and 209 are all mainly composed of organic components, the second organic film 205 is etched at a rate substantially equal to that of the first  
15 and second resist patterns 207 and 209. Accordingly, when the second organic film 205 is dry-etched, the first and second resist patterns 207 and 209 are also removed simultaneously.

If the second resist pattern 209 may have been misaligned with the first resist pattern 207, then the first resist pattern 207 and the mask pattern 208 should be dry-  
20 etched using the second resist pattern 209 as a mask. In this manner, parts of the first resist pattern 207, not overlapping with the second resist pattern 209, are removed and the openings of the mask pattern 208 are expanded to be equal  
25 to or larger than the openings for forming wiring grooves and

contact holes as described in the first embodiment.

Then, the organic-containing silicon dioxide film 204 is dry-etched using the patterned second organic film 205A as a mask, thereby forming a patterned organic-containing silicon dioxide film 204A having the openings for forming contact holes as shown in Figure 10(b). Next, the patterned second organic film 205A is dry-etched using the mask pattern 208 as a mask, thereby forming the wiring grooves 211 in the patterned second organic film 205A as shown in Figure 10(c). At the same time, the first organic film 203 is also dry-etched using the patterned organic-containing silicon dioxide film 204A as a mask, thereby forming a patterned first organic film 203A having the contact holes 210 as also shown in Figure 10(c).

Subsequently, the silicon nitride film 202 is dry-etched using the patterned organic-containing silicon dioxide film 204A as a mask, thereby forming a patterned silicon nitride film 202A and exposing the first metal interconnects 201 within the contact holes 210 as shown in Figure 11(a).

Then, the patterned first and second organic films 203A and 205A are subjected to plasma processing using ammonium gas. As a result, as shown in Figure 11(b), an adhesion layer 212, including amino and amide groups, is deposited on the wall faces of the patterned first organic film 203A exposed inside the contact holes 210 and on the wall faces of

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the patterned second organic film 205A exposed inside the wiring grooves 211. Thereafter, a metal film 213 is deposited over the entire surface of the substrate to completely fill in the contact holes 210 and the wiring grooves 211. In this embodiment, the metal film 213 may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 213 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

10 Finally, as shown in Figure 11(c), respective portions of the metal film 213 and the mask pattern 208, which are deposited on the patterned second organic film 205A, are removed by a CMP technique, for example. As a result, second metal interconnects 214 and contacts 215 are formed out of  
15 the metal film 213.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 214 through the same process steps as those described above.

20

### EMBODIMENT 3

Next, an exemplary method for forming an interconnection structure according to the third embodiment of the present invention will be described with reference to Figures 12(a) through 12(c), Figures 13(a) through 13(c) and Figures 14(a)  
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41 42



through 14(c).

First, as shown in Figure 12(a), a silicon nitride film 302 is formed over first metal interconnects 301 formed on a semiconductor substrate 300. The silicon nitride film 302 is formed to be 50 nm thick, for example, and to protect the first metal interconnects 301 during a subsequent etching process step. Thereafter, a first organic-containing silicon dioxide film 303 (first insulating film), containing an organic component in silicon dioxide, is formed to be 1 $\mu$ m thick, for example, on the silicon nitride film 302. Next, a low-dielectric-constant SOG film 304 (second insulating film), having a siloxane skeleton, is deposited to be 400 nm thick, for example, on the first organic-containing silicon dioxide film 303. Then, a second organic-containing silicon dioxide film 305 (third insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the low-dielectric-constant SOG film 304. And a titanium nitride film 306 is formed to be 50 nm thick, for example, on the second organic-containing silicon dioxide film 305.

The first and second organic-containing silicon dioxide films 303 and 305 may be deposited by any arbitrary technique. For example, these films 303 and 305 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Also, an HSQ film may be used as the low-



13(b).

Next, as shown in Figure 13(c), the second resist pattern 309 is removed and the patterned second organic-containing silicon dioxide film 305A is dry-etched using the mask pattern 308 as a mask, thereby forming openings for forming wiring grooves in the patterned second organic-containing silicon dioxide film 305A. Thereafter, the patterned low-dielectric-constant SOG film 304A is dry-etched using the mask pattern 308 and the patterned second organic-containing silicon dioxide film 305A having the openings for wiring grooves as a mask, thereby forming the wiring grooves 311. In forming the wiring grooves 311, by selecting such etching conditions that the first organic-containing silicon dioxide film 303A is etched at a rate sufficiently lower than that of the low-dielectric-constant SOG film 304A, sufficient selectivity can be secured for the patterned first organic-containing silicon dioxide film 303A. Accordingly, the depth of the wiring grooves 311 can be determined univalently at the sum of the thicknesses of the second organic-containing silicon dioxide film 305 and the low-dielectric-constant SOG film 304.

If the second resist pattern 309 may have been misaligned with the first resist pattern 307, the mask pattern 308 should be dry-etched using the second resist pattern 309 as a mask before the second organic-containing silicon dioxide film 305 is dry-etched using the second resist pattern

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ing contact holes, are exposed to oxygen plasma and damaged. However, the damaged layer, formed in the patterned low-dielectric-constant SOG film 304A, can be removed when the wiring grooves 311 are formed in the patterned low-dielectric-constant SOG film 304A, and does not have harmful effects on subsequent process steps.

Accordingly, the low-dielectric-constant SOG film 304 may be made of a material degradable with oxygen plasma. For example, in general, if an HSQ film is exposed to oxygen plasma, the Si-H bonds thereof are oxidized and the content of water and the relative dielectric constant thereof both increase to deteriorate the reliability and performance of the device. However, according to the third embodiment, the patterned low-dielectric-constant SOG film 304A, in which the wiring grooves 311 have already been formed, is not affected by oxygen plasma. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

20 MODIFIED EXAMPLE OF EMBODIMENT 3

Next, an exemplary method for forming an interconnection structure according to a modified example of the third embodiment of the present invention will be described with reference to Figures 15(a) through 15(c), Figures 16(a) through 16(c) and Figures 17(a) through 17(c).

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First, as shown in Figure 15(a), a silicon nitride film 352 is formed over first metal interconnects 351 formed on a semiconductor substrate 350. The silicon nitride film 352 is formed to be 50 nm thick, for example, and to protect the first metal interconnects 351 during a subsequent etching process step. Thereafter, a first silicon dioxide film 353 (first insulating film) is formed to be 1 $\mu$ m thick, for example, on the silicon nitride film 352. Next, an organic film 354 (second insulating film) is deposited to be 400 nm thick, for example, on the first silicon dioxide film 353. Then, a second silicon dioxide film 355 (third insulating film) is formed to be 50 nm thick, for example, on the organic film 354. And a titanium nitride film 356 is formed to be 50 nm thick, for example, on the second silicon dioxide film 355.

The first and second silicon dioxide films 353 and 355 may be deposited by any arbitrary technique. For example, these films 353 and 355 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

It should be noted that a thin film showing high etch selectivity with respect to the first and second silicon dioxide films 353 and 355 and the organic film 354, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 356.

Next, as shown in Figure 15(b), a first resist pattern 357, having openings for forming wiring grooves, is formed by



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lithography on the titanium nitride film 356. Thereafter, the titanium nitride film 356 is dry-etched using the first resist pattern 357 as a mask, thereby forming a mask pattern 358 out of the titanium nitride film 356 as shown in Figure 15(c).

5 Subsequently, as shown in Figure 16(a), the first resist pattern 357 is removed and then a second resist pattern 359, having openings for forming contact holes, is formed on the second silicon dioxide film 355. Then, the second silicon dioxide film 355 and the organic film 354 are sequentially dry-  
10 etched using the second resist pattern 359 as a mask, thereby forming a patterned second silicon dioxide film 355A and a patterned organic film 354A having openings 360 for forming contact holes as shown in Figure 16(b). In this case, the second resist pattern 359 is removed during the step of etch-  
15 ing the organic film 354.

Next, as shown in Figure 16(c), the first silicon dioxide film 353 is dry-etched using the patterned second silicon dioxide film 355A and the patterned organic film 354A as a mask, thereby forming a patterned first silicon dioxide film 353A  
20 having contact holes 361. In this etching process step, the mask pattern 358 is transferred to the patterned second silicon dioxide film 355A. Accordingly, openings for forming wiring grooves are formed in the patterned second silicon dioxide film 355A.

25 Thereafter, as shown in Figure 16(d), the patterned or-

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ganic film 354A is dry-etched using the mask pattern 358 and the patterned second silicon dioxide film 355A having the openings for forming wiring grooves as a mask, thereby forming the wiring grooves 362. In forming the wiring grooves 362, by  
5 selecting such etching conditions that the first silicon dioxide film 353A is etched at a rate sufficiently lower than that of the organic film 354A, sufficient selectivity can be secured for the patterned first silicon dioxide film 353A. Accordingly, the depth of the wiring grooves 362 can be de-  
10 termined univalently at the sum of the thicknesses of the second silicon dioxide film 355 and the organic film 354.

If the second resist pattern 359 may have been misaligned with the first resist pattern 357, then the mask pattern 358 should be dry-etched using the second resist pattern  
15 359 as a mask before the second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask. That is to say, if the mask pattern 358 is partially exposed inside the openings of the second resist pattern 359 for forming contact holes because of the misalignment of the sec-  
20 ond resist pattern 359 with the first resist pattern 357, then the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask. In this manner, the openings of the mask pattern 358 are expanded to include the openings for forming wiring grooves and contact holes.

25 Subsequently, the silicon nitride film 352 is dry-etched

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using the patterned first silicon dioxide film 353A as a mask, thereby forming a patterned silicon nitride film 352A and exposing the first metal interconnects 351 within the contact holes 361 as shown in Figure 17(a).

5 Then, as shown in Figure 17(b), an adhesion layer 363, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 361 and the wiring grooves 362. Thereafter, a metal film 364 is deposited over the entire surface of the substrate to completely fill in  
10 the contact holes 361 and the wiring grooves 362. In this embodiment, the metal film 364 may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 364 may be deposited by any arbitrary technique.  
15 For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure 17(c), respective portions of the adhesion layer 363, the metal film 364 and the mask pattern 358, which are deposited on the patterned second silicon dioxide film 355A, are removed by a CMP technique,  
20 for example. As a result, second metal interconnects 365 and contacts 366, connecting the first and second metal interconnects 351 and 365, are formed out of the metal film 364.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, inter-  
25 connects and contacts on the second metal interconnects 365

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through the same process steps as those described above.

In this modified example of the third embodiment, while the first resist pattern 357 is ashed and removed by oxygen plasma, the organic film 354 is not exposed to the oxygen plasma, because the second silicon dioxide film 355 exists on the organic film 354.

Also, in this example, the second resist pattern 359 is removed while the second silicon dioxide film 355 and the organic film 354 are dry-etched using the second resist pattern 359 as a mask. Accordingly, since there is no need to ash and remove the second resist pattern 359 with oxygen plasma, the organic film 354 is not exposed to oxygen plasma.

#### EMBODIMENT 4

Next, an exemplary method for forming an interconnection structure according to the fourth embodiment of the present invention will be described with reference to Figures 18(a) through 18(c), Figures 19(a) through 19(c) and Figures 20(a) through 20(c).

First, as shown in Figure 18(a), a silicon nitride film 402 is formed over first metal interconnects 401 formed on a semiconductor substrate 400. The silicon nitride film 402 is formed to be 50 nm thick, for example, and to protect the first metal interconnects 401 during a subsequent etching process step. Thereafter, a first low-dielectric-constant



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sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 406.

Next, as shown in Figure 18(b), a first resist pattern 407, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 406. Thereafter, the titanium nitride film 406 is dry-etched using the first resist pattern 407 as a mask, thereby forming a mask pattern 408 out of the titanium nitride film 406 as shown in Figure 18(c).

Subsequently, a second resist pattern 409, having openings for forming contact holes, is formed by lithography on the second low-dielectric-constant SOG film 405 without removing the first resist pattern 407. Then, the second low-dielectric-constant SOG film 405 and the organic-containing silicon dioxide film 404 are sequentially dry-etched using the second resist pattern 409 as a mask, thereby forming a patterned second low-dielectric-constant SOG film 405A and a patterned organic-containing silicon dioxide film 404A as shown in Figure 19(a).

Next, the first and second resist patterns 407 and 409 are ashed and removed with oxygen plasma. As a result, a damaged layer 410 is unintentionally formed in respective portions of the patterned second low-dielectric-constant SOG film 405A and the first low-dielectric-constant SOG film 403, which are exposed inside the openings for forming contact holes, as shown in Figure 19(b).

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cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 414 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure 20(c), respective portions of the adhesion layer 413, the metal film 414 and the mask pattern 408, which are deposited on the patterned second low-dielectric-constant SOG film 405A, are removed by a CMP technique, for example. As a result, second metal interconnects 415 and contacts 416, connecting the first and second metal interconnects 401 and 415, are formed out of the metal film 414.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 415 through the same process steps as those described above.

In the fourth embodiment, while the first and second resist patterns 407 and 409 are ashed and removed with oxygen plasma, a damaged layer 410 is formed in the first low-dielectric-constant SOG film 403 and the patterned second low-dielectric-constant SOG film 405A. But the damaged layer 410 can be removed while the contact holes 411 and the wiring grooves 412 are formed.

Accordingly, the first and second low-dielectric-constant SOG films 403 and 405 may be made of a material degradable with oxygen plasma. For example, in general, if an





ple, these films 504 and 506 may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films 503 and 505 and the first and second silicon dioxide films 504 and 506, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 507.

Next, as shown in Figure 21(b), a first resist pattern 508, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 507. Thereafter, the titanium nitride film 507 is dry-etched using the first resist pattern 508 as a mask, thereby forming a mask pattern 509, having openings for forming wiring grooves, out of the titanium nitride film 507 as shown in Figure 21(c).

Subsequently, as shown in Figure 22(a), the first resist pattern 508 is removed by oxygen plasma, for example. In this case, even if the first resist pattern 508 is ashed and removed using oxygen plasma, the quality of the second organic film 505 does not degrade, because the second silicon dioxide film 506 exists on the second organic film 505 mainly composed of an organic component.

Then, as shown in Figure 22(b), a second resist pattern 510, having openings for forming contact holes, is formed by lithography on the mask pattern 509. Thereafter, the second

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silicon dioxide film 506 is dry-etched using the second resist pattern 510 and the mask pattern 509 as a mask, thereby forming a patterned second silicon dioxide film 506A having openings for forming contact holes as shown in Figure 22(c).

5 Next, the second organic film 505 is dry-etched using the patterned second silicon dioxide film 506A as a mask, thereby forming a patterned second organic film 505A having openings for forming contact holes as shown in Figure 23(a). In this case, the second organic film 505 and the second resist pattern 510 are both mainly composed of organic components, the second organic film 505 is etched at a substantially equal rate to that of the second resist pattern 510. Thus, when the second organic film 505 is dry-etched, the second resist pattern 510 is also removed simultaneously. The patterned second silicon dioxide film 506A functions as an etch stopper during dry-etching the second resist pattern 510.

It should be noted that part of the second resist pattern 510 may be left in the process step of dry-etching the second organic film 505. This is because the residual second resist pattern 510 can be removed during a subsequent process step of dry-etching the first organic film 503 (see Figure 23(c)).

Thereafter, the patterned second silicon dioxide film 506A and the first silicon dioxide film 504 are dry-etched using the mask pattern 509 and the patterned second organic film

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505A as respective masks, thereby forming a patterned second silicon dioxide film 506B having openings for forming wiring grooves and a patterned first silicon dioxide film 504A having openings for forming contact holes as shown in Figure 23(b).

5 Then, the patterned second organic film 505A and the first organic film 503 are dry-etched using the mask pattern 509 and the patterned first silicon dioxide film 504A as respective masks, thereby forming a patterned second organic film 505B having wiring grooves 511 and a patterned first organic  
10 film 503A having contact holes 512 as shown in Figure 23(c).

Subsequently, the silicon nitride film 502 is dry-etched using the patterned first silicon dioxide film 504A as a mask, thereby forming a patterned silicon nitride film 502A (see Figure 23(d)) and exposing the first metal interconnects 501  
15 within the contact holes 512. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 512 and the wiring grooves 511 as in the first embodiment. Thereafter, a metal film is deposited over the entire  
20 surface of the substrate to completely fill in the contact holes 512 and the wiring grooves 511. In this embodiment, the metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be de-  
25 posited by any arbitrary technique. For instance, plating,

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CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern 509, which are deposited on the patterned second silicon dioxide film 506B, are removed by a CMP technique, for example. As a result, second metal interconnects 513 and contacts 514, connecting the first and second metal interconnects 501 and 513 together, are formed as shown in Figure 23(d).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 513 through the same process steps as those described above.

In the fifth embodiment, while the first resist pattern 508 is being removed by oxygen plasma, for example, the quality of the second organic film 505 does not degrade. This is because the second silicon dioxide film 506 exists on the second organic film 505, which is likely to be damaged by oxygen plasma.

Also, in this embodiment, the first silicon dioxide film 504 functions as an etch stopper during dry-etching the second organic film 505. Accordingly, it is possible to prevent the quality of the first organic film 503 from being degraded.

MODIFIED EXAMPLE OF EMBODIMENT 5

Next, a method for forming an interconnection structure





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posited by any arbitrary technique as in the fifth embodiment. Also, a thin film showing high etch selectivity with respect to the first and second organic films 553 and 555 and the first and second silicon dioxide films 554 and 556 may be used instead of the titanium nitride film 557.

Next, as shown in Figure 24(b), a first resist pattern 558, having openings for forming wiring grooves, is formed on the titanium nitride film 557. Thereafter, the titanium nitride film 557 is dry-etched using the first resist pattern 558 as a mask, thereby forming a mask pattern 559, having openings for forming wiring grooves, out of the titanium nitride film 557 as shown in Figure 24(c).

Subsequently, as shown in Figures 25(a) and 27(a), the first resist pattern 558 is removed. Then, a second resist pattern 560, having openings for forming contact holes, is formed on the mask pattern 559 as shown in Figure 25(b). in this modified example of the fifth embodiment, the sizes of the openings of the second resist pattern 560 for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to wiring grooves for forming second metal interconnects. The reason thereof will be described later.

Then, the second silicon dioxide film 556 is dry-etched using the second resist pattern 560 and the mask pattern 559 as a mask, thereby forming a patterned second silicon dioxide



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563 together with a lot more certainty.

Next, the second organic film 555 is dry-etched using the patterned second silicon dioxide film 556A as a mask, thereby forming a patterned second organic film 555A having openings for forming contact holes as shown in Figures 26(a) and 28(a). In this case, the second organic film 555 and the second resist pattern 560 are both mainly composed of organic components, the second organic film 555 is etched at a substantially equal rate to that of the second resist pattern 560. Thus, when the second organic film 555 is dry-etched, the second resist pattern 560 is also removed simultaneously. It should be noted that part of the second resist pattern 560 may be left in the process step of dry-etching the second organic film 555. This is because the residual second resist pattern 560 can be removed during a subsequent process step of dry-etching the first organic film 553 (see Figure 26(c)).

Thereafter, the patterned second silicon dioxide film 556A and the first silicon dioxide film 554 are dry-etched using the mask pattern 559 and the patterned second organic film 555A as respective masks, thereby forming a patterned second silicon dioxide film 556B having wiring grooves and a patterned first silicon dioxide film 554A having openings for forming contact holes as shown in Figures 26(b) and 28(b).

Then, the patterned second organic film 555A is dry-etched using the mask pattern 559 and the patterned second

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silicon dioxide film 556B as a mask, and the first organic film 553 is dry-etched using the patterned first silicon dioxide film 554A as a mask, thereby forming a patterned second organic film 555B having wiring grooves 561 and a patterned first organic film 553A having contact holes 562 as shown in Figures 26(c) and 29(a).

Subsequently, the silicon nitride film 552 is dry-etched using the patterned first silicon dioxide film 554A as a mask, thereby forming a patterned silicon nitride film 552A (see Figure 26(d)) having contact holes, and exposing the first metal interconnects 551 within the contact holes 562. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 562 and the wiring grooves 561 as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 562 and the wiring grooves 561. Finally, respective portions of the adhesion layer, the metal film and the mask pattern 559, which are deposited on the patterned second silicon dioxide film 556B, are removed by a CMP technique, for example. As a result, second metal interconnects 563 and contacts 564, connecting the first and second metal interconnects 551 and 563 together, are formed as shown in Figures 26(d) and 29(b).

It should be noted that a multilevel interconnection

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sist pattern 510 and between a first metal interconnect 501 and a contact 514 in the fifth embodiment. Specifically, the upper part of Figure 37(b) illustrates a positional relationship between an opening of the mask pattern 509 for forming a wiring groove and an associated opening of the second resist pattern 510 for forming a contact hole. The middle part of Figure 37(b) illustrates the cross section of the upper part taken along the line B-B. And the lower part of Figure 37(b) illustrates a positional relationship between a first metal interconnect 501 and an associated contact 514.

Setting the size of an opening of the second resist pattern 510 for forming a contact hole at the designed size thereof as in the fifth embodiment, if the opening of the second resist pattern 510 for forming a contact hole has misaligned with an associated opening of the mask pattern 509 for forming a wiring groove, then the contact area (indicated by hatching) between the contact 514 and the first metal interconnect 501 greatly decreases as can be seen from Figure 37(b). In contrast, setting the size of an opening of the second resist pattern 560 for forming a contact hole larger than the designed size thereof as in this modified example of the fifth embodiment, even if the opening of the second resist pattern 560 for forming a contact hole has misaligned with an associated opening of the mask pattern 559 for forming a wiring groove, the contact area (indicated by hatching) between

the contact 564 and the first metal interconnect 551 does not decrease so much as can be seen from Figure 37(a).

#### EMBODIMENT 6

5 Next, an exemplary method for forming an interconnection structure according to the sixth embodiment of the present invention will be described with reference to Figures 30(a) through 30(c), Figures 31(a) through 31(c) and Figures 32(a) through 32(c).

10 First, as shown in Figure 30(a), a silicon nitride film 602 is formed over first metal interconnects 601 formed on a semiconductor substrate 600. The silicon nitride film 602 is formed to be 50 nm thick, for example, and to protect the first metal interconnects 601 during a subsequent etching  
15 process step. Thereafter, a first organic film 603 (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film 602. Then, a silicon dioxide film 604 (second insulating film) is deposited to be 100 nm thick, for example,  
20 on the first organic film 603. Subsequently, a second organic film 605 (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the silicon dioxide film 604. And a titanium nitride film 606 (thin film) is deposited to be 50 nm thick, for example,  
25 on the second organic film 605.

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The first and second organic films 603 and 605 may be deposited by any arbitrary technique. For example, these films 603 and 605 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films 603 and 605. More specifically, the organic films 603 and 605 may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The silicon dioxide film 604 may also be deposited by any arbitrary technique. For example, the film 604 may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films 603 and 605 and the silicon dioxide film 604, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 606.

Next, as shown in Figure 30(b), a first resist pattern 607, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 606. Thereafter, the titanium nitride film 606 is dry-etched using the first resist pattern 607 as a mask, thereby forming a mask pattern 608, having openings for forming wiring grooves, out of the titani-

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um nitride film 606 as shown in Figure 30(c).

Subsequently, as shown in Figure 31(a), the first resist pattern 607 is removed using an organic parting agent, for example. In such a case, since the second organic film 605 is not exposed to oxygen plasma, the quality of the second organic film 605 does not degrade.

Then, as shown in Figure 31(b), a second resist pattern 609, having openings for forming contact holes, is formed by lithography on the mask pattern 608. Then, the second organic film 605 is dry-etched using the second resist pattern 609 and the mask pattern 608 as a mask, thereby forming a patterned second organic film 605A having openings for forming contact holes as shown in Figure 31(c). In this case, the second organic film 605 and the second resist pattern 609 are both mainly composed of organic components, the second organic film 605 is etched at a substantially equal rate to that of the second resist pattern 609. Thus, when the second organic film 605 is dry-etched, the second resist pattern 609 is also removed simultaneously.

It should be noted that part of the second resist pattern 609 may be left in the process step of dry-etching the second organic film 605. This is because the residual second resist pattern 609 can be removed during a subsequent process step of dry-etching the first organic film 603 (see Figure 32(b)).

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Thereafter, the silicon dioxide film 604 is dry-etched using the patterned second organic film 605A as a mask, thereby forming a patterned silicon dioxide film 604A having openings for forming contact holes as shown in Figure 32(a).

5 Then, the patterned second organic film 605A and the first organic film 603 are dry-etched using the mask pattern 608 and the patterned silicon dioxide film 604A as respective masks, thereby forming a patterned second organic film 605B having wiring grooves 610 and a patterned first organic film  
10 603A having contact holes 611 as shown in Figure 32(b).

Subsequently, the patterned silicon dioxide film 604A and the silicon nitride film 602 are dry-etched using the mask pattern 608 and the patterned first organic film 603A as respective masks, thereby forming a patterned silicon dioxide  
15 film 604B having wiring grooves (see Figure 32(c)) and a patterned silicon nitride film 602A having the contact holes (see Figure 32(c)), and exposing the first metal interconnects 601 within the contact holes 611. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be  
20 50 nm thick, for example, on the wall faces of the contact holes 611 and the wiring grooves 610 as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 611 and the wiring grooves 610. In this embodiment, the  
25 metal film may be made of any arbitrary metal. For example,

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copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern 608, which are deposited on the patterned second organic film 605B, are removed by a CMP technique, for example. As a result, second metal interconnects 612 and contacts 613, connecting the first and second metal interconnects 601 and 612 together, are formed as shown in Figure 32(c).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 612 through the same process steps as those described above.

In the sixth embodiment, a patterned second organic film 605B, having wiring grooves 610, and a patterned first organic film 603A, having contact holes 611, are formed by a single dry-etching process using the mask pattern 608, having the openings for forming wiring grooves, and the patterned silicon dioxide film 604A as respective masks. That is to say, the wiring grooves 610 and the contact holes 611 can be formed during the same etching process step. Accordingly, a dual damascene structure can be formed with the increase in number of process steps suppressed.

Also, in the sixth embodiment, since the first resist

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film 655 (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the silicon dioxide film 654. And a titanium nitride film 656 (thin film) is deposited to be 50 nm thick, for example, on the second organic film 655.

The first and second organic films 653 and 655 may be deposited by any arbitrary technique. For example, these films 653 and 655 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films 653 and 655. More specifically, the organic films 653 and 655 may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The silicon dioxide film 654 may also be deposited by any arbitrary technique. For example, the film 654 may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films 653 and 655 and the silicon dioxide film 654, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film 656.

Next, as shown in Figure 33(b), a first resist pattern

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657, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 656. Thereafter, the titanium nitride film 656 is dry-etched using the first resist pattern 657 as a mask, thereby forming a mask pattern 658, 5 having openings for forming wiring grooves, out of the titanium nitride film 656 as shown in Figure 33(c).

Subsequently, as shown in Figure 34(a), the first resist pattern 657 is removed by an organic parting agent, for example. In such a case, since the second organic film 655 is not 10 exposed to oxygen plasma, the quality of the second organic film 655 does not degrade.

Then, as shown in Figure 34(b), a second resist pattern 659, having openings for forming contact holes, is formed by lithography on the mask pattern 658. In this modified example 15 of the sixth embodiment, the sizes of the openings of the second resist pattern 659 for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming second metal interconnects. The reason thereof will 20 be described later.

Next, the second organic film 655 is dry-etched using the second resist pattern 659 and the mask pattern 658 as a mask, thereby forming a patterned second organic film 655A having openings for forming contact holes as shown in Figure 34(c). 25 In this case, the second organic film 655 and the second re-

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sist pattern 659 are both mainly composed of organic components, the second organic film 655 is etched at a substantially equal rate to that of the second resist pattern 659. Thus, when the second organic film 655 is dry-etched, the second resist pattern 659 is also removed simultaneously. It should be noted that part of the second resist pattern 659 may be left in the process step of dry-etching the second organic film 655. This is because the residual second resist pattern 659 can be removed during a subsequent process step of dry-etching the first organic film 653 (see Figure 35(b)).

Thereafter, the silicon dioxide film 654 is dry-etched using the patterned second organic film 655A as a mask, thereby forming a patterned second silicon dioxide film 654A having openings for forming contact holes as shown in Figure 35(a).

Then, the patterned second organic film 655A and the first organic film 653 are dry-etched using the mask pattern 658 and the patterned silicon dioxide film 654A as respective masks, thereby forming a patterned second organic film 655B having wiring grooves 660 and a patterned first organic film 653A having contact holes 661 as shown in Figure 35(b).

Subsequently, the patterned silicon dioxide film 654A and the silicon nitride film 652 are dry-etched using the mask pattern 658 and the patterned first organic film 653A as respective masks, thereby forming a patterned silicon dioxide film 654B having wiring grooves (see Figure 35(c)) and a pat-

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terned silicon nitride film 652A having the contact holes (see Figure 35(c)), and exposing the first metal interconnects 651 within the contact holes 661. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 5 50 nm thick, for example, on the wall faces of the contact holes 661 and the wiring grooves 660 as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 661 and the wiring grooves 660. In this embodiment, the 10 metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions 15 of the adhesion layer, the metal film and the mask pattern 658, which are deposited on the patterned second organic film 655B, are removed by a CMP technique, for example. As a result, second metal interconnects 662 and contacts 663, connecting the first and second metal interconnects 651 and 662 20 together, are formed as shown in Figure 35(c).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 662 through the same process steps as those described above.

25 In this modified example of the sixth embodiment, the



**WHAT IS CLAIMED IS:**

1. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a thin film over the third insulating film;

e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

g) forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;

h) dry-etching the third insulating film under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low

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rate, thereby patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left;

i) dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;

j) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and

k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

2. The method of Claim 1, further comprising the step of forming a metal adhesion layer over part of the third insulat-



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first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a thin film over the third insulating film;

e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

g) forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;

h) dry-etching the third insulating film using the first and second resist patterns as a mask under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes;

i) dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films and

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the first and second resist patterns are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;

j) removing the first and second resist patterns;

k) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and

l) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

9. The method of Claim 8, wherein the third insulating film is a low-dielectric-constant SOG film with a siloxane skeleton.

10. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the

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first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film;

e) forming a thin film over the fourth insulating film;

f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes;

j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming



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contact holes;

k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes;

l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and

m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

11. The method of Claim 10, wherein at least one of the first and third insulating films is mainly composed of an organic component.

12. The method of Claim 10, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

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i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes;

j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and

k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

14. The method of Claim 13, wherein at least one of the first and third insulating films is mainly composed of an organic component.

15. The method of Claim 13, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

**ABSTRACT OF THE DISCLOSURE**

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects.

5 Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are

10 etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film is masked with the third insulating film and dry-etched such that the

15 second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films are masked with the mask pattern and the second insulating film, respectively, and dry-etched such that the first and third insulating

20 films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal

25 interconnects and contacts are formed.

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Fig. 1(a)

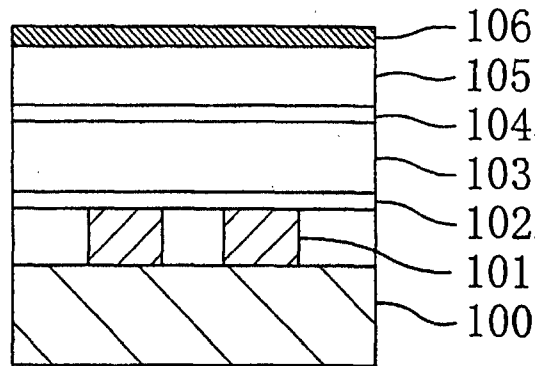


Fig. 1(b)

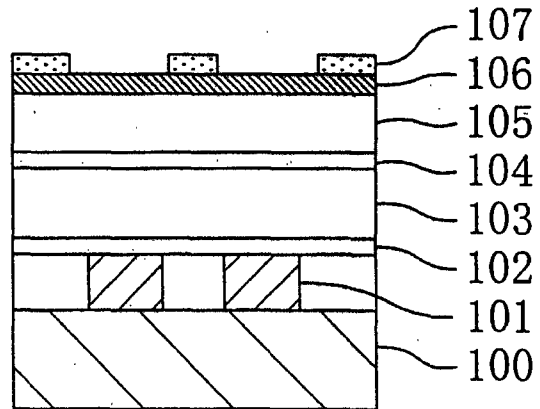
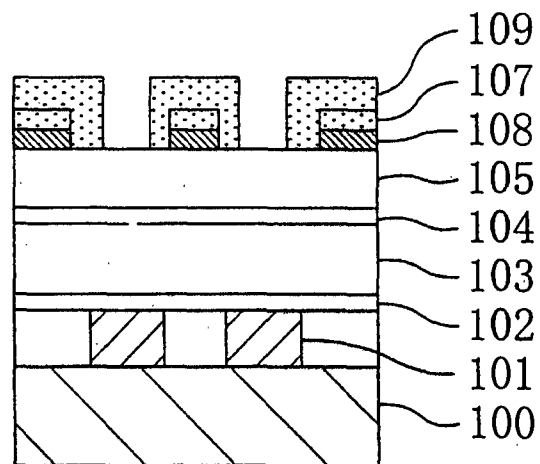


Fig. 1(c)



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Fig. 2(a)

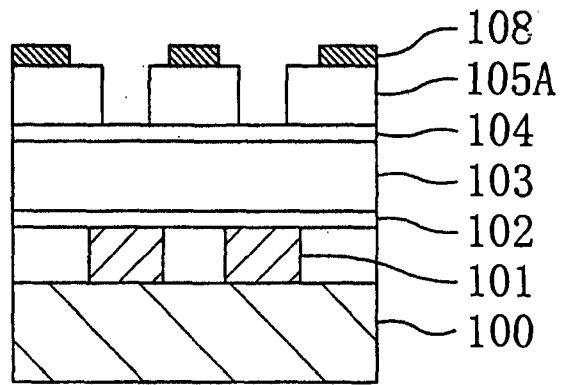


Fig. 2(b)

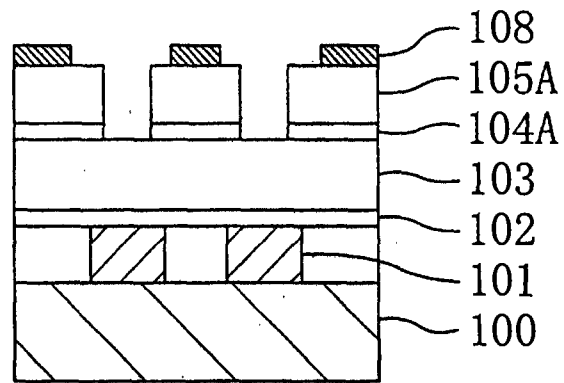
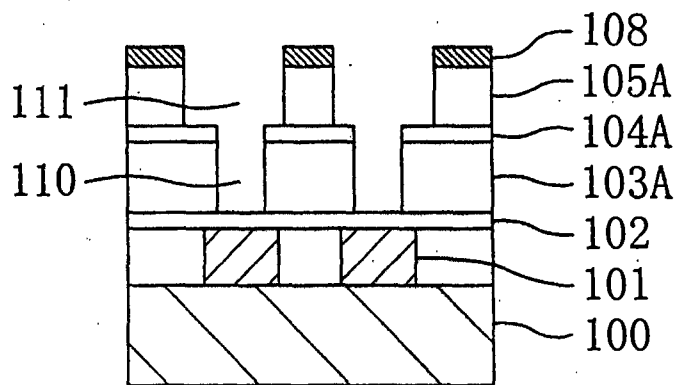


Fig. 2(c)



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Fig. 3(a)

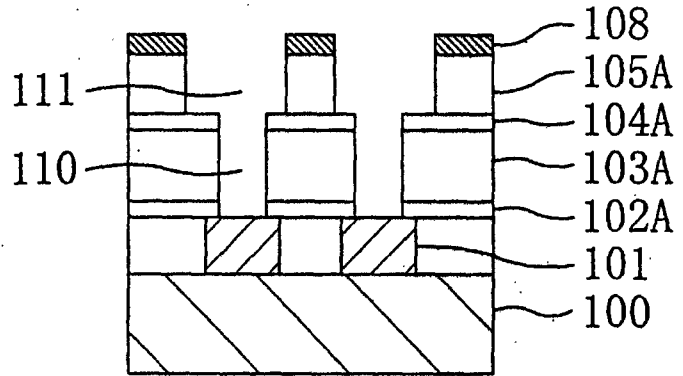


Fig. 3(b)

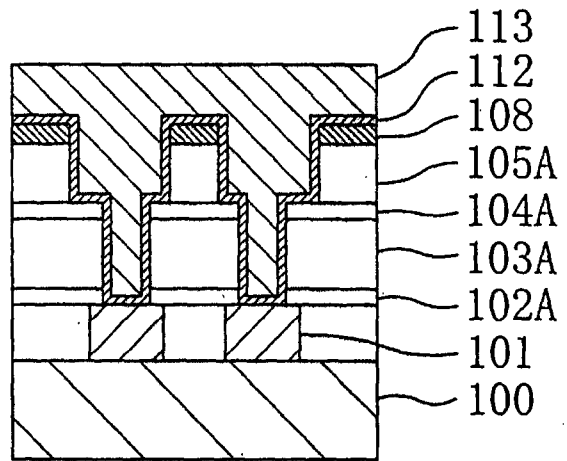
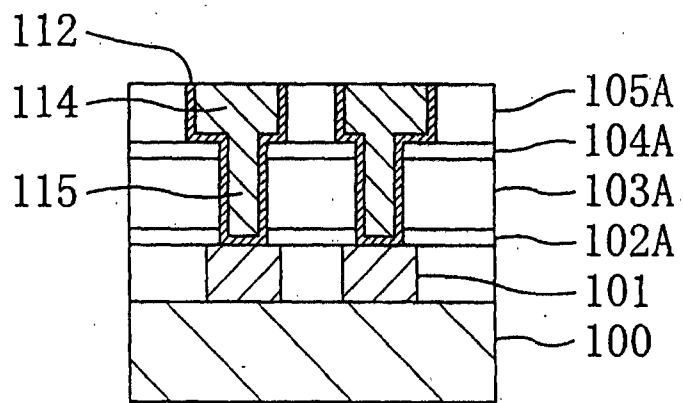


Fig. 3(c)



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Fig. 4(a)

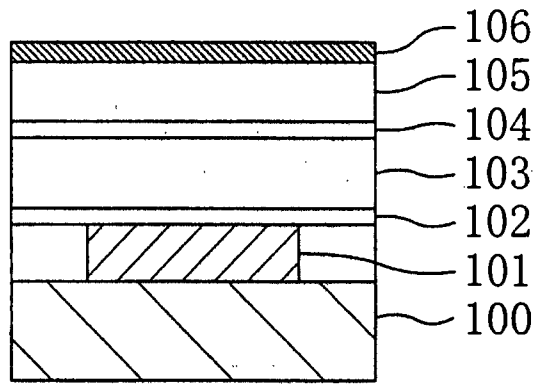


Fig. 4(b)

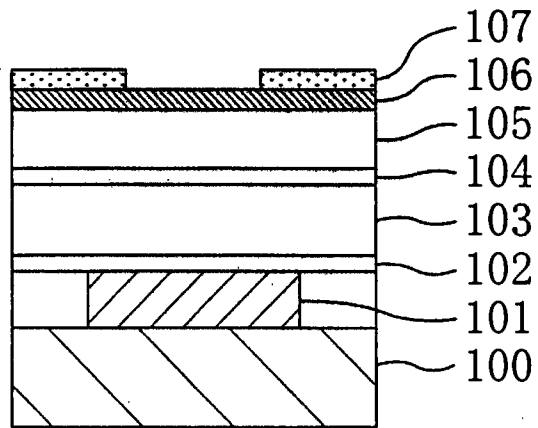
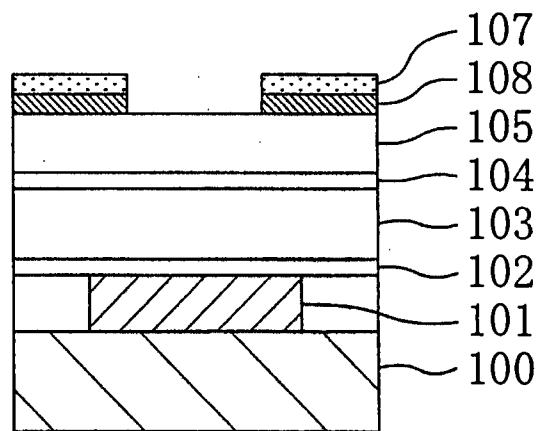


Fig. 4(c)





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Fig. 5(a)

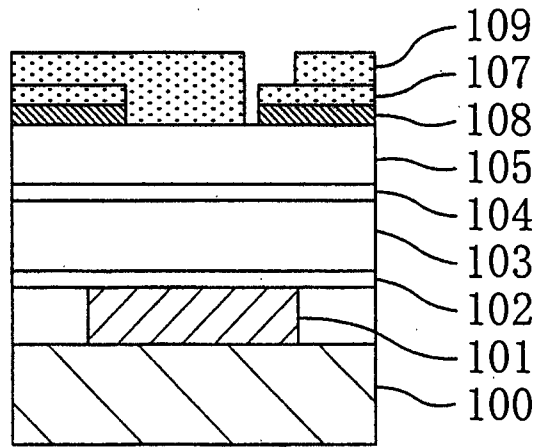


Fig. 5(b)

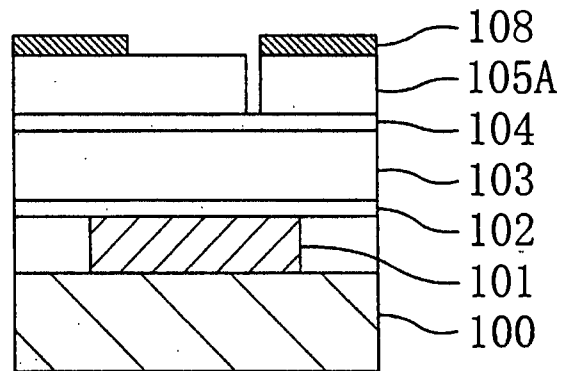
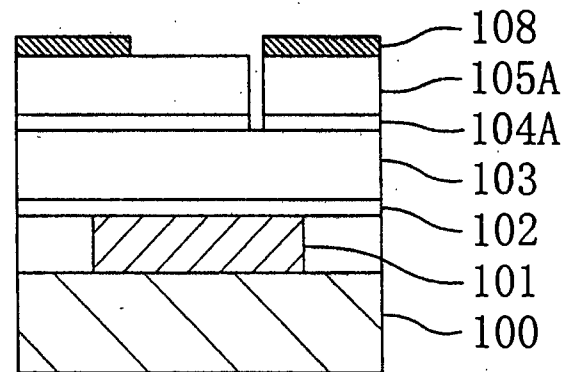


Fig. 5(c)



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Fig. 6(a)

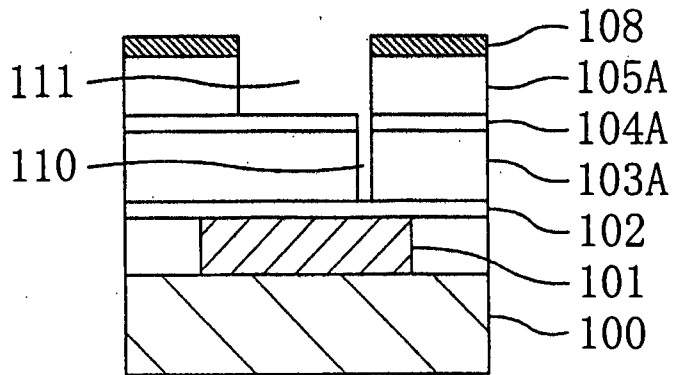


Fig. 6(b)

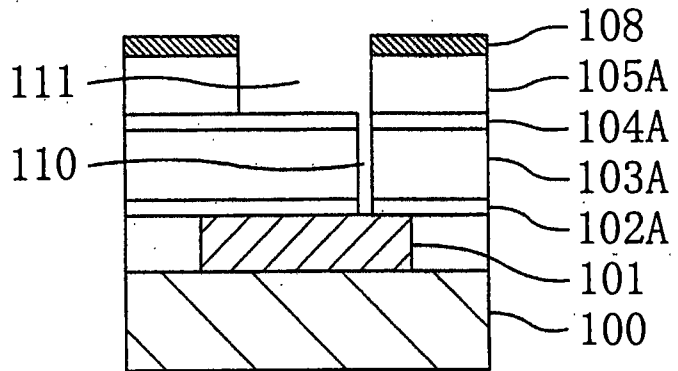


Fig. 6(c)

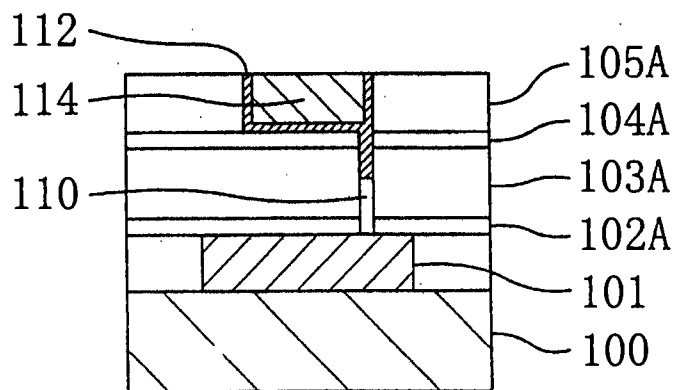


Fig. 7(a)

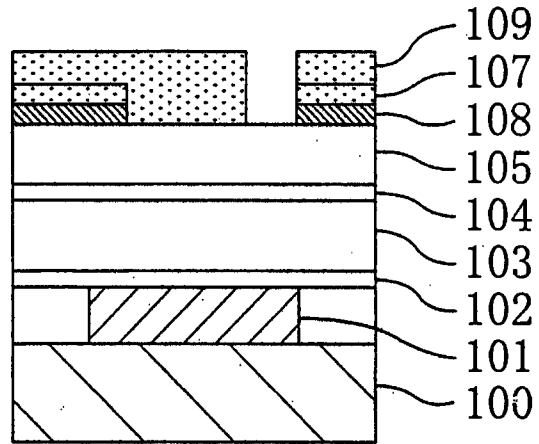


Fig. 7(b)

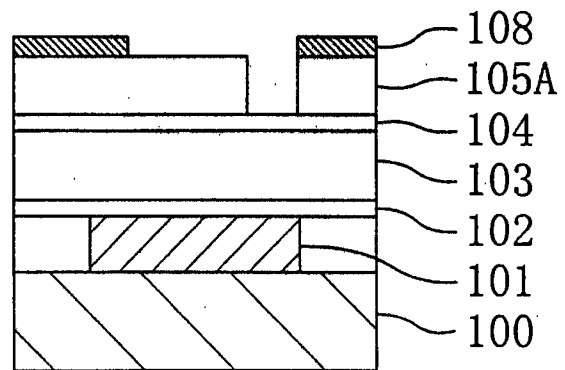
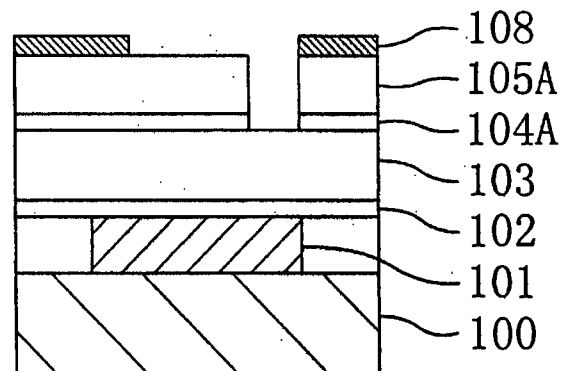


Fig. 7(c)



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Fig. 8(a)

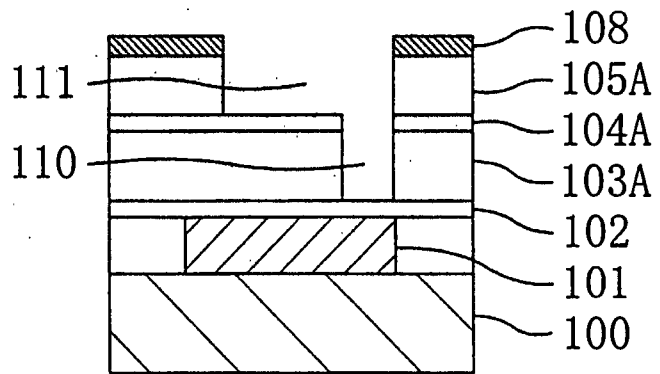


Fig. 8(b)

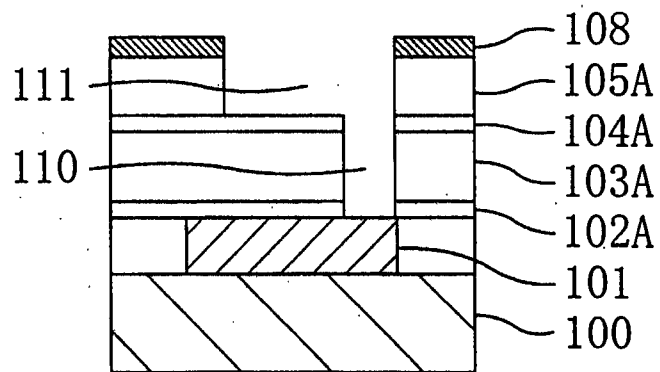
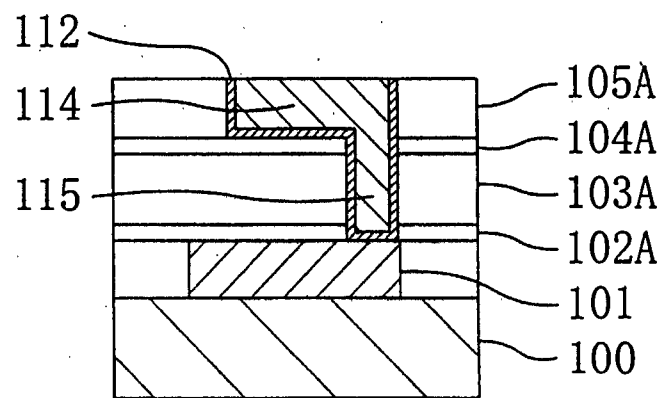


Fig. 8(c)



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Fig. 9(a)

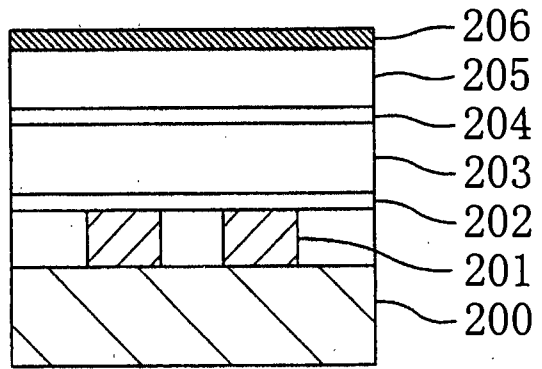


Fig. 9(b)

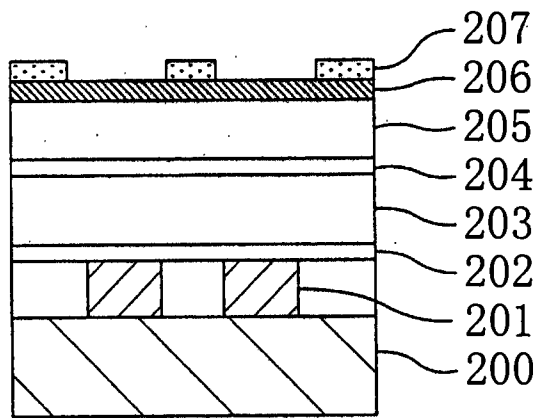
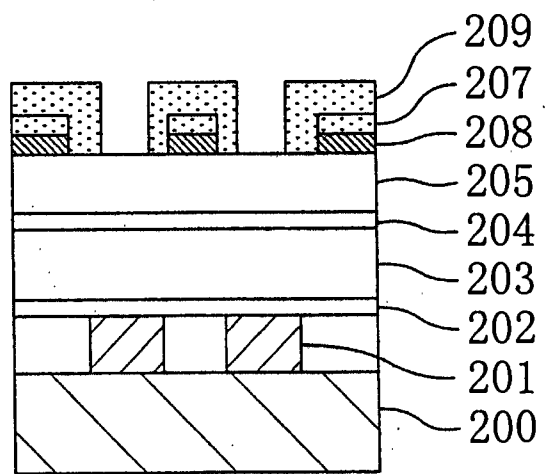


Fig. 9(c)



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Fig. 10(a)

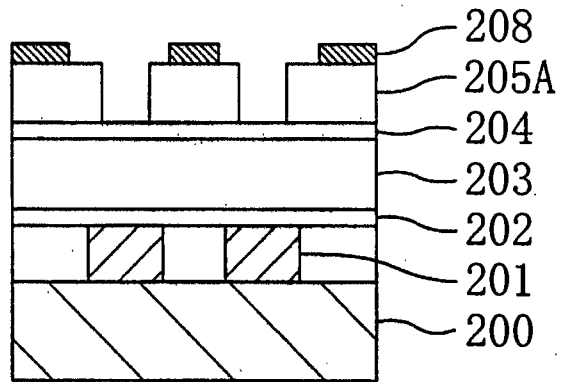


Fig. 10(b)

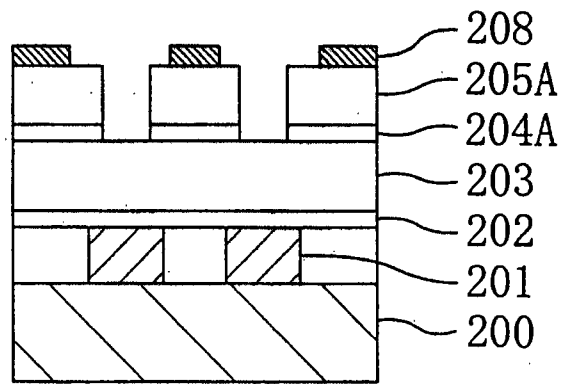
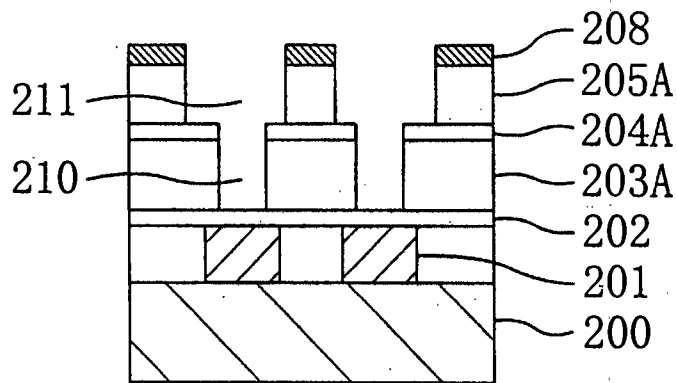


Fig. 10(c)



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Fig. 11(a)

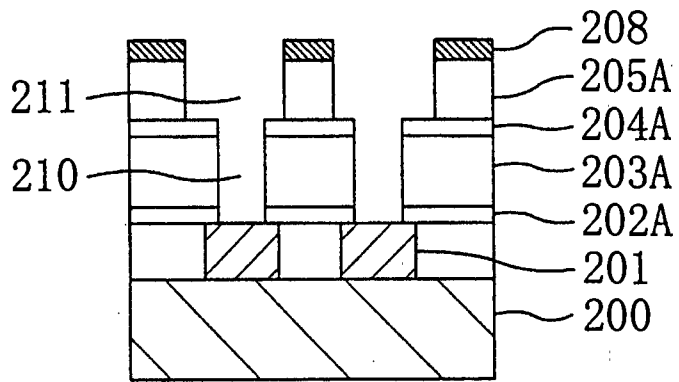


Fig. 11(b)

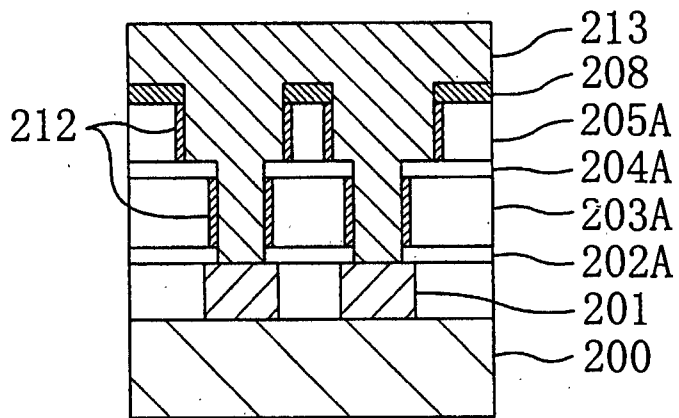
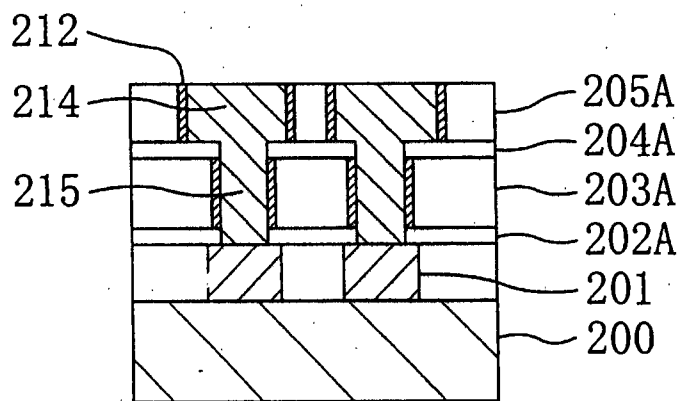


Fig. 11(c)



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Fig. 12(a)

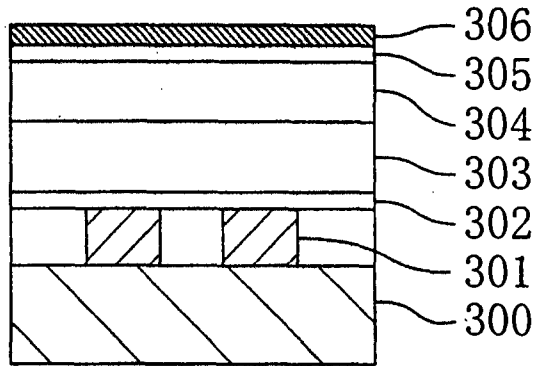


Fig. 12(b)

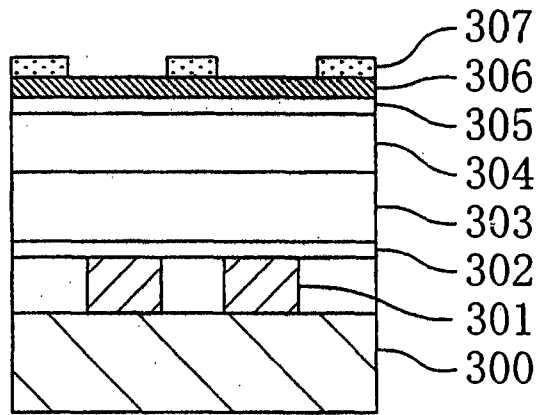


Fig. 12(c)

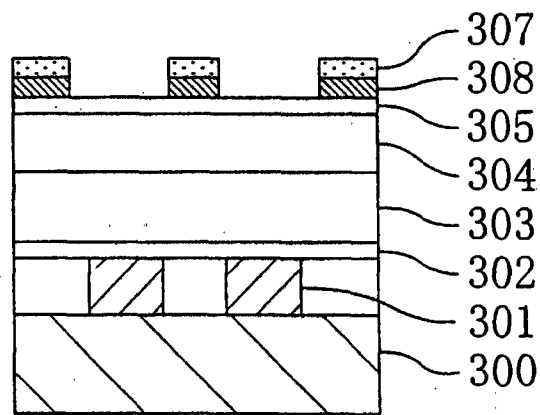




Fig. 13(a)

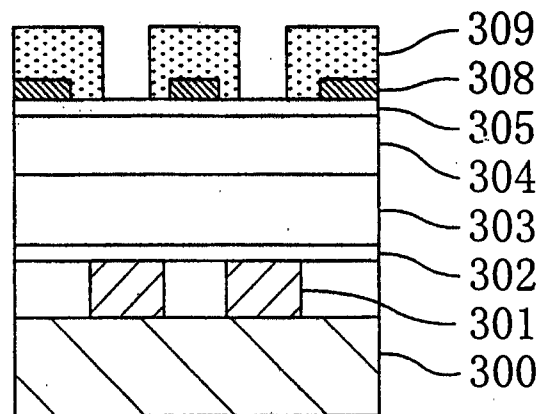


Fig. 13(b)

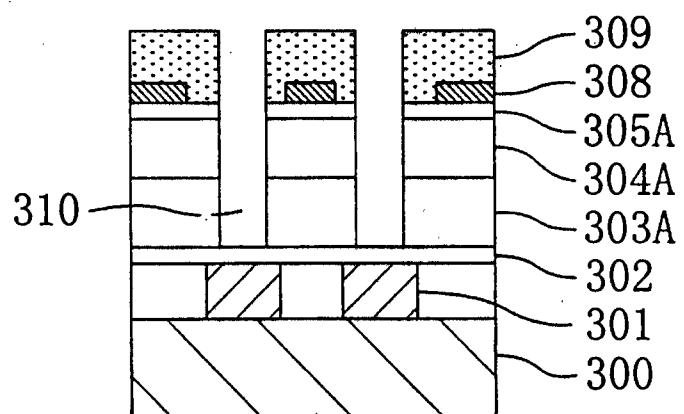
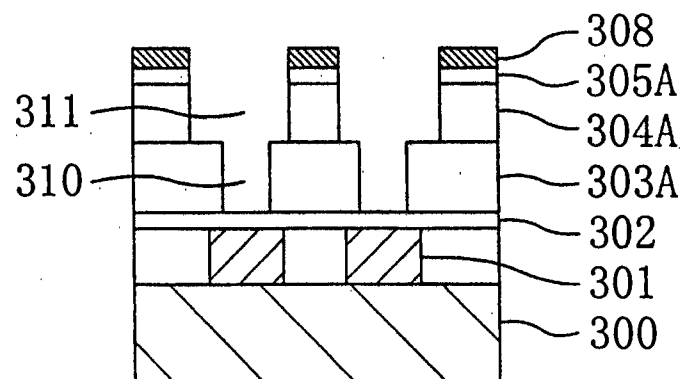


Fig. 13(c)



66220-111250

66220-1114260

Fig. 14(a)

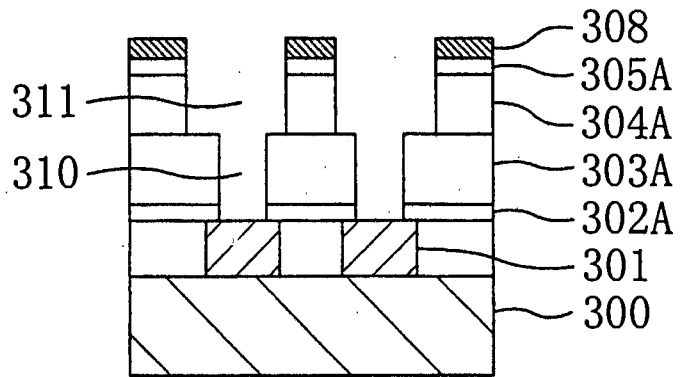


Fig. 14(b)

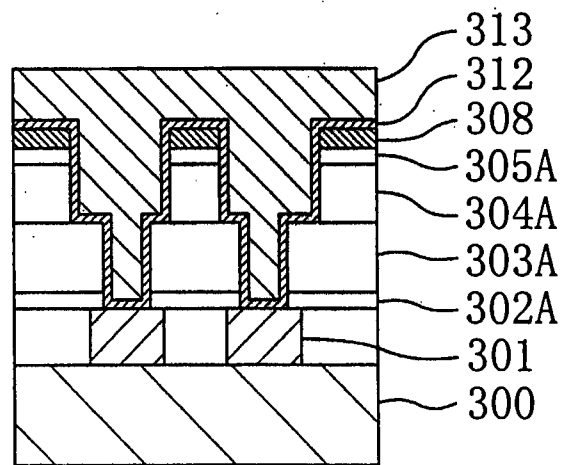
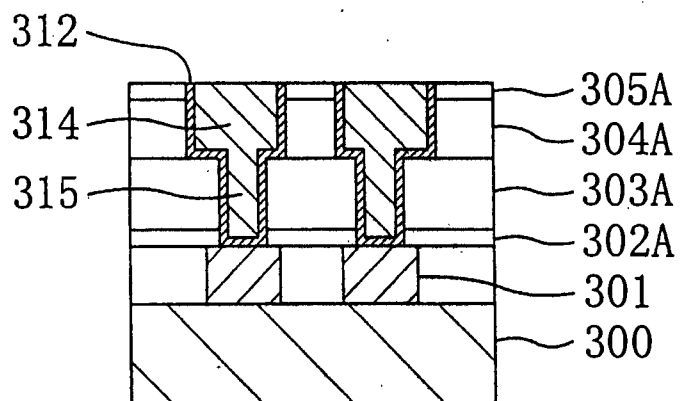


Fig. 14(c)



66220" 1114.260

Fig. 15(a)

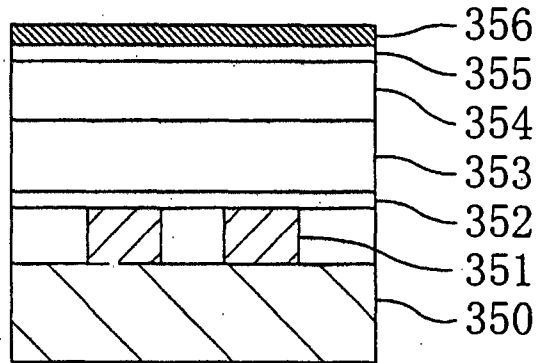


Fig. 15(b)

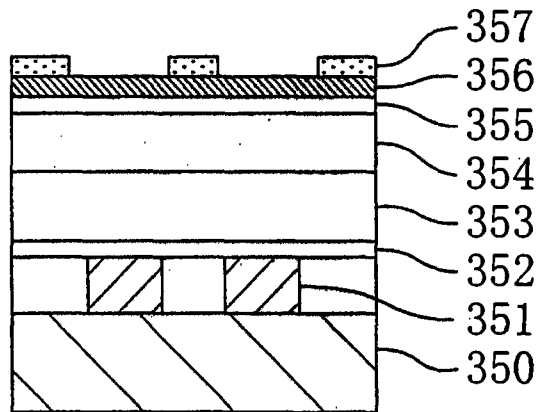
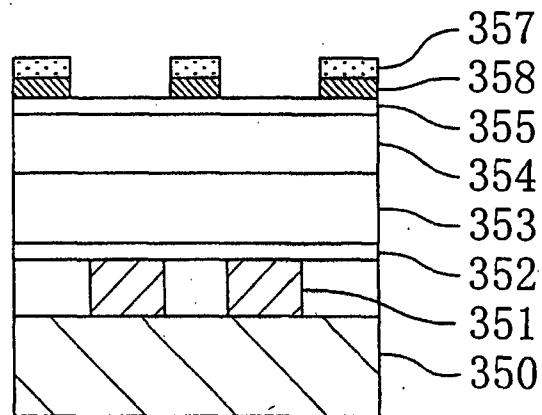


Fig. 15(c)



552260" 474250

Fig. 16 (a)

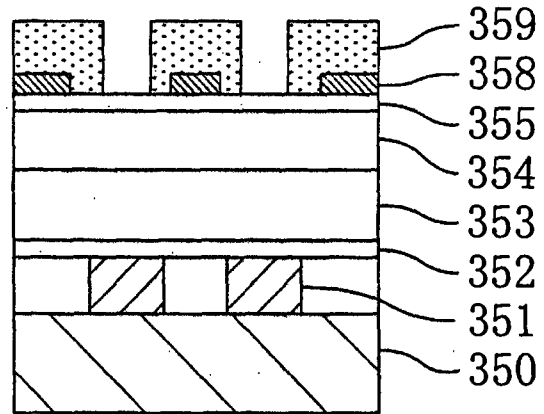


Fig. 16 (b)

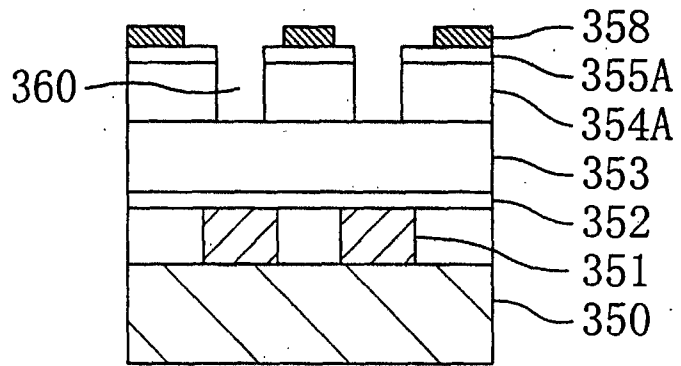


Fig. 16 (c)

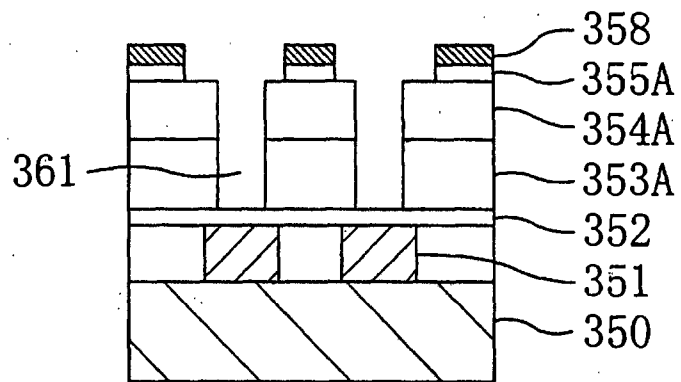


Fig. 16 (d)

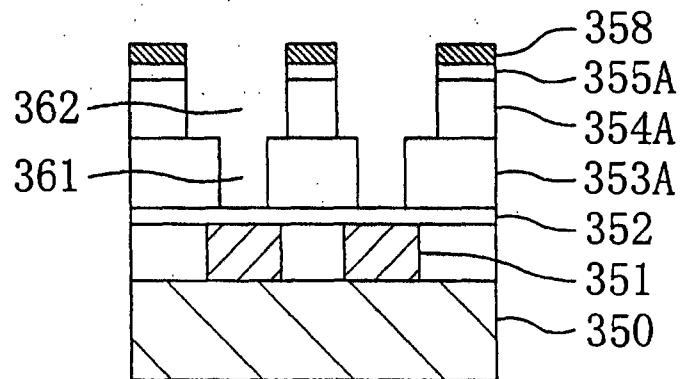


Fig. 17(a)

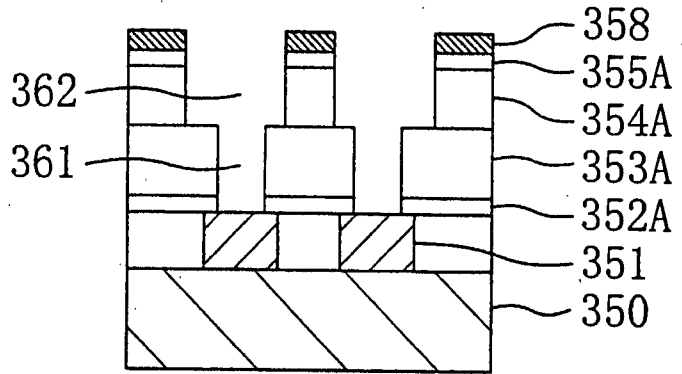


Fig. 17(b)

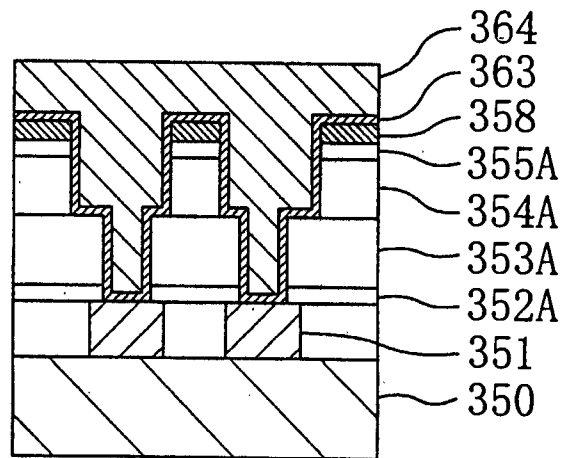
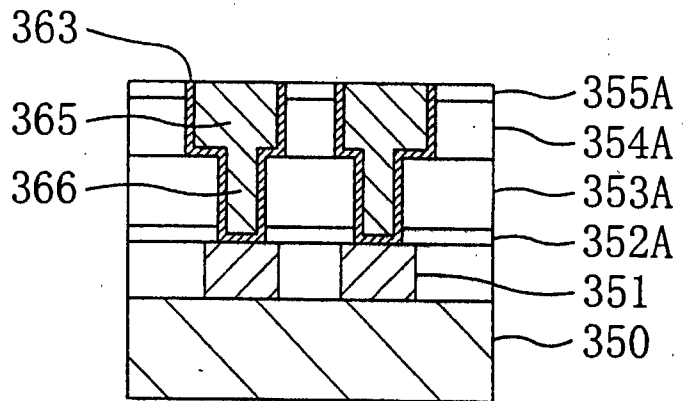


Fig. 17(c)



56220" 4744260

Fig. 18(a)

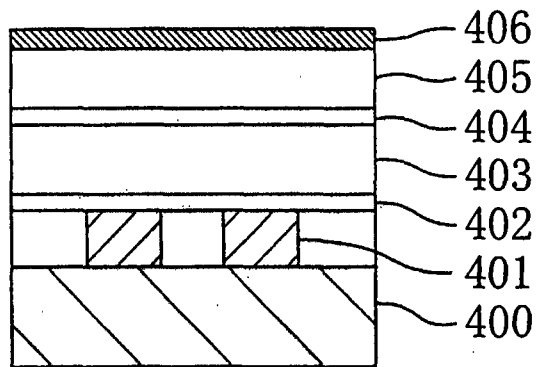


Fig. 18(b)

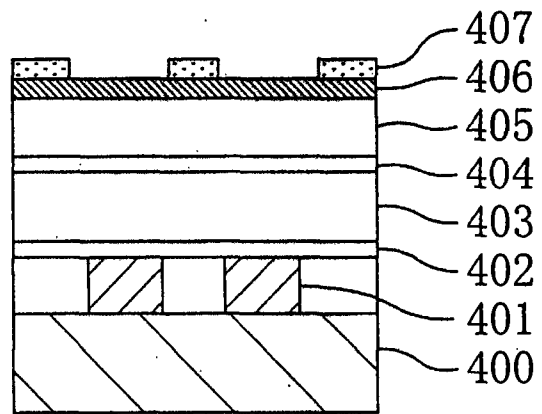
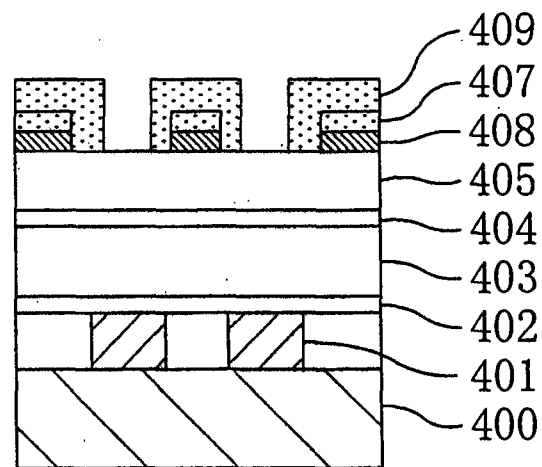


Fig. 18(c)



SEE "REF 260"

66220-474260

Fig. 19(a)

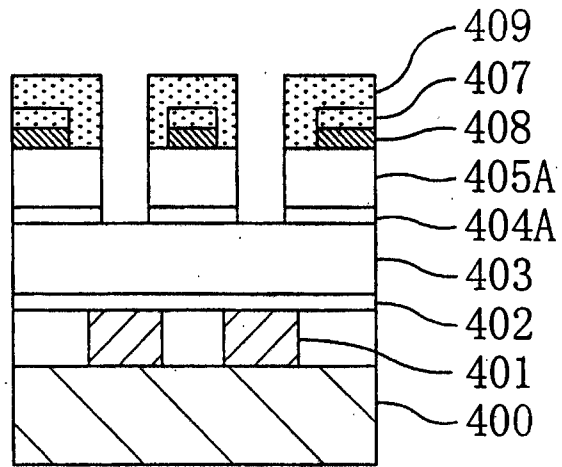


Fig. 19(b)

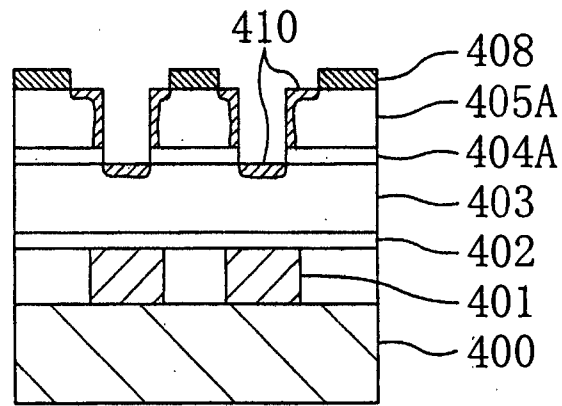
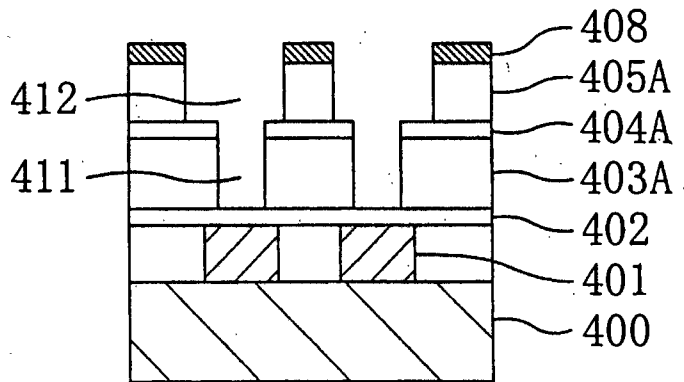


Fig. 19(c)



66260-1114260

Fig. 20(a)

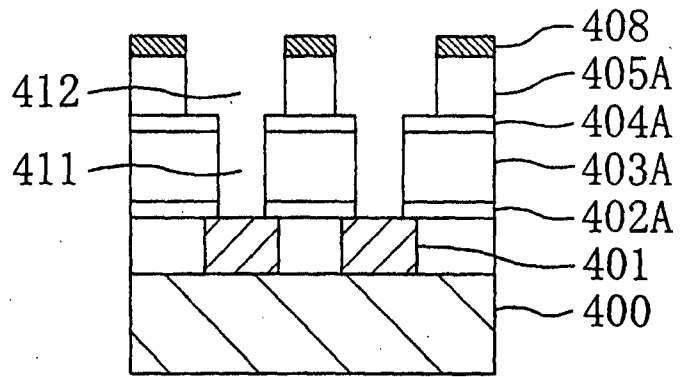


Fig. 20(b)

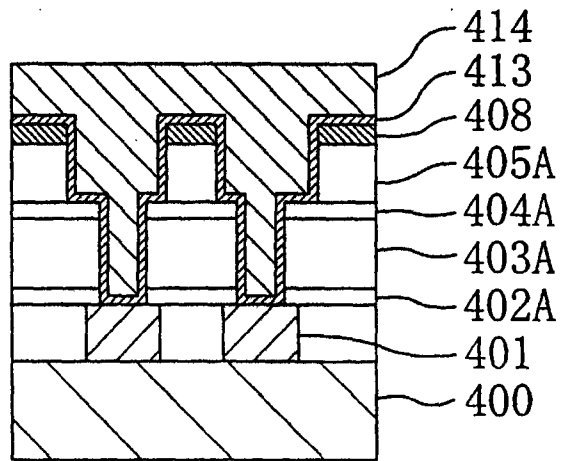


Fig. 20(c)

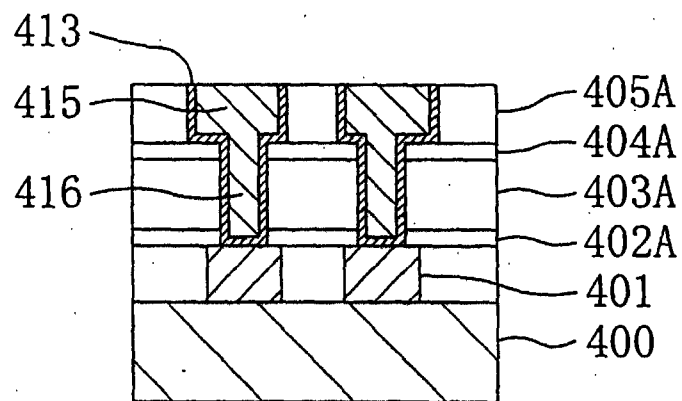




Fig. 21 (a)

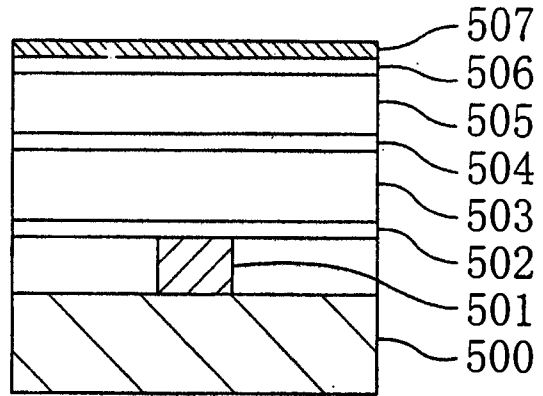


Fig. 21 (b)

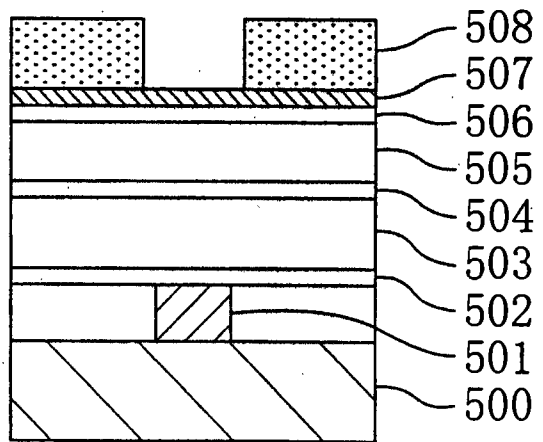
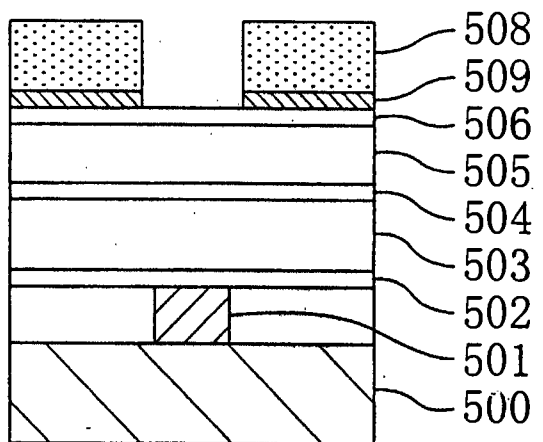


Fig. 21 (c)



65220" HT H 260

66250"4FH260

Fig. 22 (a)

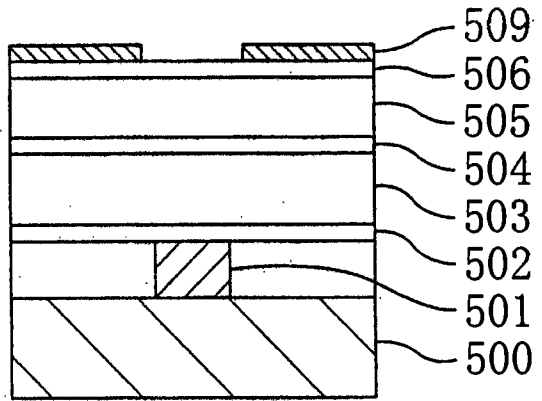


Fig. 22 (b)

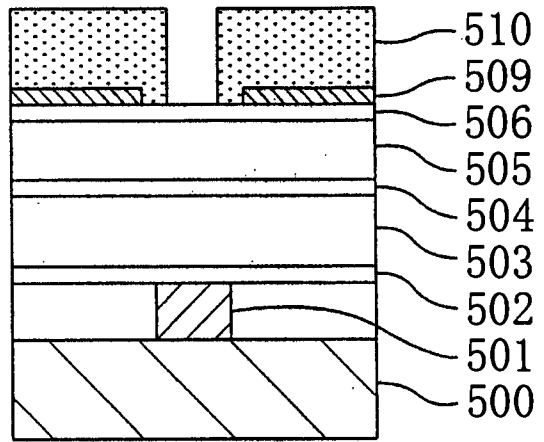
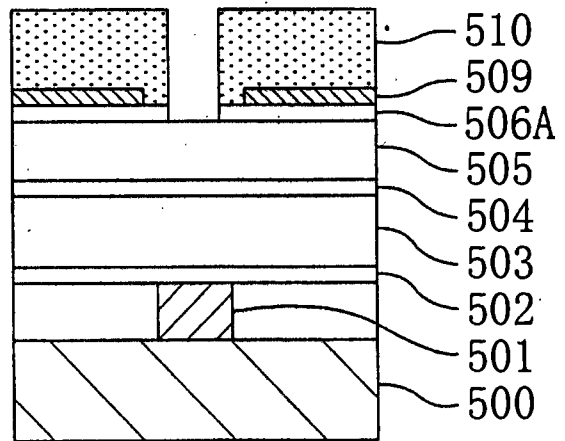


Fig. 22 (c)



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Fig. 23 (a)

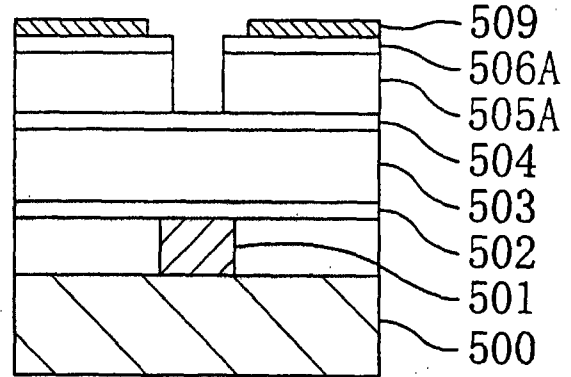


Fig. 23 (b)

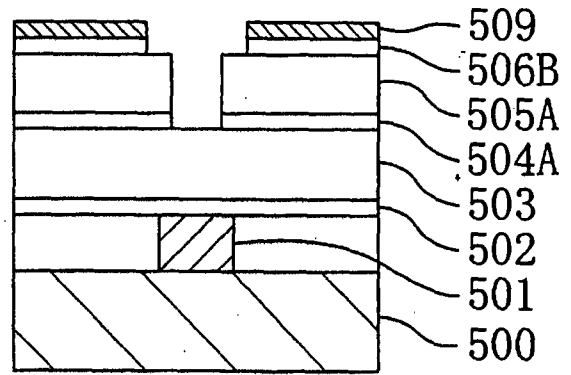


Fig. 23 (c)

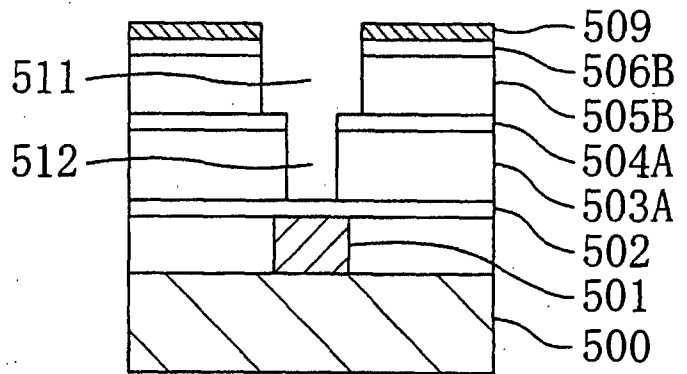
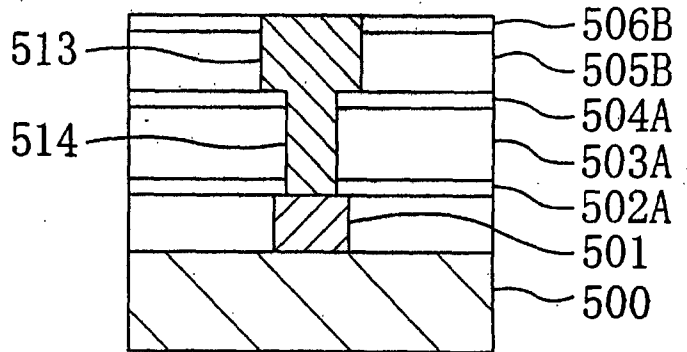


Fig. 23 (d)



66220"474260

Fig. 24(a)

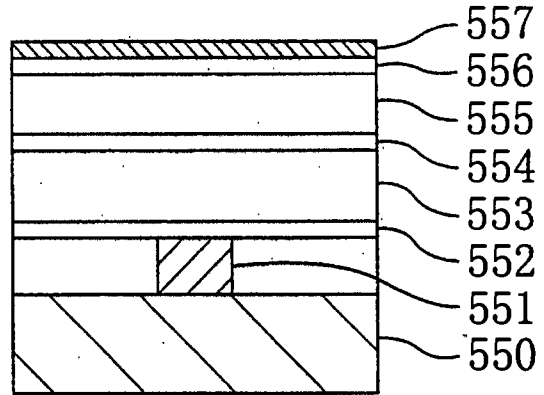


Fig. 24(b)

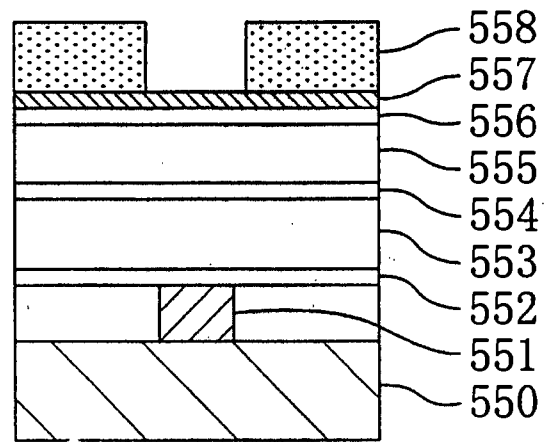


Fig. 24(c)

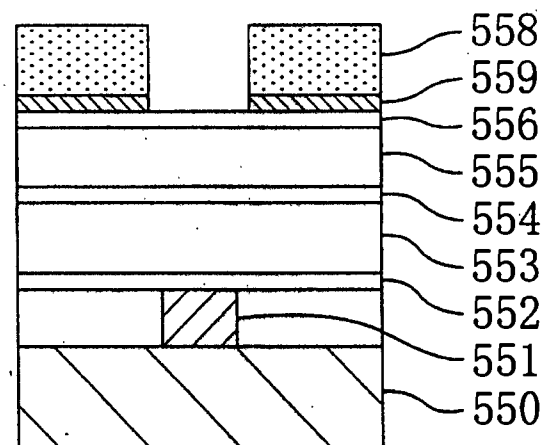


Fig. 25(a)

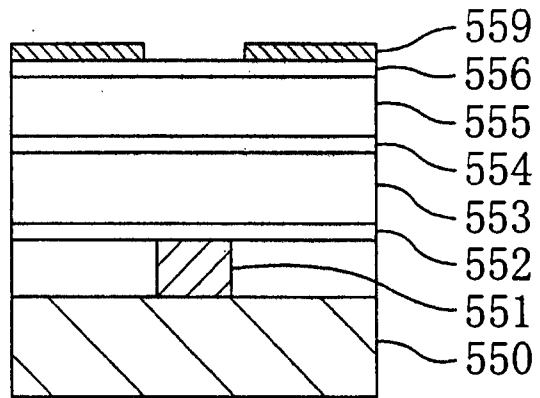


Fig. 25(b)

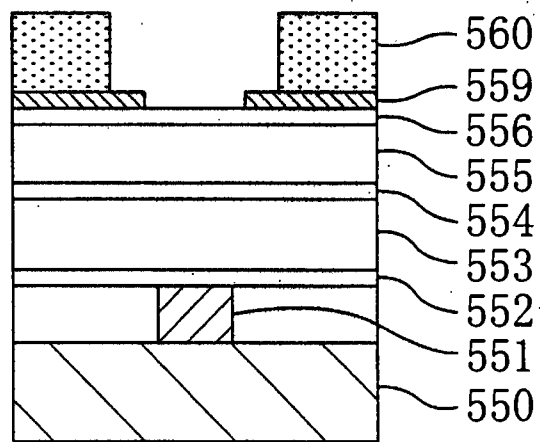
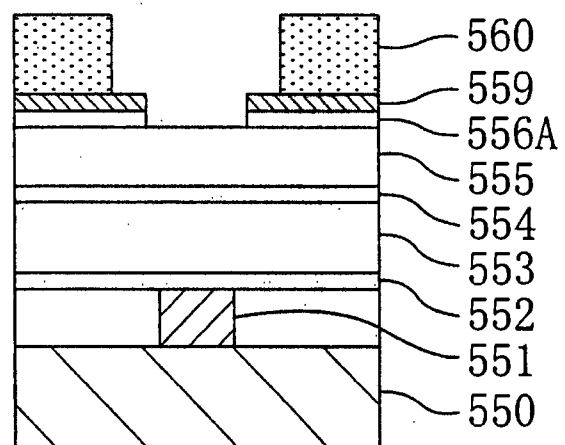


Fig. 25(c)



66260" 474250

65260-1114260

Fig. 26 (a)

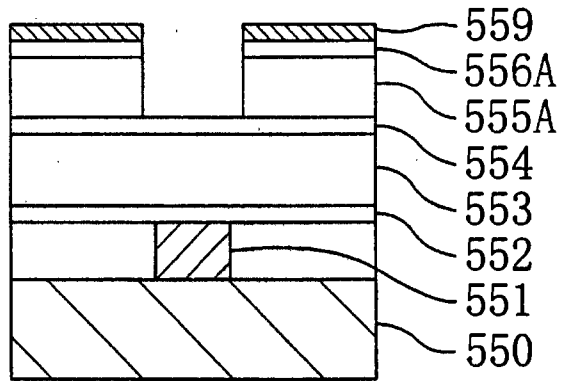


Fig. 26 (b)

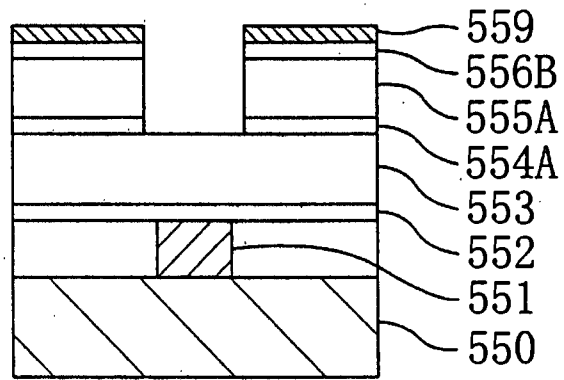


Fig. 26 (c)

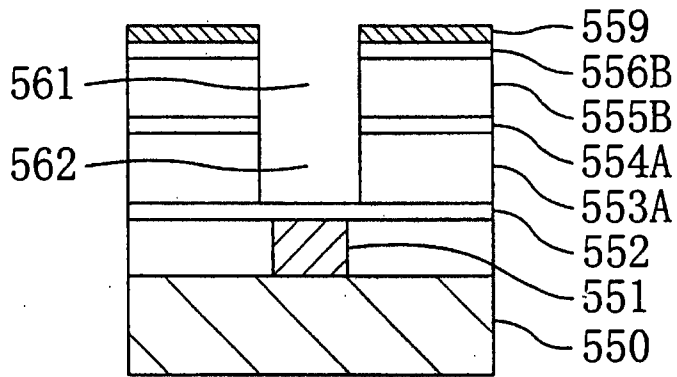
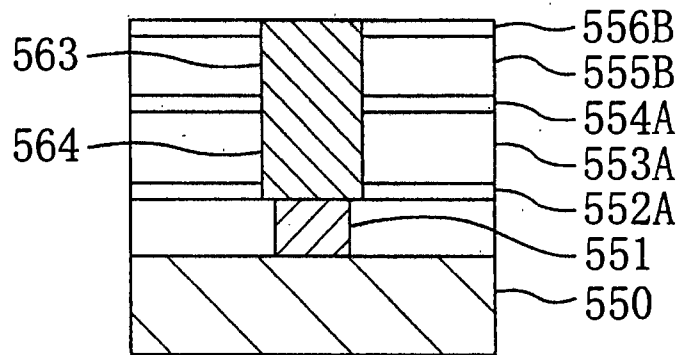


Fig. 26 (d)



66000-477260

Fig. 27(a)

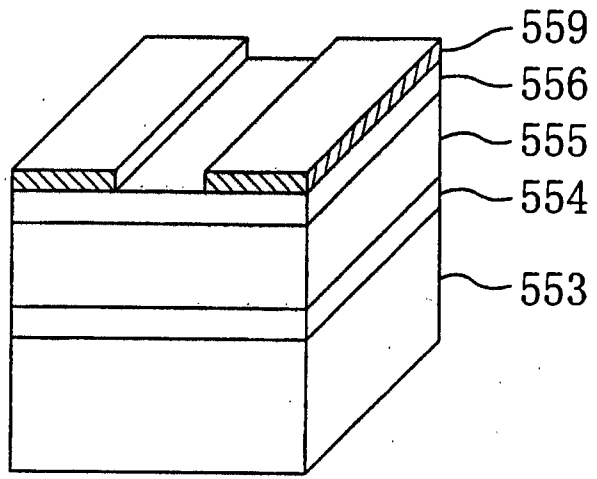
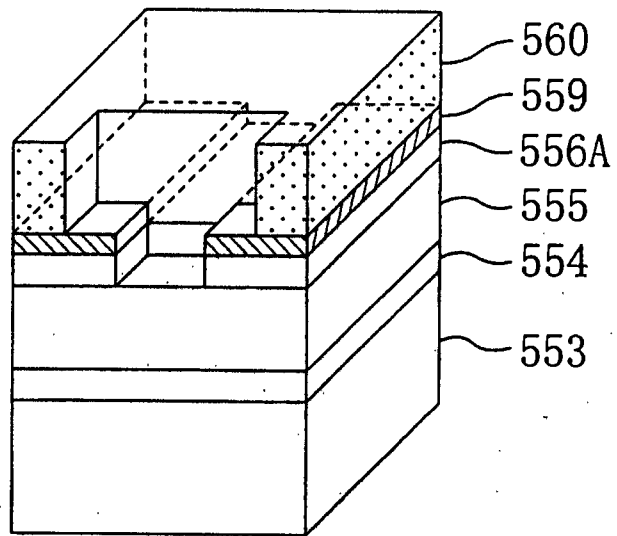


Fig. 27(b)



66260-4FFH260

Fig. 28(a)

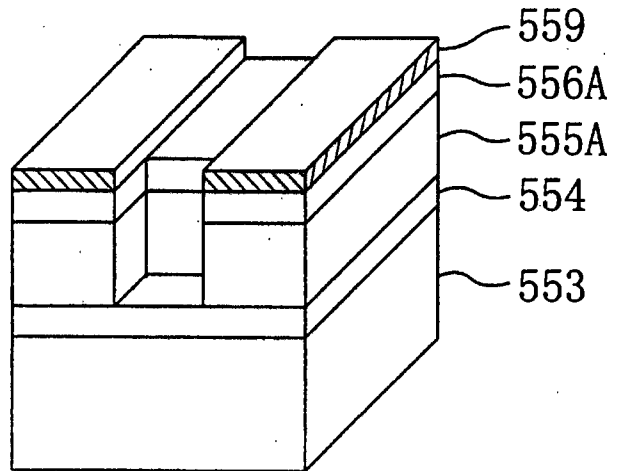


Fig. 28(b)

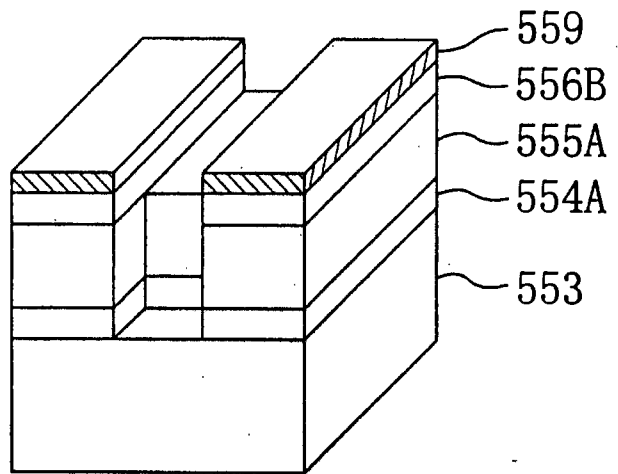




Fig. 29(a)

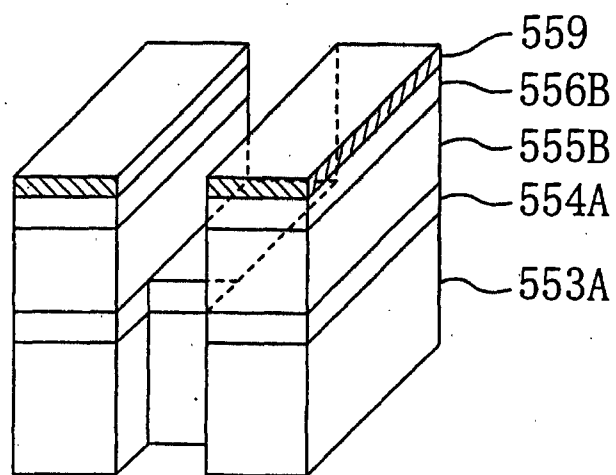
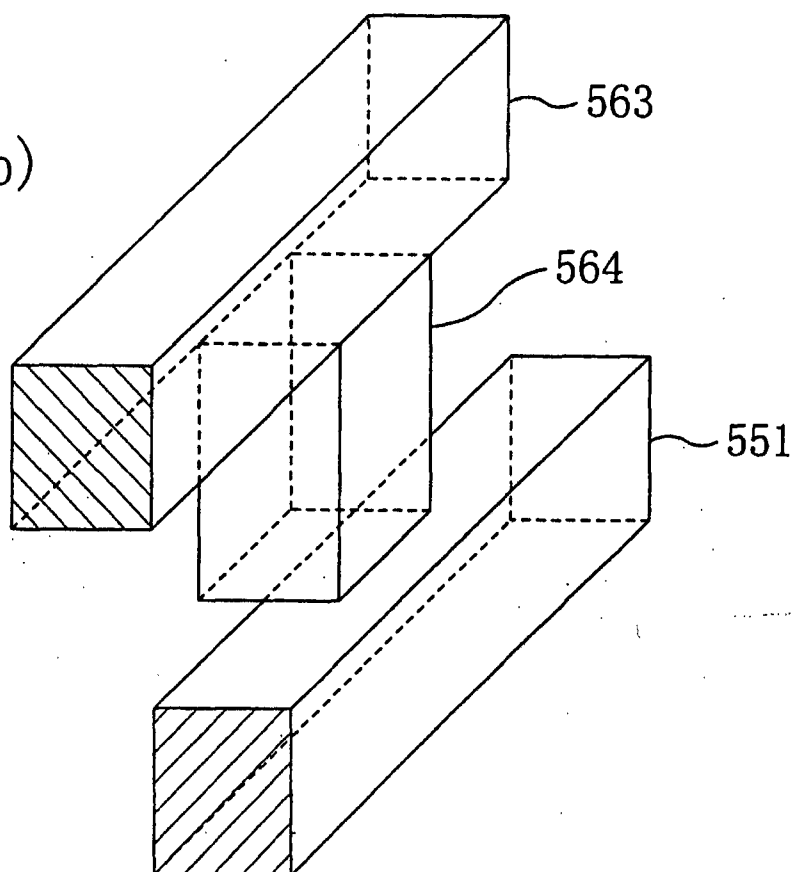


Fig. 29(b)



66220-1114260

65250" 4TFH260

Fig. 30 (a)

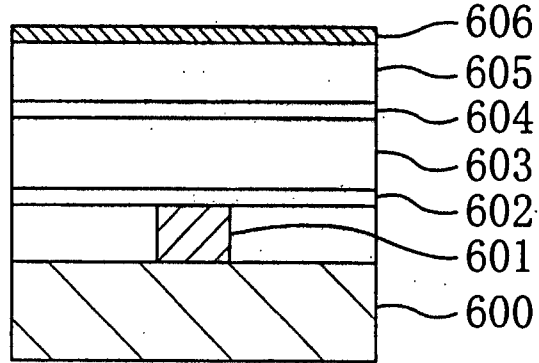


Fig. 30 (b)

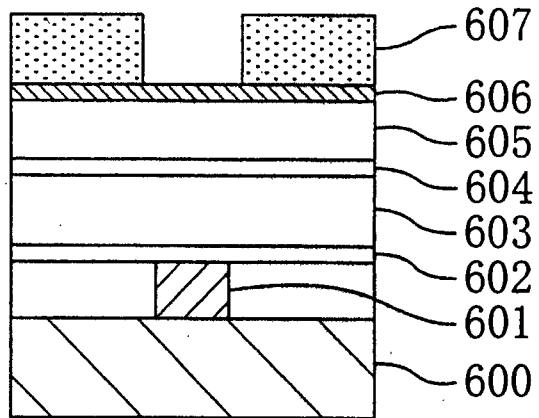
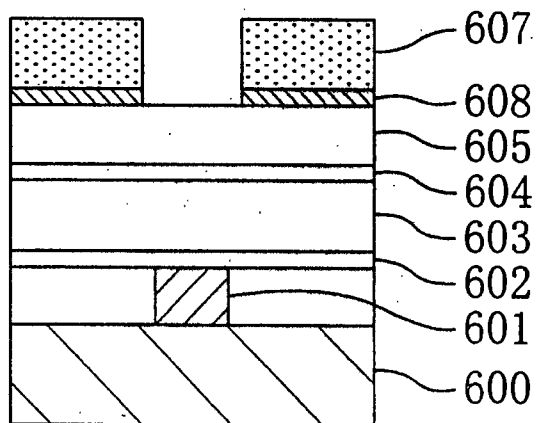


Fig. 30 (c)



66220-111250

Fig. 31 (a)

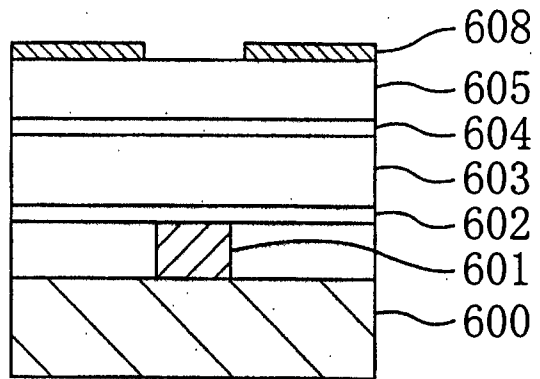


Fig. 31 (b)

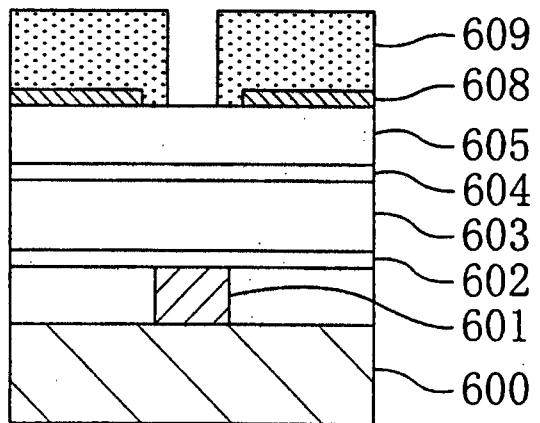


Fig. 31 (c)

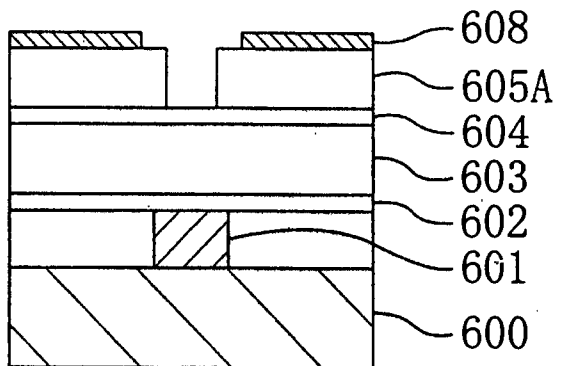


Fig. 32 (a)

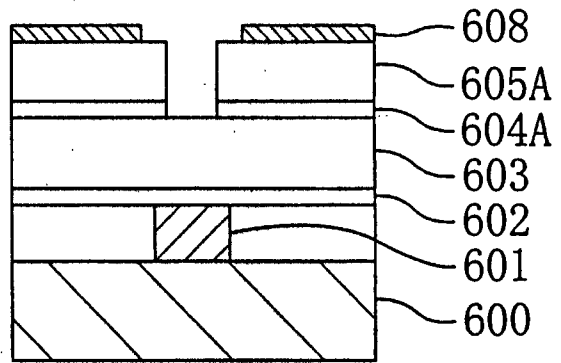


Fig. 32 (b)

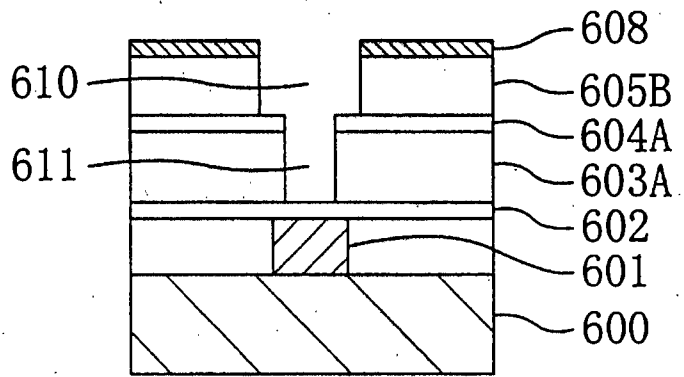
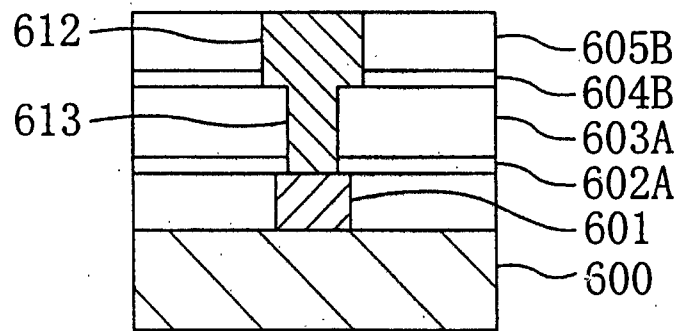


Fig. 32 (c)



66220" 4744250

66220" 417.4260

Fig. 33(a)

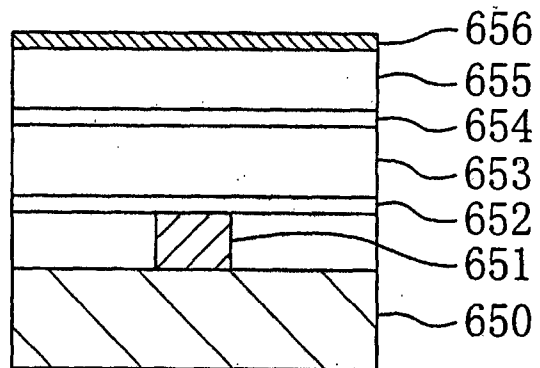


Fig. 33(b)

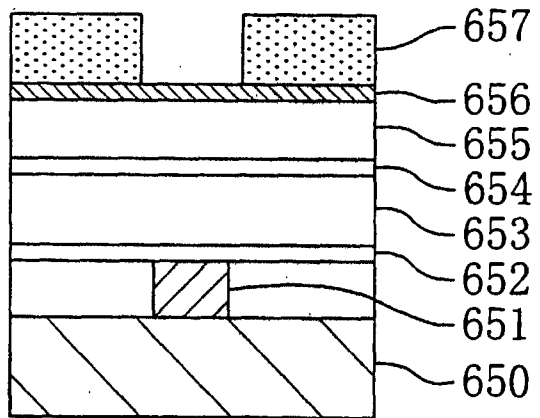


Fig. 33(c)

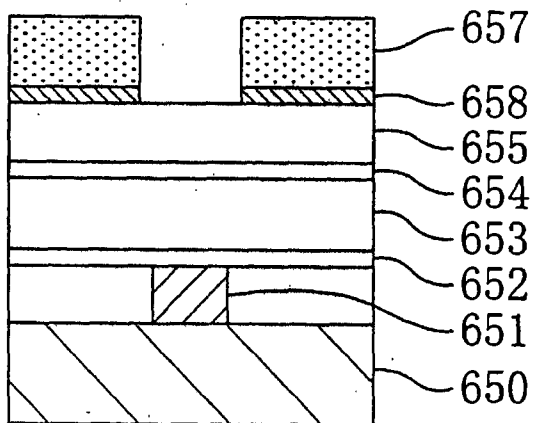


Fig. 34(a)

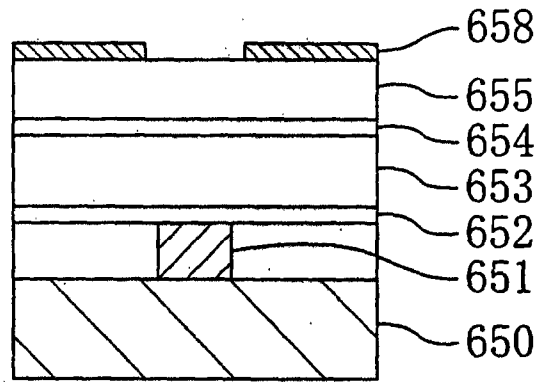


Fig. 34(b)

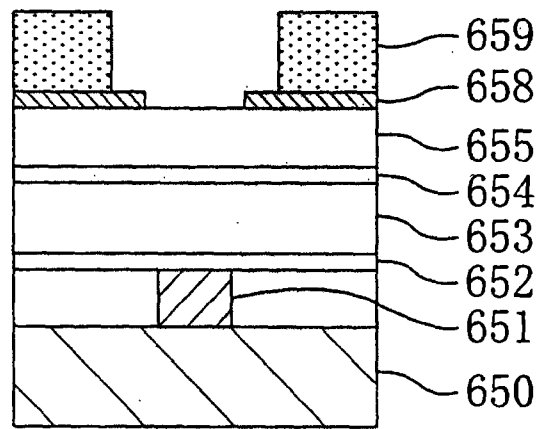
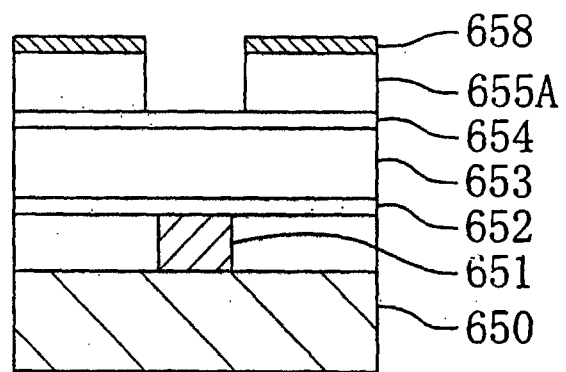


Fig. 34(c)



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Fig. 35 (a)

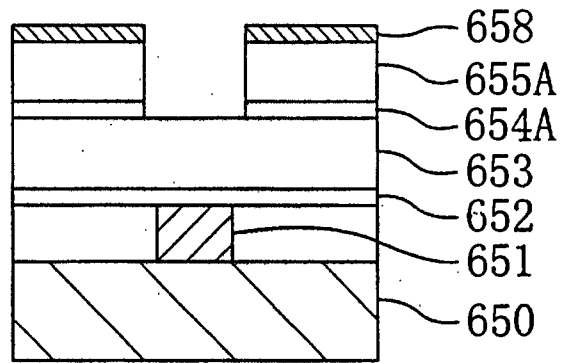


Fig. 35 (b)

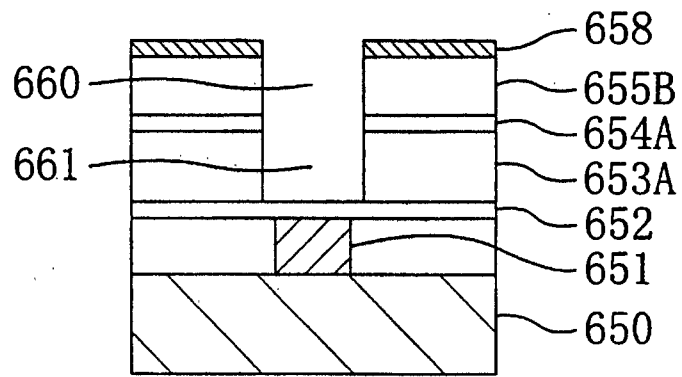


Fig. 35 (c)

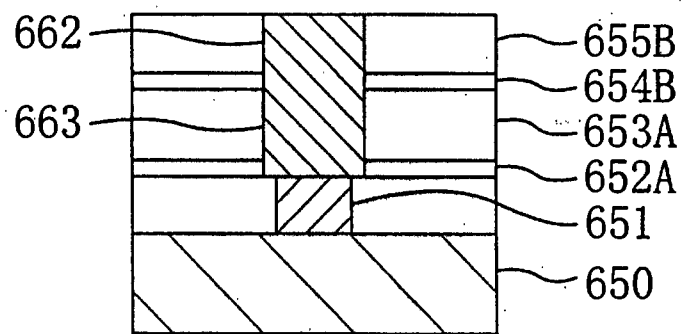
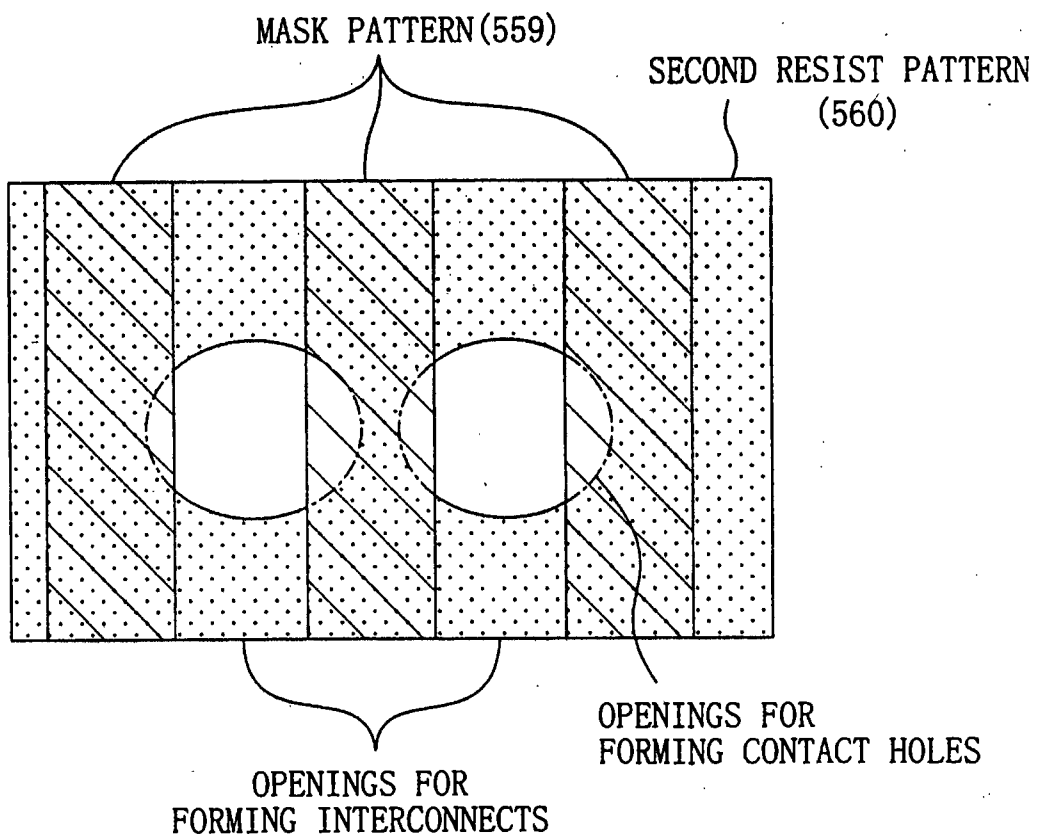


Fig. 36



66E2E0"4FFH260



Fig. 37(a)

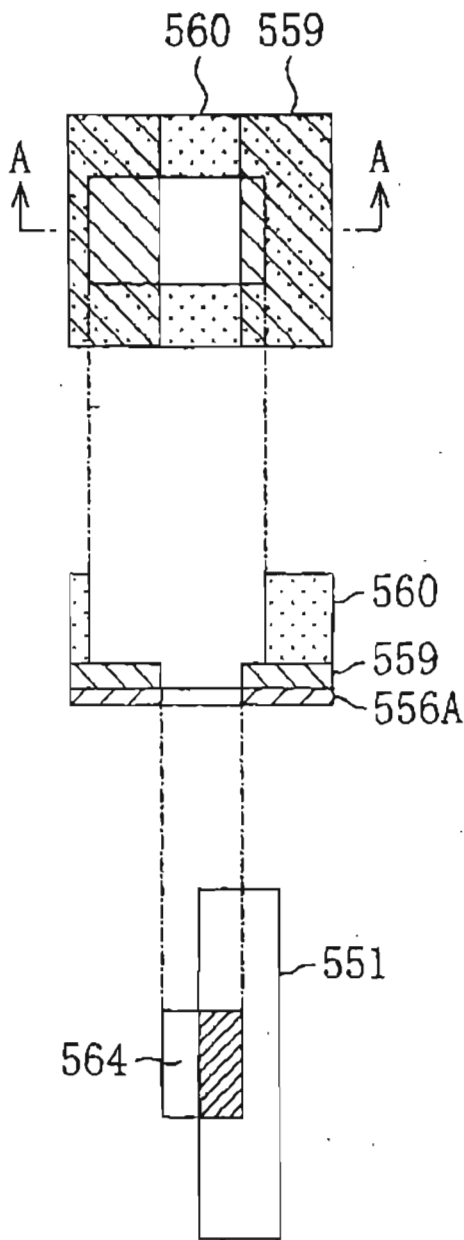
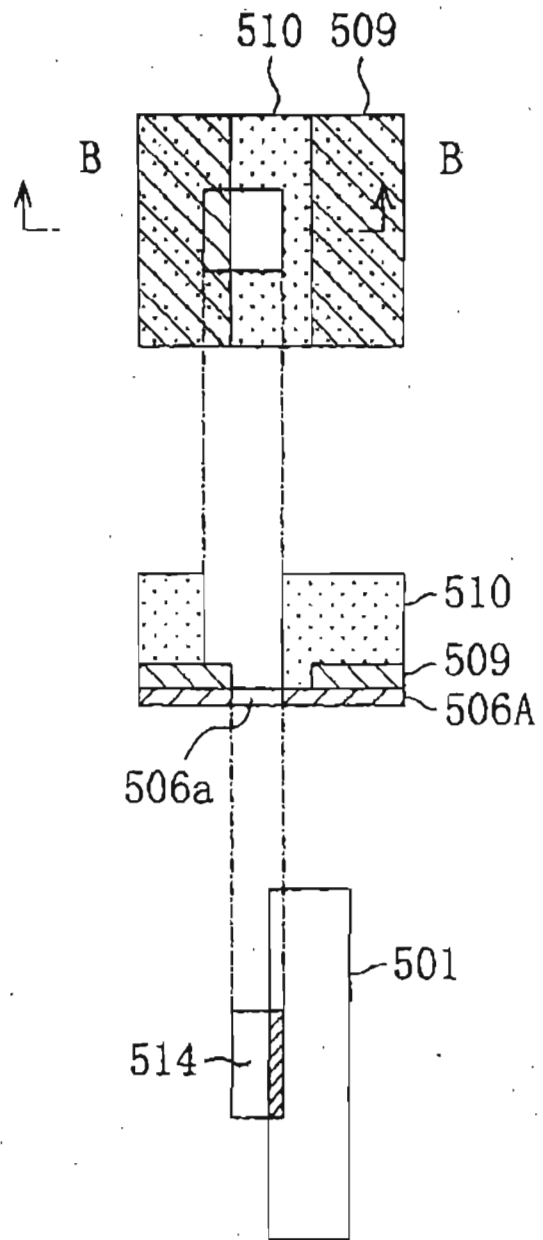


Fig. 37(b)



0927444-03399

Fig. 1(a)

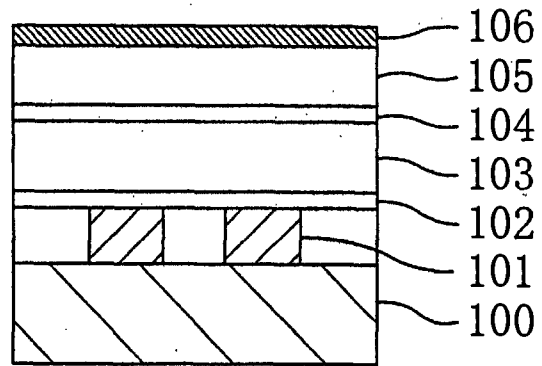


Fig. 1(b)

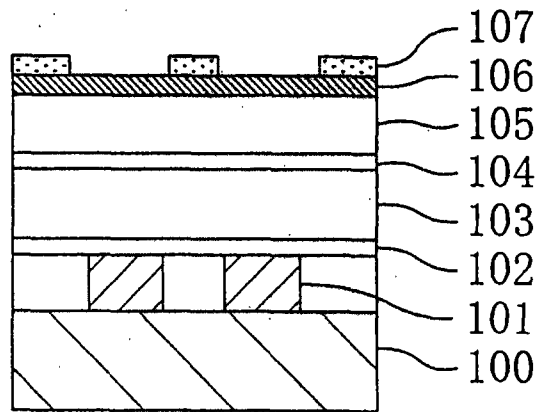
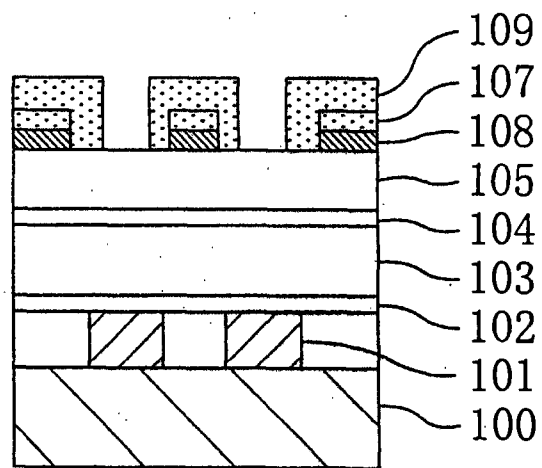


Fig. 1(c)



66220-111260

66220" 4TFH260

Fig. 2(a)

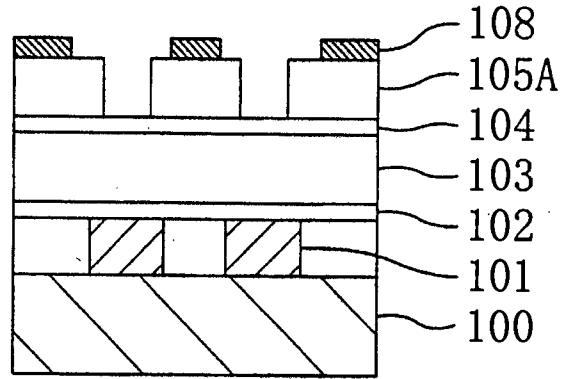


Fig. 2(b)

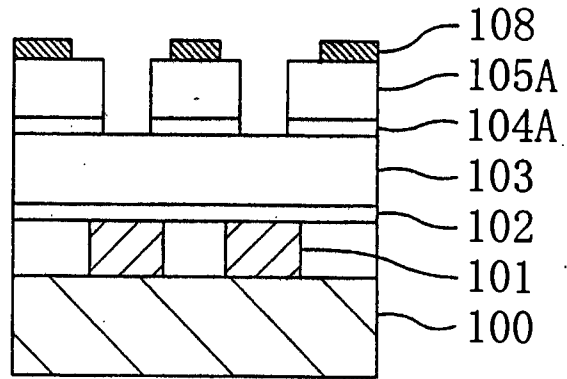
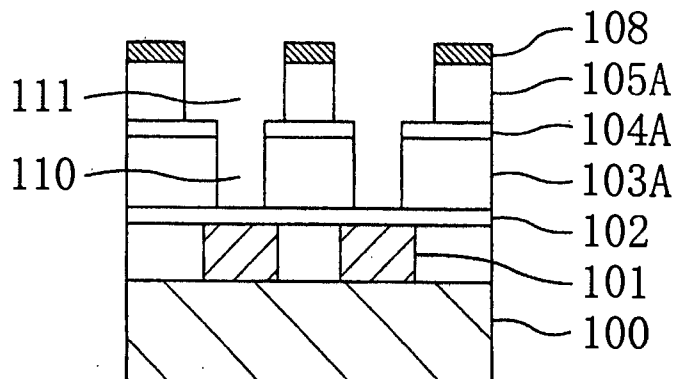


Fig. 2(c)



66250" 4774260

Fig. 3(a)

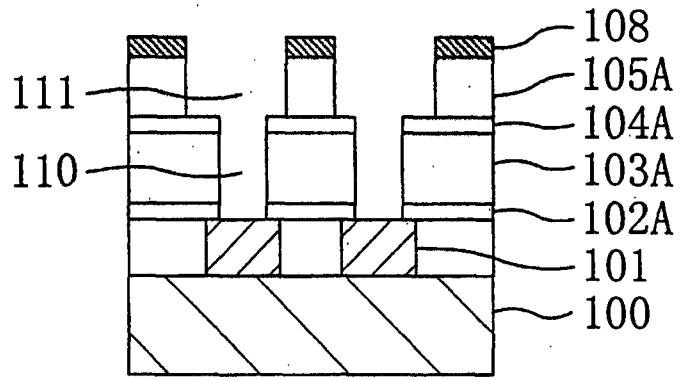


Fig. 3(b)

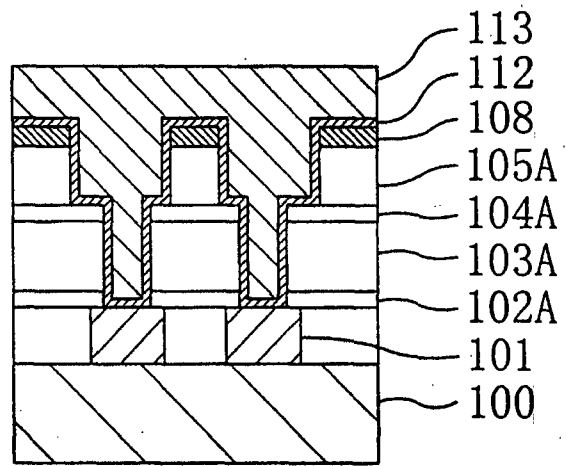
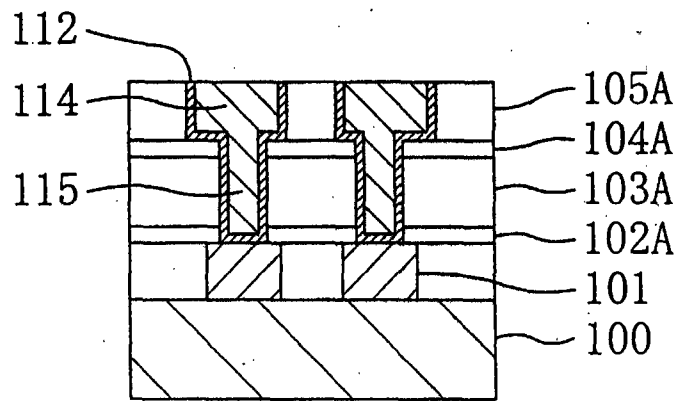


Fig. 3(c)



56220" 474250

Fig. 4(a)

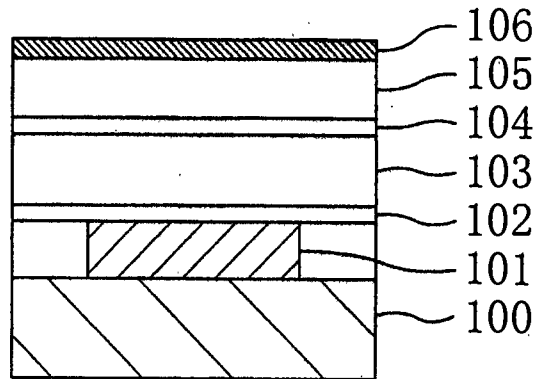


Fig. 4(b)

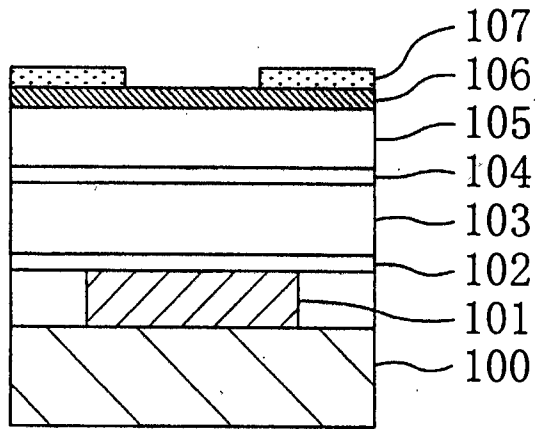
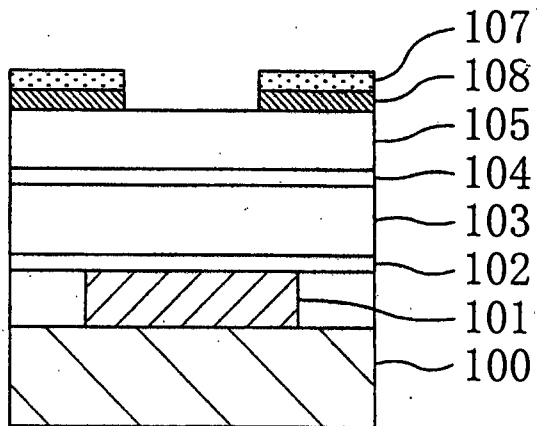


Fig. 4(c)



66260" 474260

Fig. 5(a)

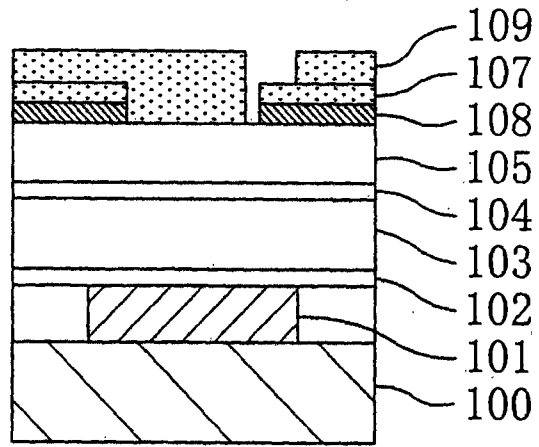


Fig. 5(b)

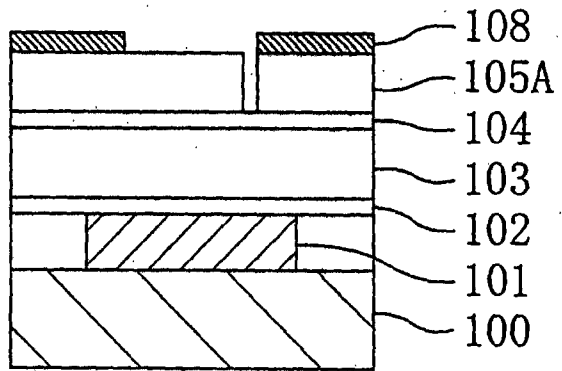
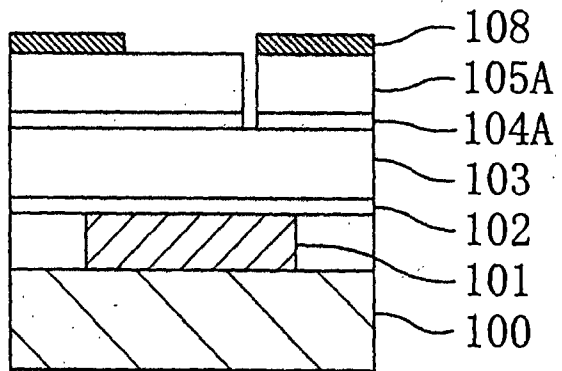


Fig. 5(c)



66220-4774260

Fig. 6(a)

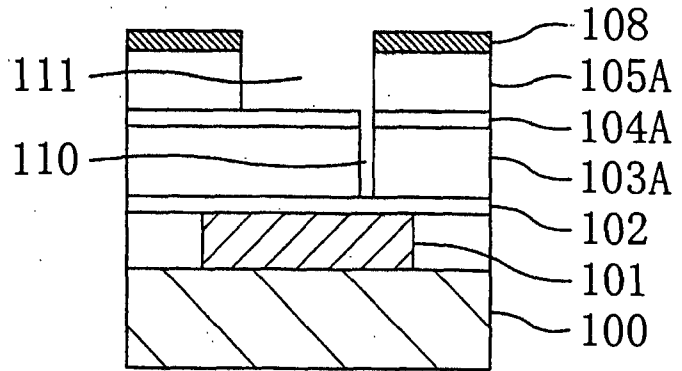


Fig. 6(b)

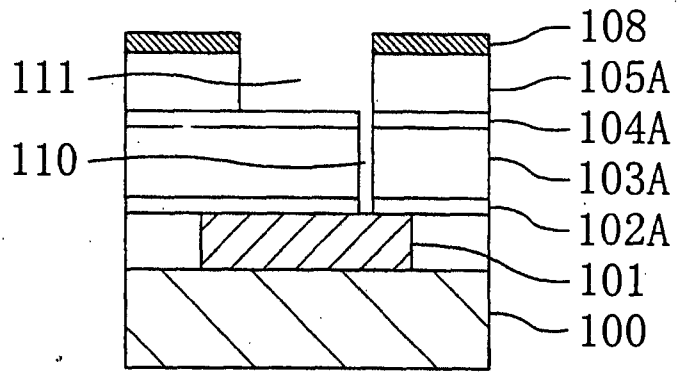
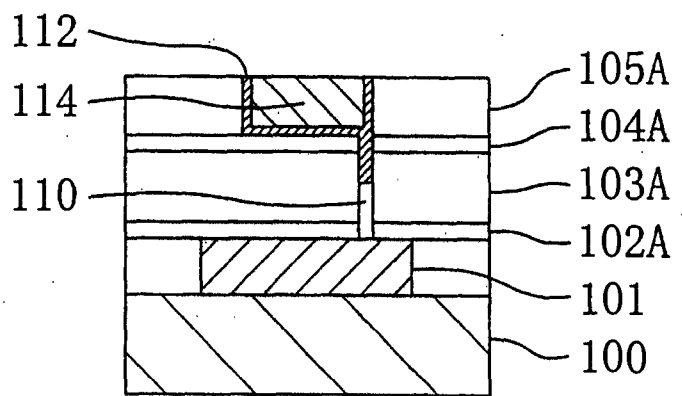


Fig. 6(c)



66250"HTFH260

Fig. 7(a)

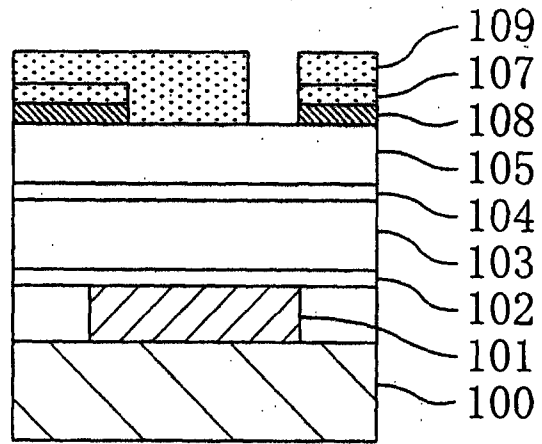


Fig. 7(b)

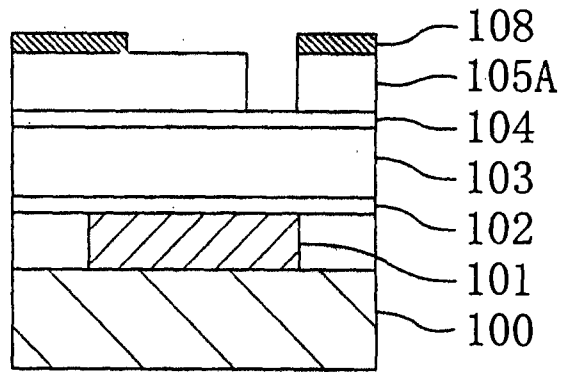
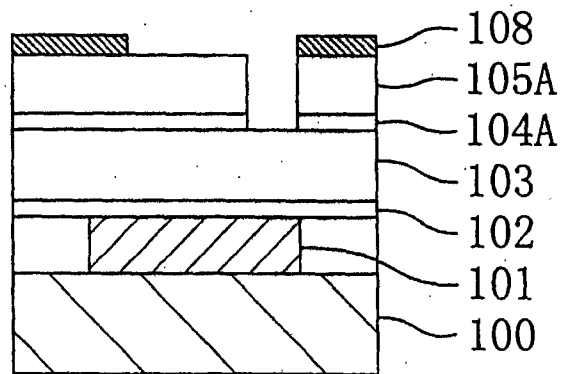


Fig. 7(c)





662250" 4TFH260

Fig. 8(a)

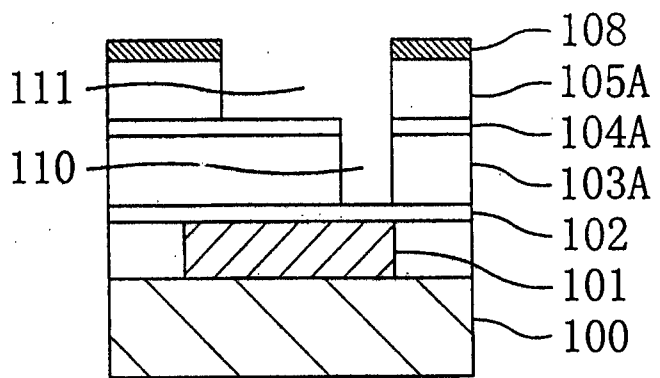


Fig. 8(b)

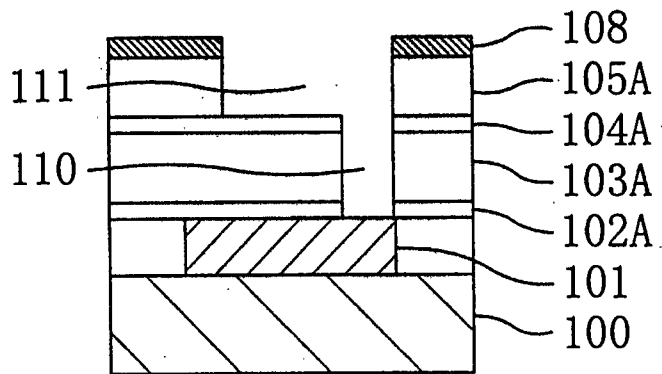
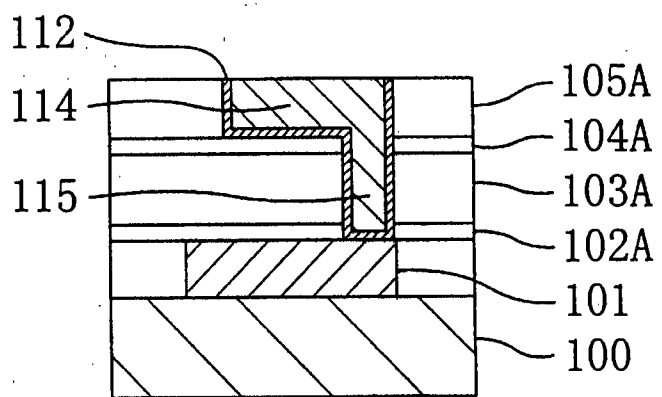


Fig. 8(c)



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Fig. 9(a)

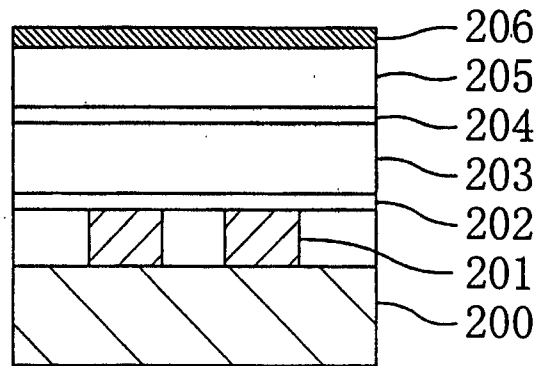


Fig. 9(b)

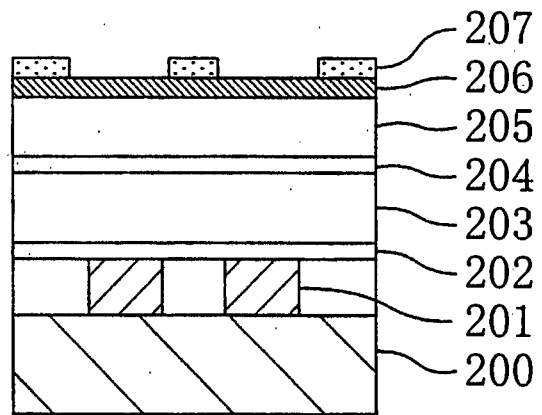
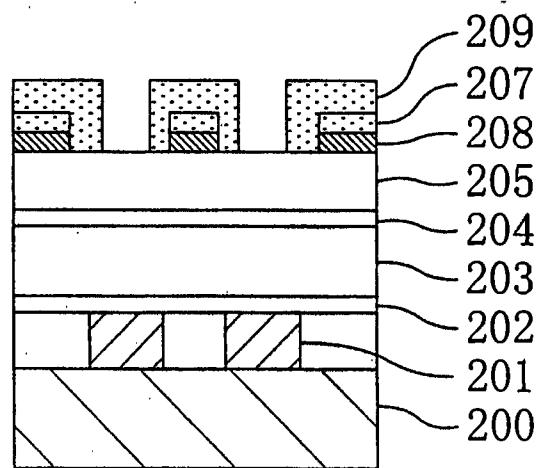


Fig. 9(c)



66220" 474260

Fig. 10(a)

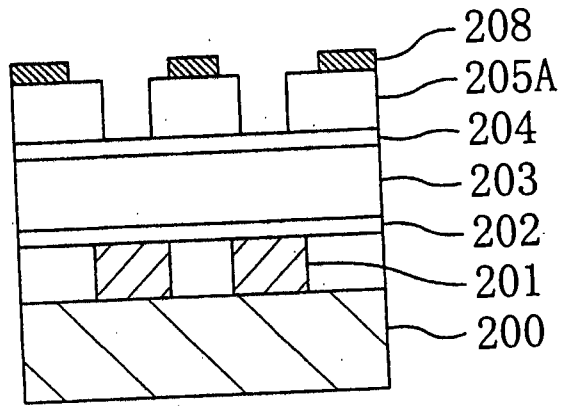


Fig. 10(b)

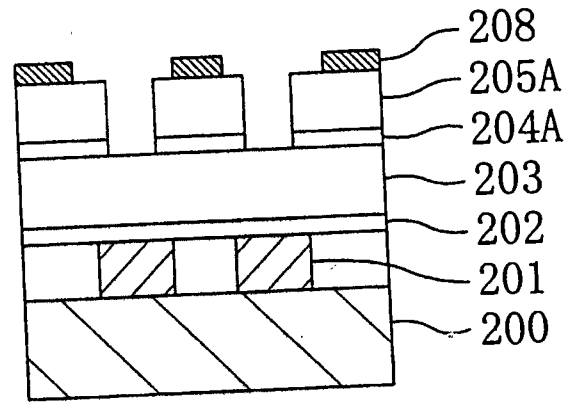
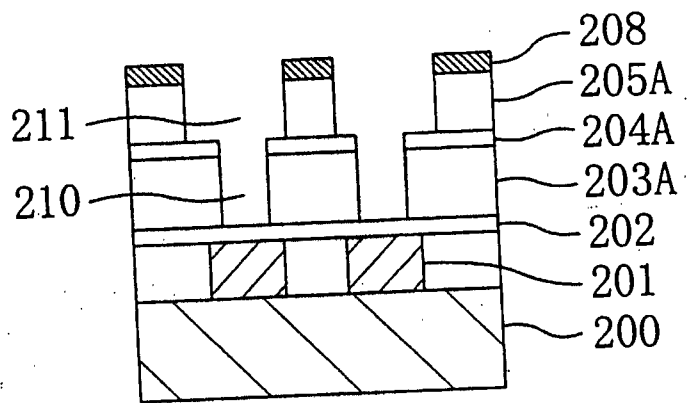


Fig. 10(c)



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Fig. 11(a)

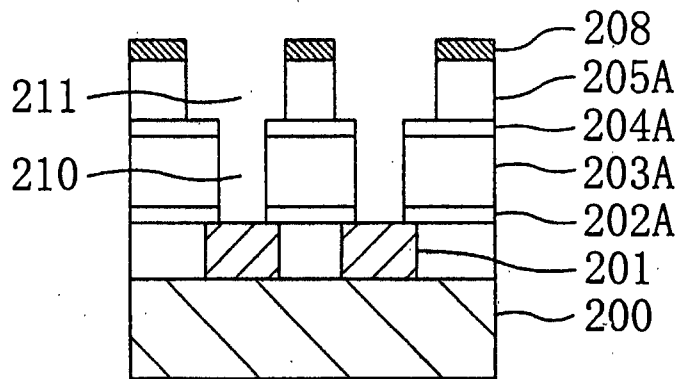


Fig. 11(b)

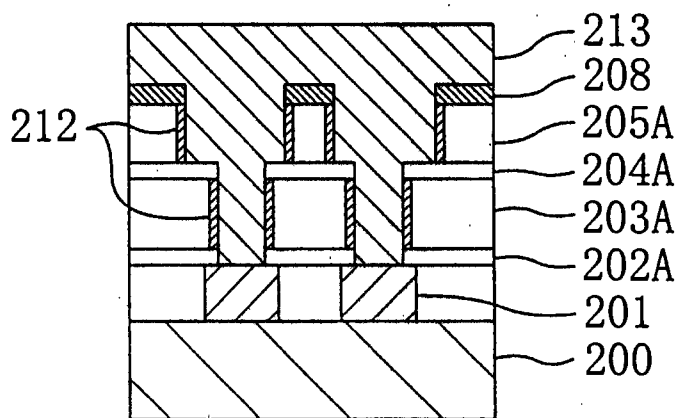


Fig. 11(c)

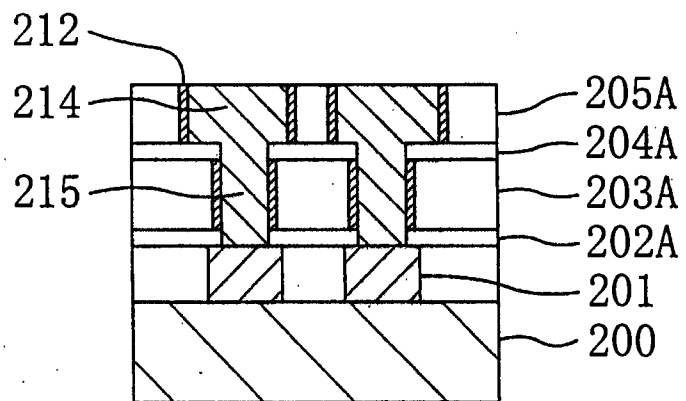


Fig. 12(a)

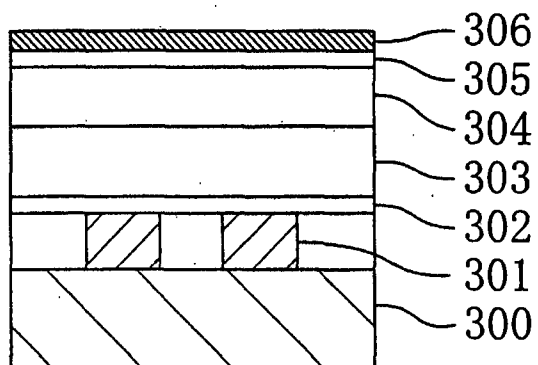


Fig. 12(b)

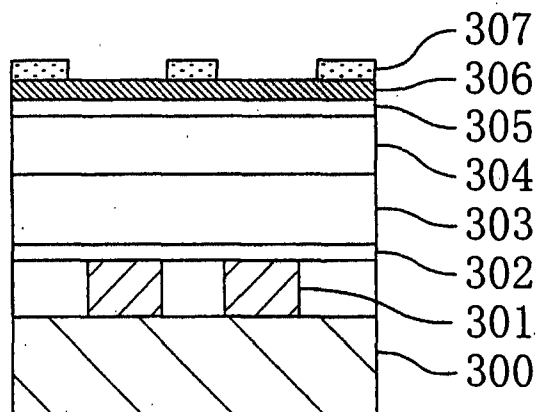
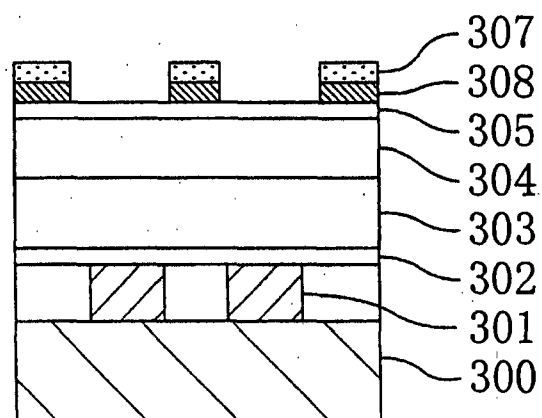


Fig. 12(c)



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Fig. 13(a)

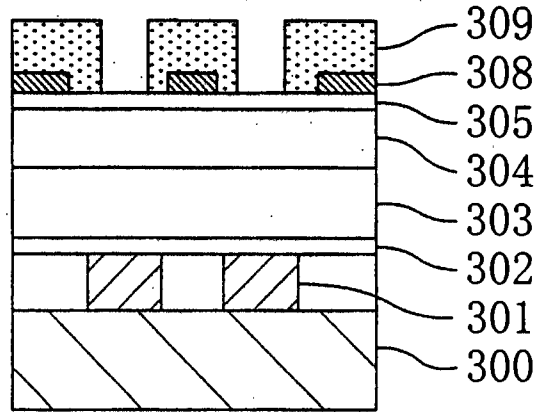


Fig. 13(b)

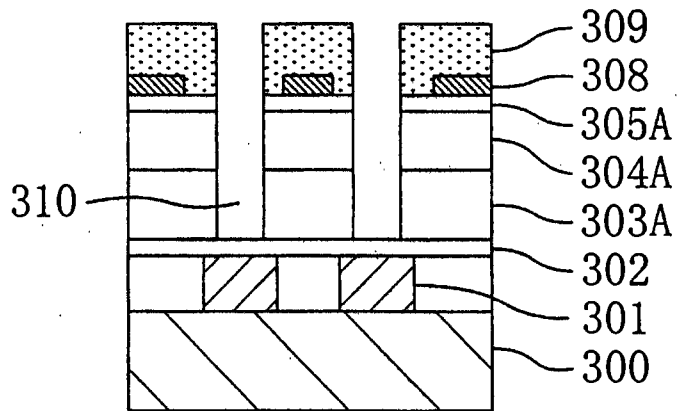
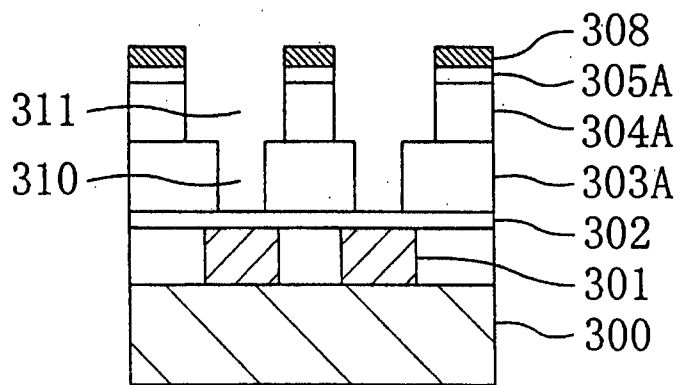


Fig. 13(c)



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Fig. 14(a)

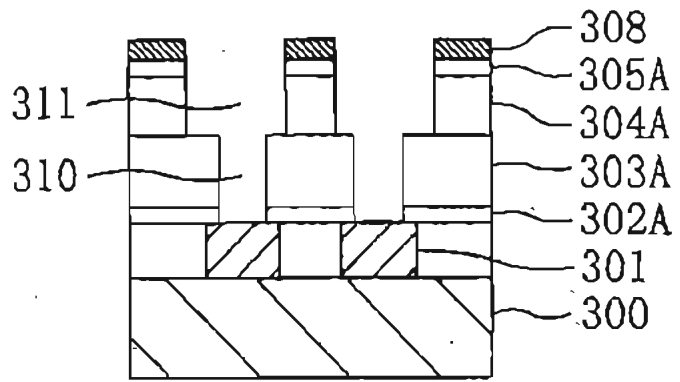


Fig. 14(b)

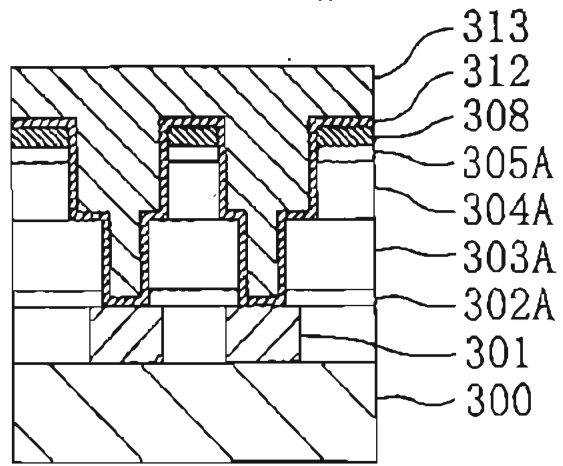
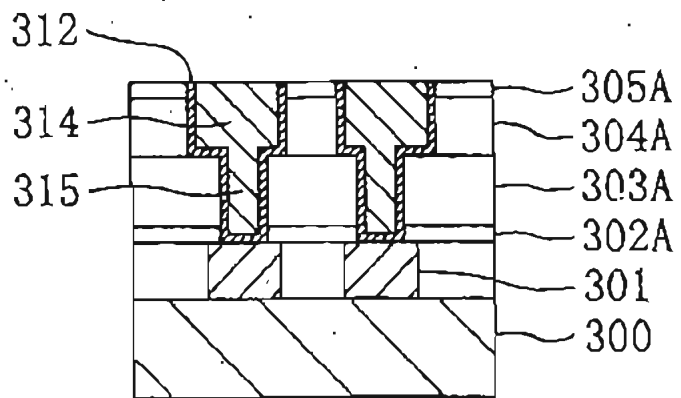


Fig. 14(c)







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Fig. 16(a)

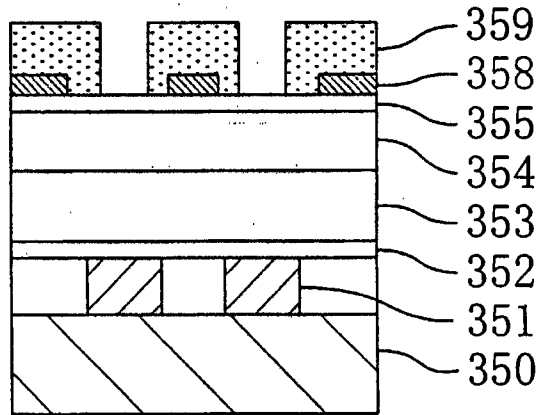


Fig. 16(b)

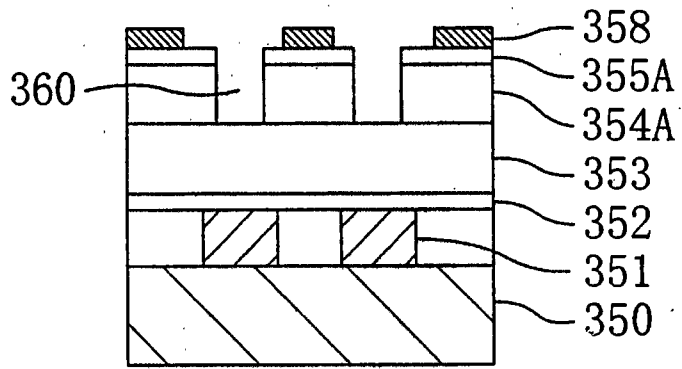


Fig. 16(c)

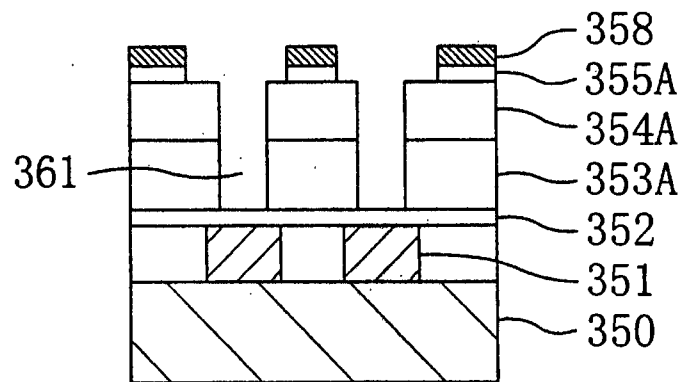
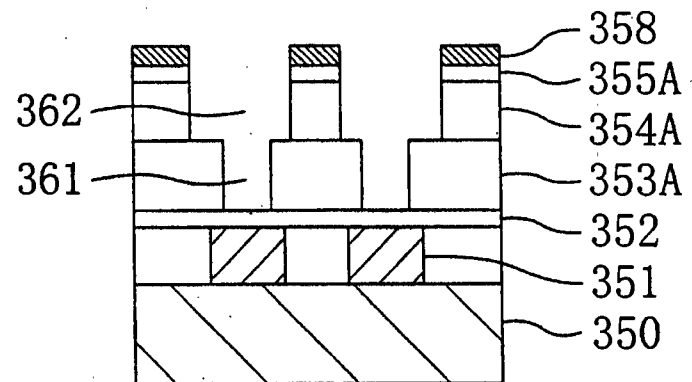


Fig. 16(d)



66220" 414260

Fig. 17(a)

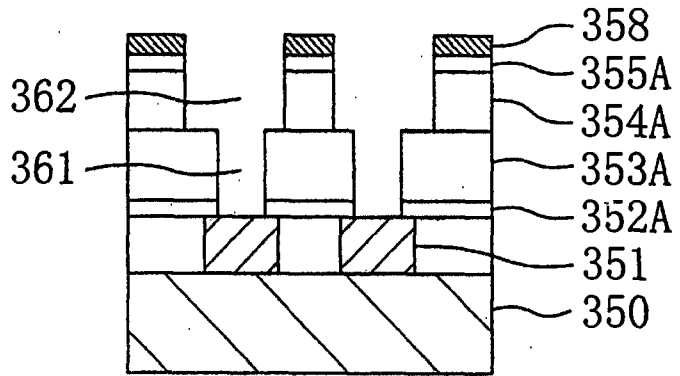


Fig. 17(b)

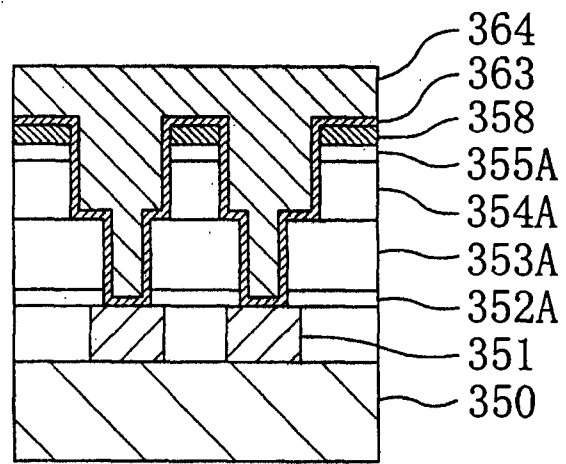


Fig. 17(c)

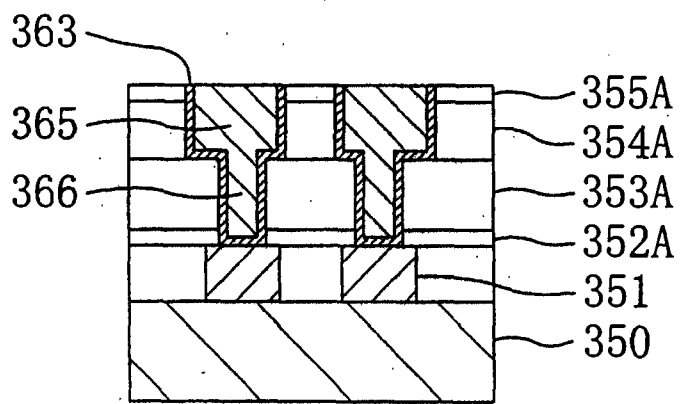


Fig. 18(a)

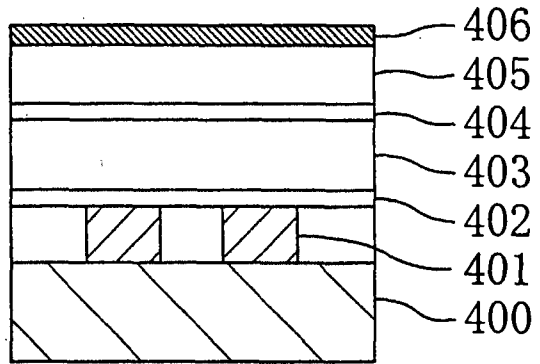


Fig. 18(b)

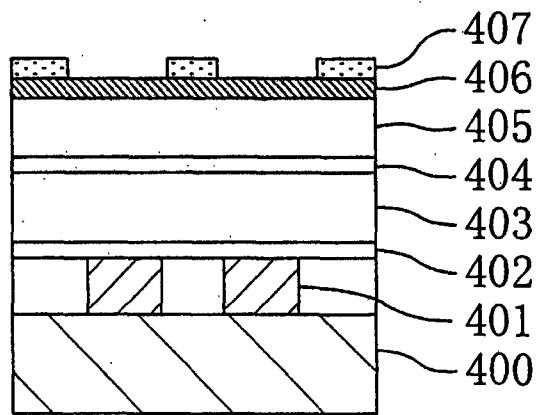
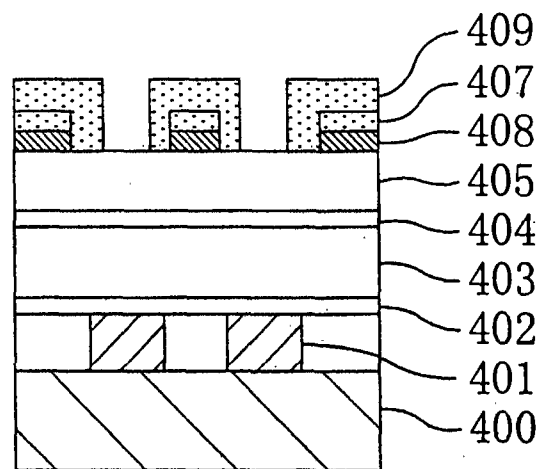


Fig. 18(c)



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Fig. 19(a)

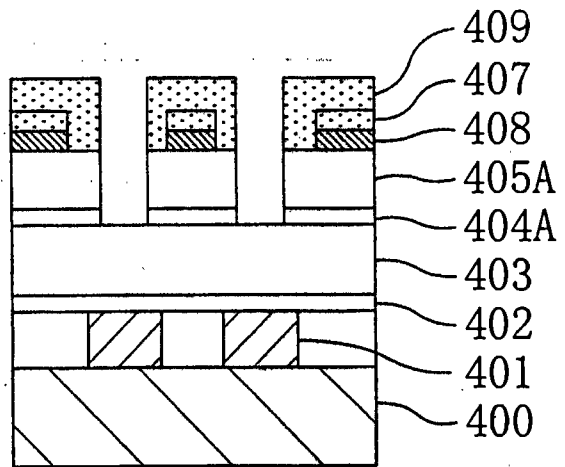


Fig. 19(b)

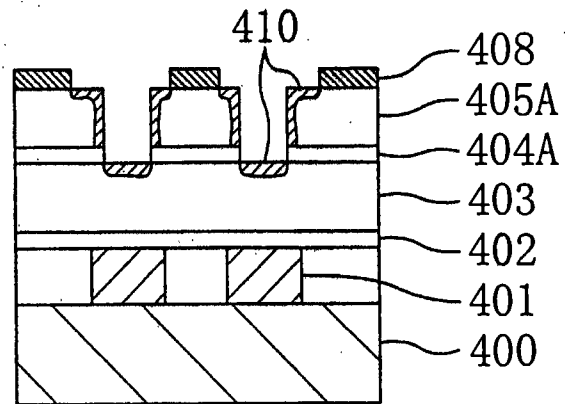
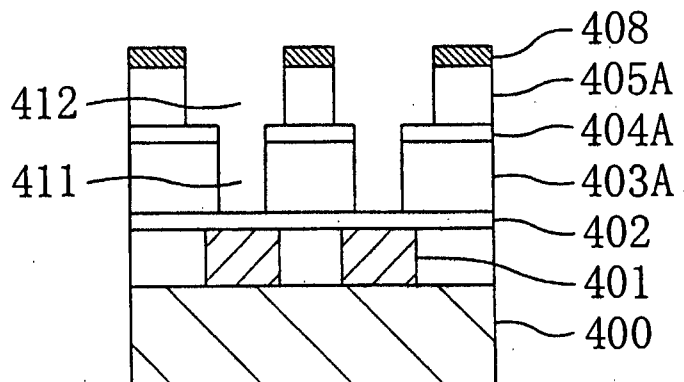


Fig. 19(c)



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Fig. 20 (a)

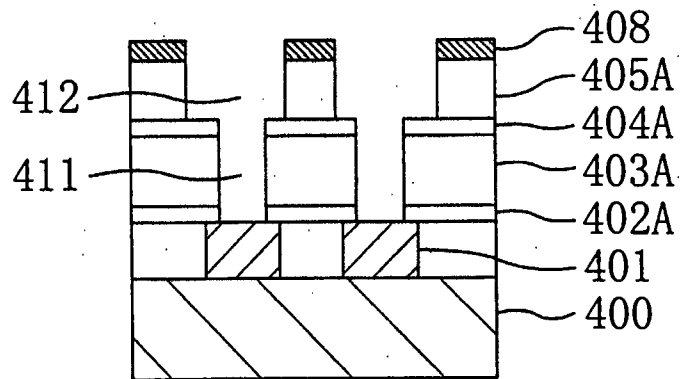


Fig. 20 (b)

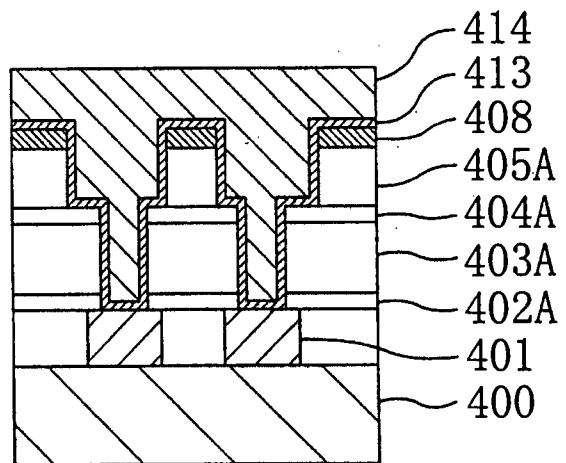
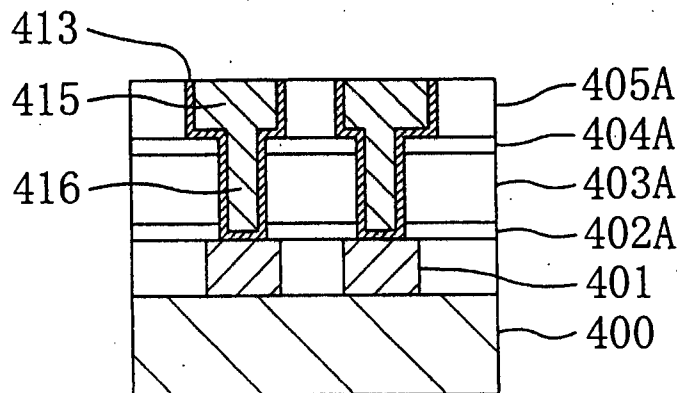


Fig. 20 (c)



66220" 474260

Fig. 21(a)

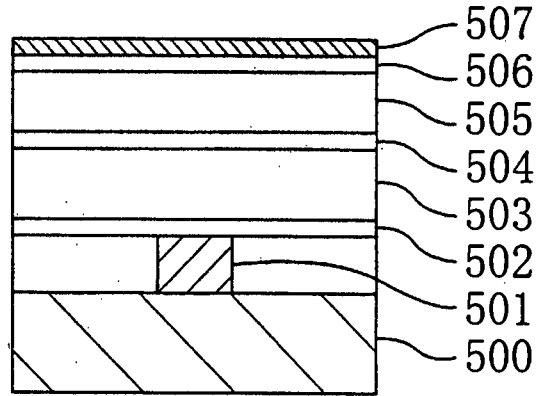


Fig. 21(b)

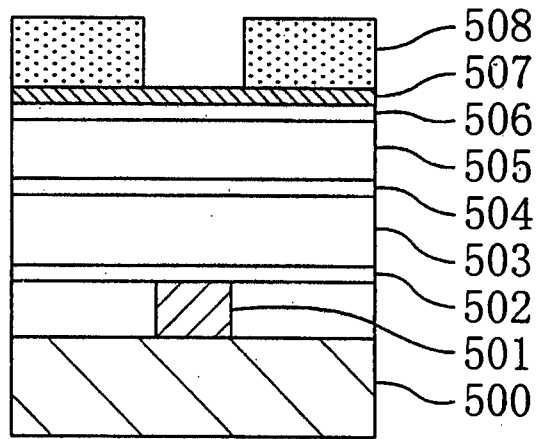
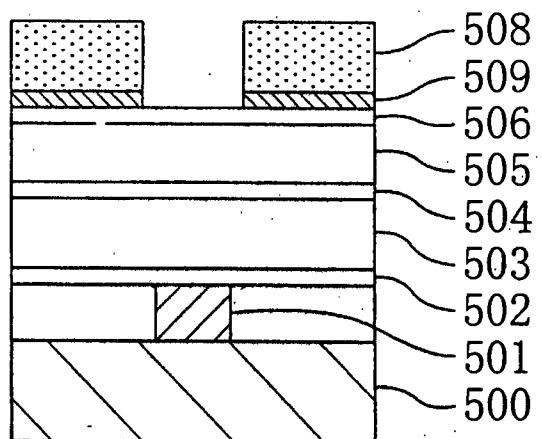


Fig. 21(c)



66260" 4774260

Fig. 22(a)

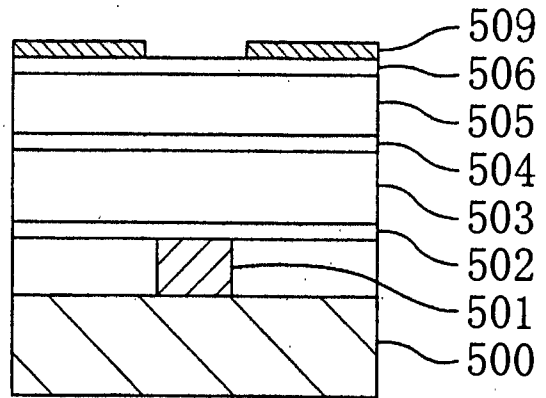


Fig. 22(b)

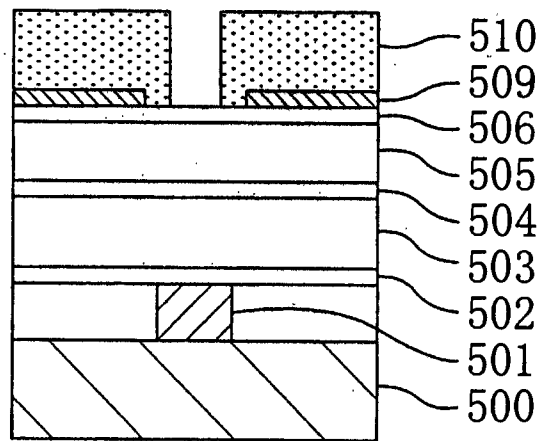
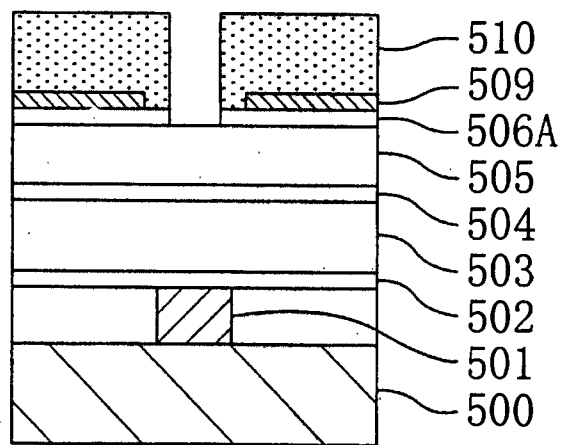


Fig. 22(c)



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Fig. 23(a)

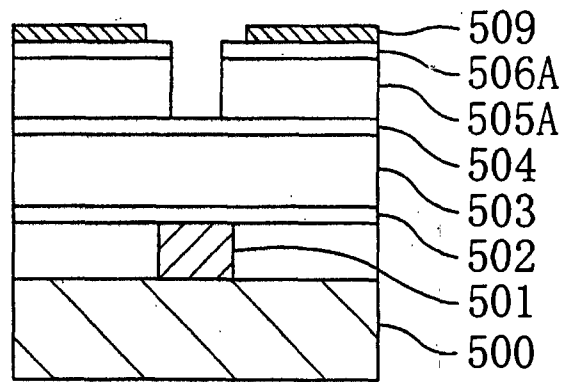


Fig. 23(b)

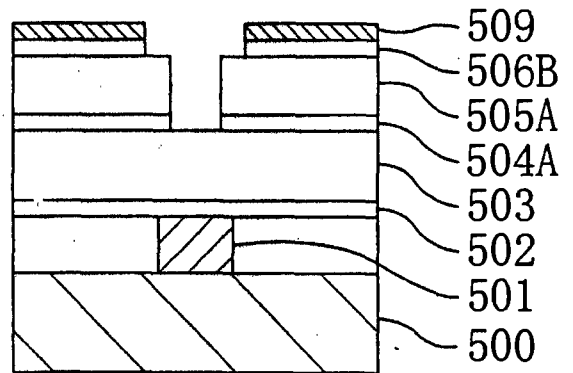


Fig. 23(c)

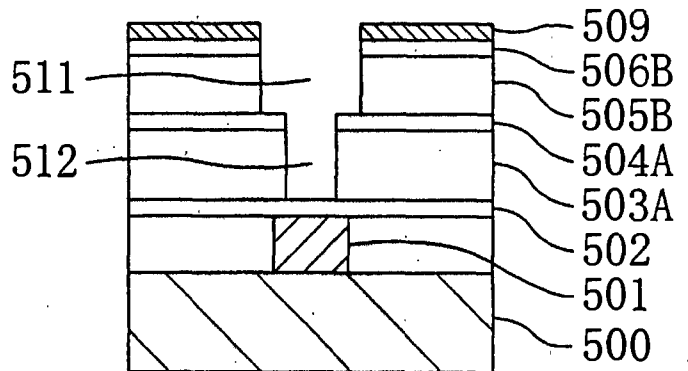


Fig. 23(d)

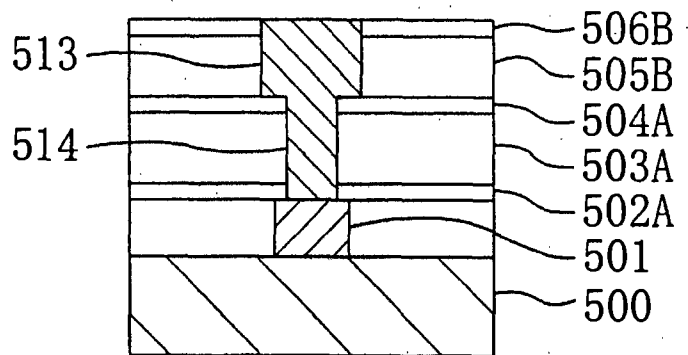




Fig. 24(a)

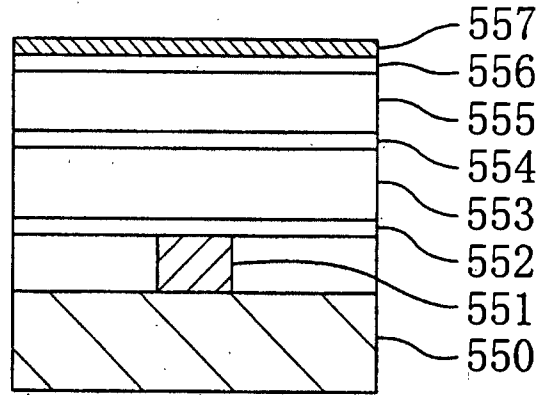


Fig. 24(b)

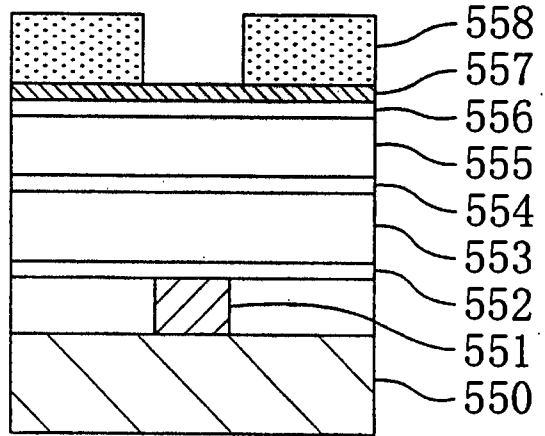
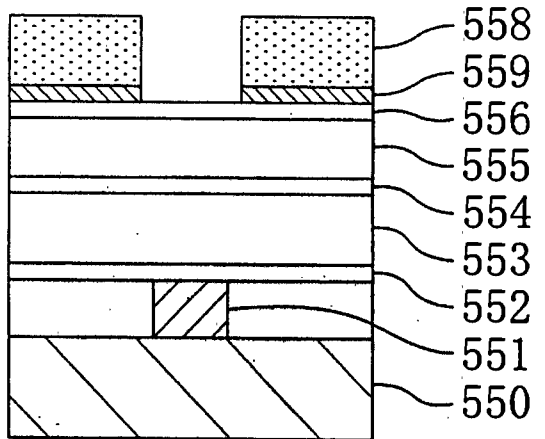


Fig. 24(c)



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Fig. 25(a)

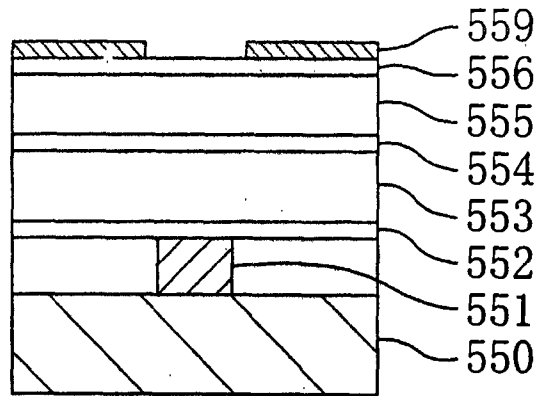


Fig. 25(b)

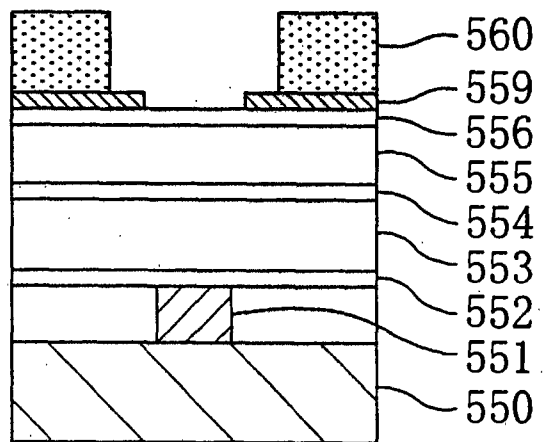
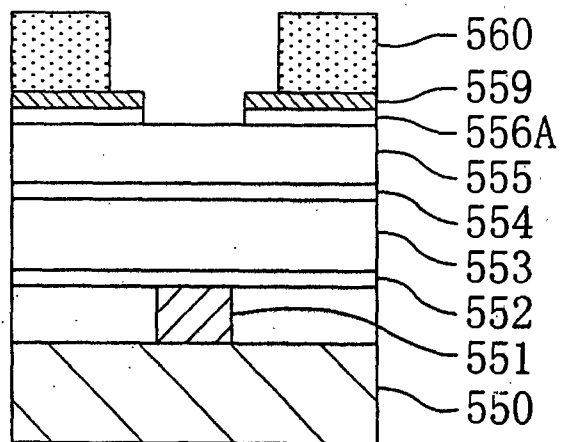


Fig. 25(c)



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Fig. 26 (a)

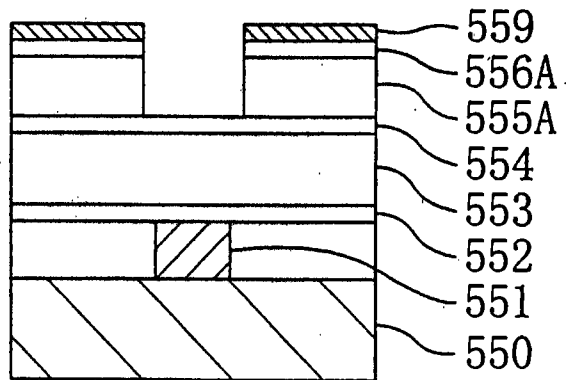


Fig. 26 (b)

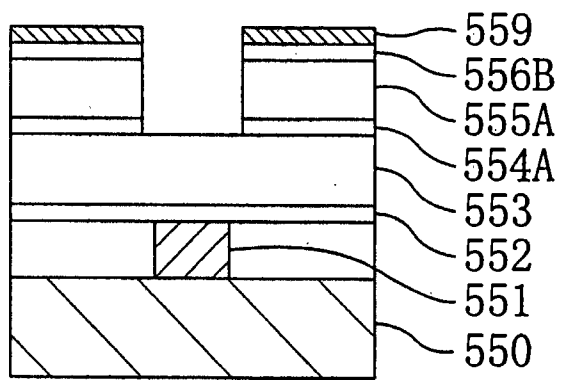


Fig. 26 (c)

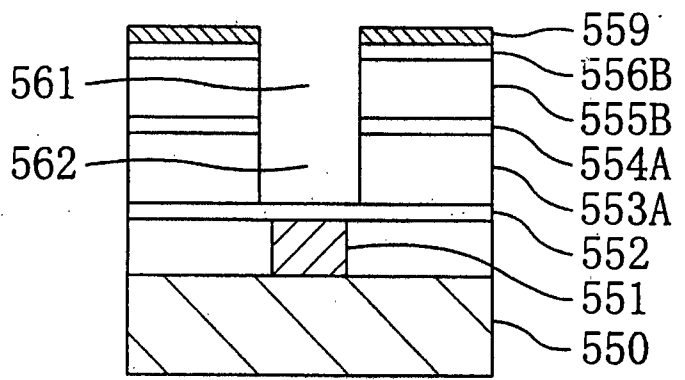
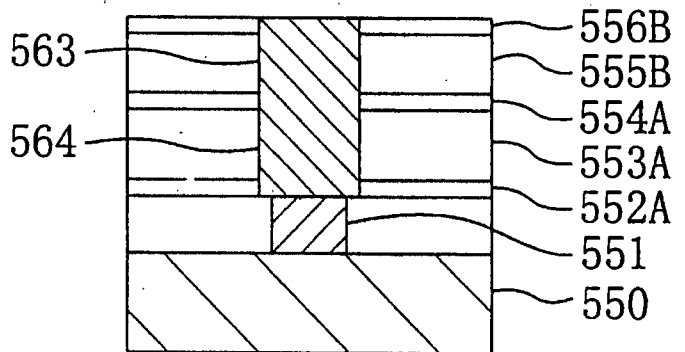


Fig. 26 (d)



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Fig. 27 (a)

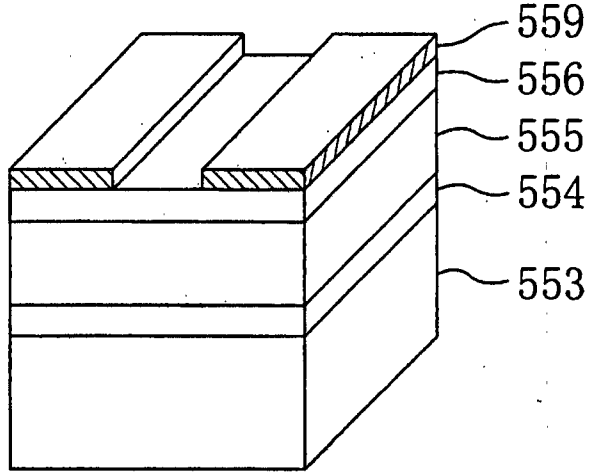
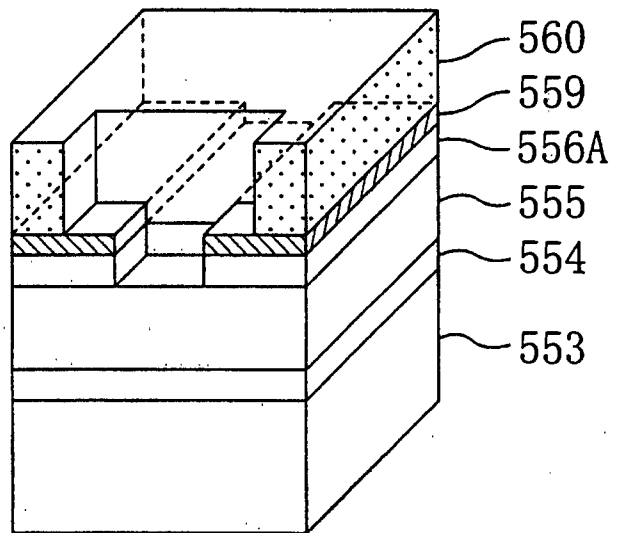


Fig. 27 (b)



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Fig. 28(a)

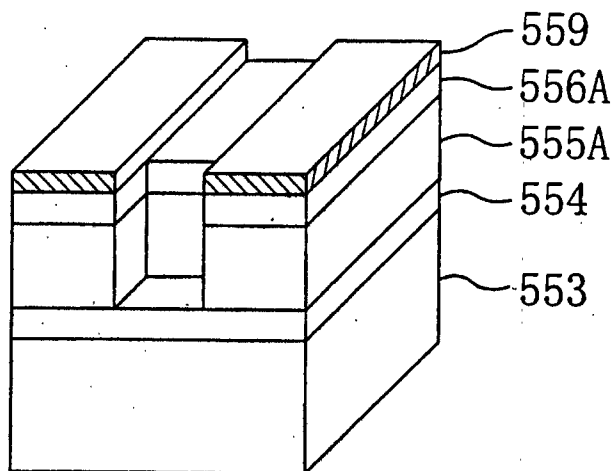


Fig. 28(b)

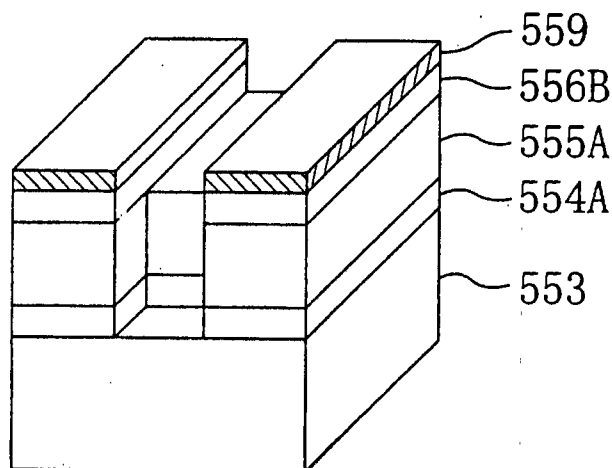


Fig. 29(a)

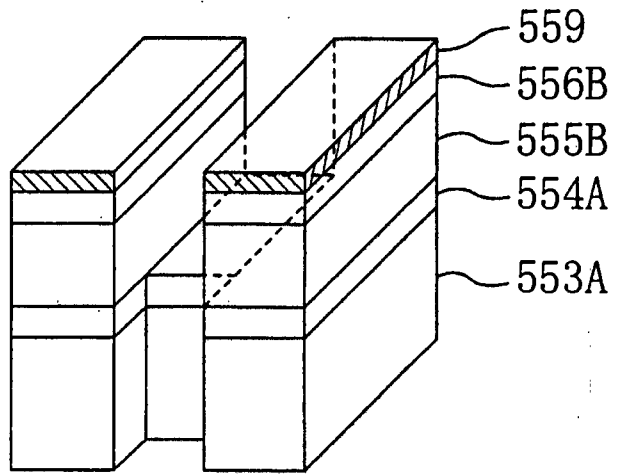
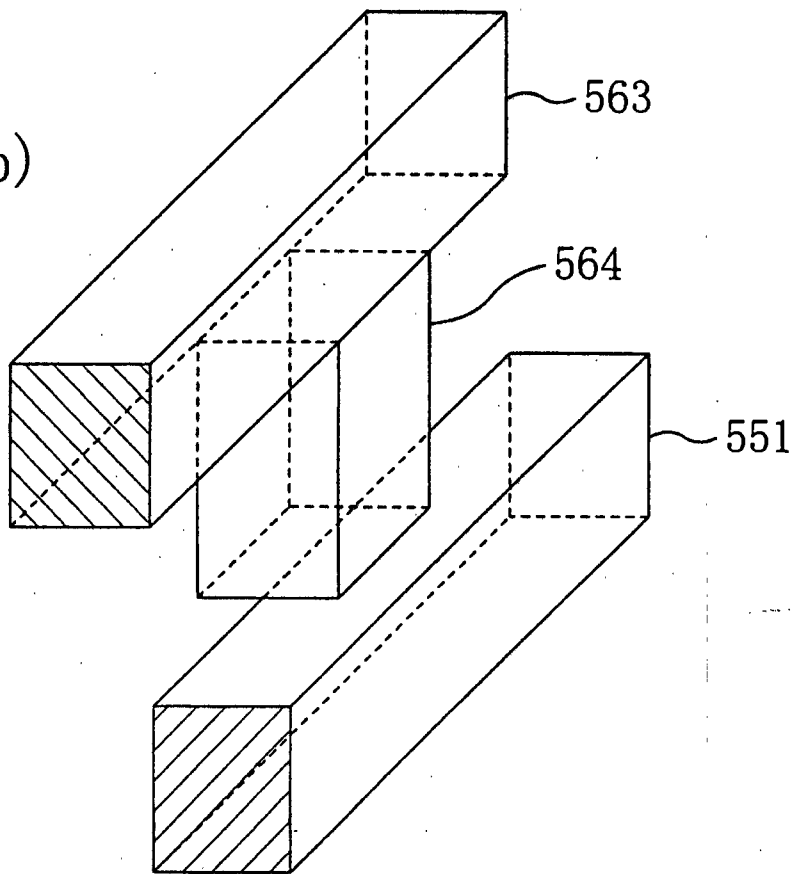


Fig. 29(b)



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Fig. 30 (a)

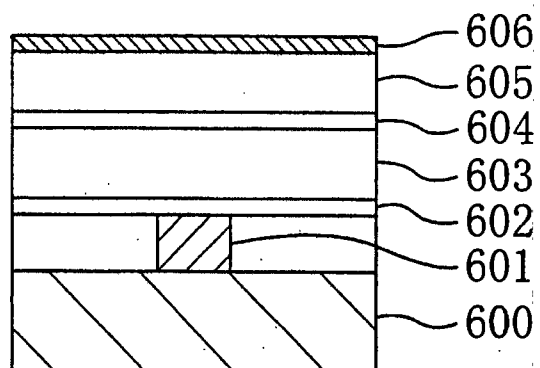


Fig. 30 (b)

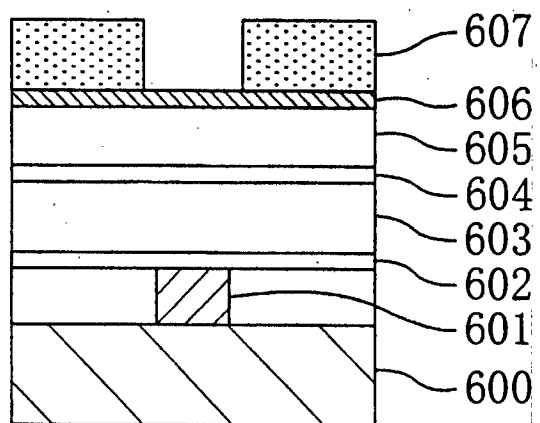
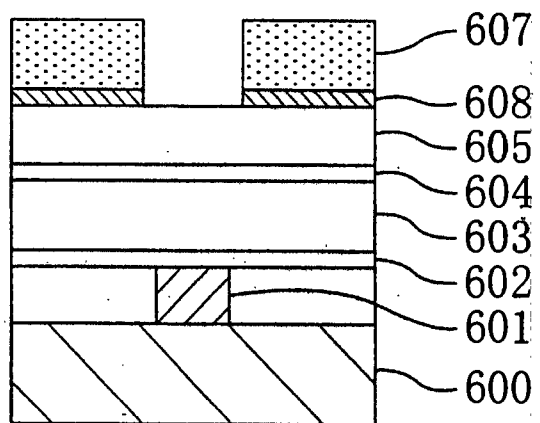


Fig. 30 (c)



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Fig. 31 (a)

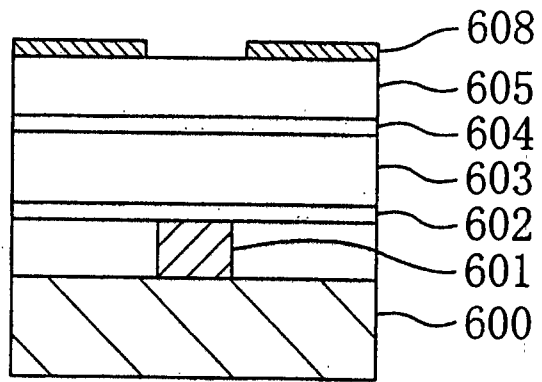


Fig. 31 (b)

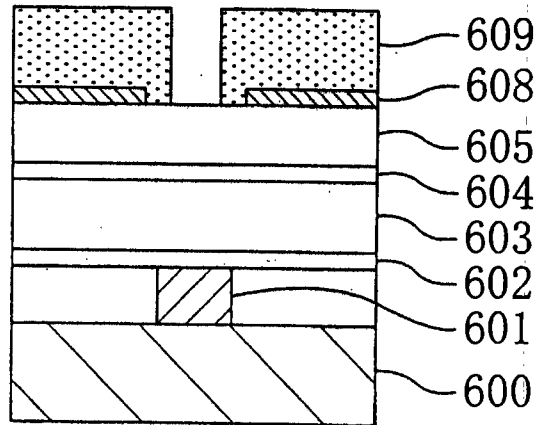
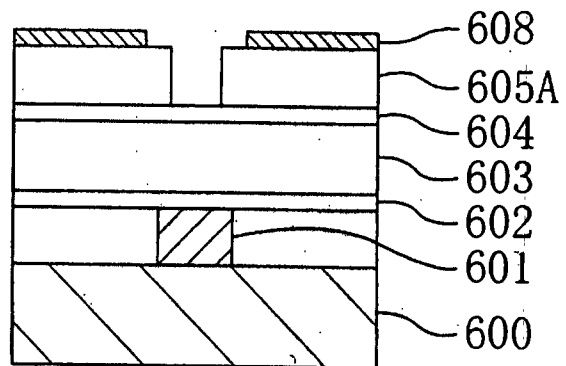


Fig. 31 (c)



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Fig. 32(a)

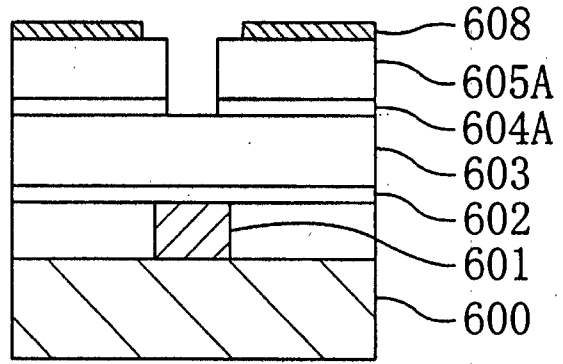


Fig. 32(b)

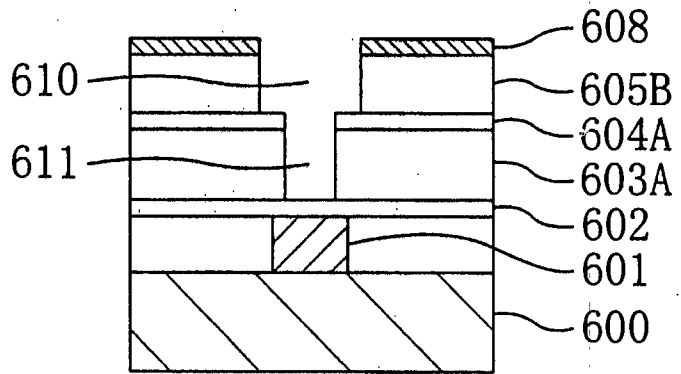
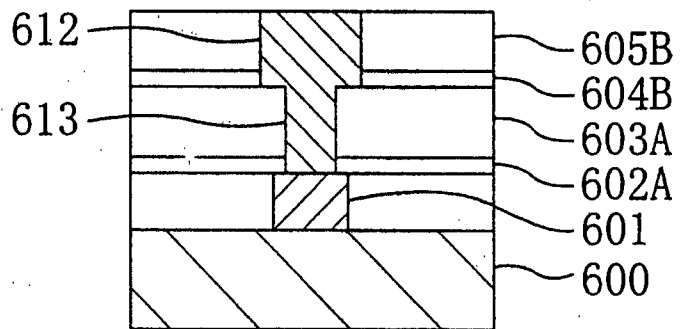


Fig. 32(c)



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Fig. 33(a)

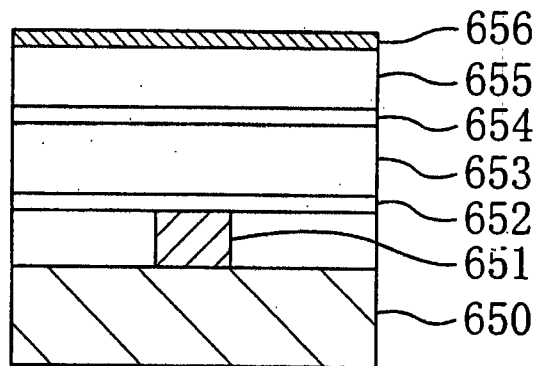


Fig. 33(b)

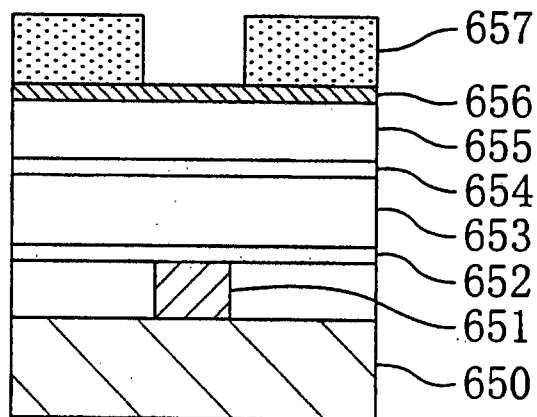


Fig. 33(c)

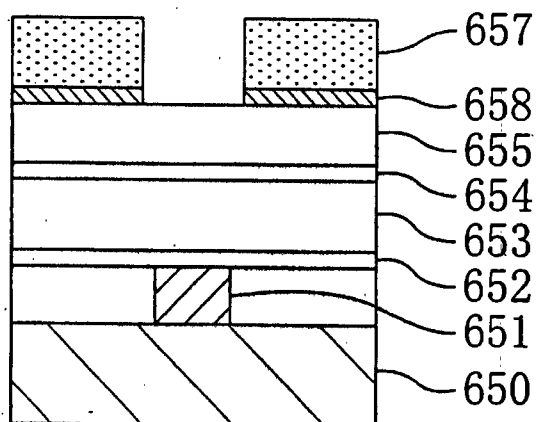




Fig. 35 (a)

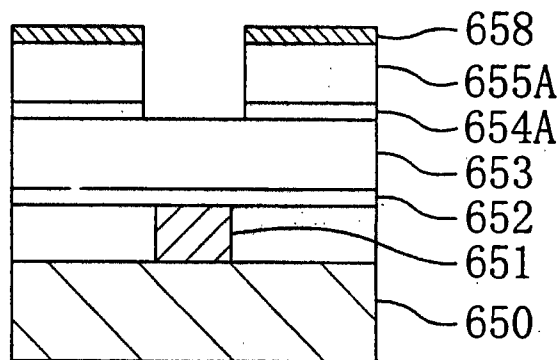


Fig. 35 (b)

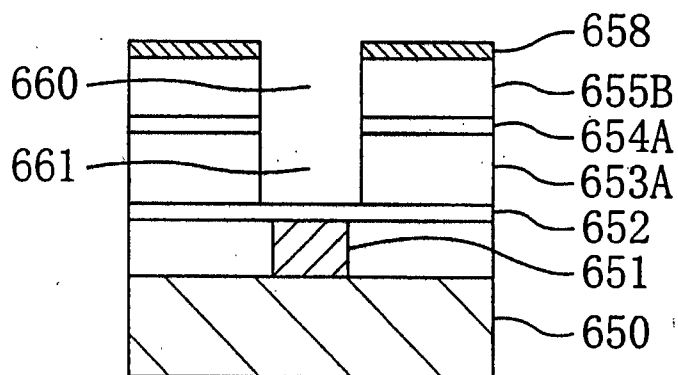
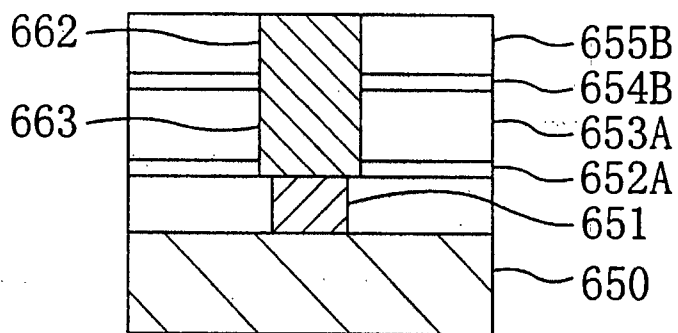
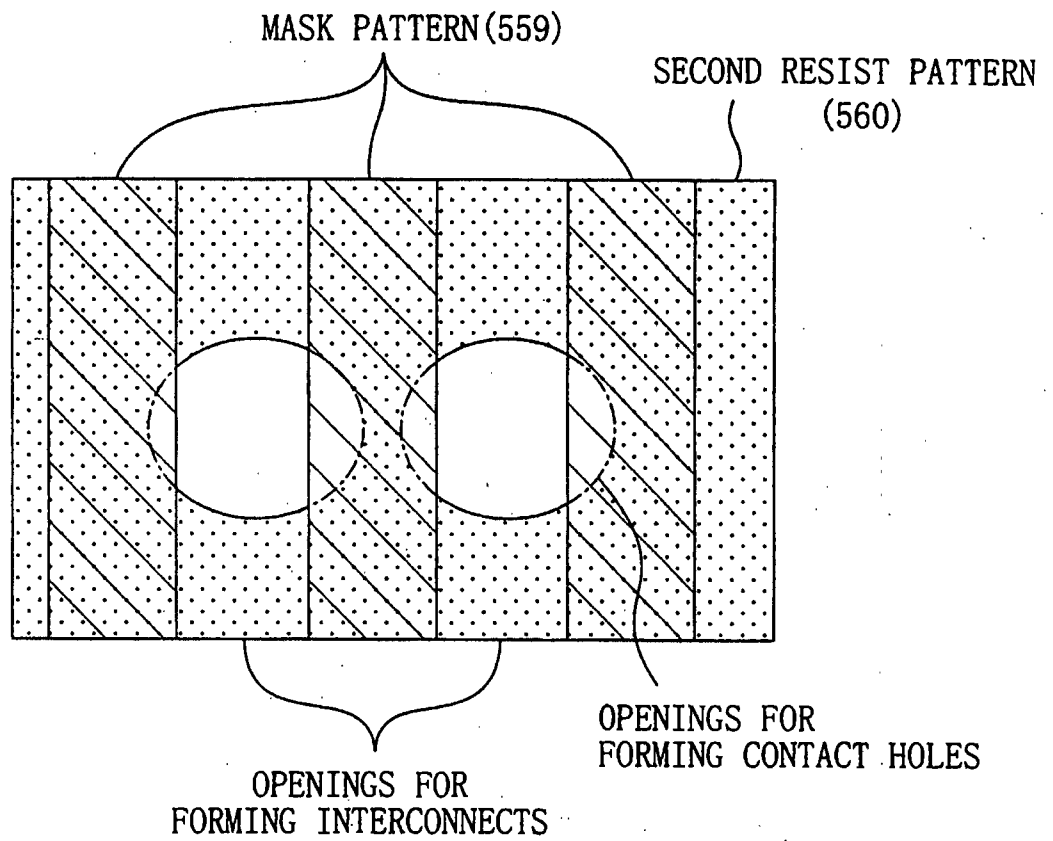


Fig. 35 (c)



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Fig. 36



66220"4774260

Fig. 37(a)

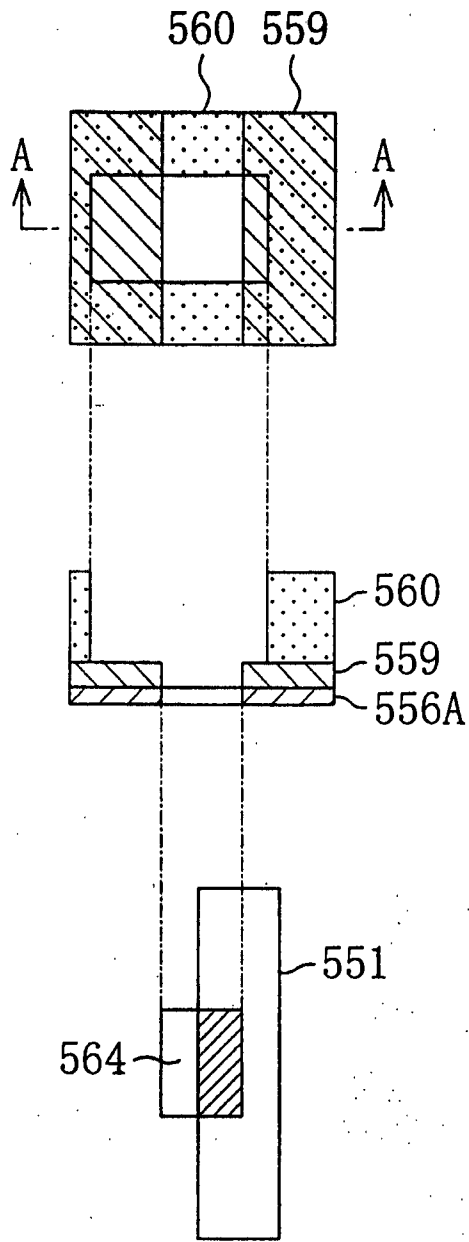
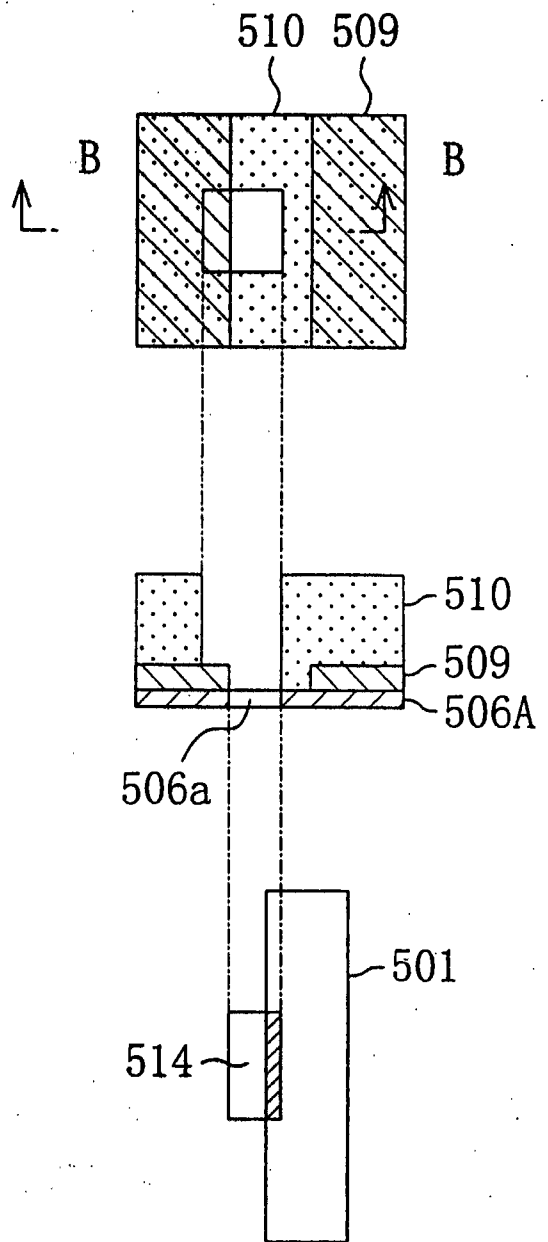


Fig. 37(b)



66260-474260

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

09/274,114

6197696

Fig. 1(a)

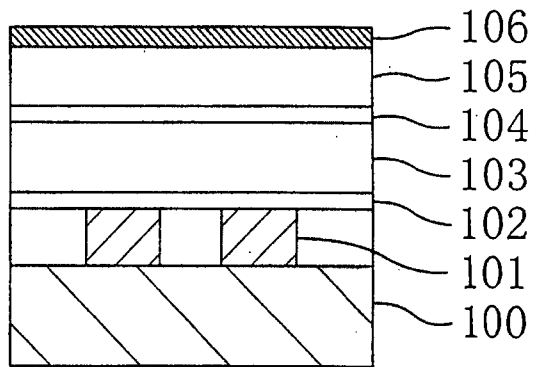


Fig. 1(b)

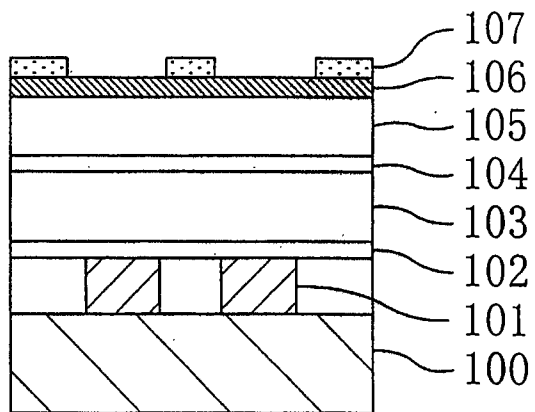
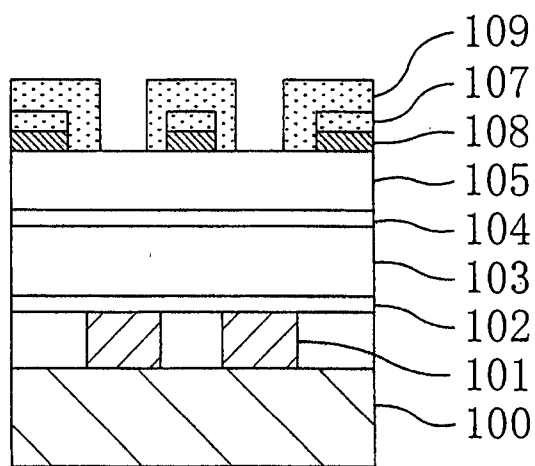


Fig. 1(c)



09/274,114-03299

APPROVED	O.G. FIG. 36	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 2(a)

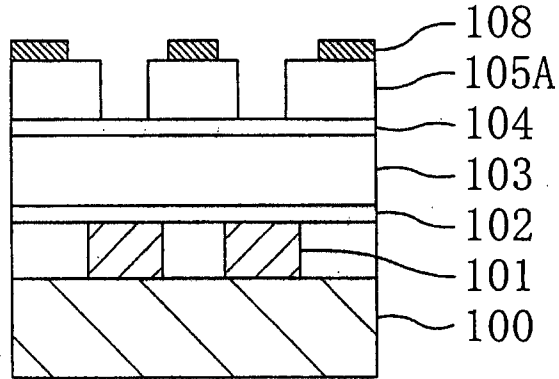


Fig. 2(b)

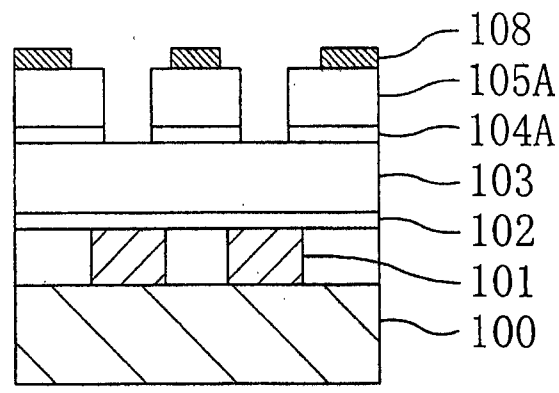
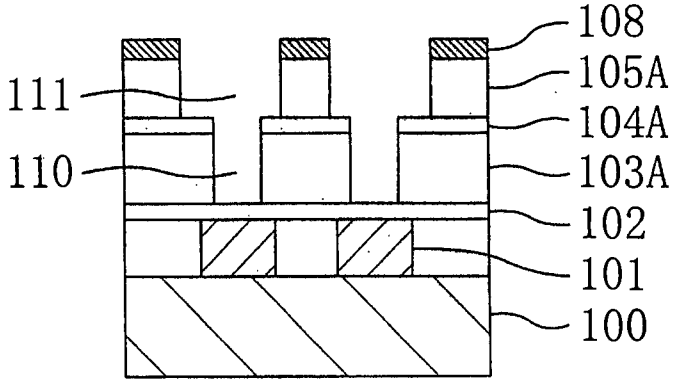


Fig. 2(c)



66220-114250



APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 3(a)

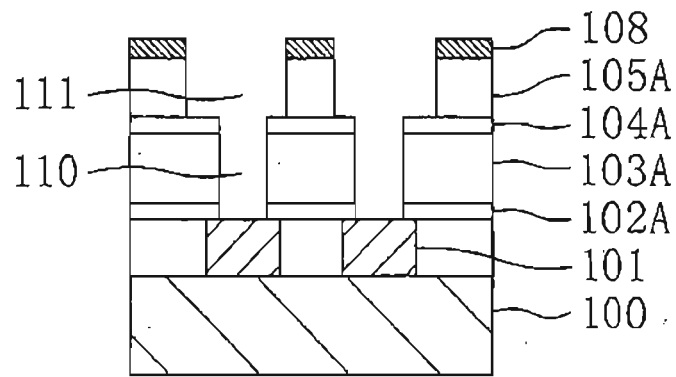


Fig. 3(b)

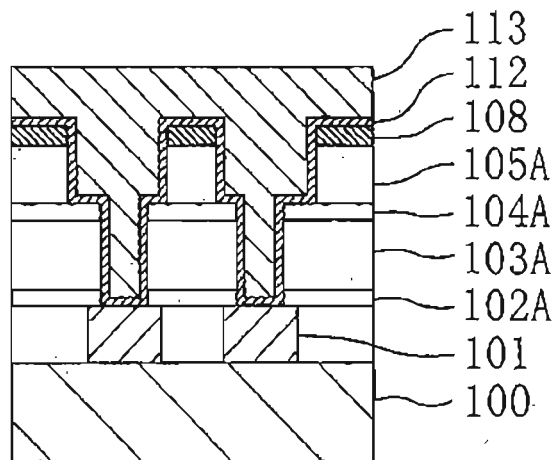
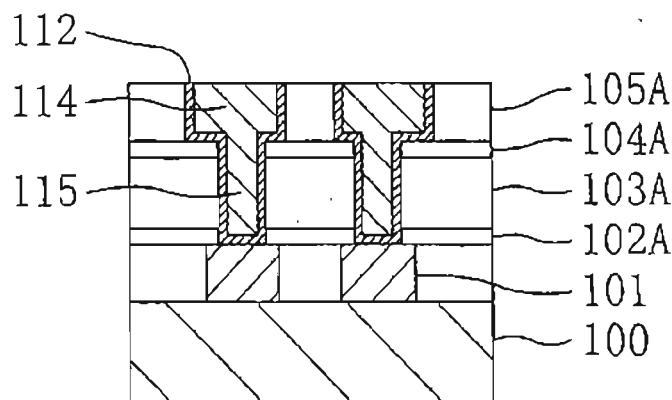


Fig. 3(c)



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APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
CRAFTSMAN	438	700

Fig. 4(a)

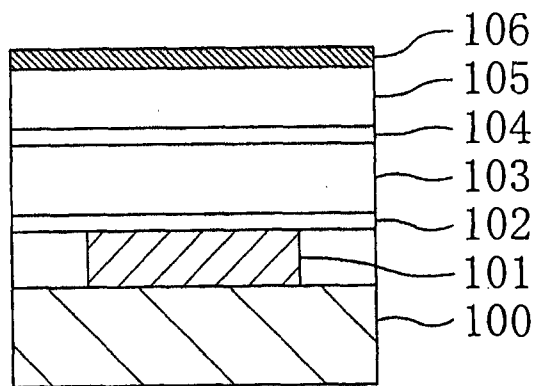


Fig. 4(b)

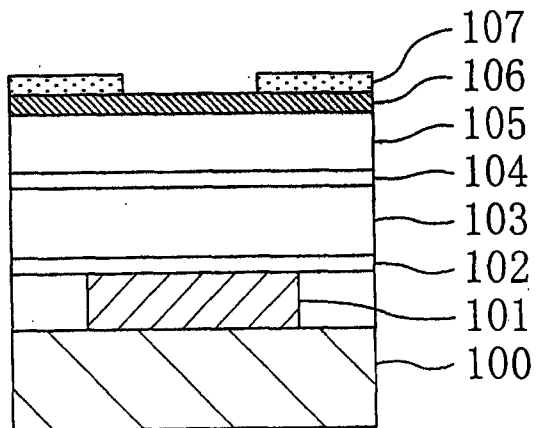
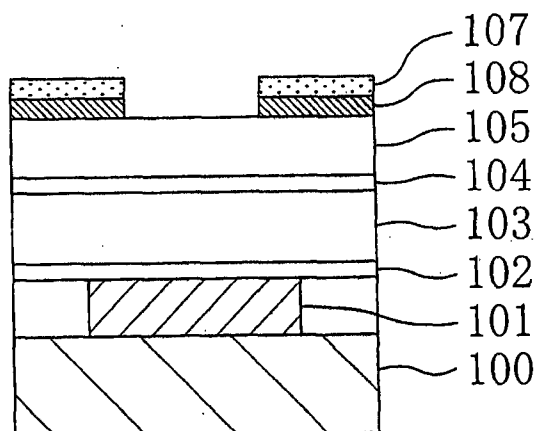


Fig. 4(c)



66220-4114250

APPROVED	U.S. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	436	700

Fig. 5(a)

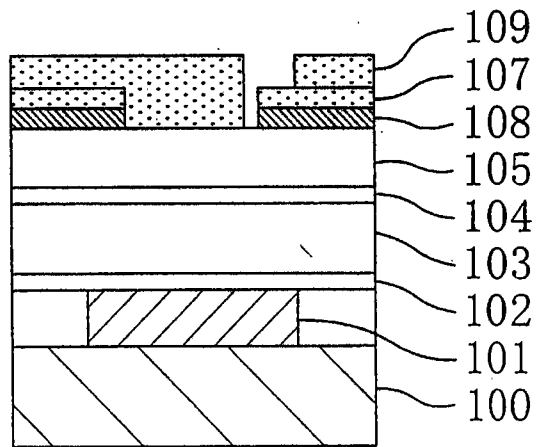


Fig. 5(b)

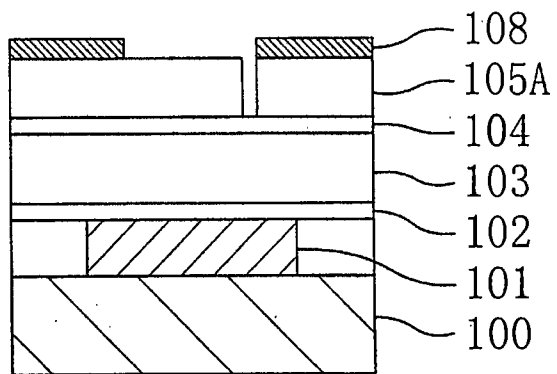
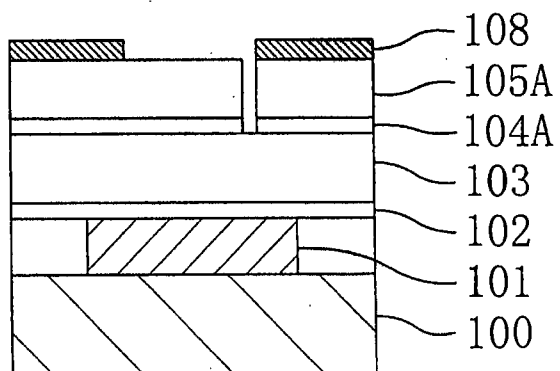


Fig. 5(c)



66220" 474250

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 6(a)

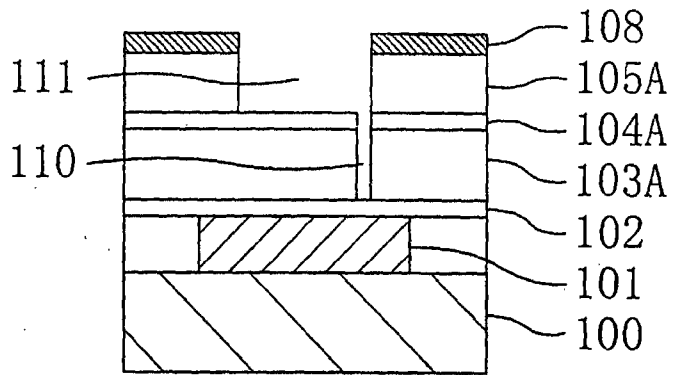


Fig. 6(b)

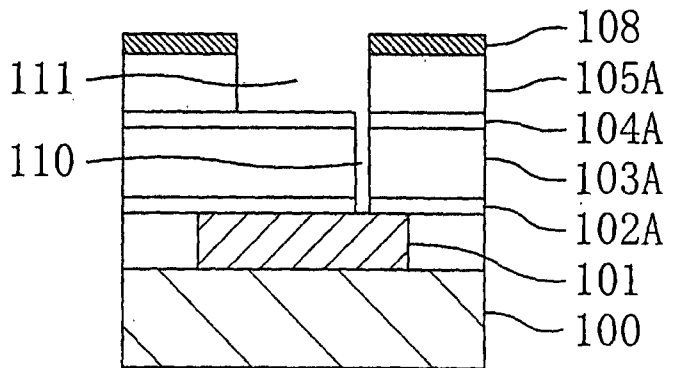
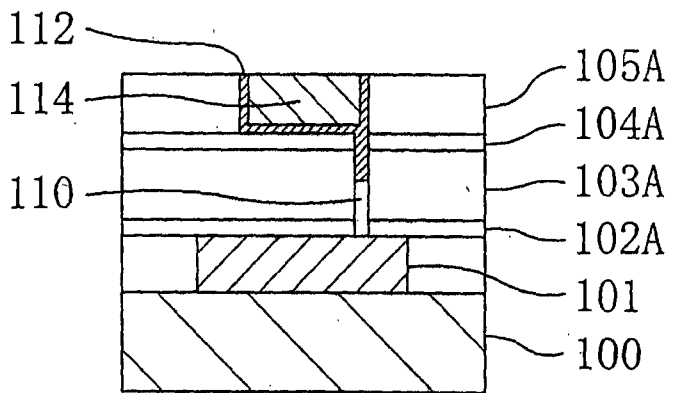


Fig. 6(c)



66220-111250

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 7(a)

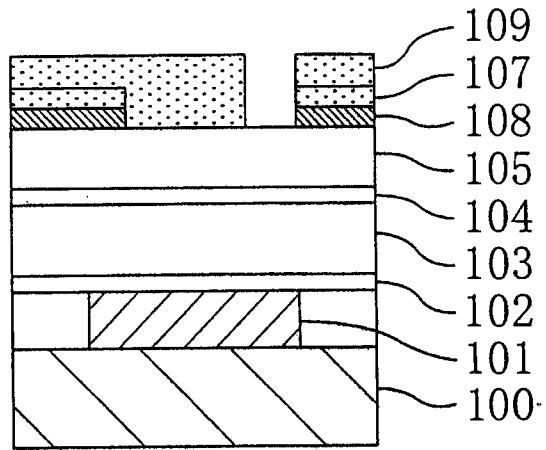


Fig. 7(b)

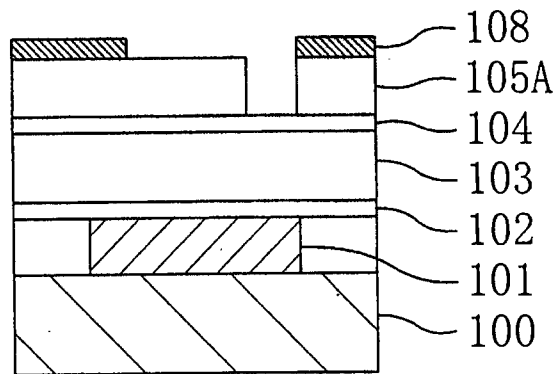
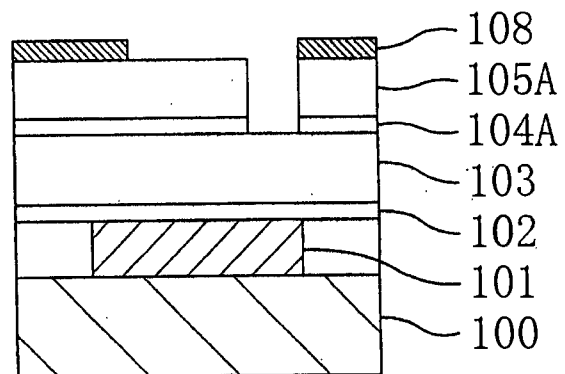


Fig. 7(c)



09244-4260

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 8(a)

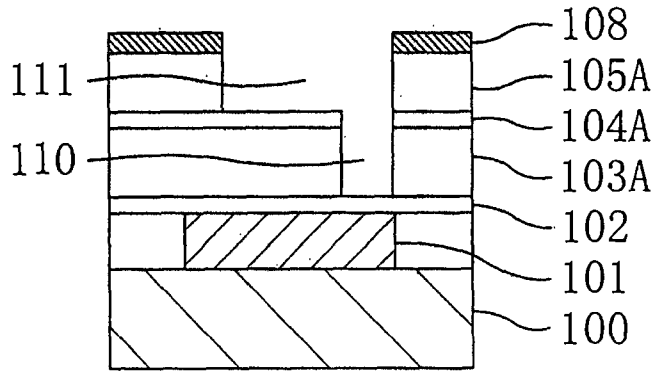


Fig. 8(b)

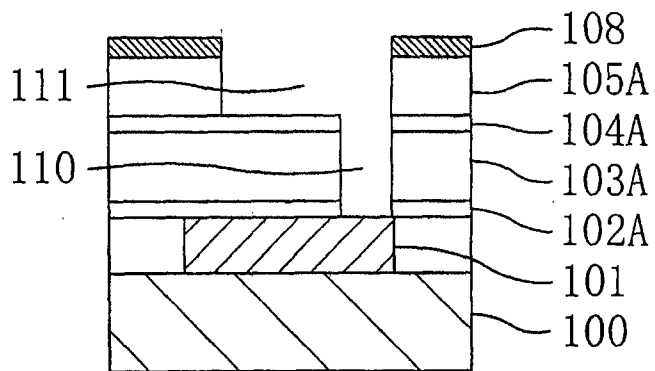
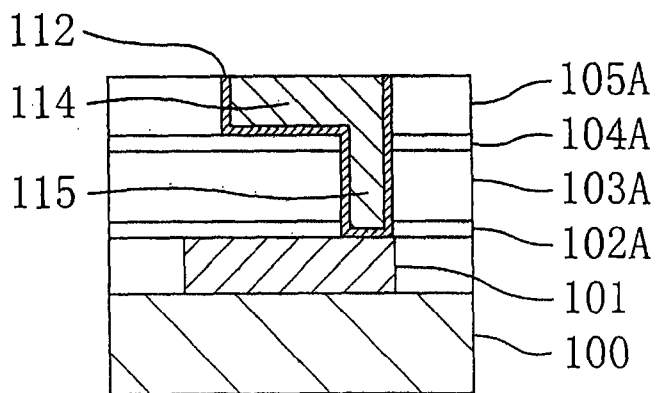


Fig. 8(c)



66220-4774260

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
CRAFTSMAN	438	700

Fig. 9(a)

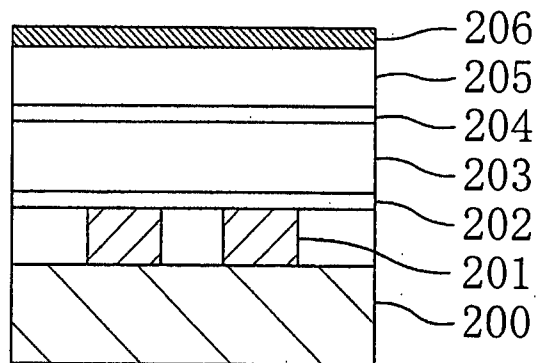


Fig. 9(b)

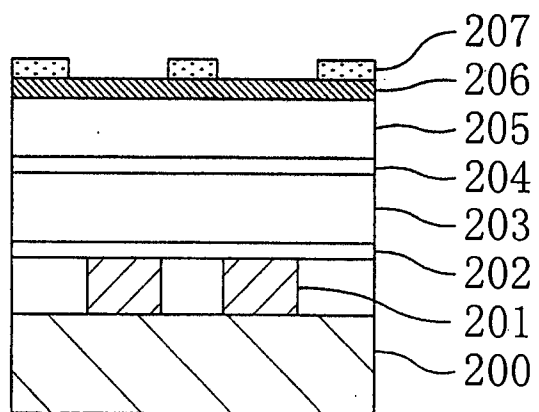
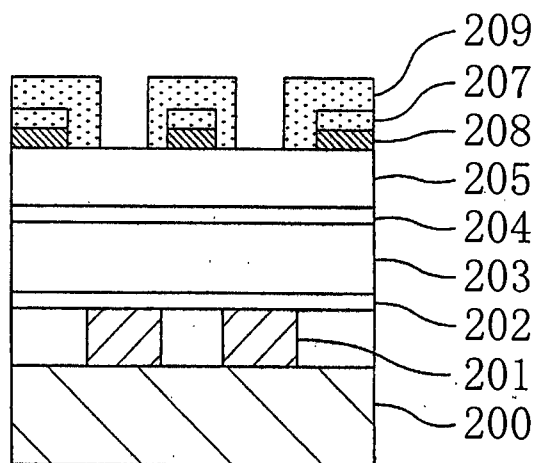


Fig. 9(c)



66220-474260

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
CRAFTSMAN	438	700

Fig. 10(a)

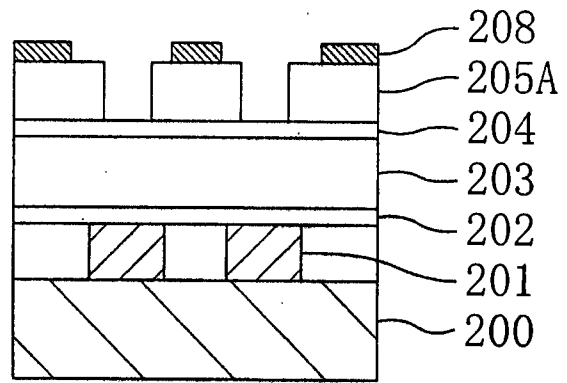


Fig. 10(b)

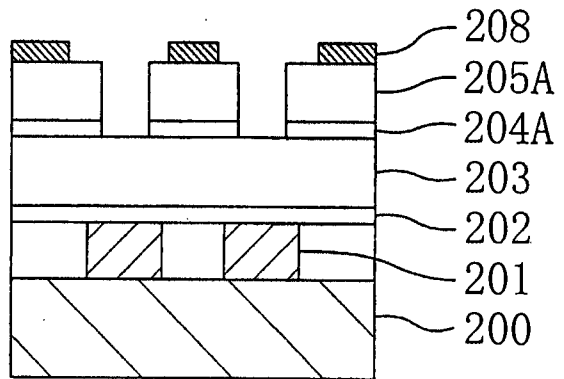
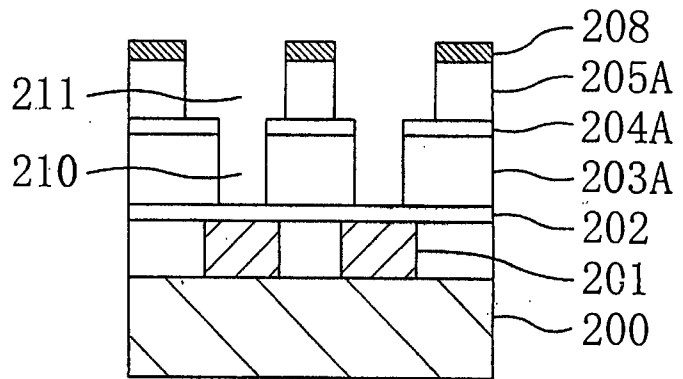


Fig. 10(c)



66250-4FH260



BY	U.S. NO. 35	
DRAFTSMAN	CLASS	SUBCLASS
	438	700

Fig. 11(a)

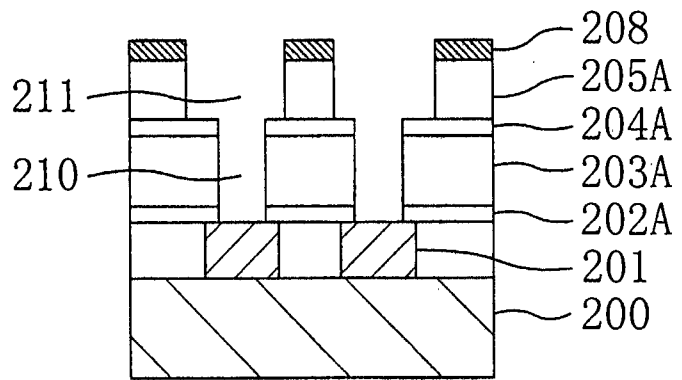


Fig. 11(b)

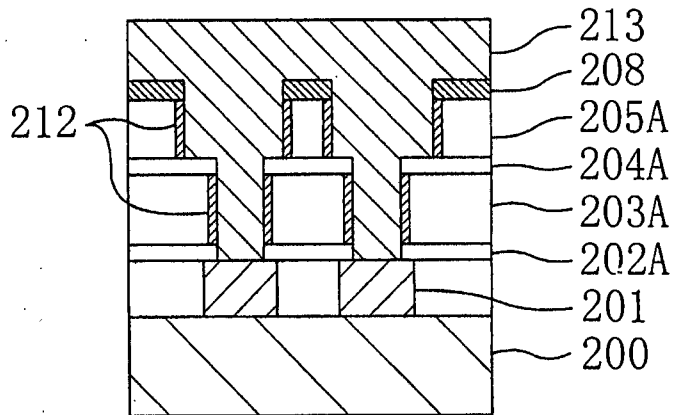
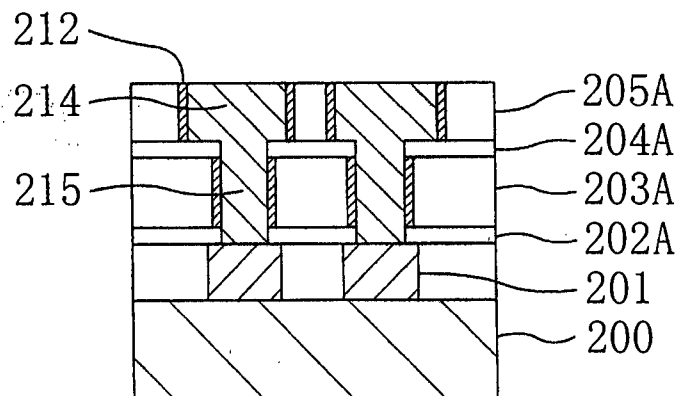


Fig. 11(c)



66220-114250

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 12(a)

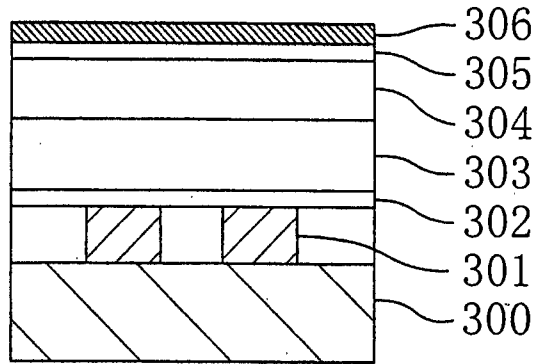


Fig. 12(b)

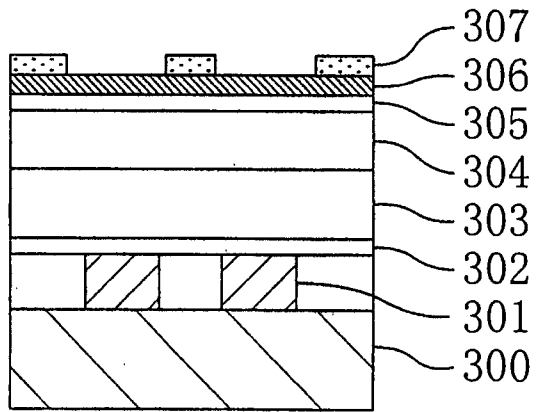
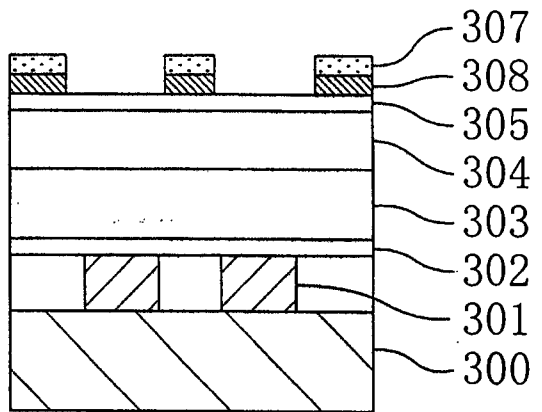


Fig. 12(c)



66260"474250

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 13(a)

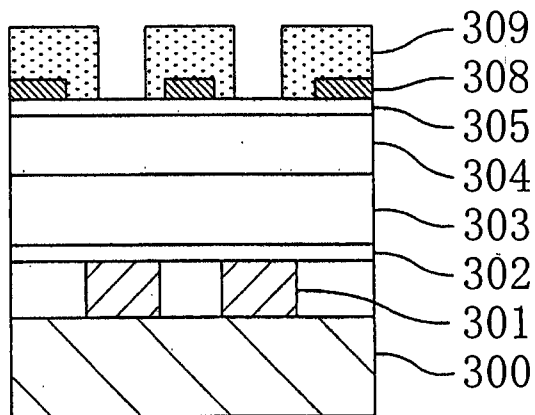


Fig. 13(b)

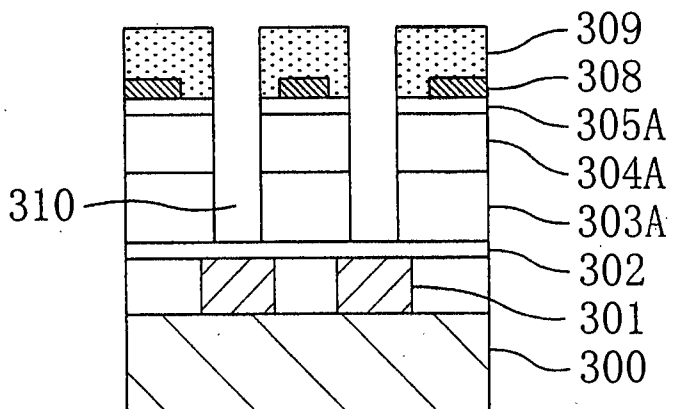
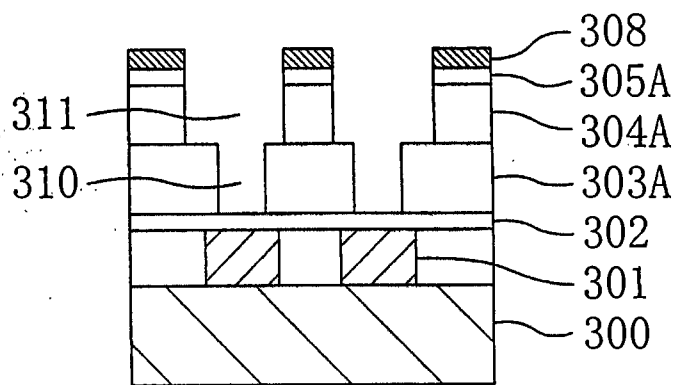


Fig. 13(c)



RECEIVED AT THE 60

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
CRAFTSMAN	438	700

Fig. 14(a)

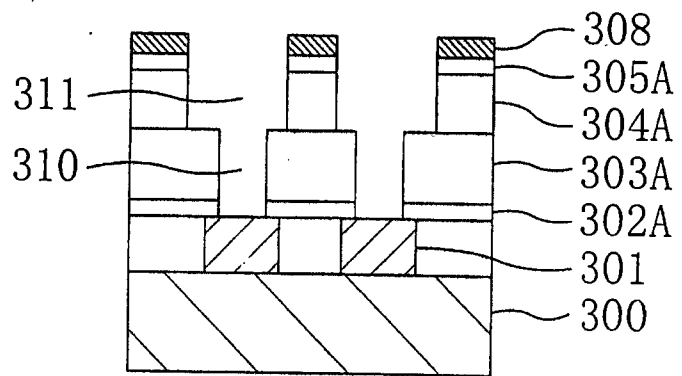


Fig. 14(b)

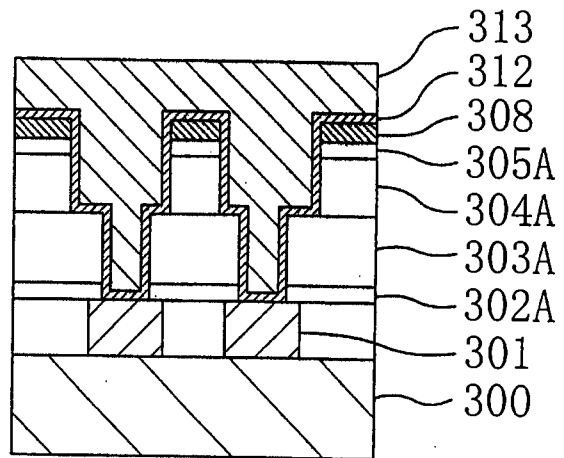
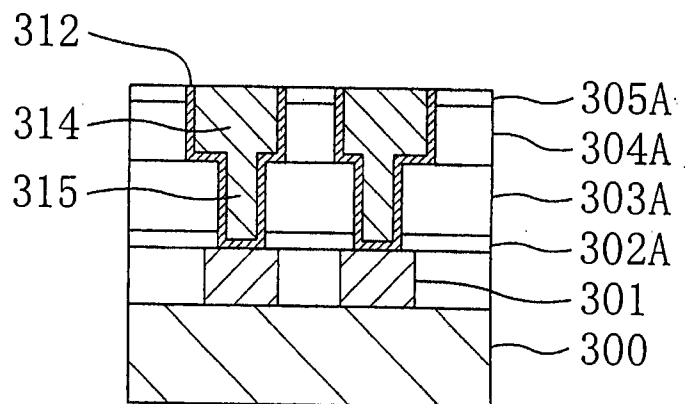


Fig. 14(c)



SECRET 474260

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 15(a)

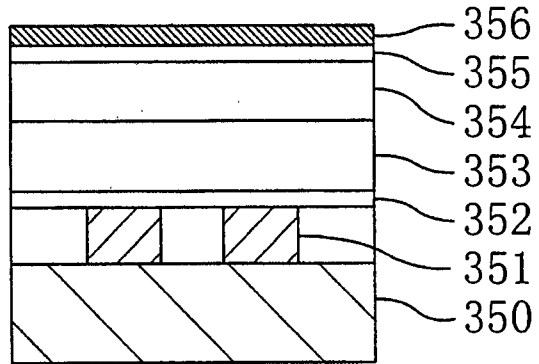


Fig. 15(b)

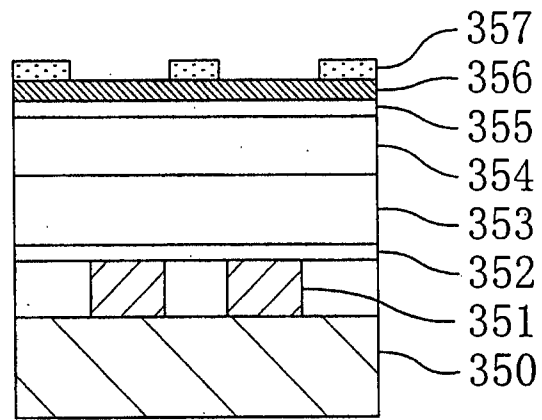
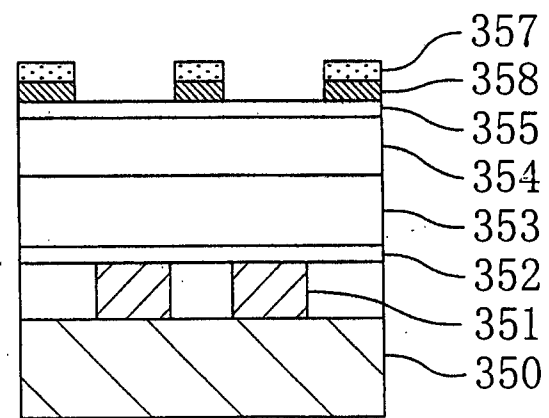


Fig. 15(c)



SEE FIG. 260



APPROVED	O.G. FIG. 36	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 17(a)

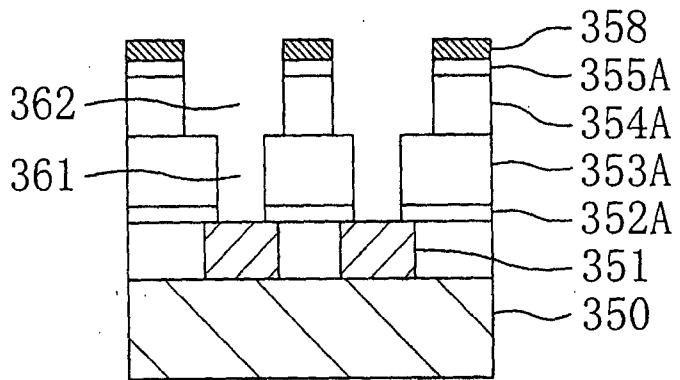


Fig. 17(b)

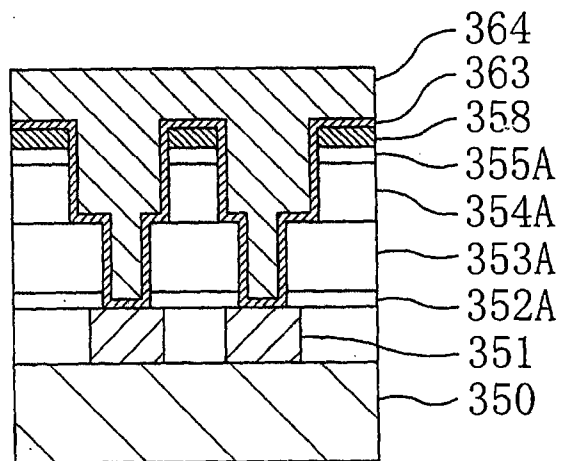
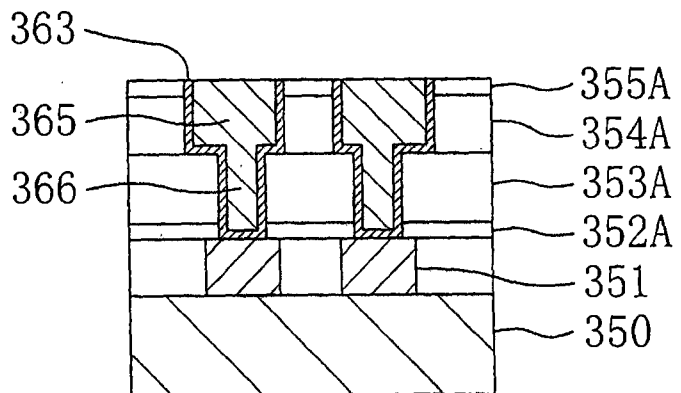


Fig. 17(c)



66250-444250

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 18(a)

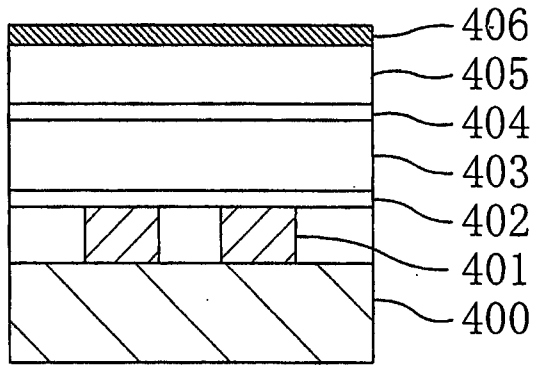


Fig. 18(b)

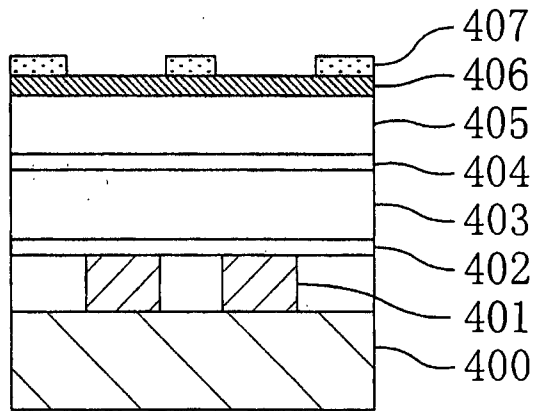
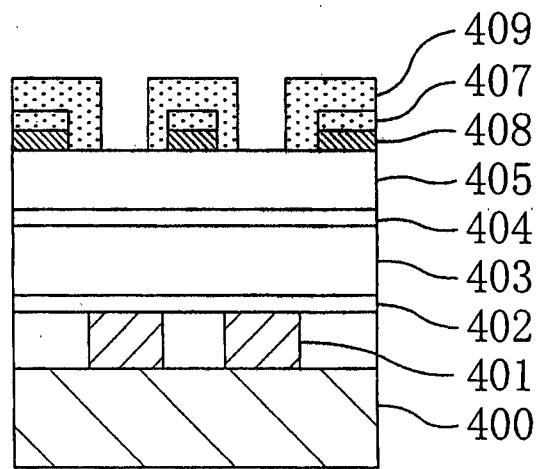


Fig. 18(c)



66250-1114250



APPROVED	O.G. FIG. 36	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 19(a)

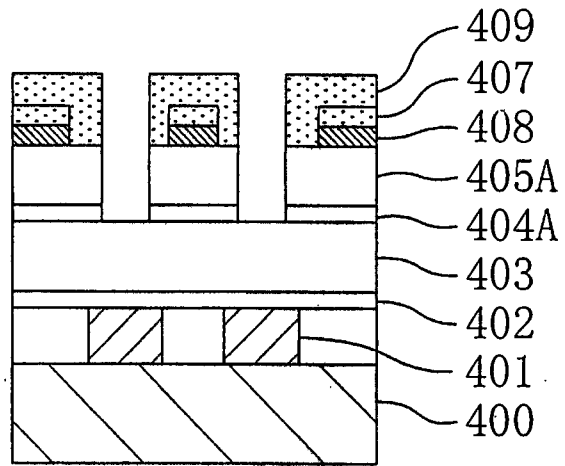


Fig. 19(b)

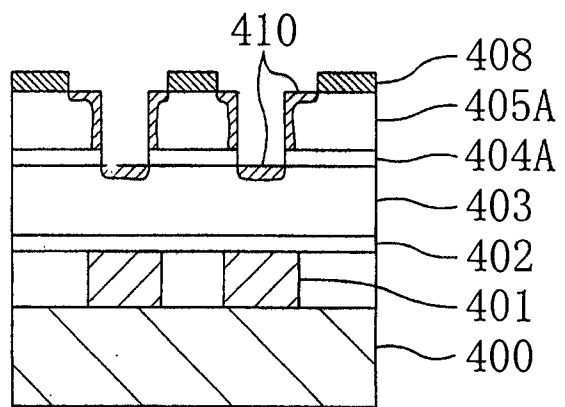
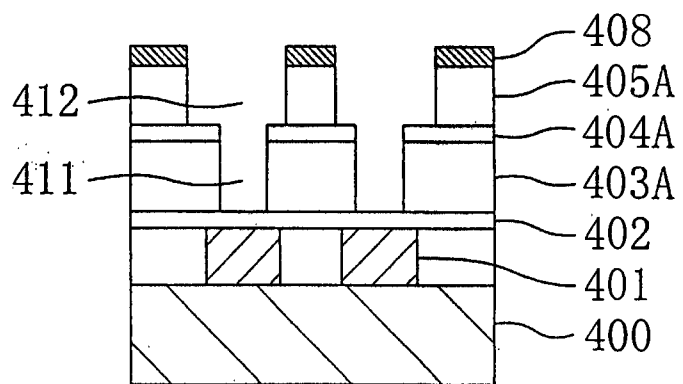


Fig. 19(c)



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APPROVED	O.G. FIG. 36	
BY	CLASS	SUBCLASS
DRAFTSMAN	436	700

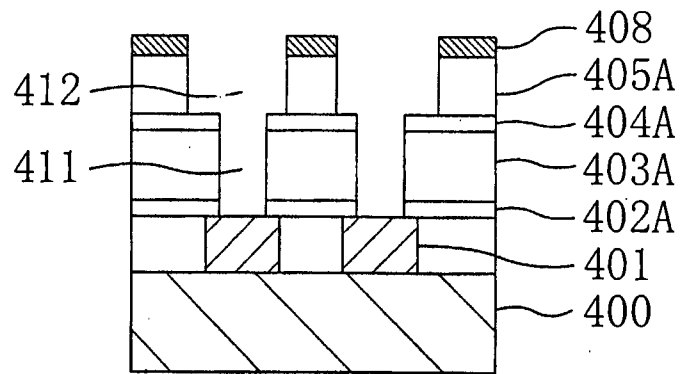


Fig. 20 (a)

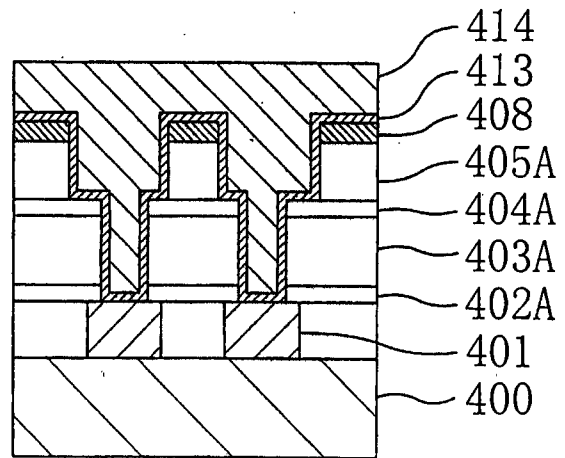


Fig. 20 (b)

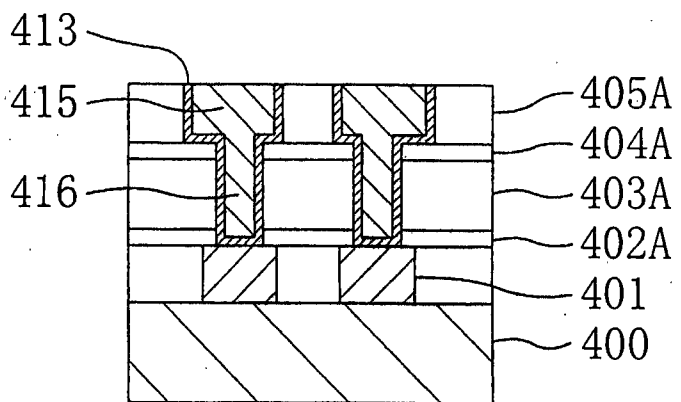


Fig. 20 (c)

09244-0399



APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 22 (a)

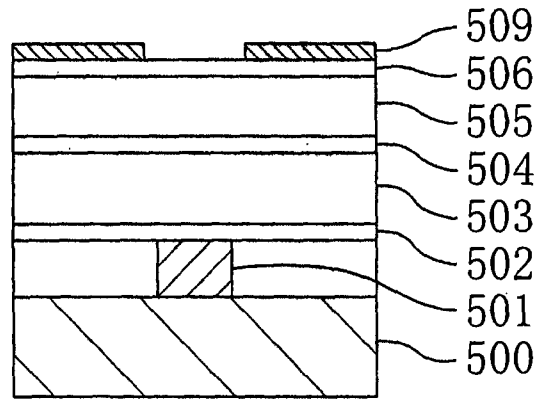


Fig. 22 (b)

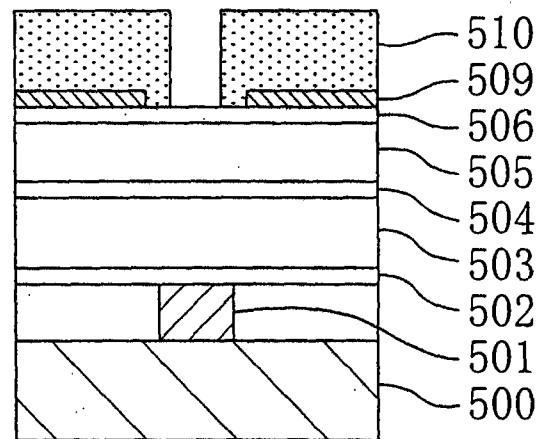
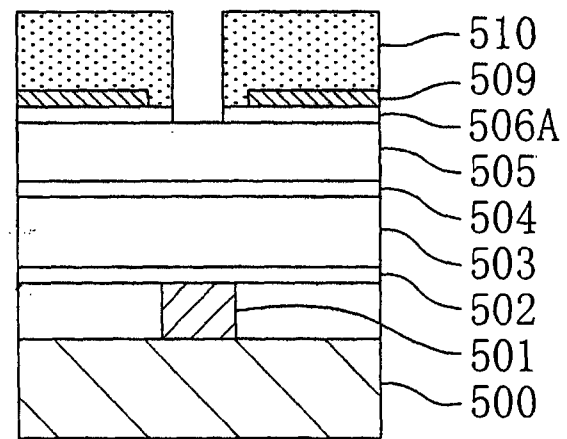


Fig. 22 (c)



66220-474250

APPROVED	C.C. MIZ 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 23(a)

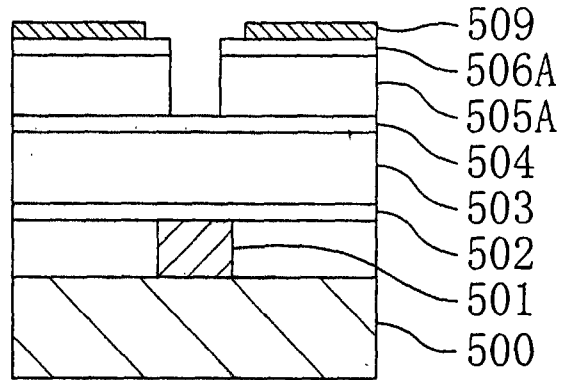


Fig. 23(b)

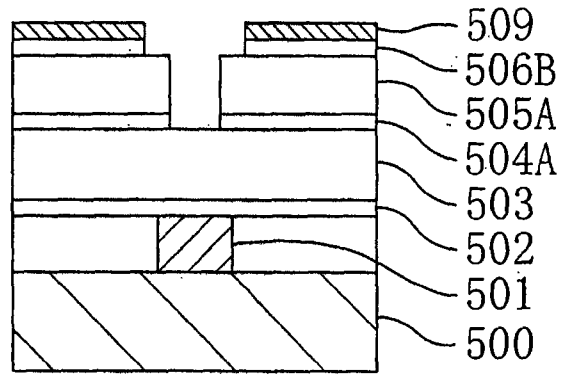


Fig. 23(c)

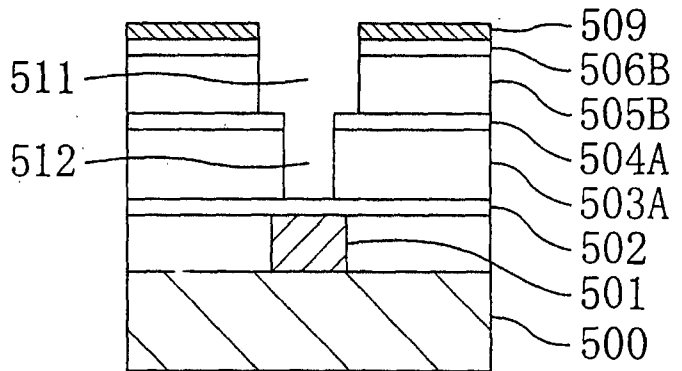
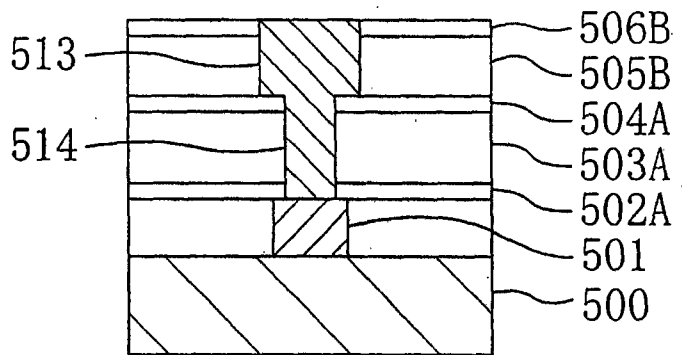


Fig. 23(d)



66250"474260

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
CRAFTSMAN	438	700

Fig. 24(a)

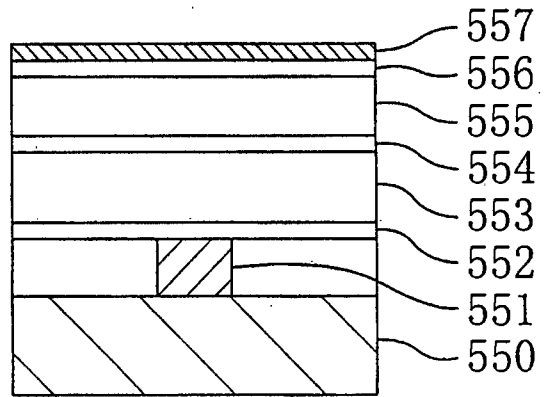


Fig. 24(b)

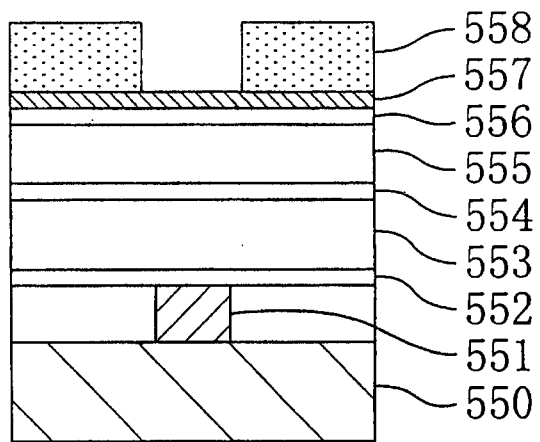
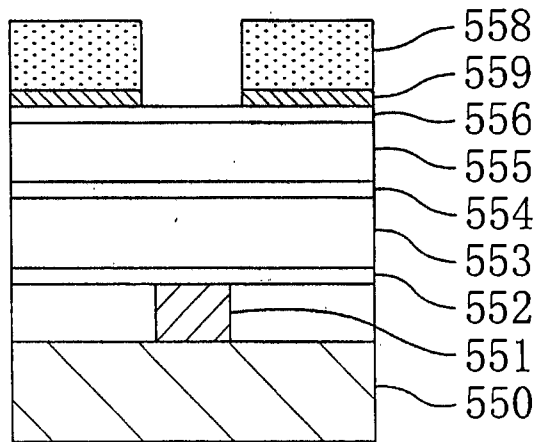


Fig. 24(c)



09244-0388

APPROVED	D.D. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 25(a)

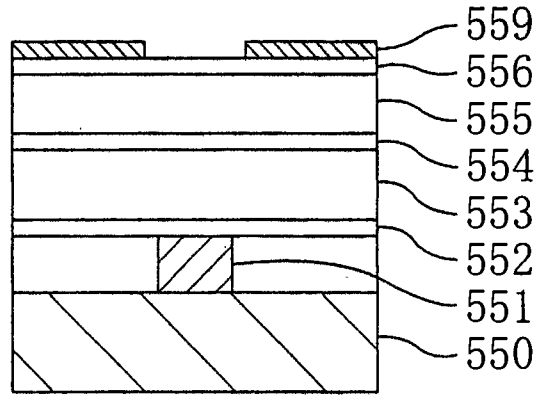


Fig. 25(b)

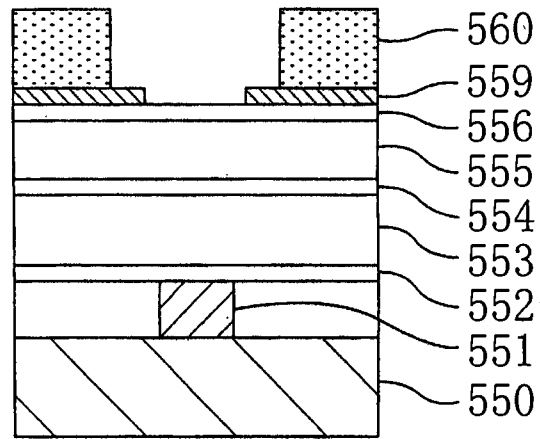
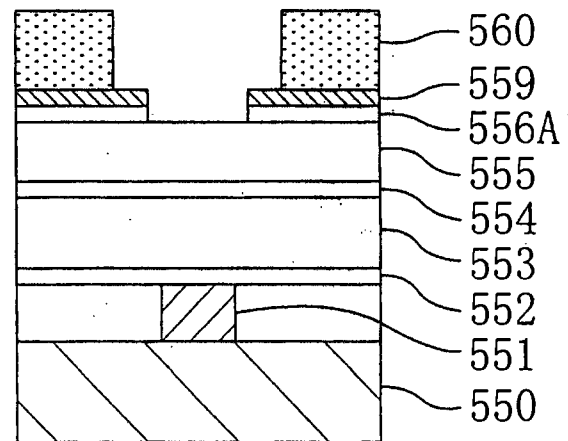


Fig. 25(c)



SUBCLASS 438

APPROVED	O.A. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 26 (a)

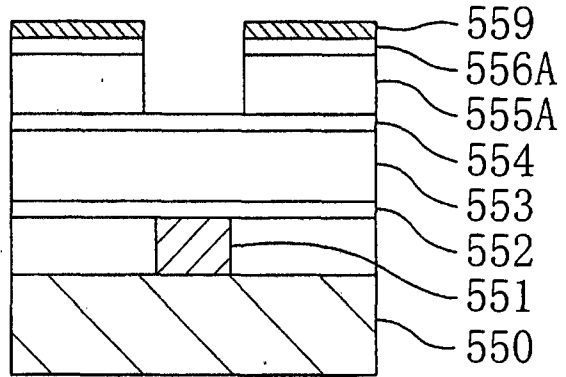


Fig. 26 (b)

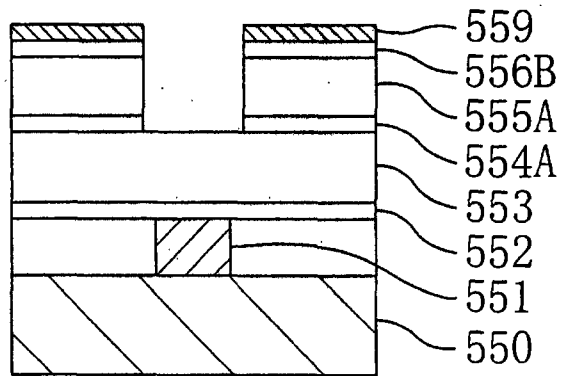


Fig. 26 (c)

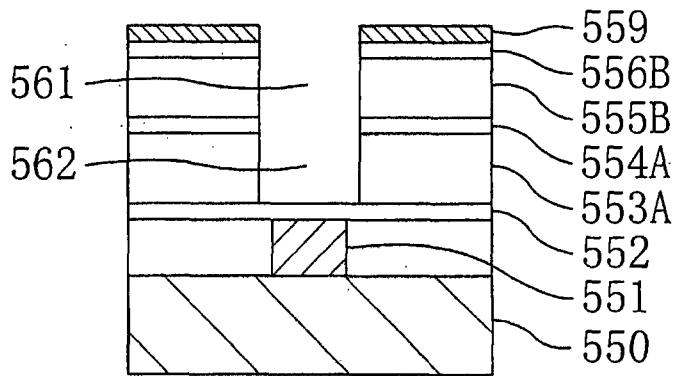
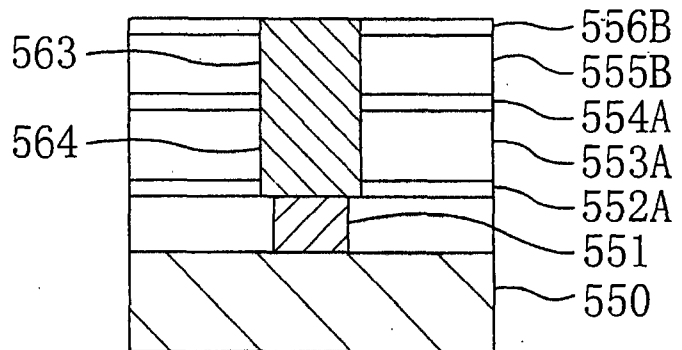


Fig. 26 (d)



09244-0339



APPROVED	D.G. FIG. 2b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 27 (a)

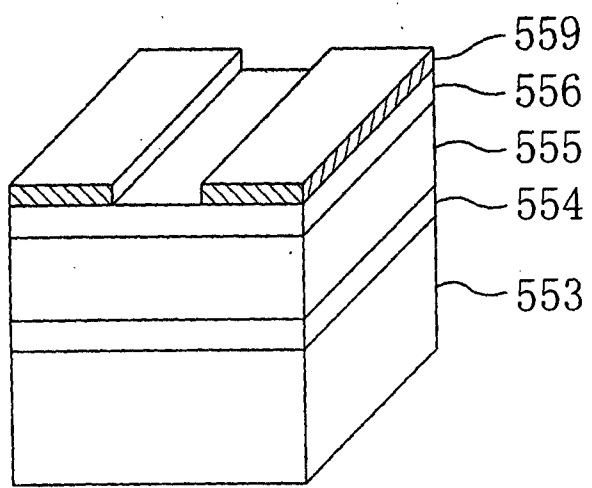
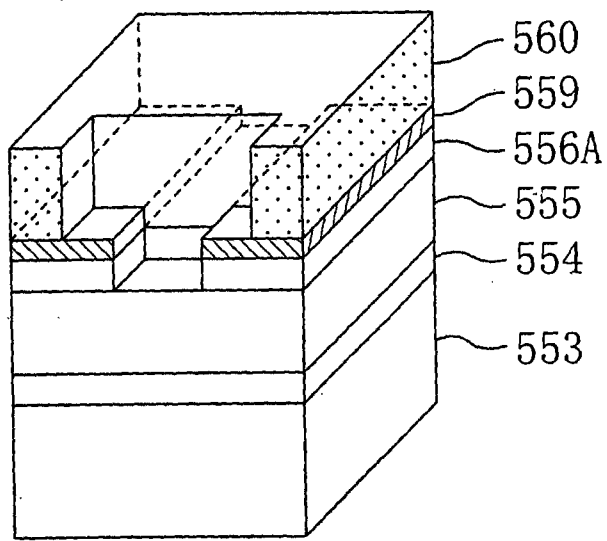


Fig. 27 (b)



66220-474260

APPROVED	D.G. FIG. 36	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 28(a)

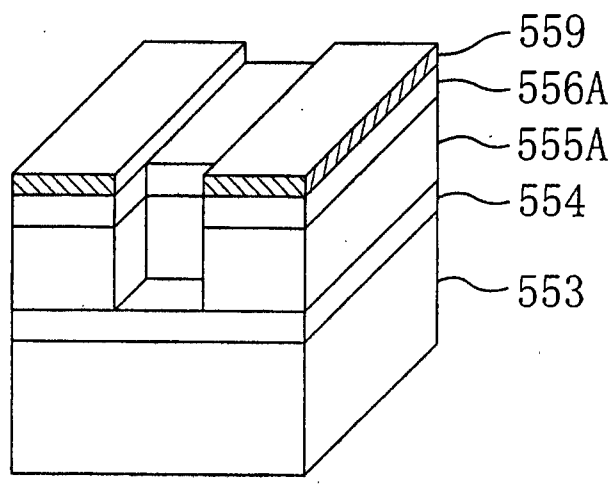
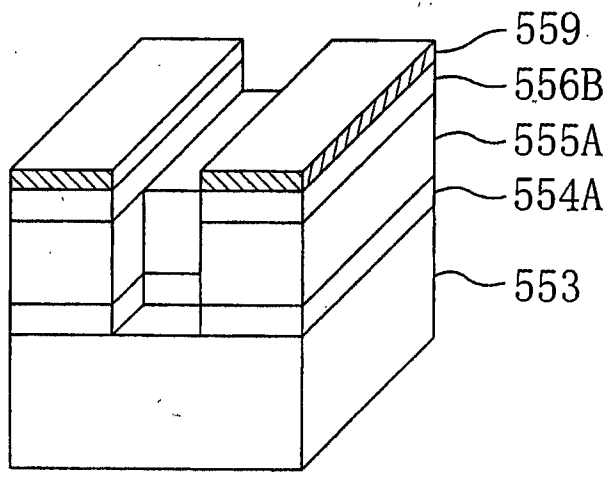


Fig. 28(b)



66260" 474260

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 29 (a)

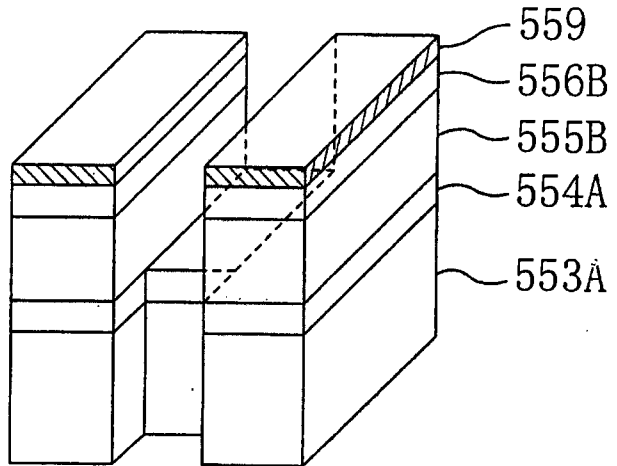
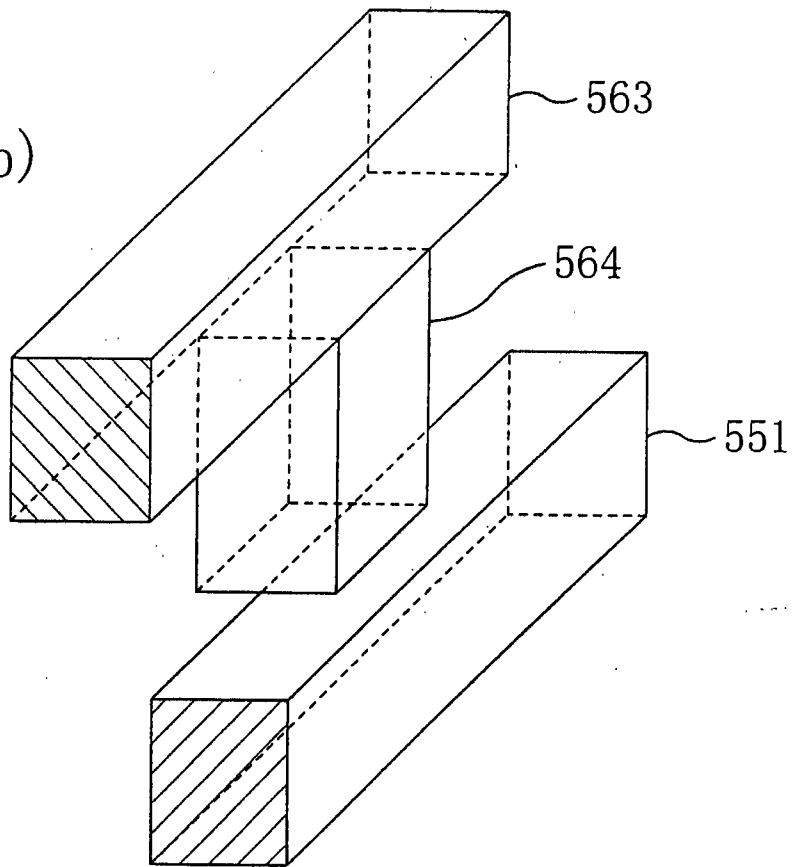


Fig. 29 (b)



66260-474260

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 30 (a)

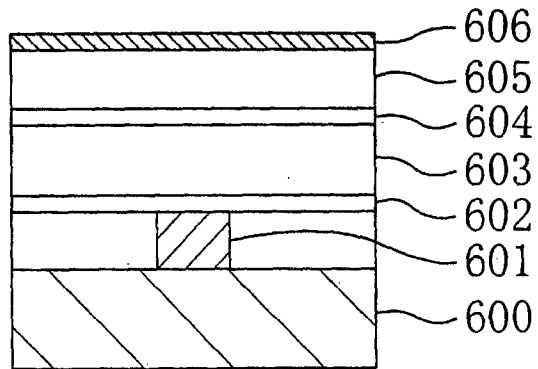


Fig. 30 (b)

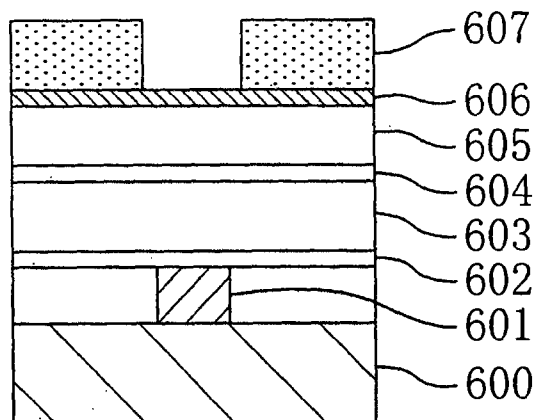
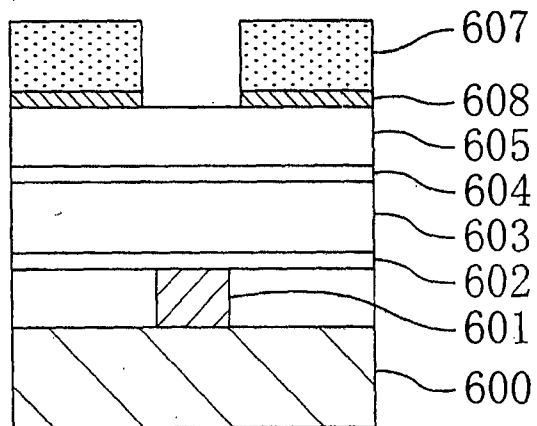


Fig. 30 (c)



66220-474260

APPROVED	O.G. FIG. 3b	
BY	CLASS	SUBCLASS
CRAFTSMAN	438	700

Fig. 31 (a)

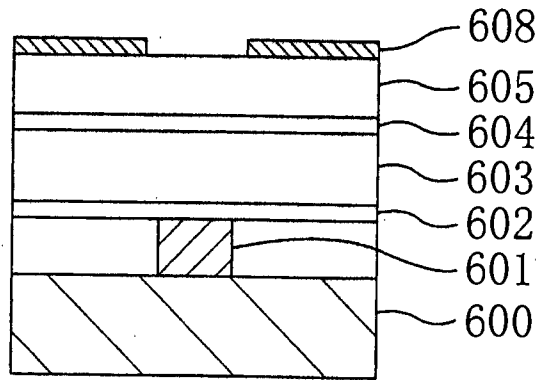


Fig. 31 (b)

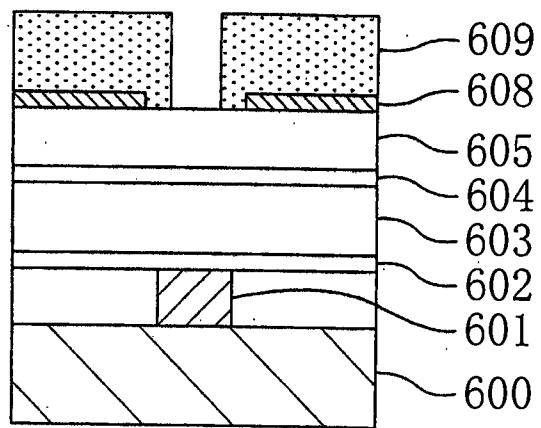
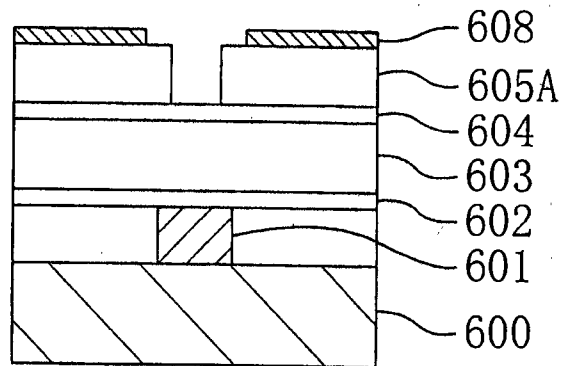


Fig. 31 (c)



65200-1174250

FIG. 3b
CLASS
SUBCLASS
438
700

Fig. 32(a)

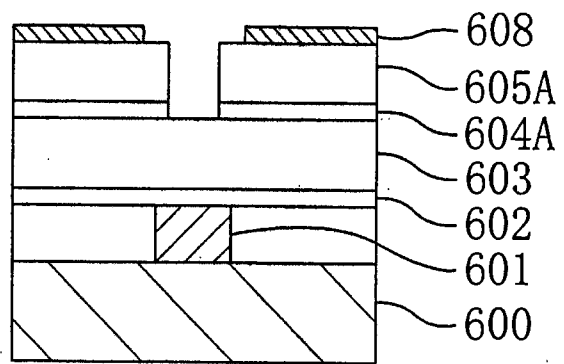


Fig. 32(b)

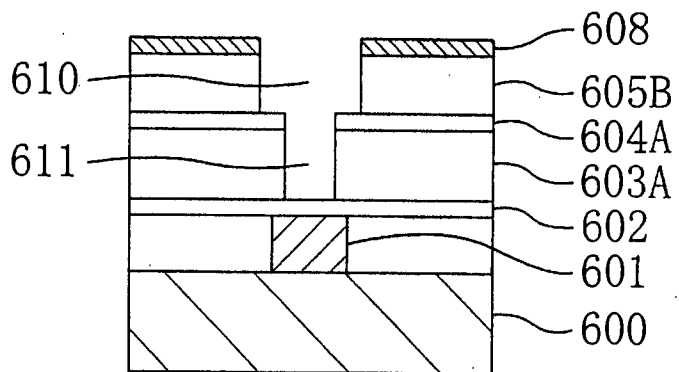
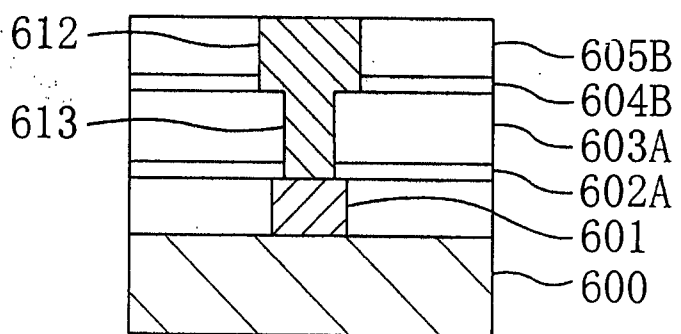


Fig. 32(c)



66320 4774260

APPROVED	J.G. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	900

Fig. 33 (a)

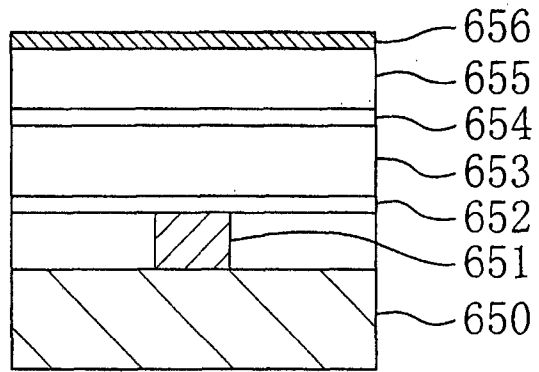


Fig. 33 (b)

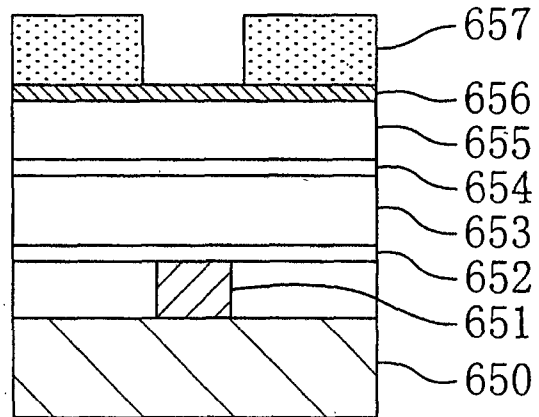
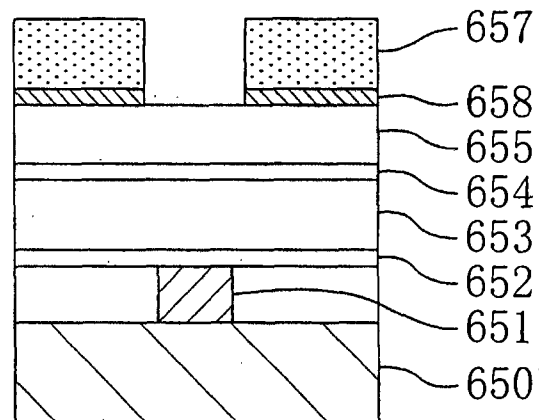


Fig. 33 (c)



092414 09260

APPROVED	D.C. FIG. 3b	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	700

Fig. 34(a)

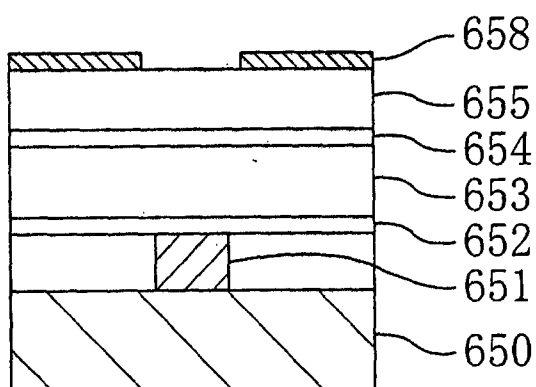


Fig. 34(b)

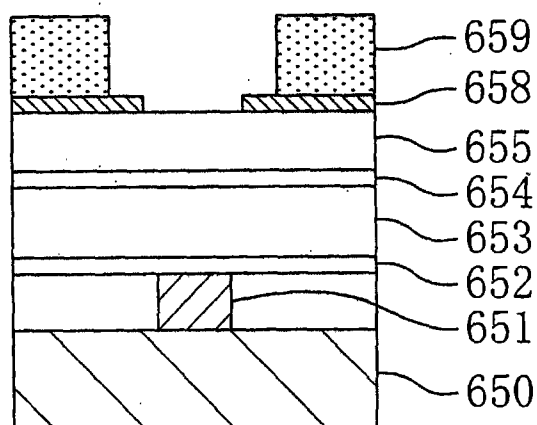
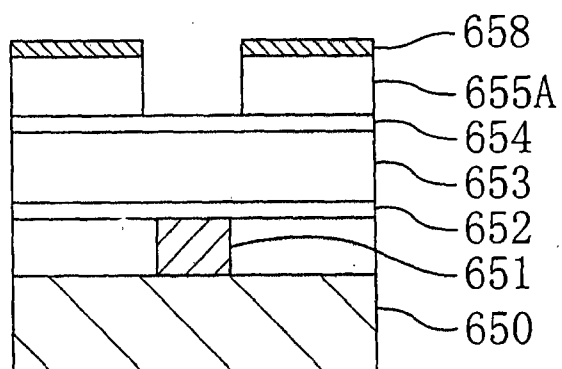


Fig. 34(c)



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APPROVED	FIG. 3b	
BY	CLASS	SUBCLASS
CRAFTSMAN	438	700

Fig. 35(a)

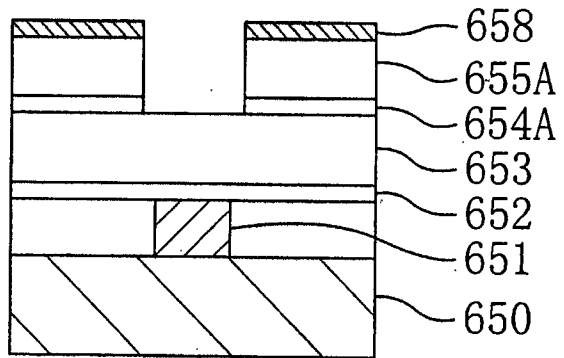


Fig. 35(b)

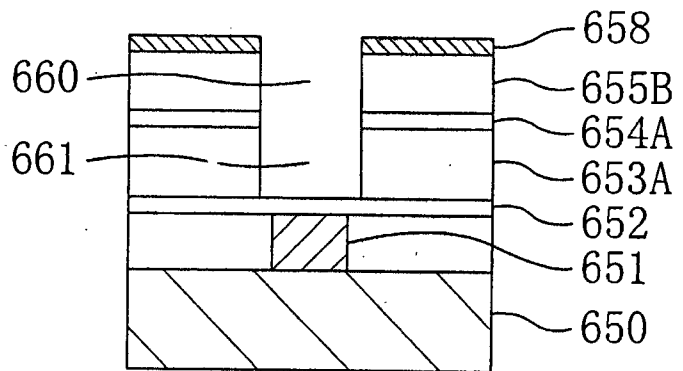
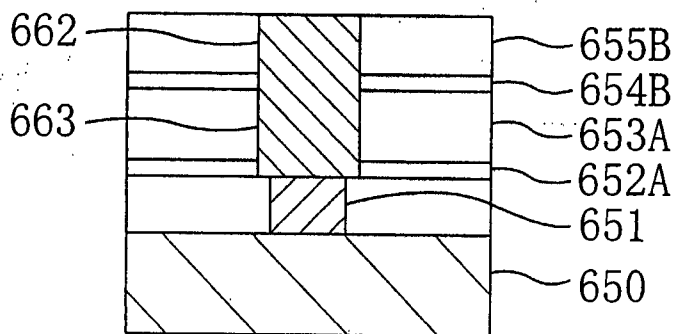


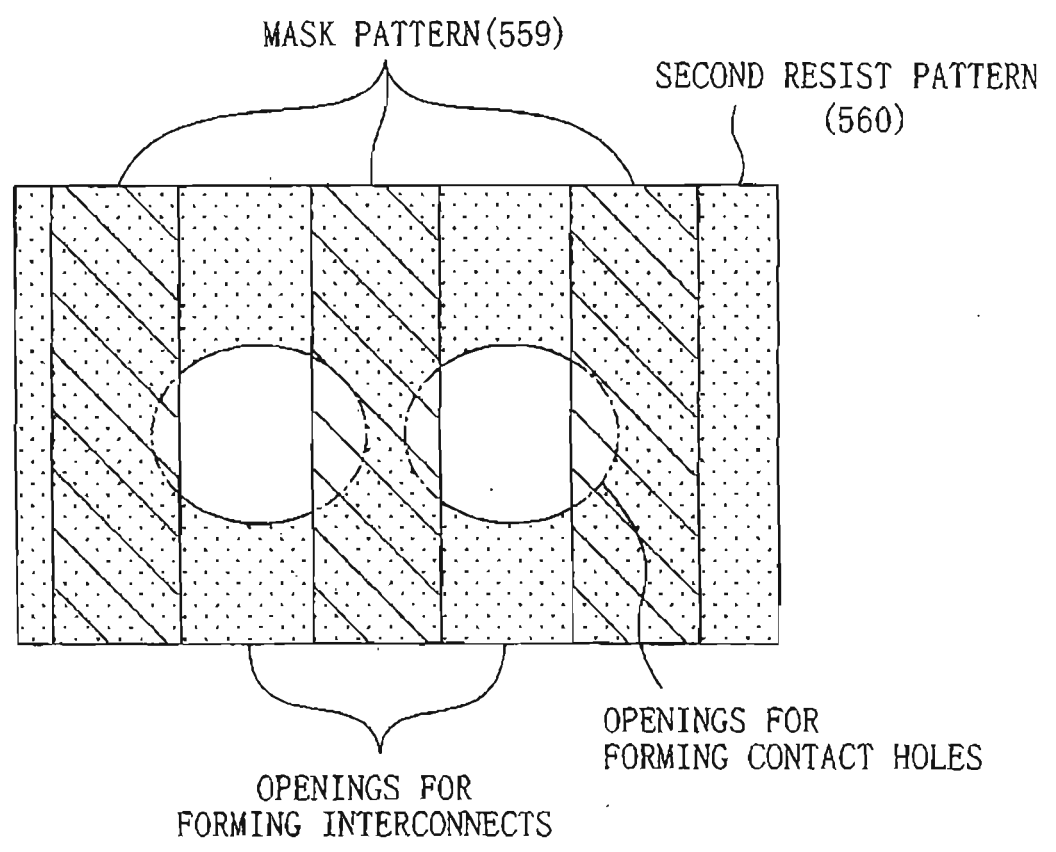
Fig. 35(c)



0927444-03399  
66260-474260

APPROVED	D.R. FIG. 3b	
BY	CLASS	SUBCLASS
DRAGTSMAN	438	700

Fig. 36



66220\*474260

APPROVED	D.G. FIG. 3b	
BY	CLASS	SUBCLASS
CRAFTSMAN	438	700

Fig. 37 (a)

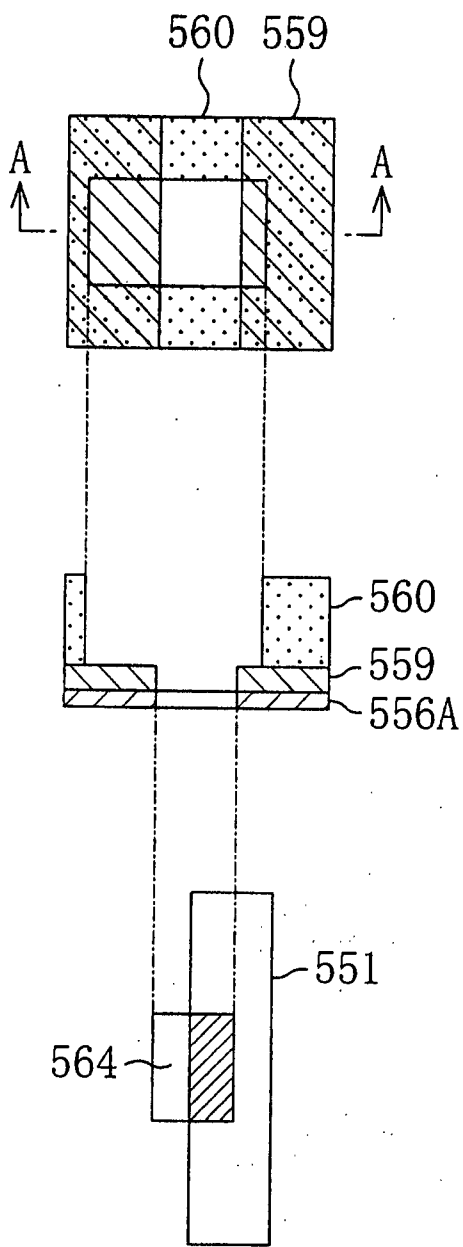
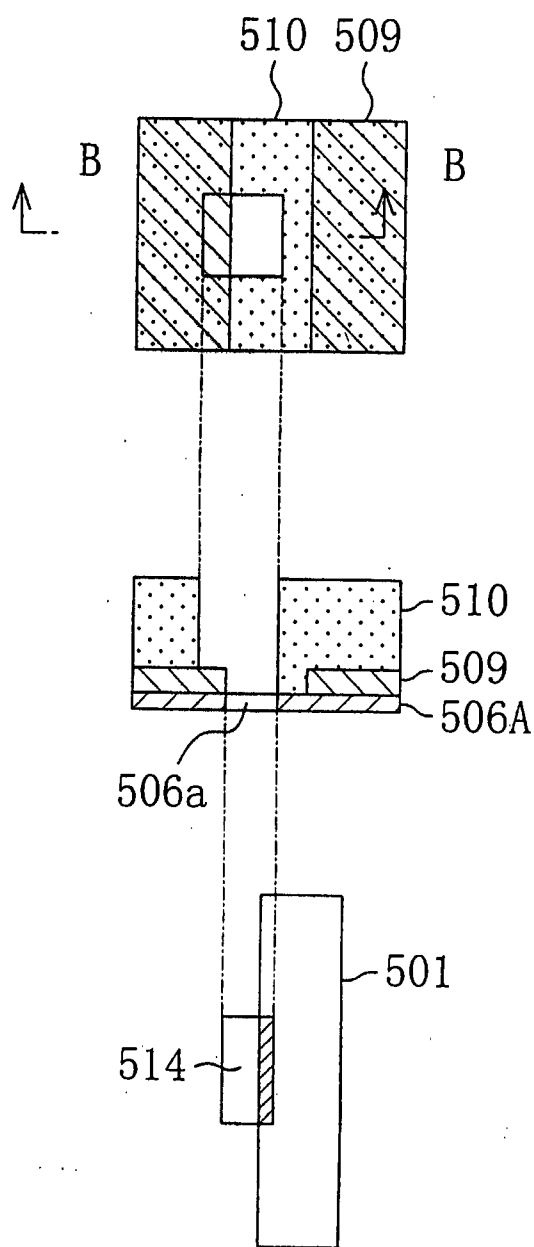


Fig. 37 (b)



66220-4FH260

199-K-033451

### DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.
---------------------

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: METHOD FOR FORMING INTERCONNECTION STRUCTURE, the specification of which is attached hereto unless the following box is checked:

The specification was filed on \_\_\_\_\_  
and was assigned Serial No. \_\_\_\_\_  
(if known)  
and was amended on \_\_\_\_\_  
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s) <small>(Number)</small>	<small>(Country)</small>	<small>(Month/Day/Year Filed)</small>	Priority Claimed	
			Yes	No
10-079371	Japan	03/26/1998	X	

All foreign applications, if any, for any Patent or Inventor's Certificate filed more than 12 months prior to the filing date of this application:

Country	Application No.	Date of Filing (Month/Day/Year)

092444-033451

I hereby claim the benefit under Title 35, United States Code, §119(e) or §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status: patented, pending, abandoned

I hereby appoint the following attorneys to prosecute this application and/or any international application and to transact all business in the Patent and Trademark Office connected therewith:

- |                                          |                                           |
|------------------------------------------|-------------------------------------------|
| Daniel W. Sixbey, (Reg. No. 20,932)      | Stuart J. Friedman (Reg. No. 24,312)      |
| Charles M. Leedom, Jr. (Reg. No. 26,477) | Gerald J. Ferguson, Jr. (Reg. No. 23,016) |
| David S. Safran (Reg. No. 27,997)        | Thomas W. Cole (Reg. No. 28,290)          |
| Donald R. Studebaker (Reg. No. 32,815)   | Jeffrey L. Costellia (Reg. No. 35,483)    |
| Tim L. Brackett (Reg. No. 36,092)        | Eric J. Robinson (Reg. No. 38,285)        |
| Frank P. Presta (Reg. No. 19,828)        | Joseph S. Presta (Reg. No. 35,329)        |
| Robert M. Schulman (Reg. No. 31,196)     | Thomas M. Blasey (Reg. No. 33,475)        |
| Lawrence D. Eisen (Reg. No. 41,009)      | Daniel S. Song (Reg. No. 43,143)          |
| Marc S. Kaufman (Reg. No. 35,212)        |                                           |

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The undersigned hereby authorize any U.S. attorney or agent named herein to accept and follow instructions from MAEDA PATENT OFFICE as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

FULL NAME OF SOLE OR FIRST INVENTOR Nobuo AOI	INVENTOR'S SIGNATURE <i>Nobuo AOI</i>	DATE March 19, '99
RESIDENCE (City, State & Country) Hyogo, Japan	CITIZENSHIP Japan	
POST OFFICE ADDRESS (Complete Address including City, State & Country) 1-41-403, Taisha-cho, Nishinomiya-shi, Hyogo 662-0867, Japan		

656210-4-1-1-2-50

# Application Assignment Record

According to the application transmittal letter, an assignment recording ownership was filed with this application; however, a copy of this record was not located in the original file history record obtained from the United States Patent and Trademark Office. Upon your request, we will attempt to obtain the assignment documents from the Assignment Recordation Branch of the United States Patent and Trademark Office or from a related application case (if applicable). Please note that additional charges will apply for this service.

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

GP 1763

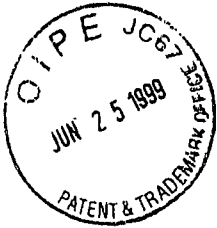
CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on June 23, 1999.

Docket No.: 0819-226

Cecilia Campbell  
Cecilia Campbell

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re PATENT application of )  
Nobuo AOI )  
Serial No. 09/274,114 ) Art Unit 1763  
Filed: March 23, 1999 )  
For: METHOD FOR FORMING )  
INTERCONNECTION STRUCTURE ) June 23, 1999

#2

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GROUP 1700

TRANSMITTAL OF CERTIFIED PRIORITY DOCUMENT

Honorable Assistant Commissioner for Patents

Washington, D. C. 20231

Sir:

At the time of filing the above-referenced application, a right of priority under 35 USC 119 was claimed in view of Application No. 10-079371, filed March 26, 1998 in Japan.

Submitted herewith is the certified copy of the priority document to perfect the claim for priority.

Acknowledgment is respectfully requested.

Respectfully submitted,

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Registration No. 38,285  
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日本国特許庁  
PATENT OFFICE  
JAPANESE GOVERNMENT

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日  
Date of Application: 1998年 3月26日

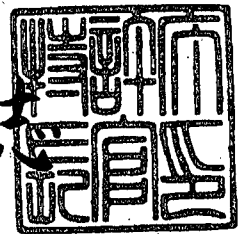
出願番号  
Application Number: 平成10年特許願第079371号

出願人  
Applicant(s): 松下電器産業株式会社

1999年 4月 9日

特許庁長官  
Commissioner,  
Patent Office

伊佐山 建



出証番号 出証特平11-3021681



特平 10-079371

【書類名】 特許願  
【整理番号】 7411290311  
【提出日】 平成10年 3月26日  
【あて先】 特許庁長官 殿  
【国際特許分類】 H01L 21/316  
【発明の名称】 配線構造体の形成方法  
【請求項の数】 9  
【発明者】  
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会社内  
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【識別番号】 100107445  
【弁理士】  
【氏名又は名称】 小根田 一郎  
【手数料の表示】  
【予納台帳番号】 014409  
【納付金額】 21,000円

1 出証特平 11-3021681

特平10-079371

【提出物件の目録】

【物件名】 明細書 1

【物件名】 図面 1

【物件名】 要約書 1

【包括委任状番号】 9601026

【プルーフの要否】 要

【書類名】 明細書

【発明の名称】 配線構造体の形成方法

【特許請求の範囲】

【請求項1】 下層の金属配線の上に第1の絶縁膜を形成する第1の工程と、  
前記第1の絶縁膜の上に該第1の絶縁膜と組成が異なる第2の絶縁膜を形成する第2の工程と、

前記第2の絶縁膜の上に該第2の絶縁膜と組成が異なる第3の絶縁膜を形成する第3の工程と、

前記第3の絶縁膜の上に導電性膜を形成する第4の工程と、

前記導電性膜の上に、配線形成用開口部を有する第1のレジストパターンを形成する第5の工程と、

前記導電性膜に対して前記第1のレジストパターンをマスクとしてエッチングを行なって、前記導電性膜からなり配線形成用開口部を有するマスクパターンを形成する第6の工程と、

前記第3の絶縁膜の上に、コンタクトホール形成用開口部を有する第2のレジストパターンを形成する第7の工程と、

前記第3の絶縁膜、第1のレジストパターン及び第2のレジストパターンに対するエッチングレートが高い一方、前記第2の絶縁膜に対するエッチングレートが低いエッチング条件で、前記第3の絶縁膜に対してドライエッチングを行なうことにより、前記第3の絶縁膜を該第3の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化すると共に、前記第1のレジストパターン及び第2のレジストパターンを全面的に又は下部を残して除去する第8の工程と、

前記第2の絶縁膜に対するエッチングレートが高い一方、前記第1の絶縁膜及び第3の絶縁膜に対するエッチングレートが低いエッチング条件で、前記第2の絶縁膜に対してパターン化された前記第3の絶縁膜をマスクとしてドライエッチングを行なうことにより、前記第2の絶縁膜を該第2の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第9の工程と、

前記第1の絶縁膜及び第3の絶縁膜に対するエッチングレートが高い一方、前記マスクパターン及び第2の絶縁膜に対するエッチングレートが低いエッチング

条件で、前記第3の絶縁膜に対して前記マスクパターンをマスクとしてドライエッチングを行なうと共に前記第1の絶縁膜に対してパターン化された前記第2の絶縁膜をマスクとしてドライエッチングを行なうことにより、前記第3の絶縁膜に配線溝を形成すると共に前記第1の絶縁膜にコンタクトホールを形成する第10の工程と、

前記配線溝及びコンタクトホールに金属膜を充填することにより、上層の金属配線及び前記下層の金属配線と前記上層の金属配線とを接続するコンタクトを形成する第11の工程とを備えていることを特徴とする配線構造体の形成方法。

【請求項2】 前記第10の工程と前記第11の工程との間に、前記第3の絶縁膜における前記配線溝に露出している部分及び前記第1の絶縁膜における前記コンタクトホールに露出している部分に金属膜からなる密着層を形成する工程をさらに備えていることを特徴とする請求項1に記載の配線構造体の形成方法。

【請求項3】 前記第3の絶縁膜は有機成分を主成分とすることを特徴とする請求項1に記載の配線構造体の形成方法。

【請求項4】 前記第3の工程は、パーフルオロデカリンを含む反応性ガスを用いるCVD法により前記第3の絶縁膜を形成する工程を含むことを特徴とする請求項3に記載の配線構造体の形成方法。

【請求項5】 前記第1の絶縁膜は有機成分を主成分とすることを特徴とする請求項3に記載の配線構造体の形成方法。

【請求項6】 前記第10の工程と前記第11の工程との間に、前記第3の絶縁膜における前記配線溝に露出している部分及び前記第1の絶縁膜における前記コンタクトホールに露出している部分に、窒素を含有する反応性ガスを用いるプラズマ処理によって密着層を形成する工程をさらに備えていることを特徴とする請求項5に記載の配線構造体の形成方法。

【請求項7】 前記第1の工程は、パーフルオロデカリンを含む反応性ガスを用いるCVD法により前記第3の絶縁膜を形成する工程を含むことを特徴とする請求項3に記載の配線構造体の形成方法。

【請求項8】 下層の金属配線の上に第1の絶縁膜を形成する第1の工程と、前記第1の絶縁膜の上に該第1の絶縁膜と組成が異なる第2の絶縁膜を形成す

る第2の工程と、

前記第2の絶縁膜の上に該第2の絶縁膜と組成が異なる第3の絶縁膜を形成する第3の工程と、

前記第3の絶縁膜の上に導電性膜を形成する第4の工程と、

前記導電性膜の上に、配線形成用開口部を有する第1のレジストパターンを形成する第5の工程と、

前記導電性膜に対して前記第1のレジストパターンをマスクとしてエッチングを行なって、前記導電性膜からなり配線形成用開口部を有するマスクパターンを形成する第6の工程と、

前記第3の絶縁膜の上に、コンタクトホール形成用開口部を有する第2のレジストパターンを形成する第7の工程と、

前記第3の絶縁膜に対するエッチングレートが高い一方、前記第2の絶縁膜、第1のレジストパターン及び第2のレジストパターンに対するエッチングレートが低いエッチング条件で、前記第3の絶縁膜に対して前記第1のレジストパターン及び第2のレジストパターンをマスクとしてドライエッチングを行なうことにより、前記第3の絶縁膜を該第3の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第8の工程と、

前記第2の絶縁膜に対するエッチングレートが高い一方、前記第1の絶縁膜、第3の絶縁膜、第1のレジストパターン及び第2のレジストパターンに対するエッチングレートが低いエッチング条件で、前記第2の絶縁膜に対して前記第1のレジストパターン及び第2のレジストパターンをマスクとしてドライエッチングを行なうことにより、前記第2の絶縁膜を該第2の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第9の工程と、

前記第1のレジストパターン及び第2のレジストパターンを除去する第10の工程と、

前記第1の絶縁膜及び第3の絶縁膜に対するエッチングレートが高い一方、前記マスクパターン及び第2の絶縁膜に対するエッチングレートが低いエッチング条件で、前記第3の絶縁膜に対して前記マスクパターンをマスクとしてドライエッチングを行なうと共に前記第1の絶縁膜に対してパターン化された前記第2の

絶縁膜をマスクとしてドライエッチングを行なうことにより、前記第3の絶縁膜に配線溝を形成すると共に前記第1の絶縁膜にコンタクトホールを形成する第11の工程と、

前記配線溝及びコンタクトホールに金属膜を充填することにより、上層の金属配線及び前記下層の金属配線と前記上層の金属配線とを接続するコンタクトを形成する第12の工程とを備えていることを特徴とする配線構造体の形成方法。

【請求項9】 前記第3の絶縁膜は、シロキサン骨格を有する低誘電率SOG膜であることを特徴とする請求項8に記載の配線構造体の形成方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】

本発明は半導体集積回路装置における配線構造体の形成方法に関する。

【0002】

【従来の技術】

半導体集積回路の高集積化の進展に伴い、金属配線同士の間寄生容量である配線間容量の増加に起因する配線遅延時間の増大が半導体集積回路の高性能化の妨げとなっている。配線遅延時間は金属配線の抵抗と配線間容量との積に比例するいわゆるRC遅延と言われるものである。

【0003】

従って、配線遅延時間を低減するためには、金属配線の抵抗を小さくするか又は配線間容量を小さくすることが必要である。

【0004】

そこで、配線抵抗を小さくために、配線材料としてアルミ系合金に代えて銅を用いる半導体集積回路装置がIBM社やモトローラ社から報告されている。銅材料はアルミ系合金材料の3分の2程度の比抵抗を有しているため、配線材料として銅材料を用いると、アルミ系合金材料を用いる場合に比べて、単純に計算すると配線遅延時間が3分の2に減少するので、1.5倍の高速化を実現することができる。

【0005】

しかしながら、半導体集積回路の高集積化がさらに進展すると、銅からなる金属配線を用いる場合でも、配線遅延時間の増大によって、高速化が限界に達すると懸念されている。また、配線材料としての銅は、金又は銀について比抵抗が小さいので、銅からなる金属配線に代えて金又は銀からなる金属配線を用いても、配線抵抗の低減は僅かなものである。

【0006】

このため、半導体集積回路の高集積化のためには、配線抵抗の低減と共に配線間容量の低減が重要になっており、配線間容量の低減のためには、層間絶縁膜の比誘電率を小さくすることが必要である。従来、層間絶縁膜としては、シリコン酸化膜が用いられているが、シリコン酸化膜の比誘電率は4~4.5程度であって、より高集積化された半導体集積回路における層間絶縁膜には採用し難いという問題がある。

【0007】

そこで、比誘電率がシリコン酸化膜よりも小さい層間絶縁膜として、フッ素添加シリコン酸化膜、低誘電率SOG膜及び有機高分子膜が提案されている。

【0008】

【発明が解決しようとする課題】

ところで、フッ素添加シリコン酸化膜の比誘電率は3.3~3.7であって、従来のシリコン酸化膜に比べて2割程度小さいが、フッ素添加シリコン酸化膜は、吸湿性が高いので大気中の水分を吸収しやすい。このため、フッ素添加シリコン酸化膜が水分を吸収して、比誘電率の高いSiOHが膜中に取り込まれるので、フッ素添加シリコン酸化膜の比誘電率が増加したり、熱処理工程においてSiOHが反応してH<sub>2</sub>Oガスを放出したりするという問題、及びフッ素添加シリコン酸化膜中に遊離しているフッ素が熱処理工程において表面に偏析し、偏析したフッ素が密着層としてのTiN膜のTi等と反応して剥がれやすいTiF膜を形成するという問題等があり、フッ素添加シリコン酸化膜は実用上の課題が多い。

【0009】

低誘電率SOG膜としては、HSQ (Hydrogen silsesquioxane: Si原子と

、O原子と、O原子の数の3分の2の数のH原子とからなる構造体)膜が検討されているが、HSQ膜は、従来のシリコン酸化膜に比べて、水分放出量が多いので加工性が悪いという問題がある。HSQ膜は加工性が悪いためHSQ膜に埋め込み配線を形成することは困難であるから、HSQ膜に金属配線を形成する場合には金属膜がパターン化されてなる金属配線を用いる必要がある。

【0010】

また、HSQ膜は金属配線との密着性が低いので、金属配線との密着性を確保するために金属配線との間に密着層としてのCVD酸化膜を形成する必要がある。ところが、金属配線の上にCVD酸化膜を形成すると、金属配線間に比誘電率の大きいCVD酸化膜が存在するため、実質的な配線間容量はHSQ膜とCVD酸化膜とから構成される直列容量になるので、HSQ膜を単体で用いた場合に比べて配線間容量が大きくなってしまいう問題がある。

【0011】

有機高分子膜は、低誘電率SOG膜と同様、金属配線との密着性が低いので、金属配線との間に密着層としてのCVD酸化膜を形成する必要がある。

【0012】

また、有機高分子膜に対するエッチングレートが酸素プラズマによりレジストパターンをアッシングする際のアッシングレートとほぼ等しいため、レジストパターンをアッシングにより除去する際に有機高分子膜がダメージを受けるので、通常のリジストプロセスが使えないという問題がある。そこで、有機高分子膜の上にCVD酸化膜を形成した後、該CVD酸化膜の上にレジスト膜を形成し、CVD酸化膜をエッチングストッパー(保護膜)としてレジスト膜をエッチング加工する方法が提案されている。

【0013】

ところが、有機高分子膜の上にCVD酸化膜を形成する際、有機高分子膜の表面が酸素を含む反応性ガスに曝されるため、有機高分子膜が酸素と反応して有機高分子膜中にカルボニル基やケトン基等の極性基が導入されるので、有機高分子膜の比誘電率が増加してしまいう問題がある。



【0014】

また、有機高分子膜に銅の埋め込み配線を形成する場合、有機高分子膜は金属配線との密着性が低いため、有機高分子膜に形成された配線用凹部の周面に例えばTiN等からなる密着層を形成する必要があるが、TiN膜は抵抗が高いため金属配線の有効断面積が減少してしまうので、銅からなる金属配線を用いて低抵抗化を図ったメリットが損なわれてしまうという問題がある。

【0015】

前記に鑑み、本発明は、通常のレジストプロセスを採用して、比誘電率が低い層間絶縁膜を形成できるようにすることを目的とする。

【0016】

【課題を解決するための手段】

本発明に係る第1の配線構造体の形成方法は、下層の金属配線の上に第1の絶縁膜を形成する第1の工程と、第1の絶縁膜の上に該第1の絶縁膜と組成が異なる第2の絶縁膜を形成する第2の工程と、第2の絶縁膜の上に該第2の絶縁膜と組成が異なる第3の絶縁膜を形成する第3の工程と、第3の絶縁膜の上に導電性膜を形成する第4の工程と、導電性膜の上に、配線形成用開口部を有する第1のレジストパターンを形成する第5の工程と、導電性膜に対して第1のレジストパターンをマスクとしてエッチングを行なって、導電性膜からなり配線形成用開口部を有するマスクパターンを形成する第6の工程と、第3の絶縁膜の上に、コンタクトホール形成用開口部を有する第2のレジストパターンを形成する第7の工程と、第3の絶縁膜、第1のレジストパターン及び第2のレジストパターンに対するエッチングレートが高い一方、第2の絶縁膜に対するエッチングレートが低いエッチング条件で、第3の絶縁膜に対してドライエッチングを行なうことにより、第3の絶縁膜を該第3の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化すると共に、第1のレジストパターン及び第2のレジストパターンを全面的に又は下部を残して除去する第8の工程と、第2の絶縁膜に対するエッチングレートが高い一方、第1の絶縁膜及び第3の絶縁膜に対するエッチングレートが低いエッチング条件で、第2の絶縁膜に対してパターン化された第3の絶縁膜をマスクとしてドライエッチングを行なうことにより、第2の絶縁膜

を該第2の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第9の工程と、第1の絶縁膜及び第3の絶縁膜に対するエッチングレートが高い一方、マスクパターン及び第2の絶縁膜に対するエッチングレートが低いエッチング条件で、第3の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なうと共に第1の絶縁膜に対してパターン化された第2の絶縁膜をマスクとしてドライエッチングを行なうことにより、第3の絶縁膜に配線溝を形成すると共に第1の絶縁膜にコンタクトホールを形成する第10の工程と、配線溝及びコンタクトホールに金属膜を充填することにより、上層の金属配線及び下層の金属配線と上層の金属配線とを接続するコンタクトを形成する第11の工程とを備えている。

## 【0017】

第1の配線構造体の形成方法によると、第8の工程において、第3の絶縁膜、第1のレジストパターン及び第2のレジストパターンに対するエッチングレートが高い一方、第2の絶縁膜に対するエッチングレートが低いエッチング条件で、第3の絶縁膜に対してドライエッチングを行なって、第3の絶縁膜をパターン化すると共に、第1のレジストパターン及び第2のレジストパターンを除去するため、第1のレジストパターン及び第2のレジストパターンを酸素プラズマを用いるアッシングにより除去する工程が不要になる。

## 【0018】

また、第2の絶縁膜の組成と第3の絶縁膜の組成とが異なるため、第10の工程において、第3の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なって配線溝を形成する際に、第2の絶縁膜をエッチングストッパーとして用いることができる。

## 【0019】

第1の配線構造体の形成方法は、第10の工程と第11の工程との間に、第3の絶縁膜における配線溝に露出している部分及び第1の絶縁膜におけるコンタクトホールに露出している部分に金属膜からなる密着層を形成する工程をさらに備えていることが好ましい。

【0020】

第1の配線構造体の形成方法において、第3の絶縁膜は有機成分を主成分とすることが好ましい。

【0021】

この場合、第3の工程は、パーフルオロデカリンを含む反応性ガスを用いるCVD法により第3の絶縁膜を形成する工程を含むことが好ましい。

【0022】

また、この場合、第1の絶縁膜も有機成分を主成分とすることが好ましい。

【0023】

第1の絶縁膜及び第2の絶縁膜が有機成分を主成分とする場合には、第10の工程と第11の工程との間に、第3の絶縁膜における配線溝に露出している部分及び第1の絶縁膜におけるコンタクトホールに露出している部分に、窒素を含有する反応性ガスを用いるプラズマ処理によって密着層を形成する工程をさらに備えていることが好ましい。

【0024】

第1の絶縁膜が有機成分を主成分とする場合には、第1の工程は、パーフルオロデカリンを含む反応性ガスを用いるCVD法により第3の絶縁膜を形成する工程を含むことが好ましい。

【0025】

本発明に係る第2の配線構造体の形成方法は、下層の金属配線の上に第1の絶縁膜を形成する第1の工程と、第1の絶縁膜の上に該第1の絶縁膜と組成が異なる第2の絶縁膜を形成する第2の工程と、第2の絶縁膜の上に該第2の絶縁膜と組成が異なる第3の絶縁膜を形成する第3の工程と、第3の絶縁膜の上に導電性膜を形成する第4の工程と、導電性膜の上に、配線形成用開口部を有する第1のレジストパターンを形成する第5の工程と、導電性膜に対して第1のレジストパターンをマスクとしてエッチングを行なって、導電性膜からなり配線形成用開口部を有するマスクパターンを形成する第6の工程と、第3の絶縁膜の上に、コンタクトホール形成用開口部を有する第2のレジストパターンを形成する第7の工程と、第3の絶縁膜に対するエッチングレートが高い一方、第2の絶縁膜、第1

のレジストパターン及び第2のレジストパターンに対するエッチングレートが低いエッチング条件で、第3の絶縁膜に対して第1のレジストパターン及び第2のレジストパターンをマスクとしてドライエッチングを行なうことにより、第3の絶縁膜を該第3の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第8の工程と、第2の絶縁膜に対するエッチングレートが高い一方、第1の絶縁膜、第3の絶縁膜、第1のレジストパターン及び第2のレジストパターンに対するエッチングレートが低いエッチング条件で、第2の絶縁膜に対して第1のレジストパターン及び第2のレジストパターンをマスクとしてドライエッチングを行なうことにより、第2の絶縁膜を該第2の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第9の工程と、第1のレジストパターン及び第2のレジストパターンを除去する第10の工程と、第1の絶縁膜及び第3の絶縁膜に対するエッチングレートが高い一方、マスクパターン及び第2の絶縁膜に対するエッチングレートが低いエッチング条件で、第3の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なうと共に第1の絶縁膜に対してパターン化された第2の絶縁膜をマスクとしてドライエッチングを行なうことにより、第3の絶縁膜に配線溝を形成すると共に第1の絶縁膜にコンタクトホールを形成する第11の工程と、配線溝及びコンタクトホールに金属膜を充填することにより、上層の金属配線及び下層の金属配線と上層の金属配線とを接続するコンタクトを形成する第12の工程とを備えている。

## 【0026】

第2の配線構造体の形成方法によると、第10の工程において、第1のレジストパターン及び第2のレジストパターンを除去する際に、第1の絶縁膜及び第3の絶縁膜における第2の絶縁膜のコンタクトホール形成用開口部に露出している部分にダメージ層が形成されても、第11の工程において、第1の絶縁膜及び第3の絶縁膜に対するエッチングレートが高い一方、マスクパターン及び第2の絶縁膜に対するエッチングレートが低いエッチング条件で、第3の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なうと共に第1の絶縁膜に対してパターン化された第2の絶縁膜をマスクとしてドライエッチングを行なって、第3の絶縁膜に配線溝を形成すると共に第1の絶縁膜にコンタクトホールを

形成するため、第1の絶縁膜及び第3の絶縁膜に形成されているダメージ層は確実に除去される。

【0027】

第2の配線構造体の形成方法において、第3の絶縁膜は、シロキサン骨格を有する低誘電率SOG膜であることが好ましい。

【0028】

【発明の実施の形態】

(第1の実施形態)

以下、本発明の第1の実施形態に係る配線構造体の形成方法について、図1(a)～(c)、図2(a)～(c)及び図3(a)～(c)を参照しながら説明する。

【0029】

まず、図1(a)に示すように、半導体基板100上に形成された第1の金属配線101の上に、後に行なわれるエッチング工程において第1の金属配線101を保護する例えば50nmの膜厚を有するシリコン窒化膜102を形成した後、該シリコン窒化膜102の上に、例えば1 $\mu$ mの膜厚を有すると共に有機成分を主成分とする第1の有機膜103を堆積する。次に、第1の有機膜103の上に、例えば50nmの膜厚を有すると共にシリコン酸化物中に有機成分を含有する有機含有シリコン酸化膜104を堆積した後、該有機含有シリコン酸化膜104の上に、例えば400nmの膜厚を有すると共に有機成分を主成分とする第2の有機膜105を堆積し、その後、該第2の有機膜105の上に例えば50nmの膜厚を有する窒化チタン膜106を堆積する。

【0030】

第1及び第2の有機膜103、105の堆積方法については、特に限定されないが、例えばパーフルオロデカシンを主原料とする反応性ガスを用いるプラズマCVD法が挙げられる。また、第1及び第2の有機膜103、105としては、プラズマCVD法、塗布法又は熱CVD法により形成された、炭化水素膜又はフッ素を含有する炭化水素膜を用いることができる。

【0031】

また、第1の有機膜103の堆積方法としては、例えばパーフルオロデカシンと、ヘキサメチルジシロキサン、アリルアルコキシシラン又はアルキルアルコキシシラン等の有機シランとを主原料とする反応性ガスを用いるプラズマCVD法でもよい。このようにすると、有機無機ハイブリッド膜が得られる。

【0032】

また、有機含有シリコン酸化膜104の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるCVD法が挙げられる。このようにすると、シリコン酸化物中にシリコン原子と結合したフェニル基が取り込まれた構造を有する有機含有シリコン酸化膜104が得られる。

【0033】

次に、図1(b)に示すように、窒化チタン膜106の上に、リソグラフィ工程により配線溝形成用開口部を有する第1のレジストパターン107を形成した後、該第1のレジストパターン107をマスクとして窒化チタン膜106に対してドライエッチングを行なって、図1(c)に示すように、窒化チタン膜106からなるマスクパターン108を形成する。

【0034】

次に、第1のレジストパターン107を除去することなく、第2の有機膜105の上に、リソグラフィ工程によりコンタクトホール形成用開口部を有する第2のレジストパターン109を形成した後、第2の有機膜105に対してドライエッチングを行なって、図2(a)に示すように、コンタクトホール形成用開口部を有するパターン化された第2の有機膜105Aを形成する。この場合、第2の有機膜105と、第1のレジストパターン107及び第2のレジストパターン109とは共に有機成分を主成分としているため、第2の有機膜105に対するエッチングレートと、第1及び第2のレジストパターン107、109に対するエッチングレートとはほぼ等しいので、第2の有機膜105に対するドライエッチング工程により、第1のレジストパターン107及び第2のレジストパターン109は除去される。

【0035】

尚、第2の有機膜105に対するドライエッチング工程において、第2のレジストパターン109が残存しても差し支えない。その理由は、残存する第2のレジストパターン109は、後に行なわれるパターン化された第2の有機膜105Aに配線溝111を形成する工程(図2(c)を参照)において除去されるからである。

【0036】

次に、パターン化された第2の有機膜105Aをマスクとして有機含有シリコン酸化膜104に対してドライエッチングを行なって、図2(b)に示すように、コンタクトホール形成用開口部を有するパターン化された有機含有シリコン酸化膜104Aを形成する。このドライエッチング工程は、有機含有シリコン酸化膜104に対するエッチングレートがパターン化された第2の有機膜105Aに対するエッチングレートよりも大きくなるようなエッチング条件を選択することにより、パターン化された第2の有機膜105Aがエッチングされる事態を防止する。

【0037】

次に、マスクパターン108をマスクとしてパターン化された第2の有機膜105Aに対し、またパターン化された有機含有シリコン酸化膜104Aをマスクとして第1の有機膜103に対してそれぞれドライエッチングを行なって、図2(c)に示すように、パターン化された第2の有機膜105Aに配線溝111を形成すると共に、コンタクトホール110を有するパターン化された第1の有機膜103Aを形成する。

【0038】

次に、パターン化された有機含有シリコン酸化膜104Aをマスクとしてシリコン窒化膜102に対してドライエッチングを行なって、図3(a)に示すように、パターン化されたシリコン窒化膜102Aを形成すると共に、第1の金属配線101をコンタクトホール110に露出させる。

【0039】

次に、図3(b)に示すように、コンタクトホール110及び配線溝111の

壁面に例えば50nmの膜厚を有する窒化チタンからなる密着層112を堆積した後、コンタクトホール110及び配線溝111が埋まるように全面に亘って金属膜113を堆積する。金属膜113の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜113の堆積方法も特に限定されず、メッキ法、CVD法又はスパッタ法等を用いることができる。

## 【0040】

次に、図3(c)に示すように、パターン化された第2の有機膜105Aの上、に堆積されている、密着層112、金属膜113及びマスクパターン108を例えばCMP法により除去して、金属膜113からなる第2の金属配線114、及び第1の金属配線101と第2の金属配線114とを接続する金属膜113からなるコンタクト115を形成する。

## 【0041】

尚、第2の金属配線114の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

## 【0042】

第1の実施形態によると、有機含有シリコン酸化膜104は、フェニルトリメトキシシランを主原料とする反応性ガスを用いるCVD法により形成された膜であるため、シリコン酸化物中にシリコン原子と結合したフェニル基(有機基)が取り込まれた構造を有している。従って、従来のCVD酸化膜と同程度に良好な加工性及びHSQ膜と同程度に低い比誘電率を有していると共に、有機膜、酸化膜及び金属膜に対する高い密着性を有している。

## 【0043】

また、窒化チタン膜106からなるマスクパターン108を形成した後、第1のレジストパターン107を除去することなく第2のレジストパターン109を形成すると共に、第2の有機膜105に対するドライエッチング工程により、第1のレジストパターン107及び第2のレジストパターン109を除去するため、第1のレジストパターン107及び第2のレジストパターン109を酸素プラズマを用いるアッシングにより除去する工程が不要になるので、レジストパター



ンをアッシングにより除去する際に第2の有機膜105がダメージを受ける事態を回避することができる。従って、層間絶縁膜として比誘電率が低い第2の有機膜105を用いるにも拘わらず、通常のレジストプロセスを採用することが可能になる。

【0044】

また、マスクパターン108をマスクとしパターン化された有機含有シリコン酸化膜104Aをエッチングストッパーとして、パターン化された第2の有機膜105Aに対してドライエッチングを行なって配線溝111を形成するため、配線溝111の深さは第2の有機膜105の膜厚と一致するので、配線溝111の深さを自己整合的に規定することができる。

【0045】

以下、第2のレジストパターン109が第1のレジストパターン107に対して位置ずれを起こした場合の問題点及びその場合の解決策について説明する。

【0046】

まず、第2のレジストパターン109が位置ずれを起こした場合の問題点について、図4(a)～(c)、図5(a)～(c)及び図6(a)～(c)を参照しながら説明する。

【0047】

第1の実施形態と同様、図4(a)に示すように、半導体基板100上に形成された第1の金属配線101の上に例えば50nmの膜厚を有するシリコン窒化膜102を形成した後、該シリコン窒化膜102の上に、例えば1 $\mu$ mの膜厚を有すると共に有機成分を主成分とする第1の有機膜103を堆積する。

【0048】

次に、第1の有機膜103の上に、例えば50nmの膜厚を有すると共にシリコン酸化物中に有機成分を含有する有機含有シリコン酸化膜104を堆積した後、該有機含有シリコン酸化膜104の上に、例えば400nmの膜厚を有すると共に有機成分を主成分とする第2の有機膜105を堆積し、その後、第2の有機膜105の上に例えば50nmの膜厚を有する窒化チタン膜106を堆積する。

【0049】

次に、図4 (b) に示すように、窒化チタン膜106の上に、配線溝形成用開口部を有する第1のレジストパターン107を形成した後、該第1のレジストパターン107をマスクとして窒化チタン膜106に対してドライエッチングを行なって、図4 (c) に示すように、窒化チタン膜106からなるマスクパターン108を形成する。

【0050】

次に、図5 (a) に示すように、第1のレジストパターン107を除去することなく、第2の有機膜105の上に、コンタクトホール形成用開口部を有する第2のレジストパターン109を形成する。この場合、図5 (a) と図1 (c) との対比から分かるように、第2のレジストパターン109は第1のレジストパターン107に対して位置ずれを起こしている。

【0051】

次に、第2の有機膜105に対してドライエッチングを行なって、図5 (b) に示すように、コンタクトホール形成用開口部を有するパターン化された第2の有機膜105Aを形成する。第1の実施形態と同様、第2の有機膜105と、第1のレジストパターン107及び第2のレジストパターン109とは共に有機成分を主成分としているため、第2の有機膜105に対するドライエッチング工程により、第1のレジストパターン107及び第2のレジストパターン109は除去される。この場合、第2のレジストパターン109が第1のレジストパターン107に対して位置ずれを起こしているため、第2の有機膜105Aに形成されるコンタクトホール形成用開口部の径は小さい。

【0052】

次に、パターン化された第2の有機膜105Aをマスクとして有機含有シリコン酸化膜104に対してドライエッチングを行なって、図5 (c) に示すように、コンタクトホール形成用開口部を有するパターン化された有機含有シリコン酸化膜104Aを形成する。

【0053】

次に、マスクパターン108をマスクとしてパターン化された第2の有機膜1

05Aに対し、またパターン化された有機含有シリコン酸化膜104Aをマスクとして第1有機膜103に対してそれぞれドライエッチングを行なって、図6(a)に示すように、パターン化された第2の有機膜105Aに配線溝111を形成すると共に、コンタクトホール110を有するパターン化された第1の有機膜103Aを形成する。その後、パターン化された有機含有シリコン酸化膜104Aをマスクとしてシリコン窒化膜102に対してドライエッチングを行なって、図6(b)に示すように、パターン化されたシリコン窒化膜102Aを形成すると共に、第1の金属配線101をコンタクトホール110に露出させる。

## 【0054】

次に、コンタクトホール110及び配線溝111の壁面に例えば50nmの膜厚を有する窒化チタン層からなる密着層112を堆積した後、全面に亘って金属膜を堆積し、その後、パターン化された第2の有機膜105Aの上に堆積されている、密着層112、金属膜及びマスクパターン108を例えばCMP法により除去する。このようにすると、図6(c)に示すように、金属膜からなる第2の金属配線114は形成されるが、コンタクトホール110の径が小さいため該コンタクトホール110には金属膜が完全には充填されないため、第1の金属配線101と第2の金属配線112とは接続されず、不良が発生する。

## 【0055】

以下、第2のレジストパターン109が位置ずれを起こした場合の解決策について、図7(a)～(c)及び図8(a)～(c)を参照しながら説明する。

## 【0056】

まず、図4(a)～(c)及び図5(a)に基づいて説明した前述の工程と同様の工程によって、コンタクトホール形成用開口部を有する第2のレジストパターン109を形成するが、この場合にも、第2のレジストパターン109は第1のレジストパターン107に対して位置ずれを起こしている(図5(a)を参照)。

## 【0057】

そこで、図7(a)に示すように、第2のレジストパターン109をマスクとして第1のレジストパターン107及びマスクパターン108に対してドライエ

ッチングを行なって、第1のレジストパターン107における第2のレジストパターン109と重なっていない領域を除去すると共に、マスクパターン108の開口部を配線溝形成用開口部及びコンタクトホール形成用開口部を含む大きさに拡大する。これによって、第2のレジストパターン109のコンタクトホール形成用開口部は、第1のレジストパターン107及びマスクパターン108に転写される。

## 【0058】

次に、第2の有機膜105に対してドライエッチングを行なって、図7(b)に示すように、コンタクトホール形成用開口部を有するパターン化された第2の有機膜105Aを形成する。この場合にも、第2の有機膜105と、第1のレジストパターン107及び第2のレジストパターン109とは共に有機成分を主成分としているため、第2の有機膜105に対するドライエッチング工程により、第1のレジストパターン107及び第2のレジストパターン109は除去される。

## 【0059】

次に、パターン化された有機膜105Aをマスクとして有機含有シリコン酸化膜104に対してドライエッチングを行なって、図7(c)に示すように、コンタクトホール形成用開口部を有するパターン化された有機含有シリコン酸化膜104Aを形成する。

## 【0060】

前述のように、第2のレジストパターン109が第1のレジストパターン107に対して位置ずれを起こしているが、第2のレジストパターン109のコンタクトホール形成用開口部を第1のレジストパターン107及びマスクパターン108に転写しているため、パターン化された第2の有機膜105A及びパターン化された有機含有シリコン酸化膜104Aに形成されるコンタクトホール形成用開口部の径は所定の大きさを有している。

## 【0061】

次に、マスクパターン108及びパターン化された有機含有シリコン酸化膜104Aをマスクとしてパターン化された第2の有機膜105A及び第1の有機膜

103に対してドライエッチングを行なって、図8(a)に示すように、パターン化された第2の有機膜105Aに配線溝111を形成すると共に、コンタクトホール110を有するパターン化された第1の有機膜103Aを形成する。その後、パターン化された有機含有シリコン酸化膜104Aをマスクとしてシリコン窒化膜102に対してドライエッチングを行なって、図8(b)に示すように、パターン化されたシリコン窒化膜102Aを形成すると共に、第1の金属配線101をコンタクトホール110に露出させる。

## 【0062】

次に、コンタクトホール110及び配線溝111の壁面に例えば50nmの膜厚を有する窒化チタン層からなる密着層112を堆積した後、全面に亘って金属膜を堆積し、その後、パターン化された第2の有機膜105Aの上に堆積されている、密着層112、金属膜及びマスクパターン108を例えばCMP法により除去する。このようにすると、図8(c)に示すように、窒化チタン膜112及び金属膜からなる、第2の金属配線114及びコンタクト115が形成される。

## 【0063】

## (第2の実施形態)

以下、本発明の第2の実施形態に係る配線構造体の形成方法について、図9(a)～(c)、図10(a)～(c)及び図11(a)～(c)を参照しながら説明する。

## 【0064】

まず、図9(a)に示すように、半導体基板200上に形成された第1の金属配線201の上に例えば50nmの膜厚を有するシリコン窒化膜202を形成した後、該シリコン窒化膜202の上に、例えば1 $\mu$ mの膜厚を有すると共に有機成分を主成分とする第1の有機膜203を堆積する。次に、第1の有機膜203の上に、例えば50nmの膜厚を有すると共にシリコン酸化物中に有機成分を含有する有機含有シリコン酸化膜204を堆積した後、該有機含有シリコン酸化膜204の上に、例えば400nmの膜厚を有すると共に有機成分を主成分とする第2の有機膜205を堆積し、その後、該第2の有機膜の上に例えば50nmの膜厚を有する窒化チタン膜206を堆積する。

【0065】

第1及び第2の有機膜203、205の堆積方法については、特に限定されないが、例えばパーフルオロデカシンを主原料とする反応性ガスを用いるプラズマCVD法が挙げられる。また、第1及び第2の有機膜203、205としては、プラズマCVD法、塗布法又は熱CVD法により形成された、炭化水素膜又はフッ素を含有する炭化水素膜を用いることができる。

【0066】

また、有機含有シリコン酸化膜204の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるCVD法が挙げられる。

【0067】

次に、図9(b)に示すように、窒化チタン膜206の上に、リソグラフィ工程により配線溝形成用開口部を有する第1のレジストパターン207を形成した後、該第1のレジストパターン207をマスクとして窒化チタン膜206に対してドライエッチングを行なって、図9(c)に示すように、窒化チタン膜206からなるマスクパターン208を形成する。

【0068】

次に、第1のレジストパターン207を除去することなく、第2の有機膜205の上に、リソグラフィ工程によりコンタクトホール形成用開口部を有する第2のレジストパターン209を形成した後、第2の有機膜205に対してドライエッチングを行なって、図10(a)に示すように、コンタクトホール形成用開口部を有するパターン化された第2の有機膜205Aを形成する。この場合、第2の有機膜205と、第1のレジストパターン207及び第2のレジストパターン209とは共に有機成分を主成分としているため、第2の有機膜205に対するエッチングレートと、第1及び第2のレジストパターン207、209に対するエッチングレートとはほぼ等しいので、第2の有機膜205に対するドライエッチング工程により、第1のレジストパターン207及び第2のレジストパターン209は除去される。

【0069】

尚、第2のレジストパターン209が第1のレジストパターン207に対して位置ずれしている恐れがある場合には、第1の実施形態において説明したように、第2のレジストパターン209をマスクとして第1のレジストパターン207及びマスクパターン208に対してドライエッチングを行なって、第1のレジストパターン207における第2のレジストパターン209と重なっていない領域を除去すると共に、マスクパターン208の開口部を配線溝形成用開口部及びコンタクトホール形成用開口部を含む大きさに拡大する。

【0070】

次に、パターン化された第2の有機膜205Aをマスクとして有機含有シリコン酸化膜204に対してドライエッチングを行なって、図10(b)に示すように、コンタクトホール形成用開口部を有するパターン化された有機含有シリコン酸化膜204Aを形成する。その後、マスクパターン208をマスクとしてパターン化された第2の有機膜205Aに対し、またパターン化された有機含有シリコン酸化膜204Aをマスクとして第1の有機膜203に対してそれぞれドライエッチングを行なって、図10(c)に示すように、パターン化された第2の有機膜205Aに配線溝211を形成すると共に、コンタクトホール210を有するパターン化された第1の有機膜203Aを形成する。

【0071】

次に、パターン化された有機含有シリコン酸化膜203Aをマスクとしてシリコン窒化膜202に対してドライエッチングを行なって、図11(a)に示すように、パターン化されたシリコン窒化膜202Aを形成すると共に、第1の金属配線201をコンタクトホール210に露出させる。

【0072】

次に、パターン化された第1の有機膜203A及びパターン化された第2の有機膜205Aに対してアンモニアガスを用いるプラズマ処理を行なう。このようにすると、図11(b)に示すように、パターン化された第1の有機膜203Aにおけるコンタクトホール210に露出する壁部及びパターン化された第2の有機膜205Aにおける配線溝211に露出する壁部に、アミノ基及びアミド基を

有する密着層212がそれぞれ形成される。その後、コンタクトホール210及び配線溝211が埋まるように全面に亘って金属膜213を堆積する。金属膜213の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜213の堆積方法も特に限定されず、メッキ法、CVD法又はスパッタ法等を用いることができる。

## 【0073】

次に、図11(c)に示すように、パターン化された第2の有機膜205Aの上に堆積されている、金属膜213及びマスクパターン208を例えばCMP法により除去して、金属膜213からなる、第2の金属配線214及びコンタクト215を形成する。

## 【0074】

尚、第2の金属配線214の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

## 【0075】

## (第3の実施形態)

以下、本発明の第3の実施形態に係る配線構造体の形成方法について、図12(a)～(c)、図13(a)～(c)及び図14(a)～(c)を参照しながら説明する。

## 【0076】

まず、図12(a)に示すように、半導体基板300上に形成された第1の金属配線301の上に、後に行なわれるエッチング工程において第1の金属配線301を保護する例えば50nmの膜厚を有するシリコン窒化膜302を形成した後、該シリコン窒化膜302の上に、例えば1 $\mu$ mの膜厚を有すると共にシリコン酸化物中に有機成分を含有する第1の有機含有シリコン酸化膜303を堆積する。次に、第1の有機含有シリコン酸化膜303の上に、例えば400nmの膜厚を有すると共にシロキサン骨格を有する低誘電率SOG膜304を堆積した後、該低誘電率SOG膜304の上に、例えば50nmの膜厚を有すると共にシリコン酸化物中に有機成分を含有する第2の有機含有シリコン酸化膜305を堆積



し、その後、第2の有機含有シリコン酸化膜305の上に例えば50nmの膜厚を有する窒化チタン膜306を形成する。

【0077】

第1の有機含有シリコン酸化膜303及び第2の有機含有シリコン酸化膜305の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるCVD法が挙げられる。また、シロキサン骨格を有する低誘電率SOG膜304としてはHSQ膜を用いることができる。

【0078】

次に、図12(b)に示すように、窒化チタン膜306の上に、リソグラフィ工程により配線溝形成用開口部を有する第1のレジストパターン307を形成した後、該第1のレジストパターン307をマスクとして窒化チタン膜306に対してドライエッチングを行なって、図12(c)に示すように、窒化チタン膜306からなるマスクパターン308を形成する。

【0079】

次に、図13(a)に示すように、第1のレジストパターン307を除去した後、第2の有機含有シリコン酸化膜305の上に、コンタクトホール形成用開口部を有する第2のレジストパターン309を形成する。その後、第2のレジストパターン309をマスクとして、第2の有機含有シリコン酸化膜305、低誘電率SOG膜304及び第1の有機含有シリコン酸化膜303に対して順次ドライエッチングを行なって、図13(b)に示すように、パターン化された第2の有機含有シリコン酸化膜305A、パターン化された低誘電率SOG膜304A及びコンタクトホール310を有するパターン化された第1の有機含有シリコン酸化膜303Aをそれぞれ形成する。

【0080】

次に、図13(c)に示すように、第2のレジストパターン309を除去した後、マスクパターン308をマスクとしてパターン化された第2の有機含有シリコン酸化膜305Aに対してドライエッチングを行なって、パターン化された第2の有機含有シリコン酸化膜305Aに配線溝形成用開口部を形成し、その後、マスクパターン308及び配線溝形成用開口部を有するパターン化された第2の

有機含有シリコン酸化膜305Aをマスクとしてパターン化された低誘電率SOG膜304Aに対してドライエッチングを行なって配線溝311を形成する。配線溝311を形成する工程においては、第1の有機含有シリコン酸化膜303Aに対するエッチングレートが低誘電率SOG膜304Aに対するエッチングレートに比べて十分に遅くなるようなエッチング条件を設定することにより、パターン化された第1の有機含有シリコン酸化膜303Aに対する十分な選択比を確保できるので、配線溝311の深さを第2の有機含有シリコン酸化膜305及び低誘電率SOG膜304の合計膜厚により一義的に決定することができる。

## 【0081】

尚、第2のレジストパターン309が第1のレジストパターン307に対して位置ずれしている恐れがある場合には、第2のレジストパターン309をマスクとして第2の有機含有シリコン酸化膜305に対してドライエッチングを行なう前に、第2のレジストパターン309をマスクとしてマスクパターン308に対するドライエッチングを行なうことが好ましい。すなわち、第2のレジストパターン309が第1のレジストパターン307に対して位置ずれしているために、マスクパターン308が第2のレジストパターン309のコンタクトホール形成用開口部に露出している場合には、第2のレジストパターン309をマスクとしてマスクパターン308に対してドライエッチングを行なうことにより、マスクパターン308の開口部を配線溝形成用開口部及びコンタクトホール形成用開口部を含む大きさに拡大する。

## 【0082】

次に、パターン化された第1の有機含有シリコン酸化膜303Aをマスクとしてシリコン窒化膜302に対してドライエッチングを行なって、図14(a)に示すように、パターン化されたシリコン窒化膜302Aを形成すると共に、第1の金属配線301をコンタクトホール310に露出させる。

## 【0083】

次に、図14(b)に示すように、コンタクトホール310及び配線溝311の壁面に例えば50nmの膜厚を有する窒化チタン層からなる密着層312を堆積した後、コンタクトホール310及び配線溝311が埋まるように全面に亘っ

て金属膜313を堆積する。金属膜313の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜313の堆積方法も特に限定されず、メッキ、CVD法又はスパッタ法等を用いることができる。

【0084】

次に、図14(c)に示すように、パターン化された第2の有機含有シリコン酸化膜305Aの上に堆積されている、密着層312、金属膜313及びマスクパターン308を例えばCMP法により除去して、金属膜313からなる第2の金属配線314、及び第1の金属配線301と第2の金属配線314とを接続する金属膜313からなるコンタクト315を形成する。

【0085】

尚、第2の金属配線314の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

【0086】

第3の実施形態によると、第1のレジストパターン307を酸素プラズマを用いるアッシングにより除去する際には、低誘電率SOG膜304の上に第2の有機含有シリコン酸化膜305が存在しているため、低誘電率SOG膜304が酸素プラズマに曝されることはない。

【0087】

また、第2のレジストパターン309をマスクとして、第2の有機含有シリコン酸化膜305、低誘電率SOG膜304及び第1の有機含有シリコン酸化膜303に対して順次ドライエッチングを行なった後、第2のレジストパターン309を酸素プラズマを用いるアッシングにより除去するため、パターン化された低誘電率SOG膜304Aにおけるコンタクトホール形成用開口部に露出する領域は酸素プラズマに曝されるのでダメージを受ける。しかしながら、パターン化された低誘電率SOG膜304Aにおけるダメージ層は、パターン化された低誘電率SOG膜304Aに配線溝311を形成する際に除去されるので、後工程において悪影響を及ぼさない。

【0088】

従って、低誘電率SOG膜304としては、酸素プラズマによって劣化する材料を使用することが可能である。例えば、HSQ膜は、酸素プラズマに曝されると、Si-H結合が酸化されてしまうため、含有水分量の増加及び比誘電率の増加が起こって、素子の信頼性及び性能の劣化が引き起こされるが、第3の実施形態によると、配線溝311が形成された後のパターン化された低誘電率SOG膜304Aは酸素プラズマの影響を受けていないので、層間絶縁膜としてHSQ膜を用いても、素子の信頼性及び性能の劣化を回避することができる。

【0089】

(第3の実施形態の変形例)

以下、本発明の第3の実施形態の変形例に係る配線構造体の形成方法について、図15(a)～(c)、図16(a)～(d)及び図17(a)～(c)を参照しながら説明する。

【0090】

まず、図15(a)に示すように、半導体基板350上に形成された第1の金属配線351の上に、後に行なわれるエッチング工程において第1の金属配線351を保護する例えば50nmの膜厚を有するシリコン窒化膜352を形成した後、該シリコン窒化膜352の上に、例えば1 $\mu$ mの膜厚を有する第1のシリコン酸化膜353を堆積する。次に、第1のシリコン酸化膜353の上に、例えば400nmの膜厚を有する有機膜354を堆積した後、該有機膜354の上に、例えば50nmの膜厚を有する第2のシリコン酸化膜355を堆積し、その後、第2のシリコン酸化膜355の上に例えば50nmの膜厚を有する窒化チタン膜356を形成する。

【0091】

第1のシリコン酸化膜353及び第2のシリコン酸化膜355の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるCVD法が挙げられる。

【0092】

次に、図15(b)に示すように、窒化チタン膜356の上に、リソグラフィ

工程により配線溝形成用開口部を有する第1のレジストパターン357を形成した後、該第1のレジストパターン357をマスクとして窒化チタン膜356に対してドライエッチングを行なって、図15(c)に示すように、窒化チタン膜356からなるマスクパターン358を形成する。

## 【0093】

次に、図16(a)に示すように、第1のレジストパターン357を除去した後、第2のシリコン酸化膜355の上に、コンタクトホール形成用開口部を有する第2のレジストパターン359を形成する。その後、第2のレジストパターン359をマスクとして、第2のシリコン酸化膜355及び有機膜354に対して順次ドライエッチングを行なって、図16(b)に示すように、コンタクトホール形成用開口部360を有する、パターン化された第2のシリコン酸化膜355A及びパターン化された有機膜354Aをそれぞれ形成する。この場合、有機膜354に対するエッチング工程において第2のレジストパターン359が除去される。

## 【0094】

次に、図16(c)に示すように、パターン化された第2のシリコン酸化膜355A及びパターン化された有機膜354Aをマスクとして第1のシリコン酸化膜353に対してドライエッチングを行なって、コンタクトホール361を有するパターン化された第1のシリコン酸化膜353Aを形成する。このエッチング工程において、パターン化された第2のシリコン酸化膜355Aにマスクパターン358が転写されるので、パターン化された第2のシリコン酸化膜355Aに配線溝形成用開口部が形成される。

## 【0095】

次に、図16(d)に示すように、マスクパターン358及び配線溝形成用開口部を有するパターン化された第2のシリコン酸化膜355Aをマスクとしてパターン化された有機膜354Aに対してドライエッチングを行なって配線溝362を形成する。配線溝362を形成する工程においては、第1のシリコン酸化膜353Aに対するエッチングレートが有機膜354Aに対するエッチングレートに比べて十分に遅くなるようなエッチング条件を設定することにより、パターン

化された第1のシリコン酸化膜353Aに対する十分な選択比を確保できるので、配線溝362の深さを第2のシリコン酸化膜355及び有機膜354の合計膜厚により一義的に決定することができる。

## 【0096】

尚、第2のレジストパターン359が第1のレジストパターン357に対して位置ずれしている恐れがある場合には、第2のレジストパターン359をマスクとして第2のシリコン酸化膜355に対してドライエッチングを行なう前に、第2のレジストパターン359をマスクとしてマスクパターン358に対するドライエッチングを行なうことが好ましい。すなわち、第2のレジストパターン359が第1のレジストパターン357に対して位置ずれしているために、マスクパターン358が第2のレジストパターン359のコンタクトホール形成用開口部に露出している場合には、第2のレジストパターン359をマスクとしてマスクパターン358に対してドライエッチングを行なうことにより、マスクパターン358の開口部を配線溝形成用開口部及びコンタクトホール形成用開口部を含む大きさに拡大する。

## 【0097】

次に、パターン化された第1のシリコン酸化膜353Aをマスクとしてシリコン窒化膜352に対してドライエッチングを行なって、図17(a)に示すように、パターン化されたシリコン窒化膜352Aを形成すると共に、第1の金属配線351をコンタクトホール361に露出させる。

## 【0098】

次に、図17(b)に示すように、コンタクトホール361及び配線溝362の壁面に例えば50nmの膜厚を有する窒化チタン層からなる密着層363を堆積した後、コンタクトホール361及び配線溝362が埋まるように全面に亘って金属膜364を堆積する。金属膜364の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜364の堆積方法も特に限定されず、メッキ法、CVD法又はスパッタ法等を用いることができる。

【0099】

次に、図17(c)に示すように、パターン化された第2のシリコン酸化膜355Aの上に堆積されている、密着層363、金属膜364及びマスクパターン358を例えばCMP法により除去して、金属膜364からなる第2の金属配線365、及び第1の金属配線351と第2の金属配線365とを接続する金属膜364からなるコンタクト366を形成する。

【0100】

尚、第2の金属配線365の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

【0101】

第3の実施形態の変形例によると、第1のレジストパターン357を酸素プラズマを用いるアッシングにより除去する際には、有機膜354の上に第2のシリコン酸化膜355が存在しているため、有機膜354が酸素プラズマに曝されることはない。

【0102】

また、第2のレジストパターン359をマスクとして、第2のシリコン酸化膜355及び有機膜354に対してドライエッチングを行なう際に、第2のレジストパターン359が除去されるため、第2のレジストパターン359を酸素プラズマを用いるアッシングによって除去する必要がないので、有機膜354は酸素プラズマに曝されることがない。

【0103】

(第4の実施形態)

以下、本発明の第4の実施形態に係る配線構造体の形成方法について、図18(a)～(c)、図19(a)～(c)及び図20(a)～(c)を参照しながら説明する。

【0104】

まず、図18(a)に示すように、半導体基板400上に形成された第1の金属配線401の上に、後に行なわれるエッチング工程において第1の金属配線401を保護する例えば50nmの膜厚を有するシリコン窒化膜402を形成した

後、該シリコン窒化膜402の上に、例えば1 $\mu$ mの膜厚を有すると共にシロキサン骨格を有する第1の低誘電率SOG膜403を堆積する。次に、第1の低誘電率SOG膜403の上に、例えば50nmの膜厚を有すると共にシリコン酸化物中に有機成分を含有する有機含有シリコン酸化膜404を堆積した後、該有機含有シリコン酸化膜404の上に、例えば400nmの膜厚を有すると共にシロキサン骨格を有する第2の低誘電率SOG膜405を堆積し、その後、該第2の低誘電率SOG膜405の上に例えば50nmの膜厚を有する窒化チタン膜406を堆積する。

## 【0105】

第1及び第2の低誘電率SOG膜403、405としては例えばHSQ膜を用いることができる。また、有機含有シリコン酸化膜404の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるCVD法が挙げられる。このようにすると、シリコン酸化物中にシリコン原子と結合したフェニル基が取り込まれた構造を有する有機含有シリコン酸化膜404が得られる。

## 【0106】

次に、図18(b)に示すように、窒化チタン膜406の上に、リソグラフィ工程により配線溝形成用開口部を有する第1のレジストパターン407を形成した後、該第1のレジストパターン407をマスクとして窒化チタン膜406に対してドライエッチングを行なって、図18(c)に示すように、窒化チタン膜406からなるマスクパターン408を形成する。

## 【0107】

次に、第1のレジストパターン407を除去することなく、第2の低誘電率SOG膜405の上に、リソグラフィ工程によりコンタクトホール形成用開口部を有する第2のレジストパターン409を形成した後、該第2のレジストパターン409をマスクとして、第2の低誘電率SOG膜405及び有機含有シリコン酸化膜404に対して順次ドライエッチングを行なって、図19(a)に示すように、パターン化された第2の低誘電率SOG膜405A及びパターン化された有機含有シリコン酸化膜404Aをそれぞれ形成する。



## 【0108】

次に、第1及び第2のレジストパターン407、409を酸素プラズマを用いるアッシングにより除去すると、図19(b)に示すように、パターン化された第2の低誘電率SOG膜405A及び第1の低誘電率SOG膜403におけるコンタクトホール形成用開口部に露出する領域にダメージ層410が形成されてしまう。

## 【0109】

次に、マスクパターン408をマスクとしてパターン化された第2の低誘電率SOG膜405Aに対して、またパターン化された有機含有シリコン酸化膜404Aをマスクとして第1の低誘電率SOG膜403に対してそれぞれドライエッチングを行なって、図19(c)に示すように、パターン化された第2の低誘電率SOG膜405Aに配線溝412を形成すると共に、コンタクトホール411を有するパターン化された第1の低誘電率SOG膜403Aを形成する。このドライエッチング工程により、パターン化された第2の低誘電率SOG膜405A及び第1の低誘電率SOG膜403のダメージ層410は除去される。

## 【0110】

次に、パターン化された有機含有シリコン酸化膜404Aをマスクとしてシリコン窒化膜402に対してドライエッチングを行なって、図20(a)に示すように、パターン化されたシリコン窒化膜402Aを形成すると共に、第1の金属配線401をコンタクトホール411に露出させる。

## 【0111】

次に、図20(b)に示すように、コンタクトホール411及び配線溝412の壁面に例えば50nmの膜厚を有する窒化チタン層からなる密着層413を堆積した後、コンタクトホール411及び配線溝412が埋まるように全面に亘って金属膜414を堆積する。金属膜414の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜414の堆積方法も特に限定されず、メッキ法、CVD法又はスパッタ法等を用いることができる。

【0112】

次に、図20(c)に示すように、パターン化された第2の低誘電率SOG膜405Aの上に堆積されている、密着層413、金属膜414及びマスクパターン408を例えばCMP法により除去して、金属膜414からなる第2の金属配線415、及び第1の金属配線401と第2の金属配線415とを接続する金属膜414からなるコンタクト416を形成する。

【0113】

尚、第2の金属配線114の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

【0114】

第4の実施形態によると、第1及び第2のレジストパターン407、409を酸素プラズマを用いるアッシングにより除去する際に、パターン化された第2の低誘電率SOG膜405A及び第1の低誘電率SOG膜403にダメージ層410が形成されてしまうが、該ダメージ層410はコンタクトホール411及び配線溝412を形成する際に除去される。

【0115】

従って、第1及び第2の低誘電率SOG膜403、405としては、酸素プラズマによって劣化する材料を使用することが可能である。例えば、HSQ膜は、酸素プラズマに曝されると、Si-H結合が酸化されてしまうため、含有水分量の増加及び比誘電率の増加が起こって、素子の信頼性及び性能の劣化が引き起こされるが、第4の実施形態によると、コンタクトホール411が形成された後のパターン化された第1の低誘電率SOG膜403A、及び配線溝412が形成された後のパターン化された第2の低誘電率SOG膜405Aは酸素プラズマの影響を受けていないので、層間絶縁膜としてHSQ膜を用いても、素子の信頼性及び性能の劣化を回避することができる。

【0116】

【発明の効果】

第1の配線構造体の形成方法によると、第1のレジストパターン及び第2のレジストパターンを酸素プラズマを用いるアッシングにより除去する工程が不要に

なり、レジストパターンをアッシングにより除去する際に第3の絶縁膜がダメージを受ける事態を回避できるため、第3の絶縁膜として、酸素プラズマによりダメージを受けるが比誘電率は低い絶縁膜を用いることが可能になるので、通常のレジストプロセスを採用しつつ比誘電率が低い層間絶縁膜を形成することができる。

【0117】

また、第10の工程において、第3の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なって配線溝を形成する際に第2の絶縁膜をエッチングストッパーとできるため、配線溝の深さを第3の絶縁膜の膜厚と一致させることができるので、配線溝の深さを自己整合的に規定することができる。

【0118】

第1の配線構造体の形成方法が、第10の工程と第11の工程との間に、第3の絶縁膜における配線溝に露出している部分及び第1の絶縁膜におけるコンタクトホールに露出している部分に金属膜からなる密着層を形成する工程を備えていると、上層の金属配線と第3の絶縁膜との密着性及びコンタクトと第1の絶縁膜との密着性を確保することができる。

【0119】

第1の配線構造体の形成方法において、第3の絶縁膜が有機成分を主成分とすると、第8の工程において、第3の絶縁膜、第1のレジストパターン及び第2のレジストパターンに対するエッチングレートが高い一方、第2の絶縁膜に対するエッチングレートが低いエッチング条件を確実に実現することができる。

【0120】

この場合、第3の工程が、パーフルオロデカリンを含む反応性ガスを用いるCVD法により第3の絶縁膜を形成する工程を含むと、有機成分を主成分とし且つ比誘電率が低い第3の絶縁膜を確実に形成することができる。

【0121】

また、この場合、第1の絶縁膜も有機成分を主成分とすると、第9の工程において、第2の絶縁膜に対するエッチングレートが高い一方、第1の絶縁膜及び第3の絶縁膜に対するエッチングレートが低いエッチング条件を確実に実現できる。

と共に、第10の工程において、第1の絶縁膜及び第3の絶縁膜に対するエッチングレートが高い一方、マスクパターン及び第2の絶縁膜に対するエッチングレートが低いエッチング条件を確実に実現することができる。

【0122】

第1の絶縁膜及び第2の絶縁膜が有機成分を主成分とする場合において、第10の工程と第11の工程との間に、第3の絶縁膜における配線溝に露出している部分及び第1の絶縁膜におけるコンタクトホールに露出している部分に、窒素を含有する反応性ガスを用いるプラズマ処理によって密着層を形成する工程を備えていると、上層の金属配線及びコンタクトと、有機成分を主成分とする第1の絶縁膜及び第3の絶縁膜との密着性を確実に確保することができる。

【0123】

第1の絶縁膜が有機成分を主成分とする場合において、第1の工程が、パーフルオロデカリンを含む反応性ガスを用いるCVD法により第1の絶縁膜を形成工程を含むと、有機成分を主成分とし且つ比誘電率が低い第1の絶縁膜を確実に形成することができる。

【0124】

第2の配線構造体の形成方法によると、第10の工程において、第1のレジストパターン及び第2のレジストパターンを除去する際に、第1の絶縁膜及び第3の絶縁膜における第2の絶縁膜のコンタクトホール形成用開口部に露出している部分にダメージ層が形成されても、該ダメージ層は第11の工程において確実に除去されるため、第1及び第3の絶縁膜として、酸素プラズマによりダメージを受けるが比誘電率は低い絶縁膜を用いることが可能になるので、通常のレジストプロセスを採用しつつ比誘電率が低い層間絶縁膜を形成することができる。

【0125】

第2の配線構造体の形成方法において、第3の絶縁膜がシロキサン骨格を有する低誘電率SOG膜であると、通常のレジストプロセスを採用しつつ比誘電率が低い層間絶縁膜を確実に形成することができる。

【図面の簡単な説明】

【図1】

(a) ~ (c) は本発明の第1の実施形態に係る配線構造体の形成方法を示す断面図である。

【図2】

(a) ~ (c) は本発明の第1の実施形態に係る配線構造体の形成方法を示す断面図である。

【図3】

(a) ~ (c) は本発明の第1の実施形態に係る配線構造体の形成方法を示す断面図である。

【図4】

(a) ~ (c) は本発明の第1の実施形態に係る配線構造体の形成方法において、第2のレジストパターンが位置ずれを起こした場合の問題点を説明する断面図である。

【図5】

(a) ~ (c) は本発明の第1の実施形態に係る配線構造体の形成方法において、第2のレジストパターンが位置ずれを起こした場合の問題点を説明する断面図である。

【図6】

(a) ~ (c) は本発明の第1の実施形態に係る配線構造体の形成方法において、第2のレジストパターンが位置ずれを起こした場合の問題点を説明する断面図である。

【図7】

(a) ~ (c) は本発明の第1の実施形態に係る配線構造体の形成方法において、第2のレジストパターンが位置ずれを起こした場合の解決策を説明する断面図である。

【図8】

(a) ~ (c) は本発明の第1の実施形態に係る配線構造体の形成方法において、第2のレジストパターンが位置ずれを起こした場合の解決策を説明する断面

図である。

【図9】

(a)～(c)は本発明の第2の実施形態に係る配線構造体の形成方法を示す断面図である。

【図10】

(a)～(c)は本発明の第2の実施形態に係る配線構造体の形成方法を示す断面図である。

【図11】

(a)～(c)は本発明の第2の実施形態に係る配線構造体の形成方法を示す断面図である。

【図12】

(a)～(c)は本発明の第3の実施形態に係る配線構造体の形成方法を示す断面図である。

【図13】

(a)～(c)は本発明の第3の実施形態に係る配線構造体の形成方法を示す断面図である。

【図14】

(a)～(c)は本発明の第3の実施形態に係る配線構造体の形成方法を示す断面図である。

【図15】

(a)～(c)は本発明の第3の実施形態の変形例に係る配線構造体の形成方法を示す断面図である。

【図16】

(a)～(d)は本発明の第3の実施形態の変形例に係る配線構造体の形成方法を示す断面図である。

【図17】

(a)～(c)は本発明の第3の実施形態の変形例に係る配線構造体の形成方法を示す断面図である。

【図18】

(a) ~ (c) は本発明の第4の実施形態に係る配線構造体の形成方法を示す断面図である。

【図19】

(a) ~ (c) は本発明の第4の実施形態に係る配線構造体の形成方法を示す断面図である。

【図20】

(a) ~ (c) は本発明の第4の実施形態に係る配線構造体の形成方法を示す断面図である。

【符号の説明】

- 100 半導体基板
- 101 第1の金属膜
- 102 シリコン窒化膜
- 102A パターン化されたシリコン窒化膜
- 103 第1の有機膜
- 103A パターン化された第1の有機膜
- 104 有機含有シリコン酸化膜
- 104A パターン化された有機含有シリコン酸化膜
- 105 第2の有機膜
- 105A パターン化された第2の有機膜
- 106 窒化チタン膜
- 107 第1のレジストパターン
- 108 マスクパターン
- 109 第2のレジストパターン
- 110 コンタクトホール
- 111 配線溝
- 112 密着層
- 113 金属膜
- 114 第2の金属配線

- 115 コンタクト
- 200 半導体基板
- 201 第1の金属膜
- 202 シリコン窒化膜
- 202A パターン化されたシリコン窒化膜
- 203 第1の有機膜
- 203A パターン化された第1の有機膜
- 204 有機含有シリコン酸化膜
- 204A パターン化された有機含有シリコン酸化膜
- 205 第2の有機膜
- 205A パターン化された第2の有機膜
- 206 窒化チタン膜
- 207 第1のレジストパターン
- 208 マスクパターン
- 209 第2のレジストパターン
- 210 コンタクトホール
- 211 配線溝
- 212 密着層
- 213 金属膜
- 214 第2の金属配線
- 215 コンタクト
- 300 半導体基板
- 301 第1の金属膜
- 302 シリコン窒化膜
- 302A パターン化されたシリコン窒化膜
- 303 第1の有機含有シリコン酸化膜
- 303A パターン化された第1の有機含有シリコン酸化膜
- 304 低誘電率SOG膜
- 305 第2の有機含有シリコン酸化膜

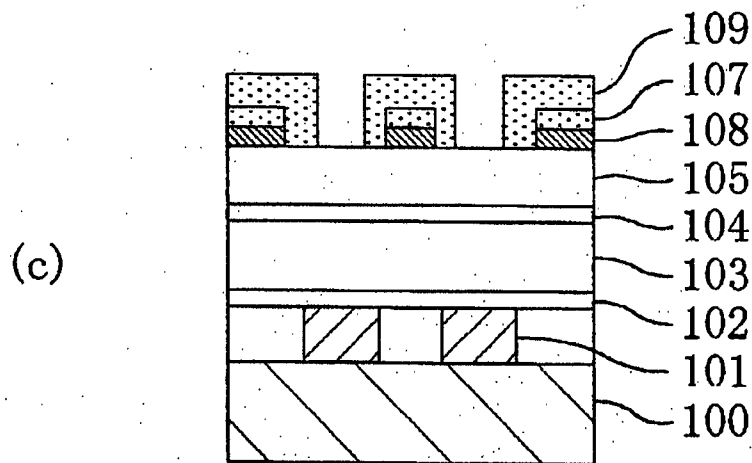
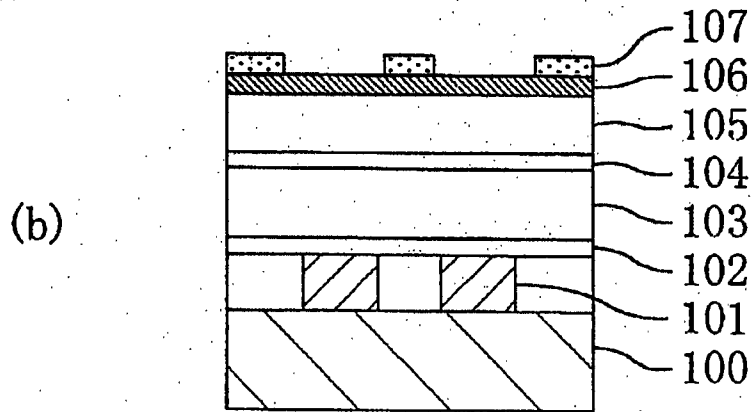
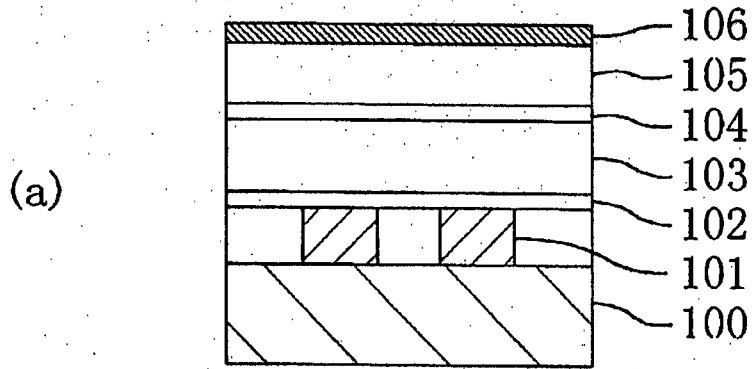


- 305A パターン化された第2の有機含有シリコン酸化膜
- 306 窒化チタン膜
- 307 第1のレジストパターン
- 308 マスクパターン
- 309 第2のレジストパターン
- 310 コンタクトホール
- 311 配線溝
- 312 密着層
- 313 金属膜
- 314 第2の金属配線
- 315 コンタクト
- 350 半導体基板
- 351 第1の金属膜
- 352 シリコン窒化膜
- 352A パターン化されたシリコン窒化膜
- 353 第1のシリコン酸化膜
- 353A パターン化された第1のシリコン酸化膜
- 354 有機膜
- 355 第2のシリコン酸化膜
- 355A パターン化された第2のシリコン酸化膜
- 356 窒化チタン膜
- 357 第1のレジストパターン
- 358 マスクパターン
- 359 第2のレジストパターン
- 360 コンタクトホール形成用開口部
- 361 コンタクトホール
- 362 配線溝
- 363 密着層
- 364 金属膜

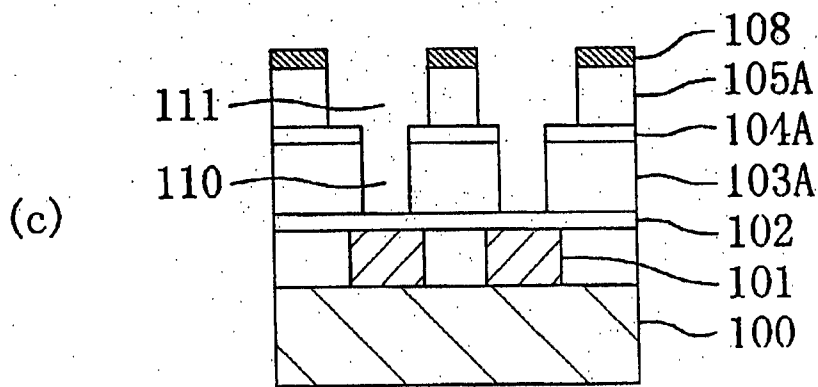
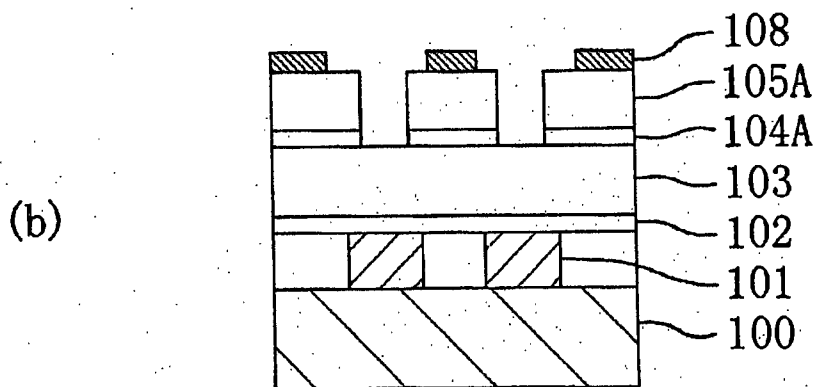
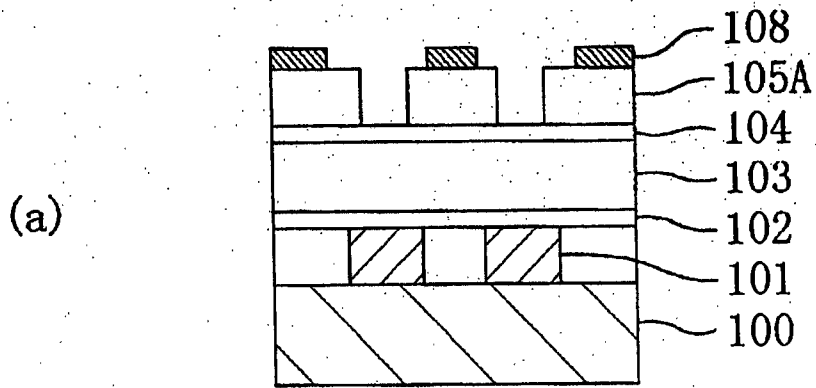
- 365 第2の金属配線
- 366 コンタクト
- 400 半導体基板
- 401 第1の金属配線
- 402 シリコン窒化膜
- 402A パターン化されたシリコン窒化膜
- 403 第1の低誘電率SOG膜
- 403A パターン化された第1の低誘電率SOG膜
- 404 有機含有シリコン酸化膜
- 404A パターン化された有機含有シリコン酸化膜
- 405 第2の低誘電率SOG膜
- 405A パターン化された第2の低誘電率SOG膜
- 406 窒化チタン膜
- 407 第1のレジストパターン
- 408 マスクパターン
- 409 第2のレジストパターン
- 410 ダメージ層
- 411 コンタクトホール
- 412 配線溝
- 413 密着層
- 414 金属膜
- 415 第2の金属膜
- 416 コンタクト

【書類名】 図面

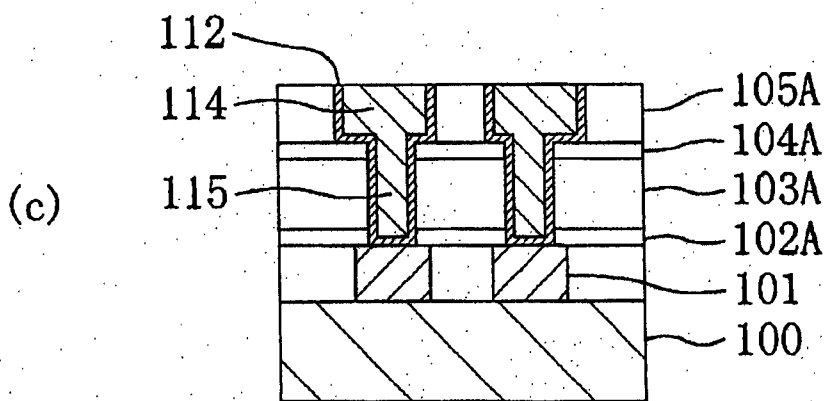
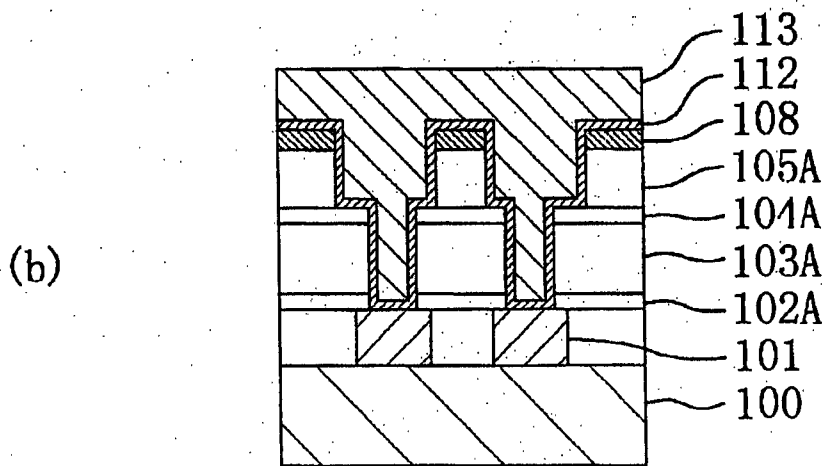
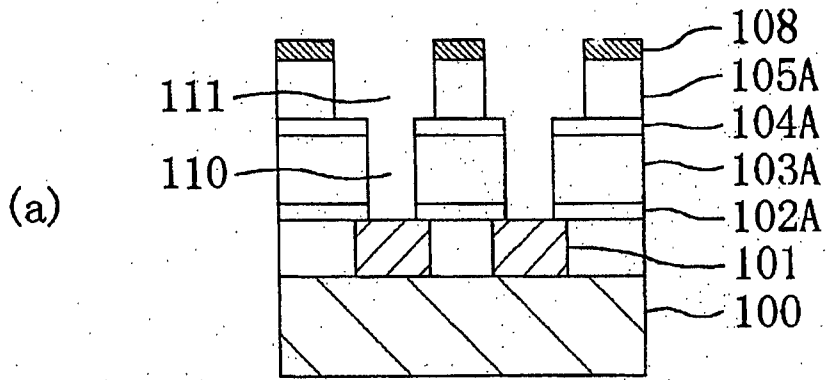
【図1】



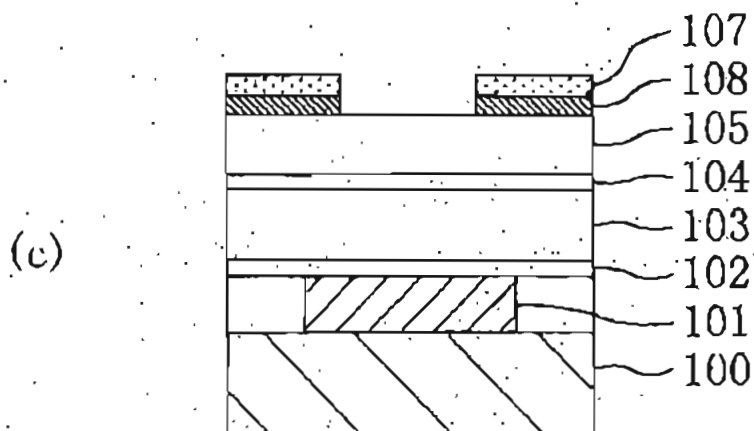
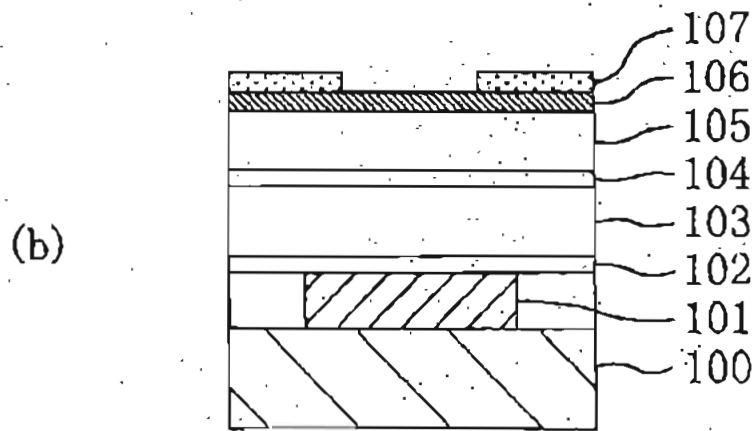
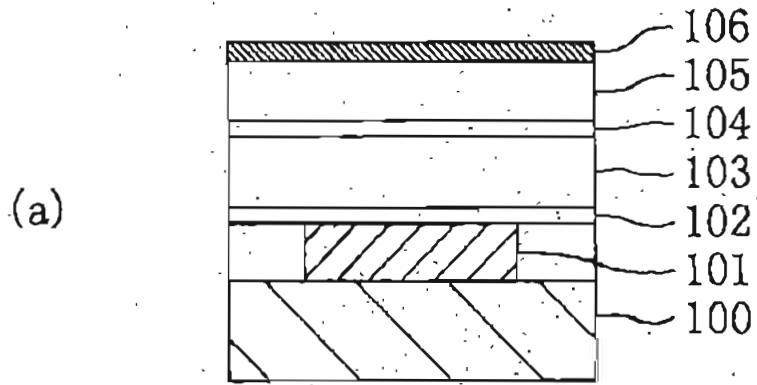
【图2】



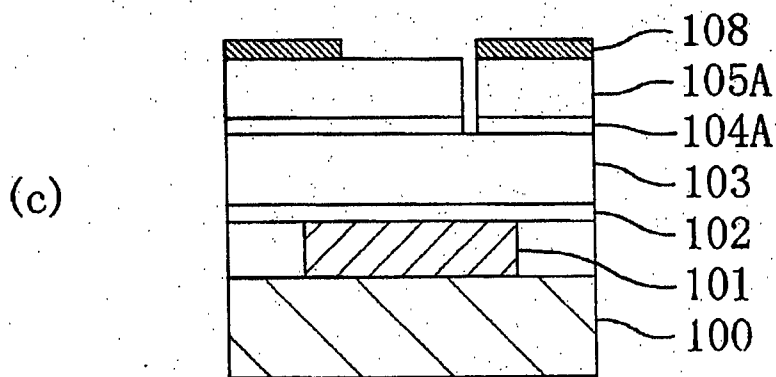
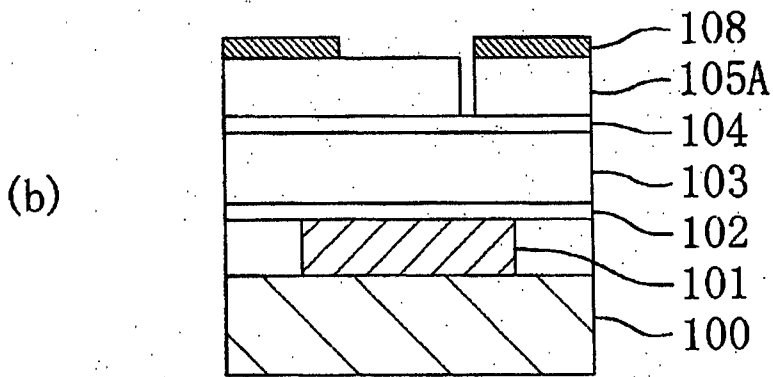
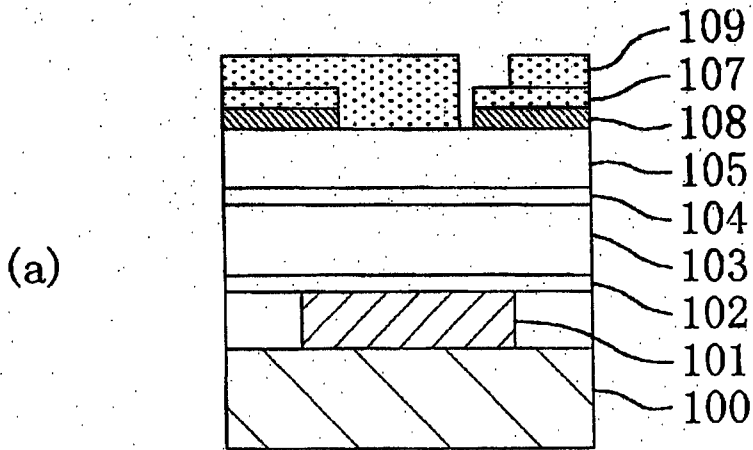
【図3】



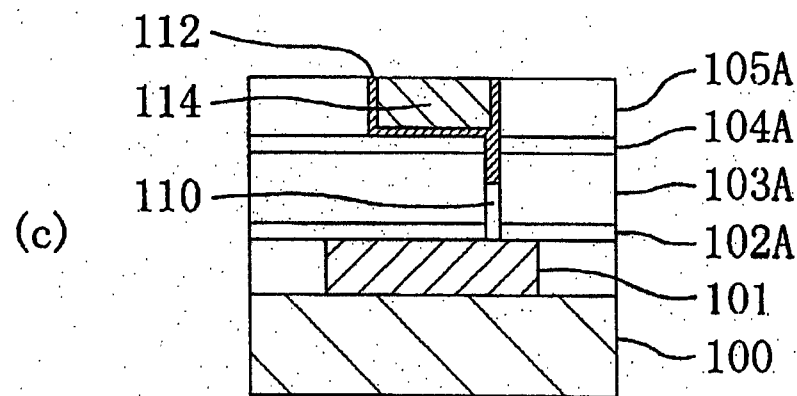
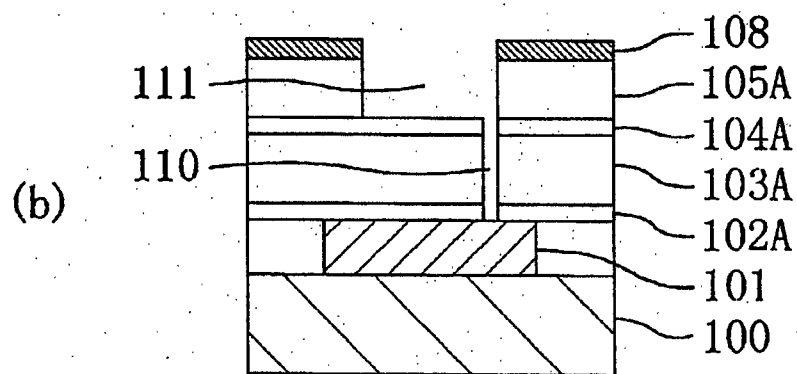
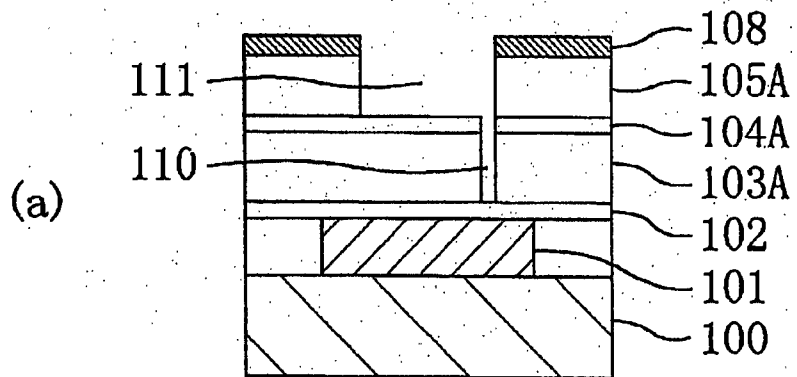
【图4】



【图5】

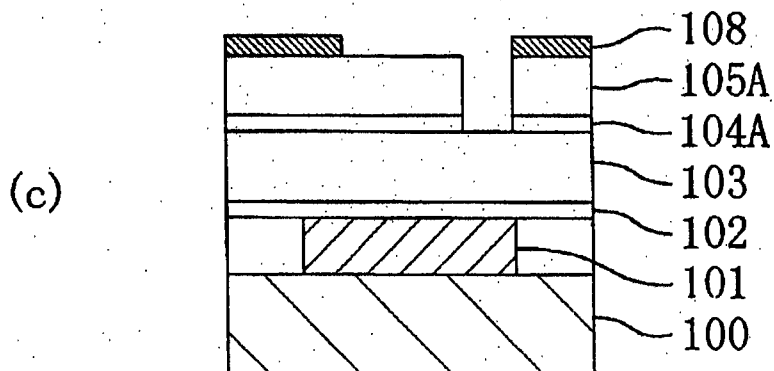
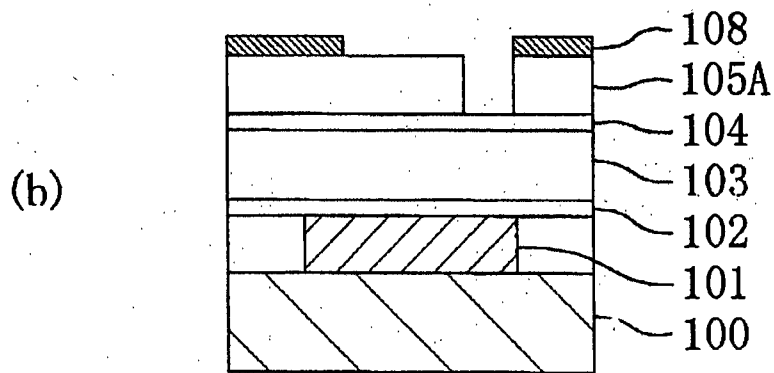
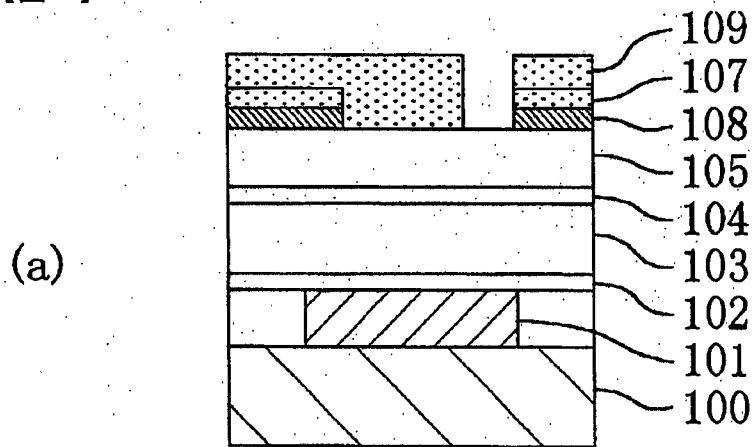


【图6】

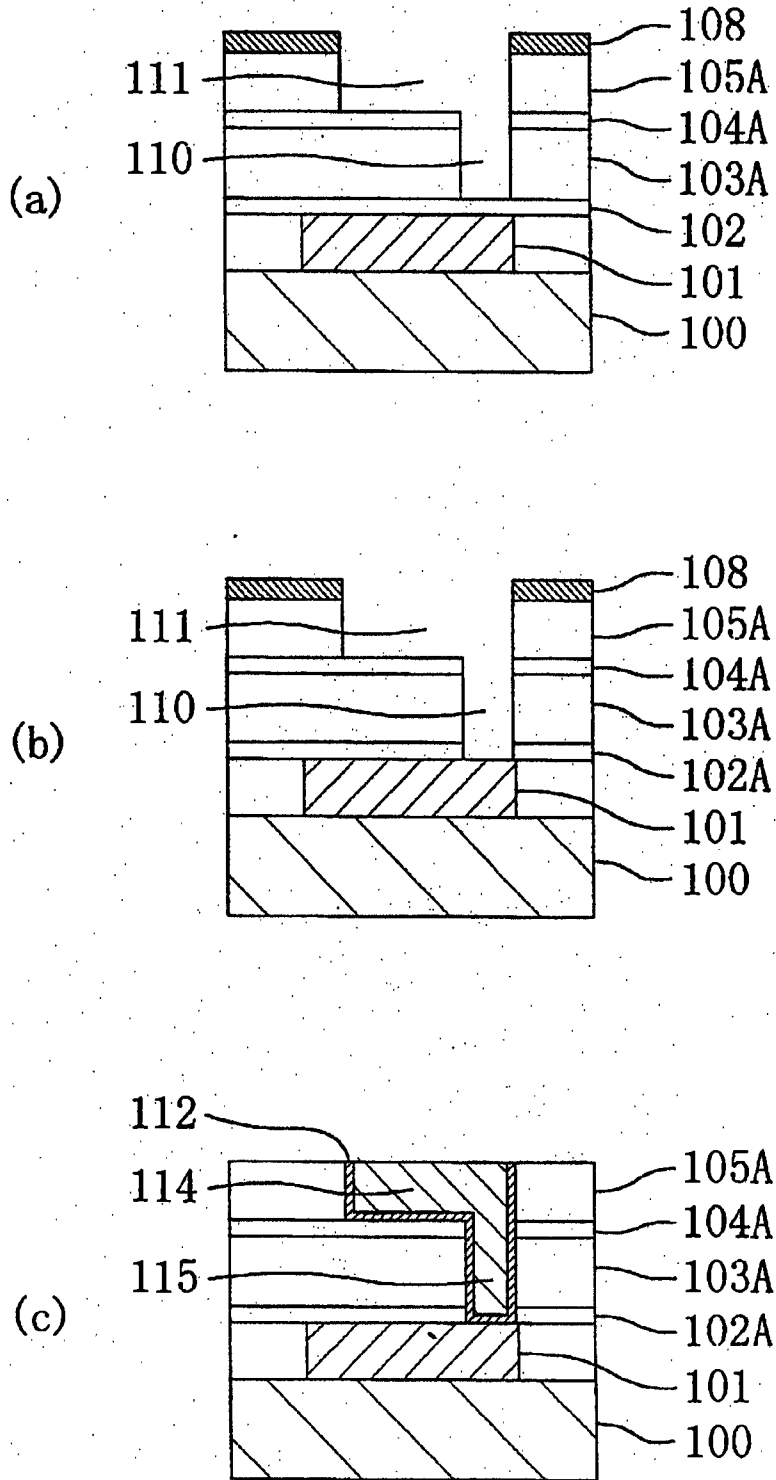




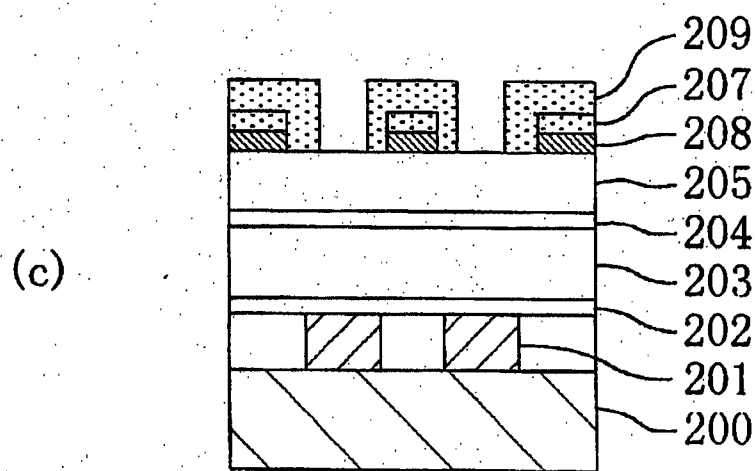
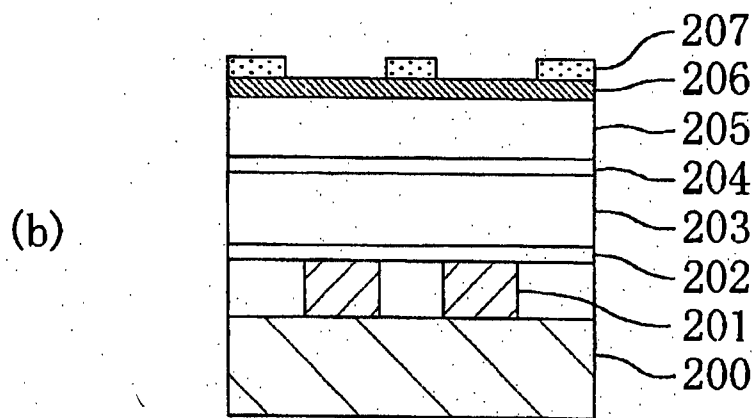
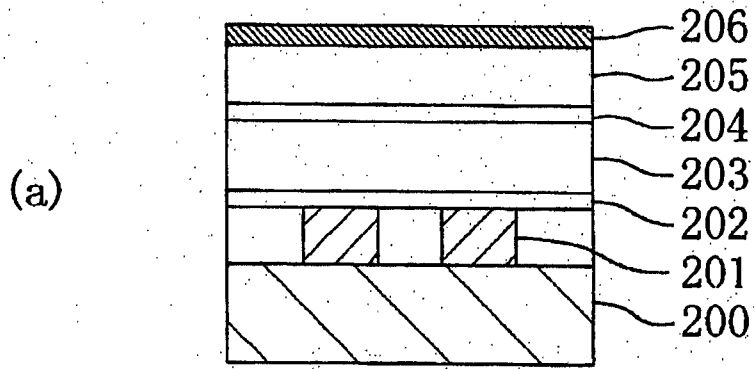
【图7】



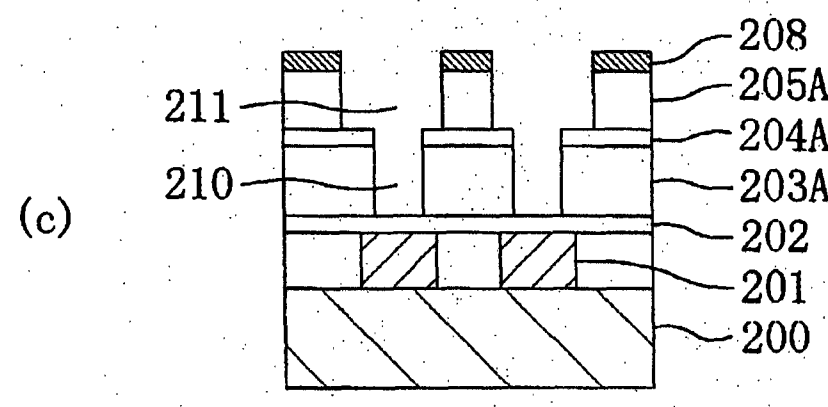
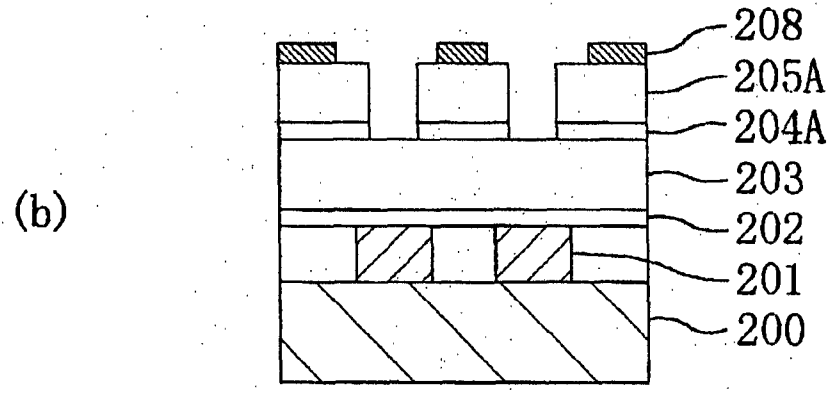
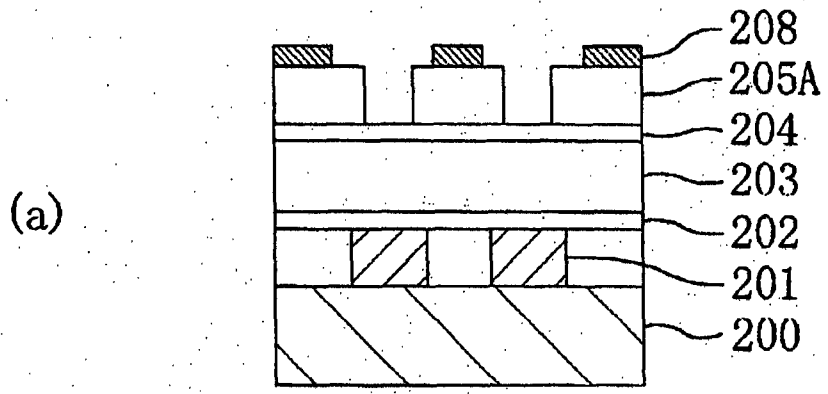
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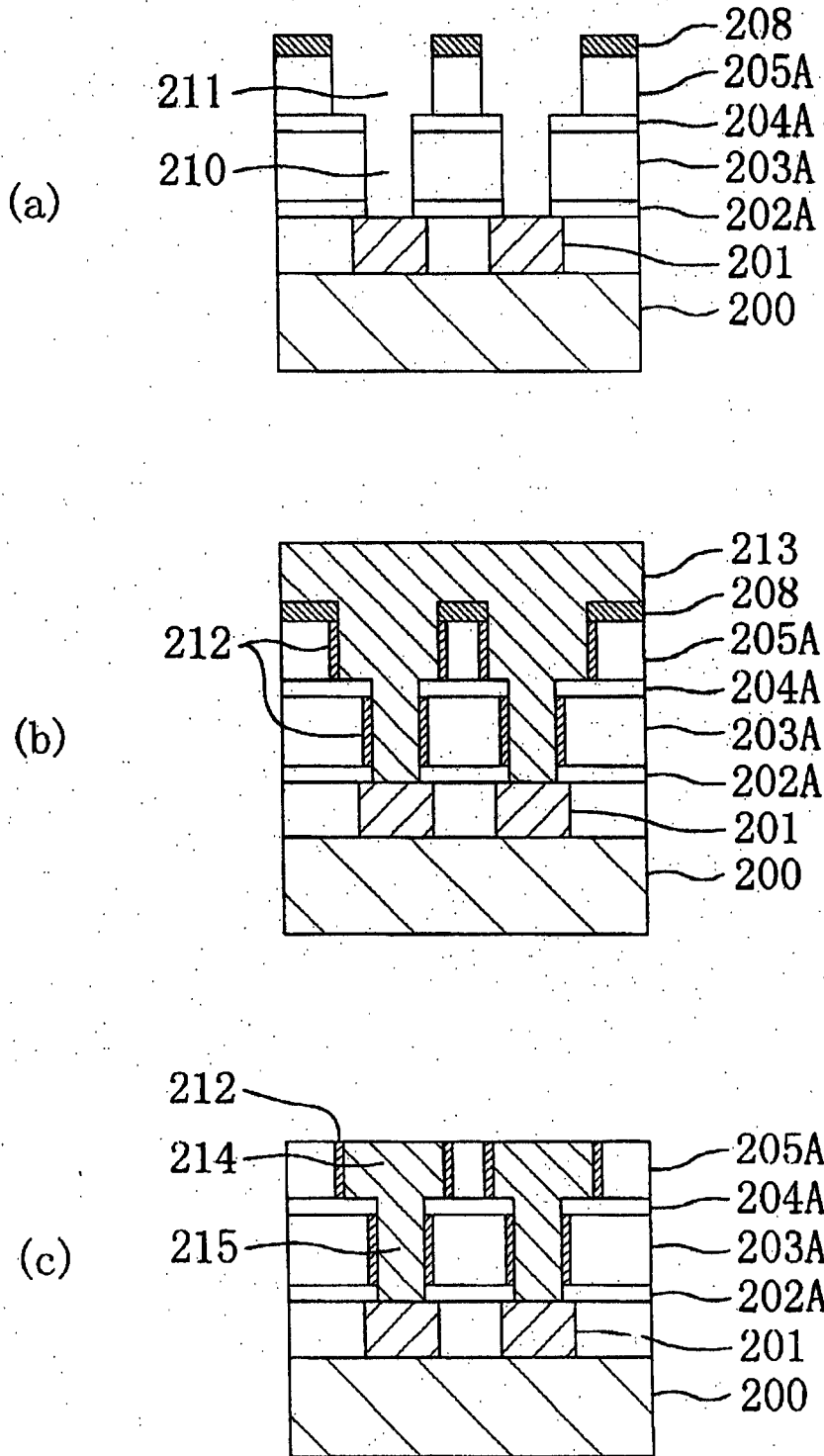
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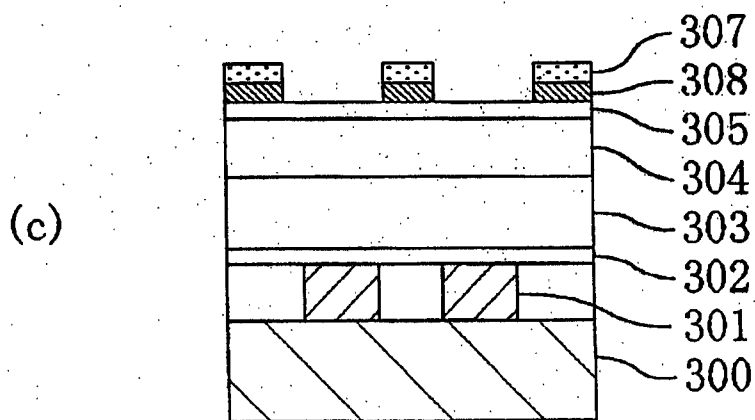
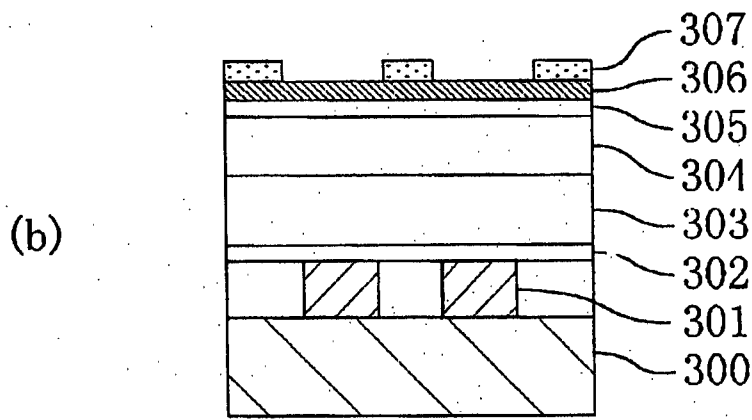
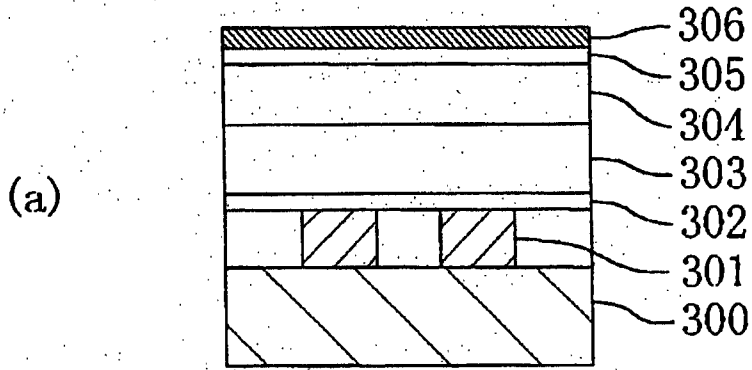
【図10】



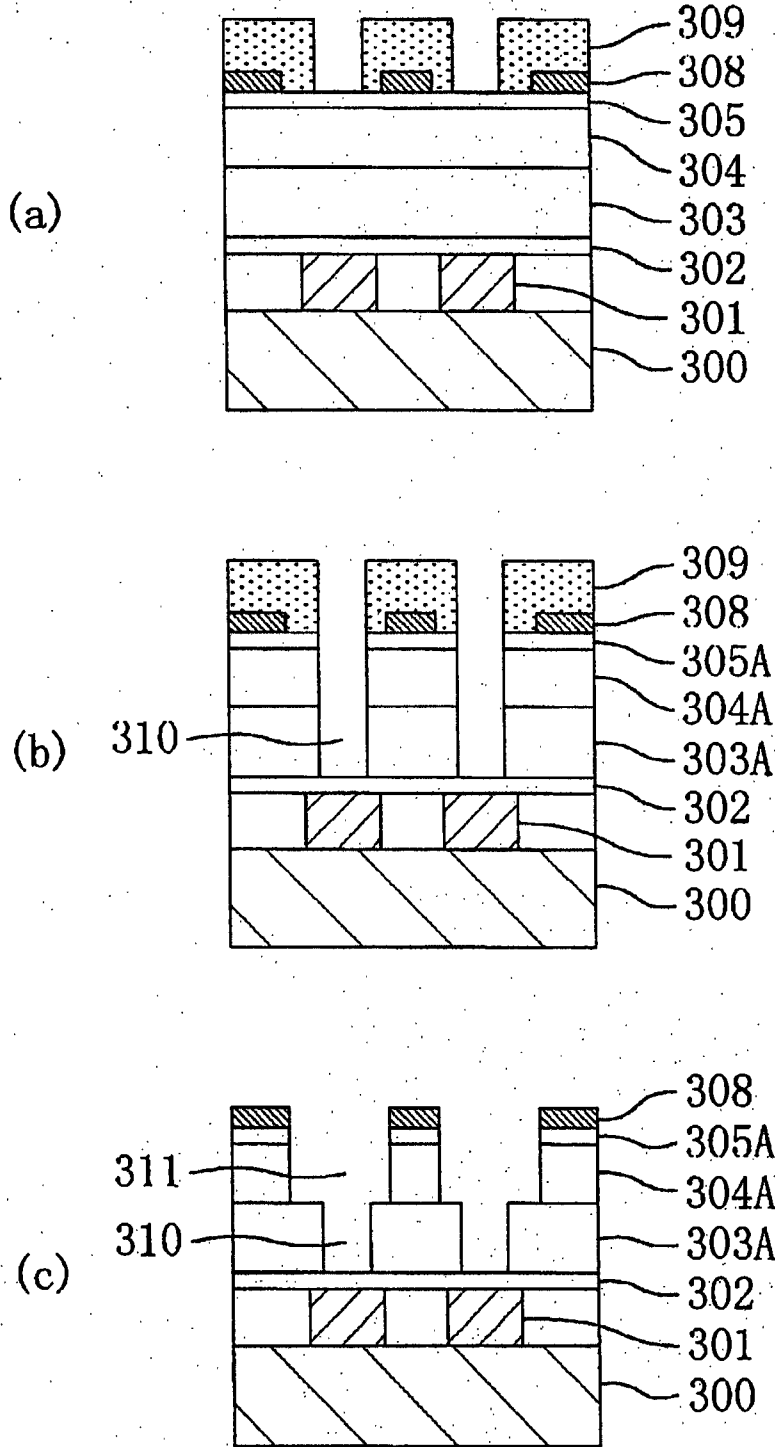
【図11】



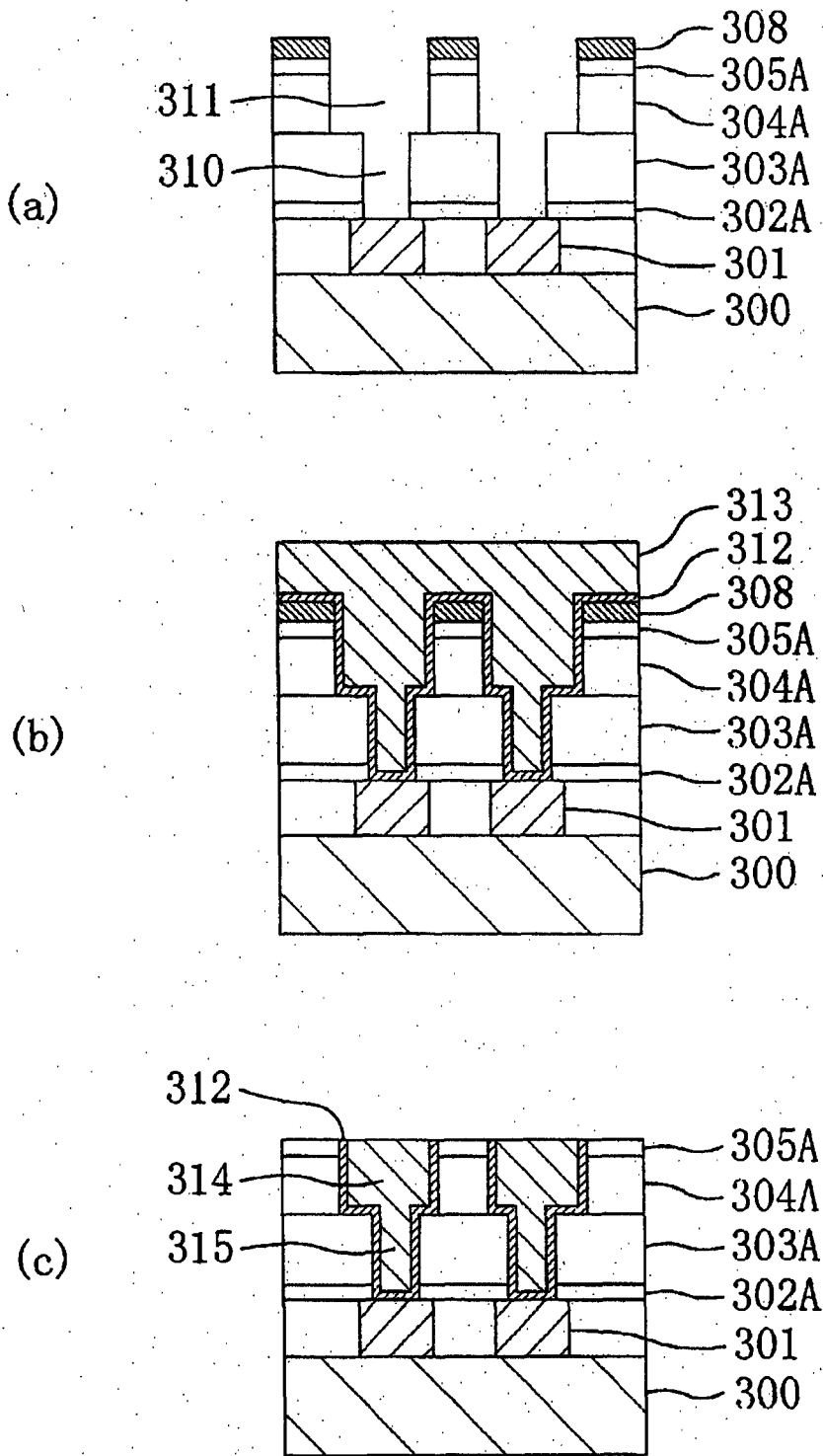
【図12】



【図 13】

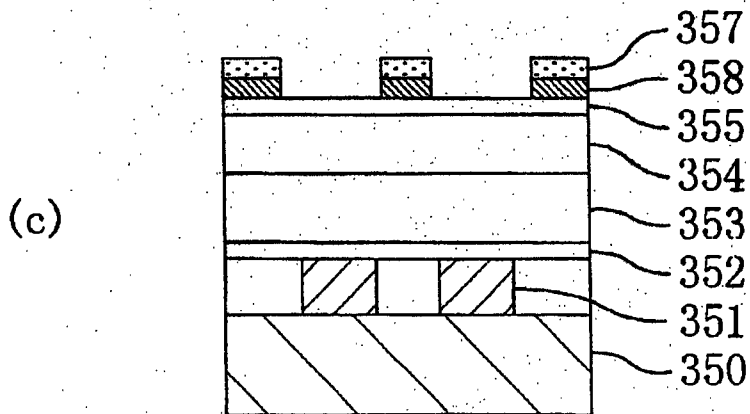
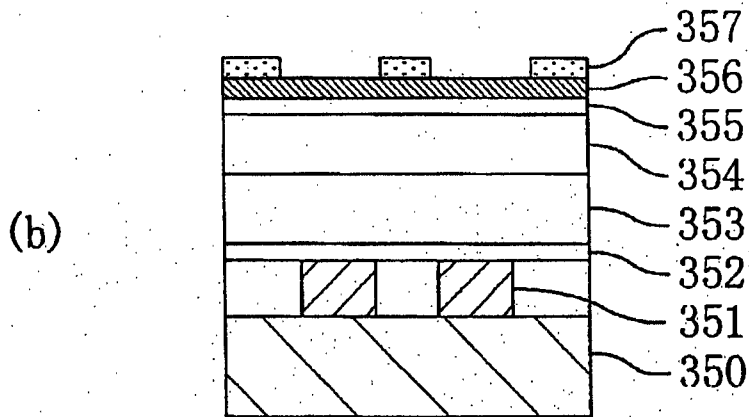
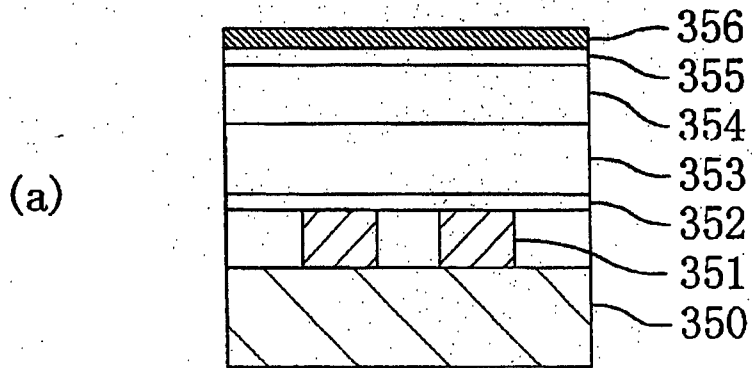


【図14】

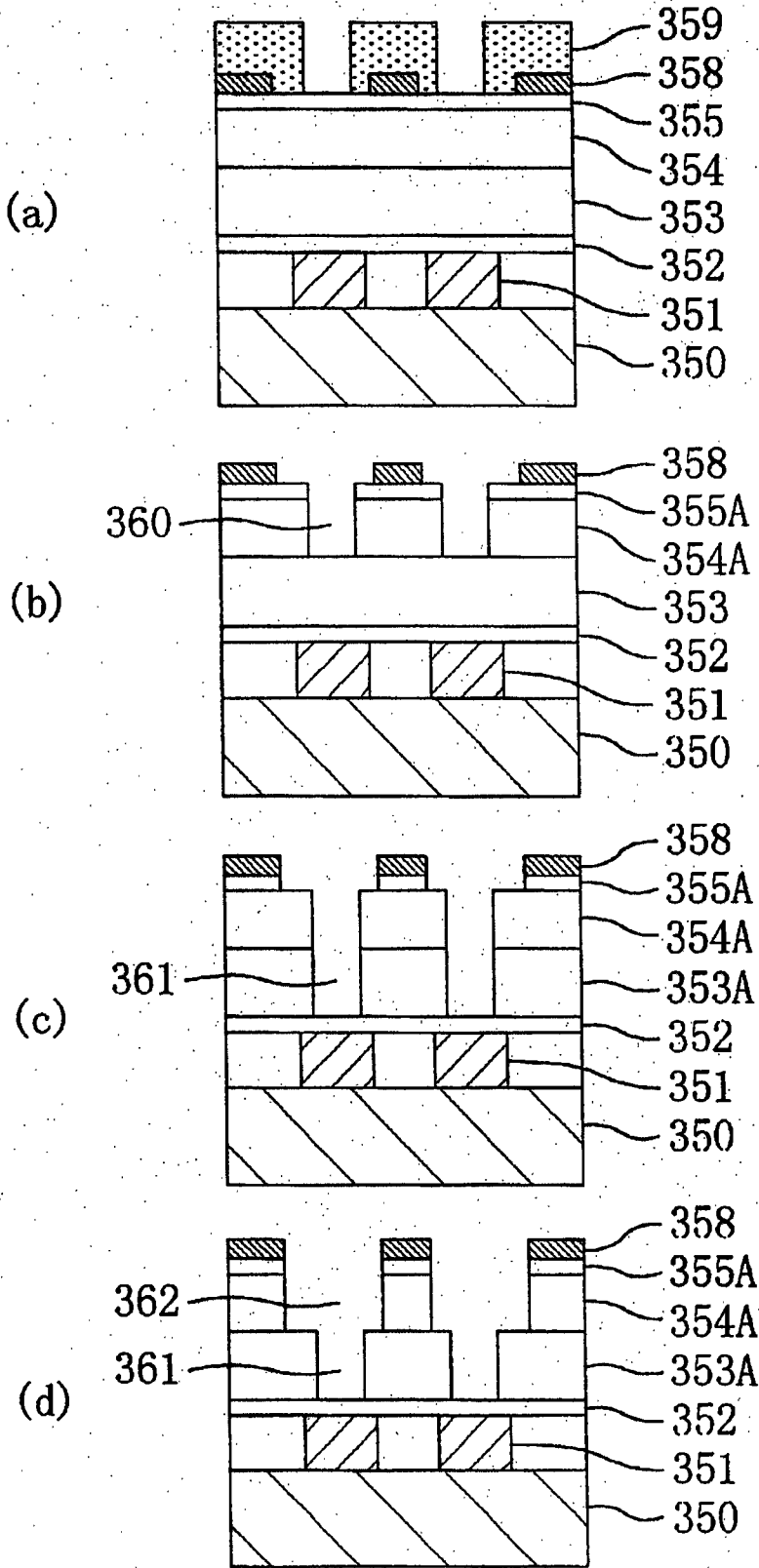




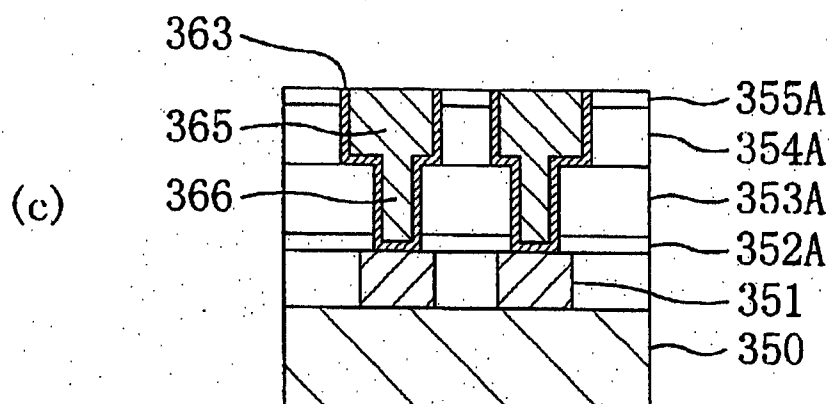
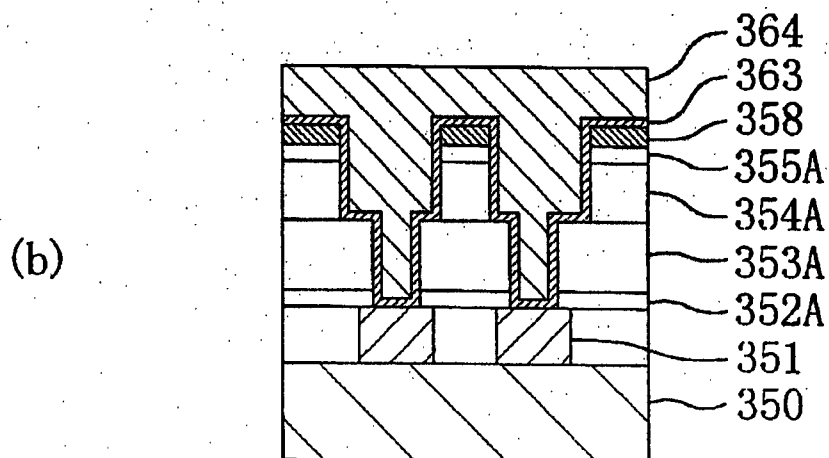
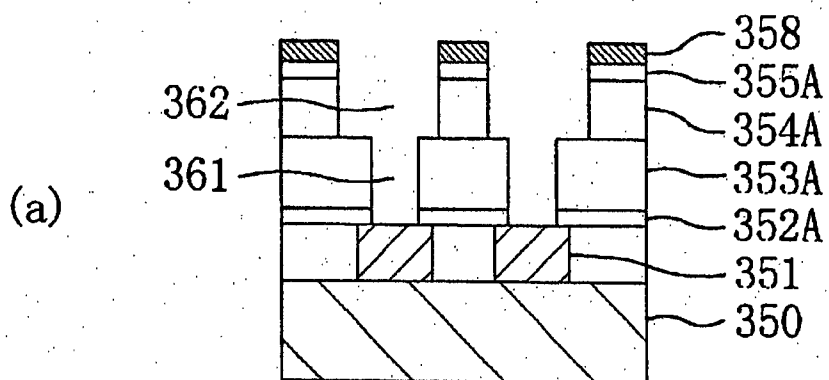
【図15】



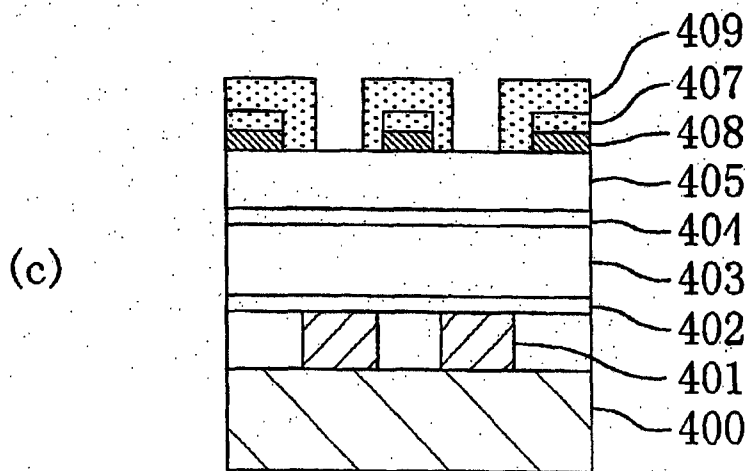
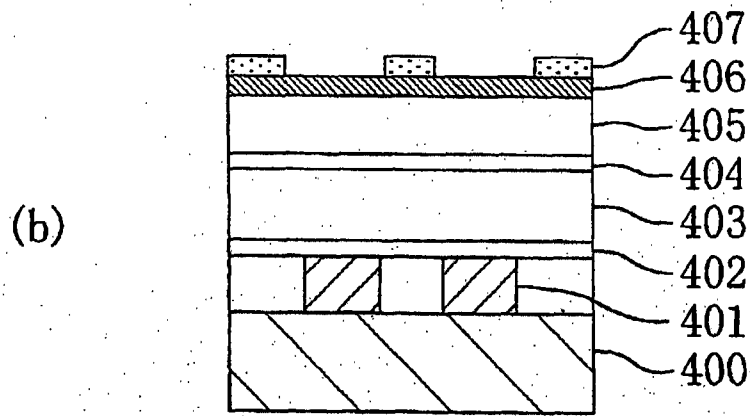
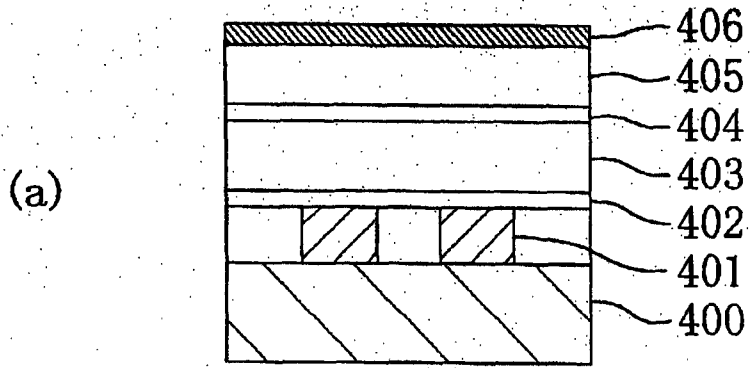
【図16】



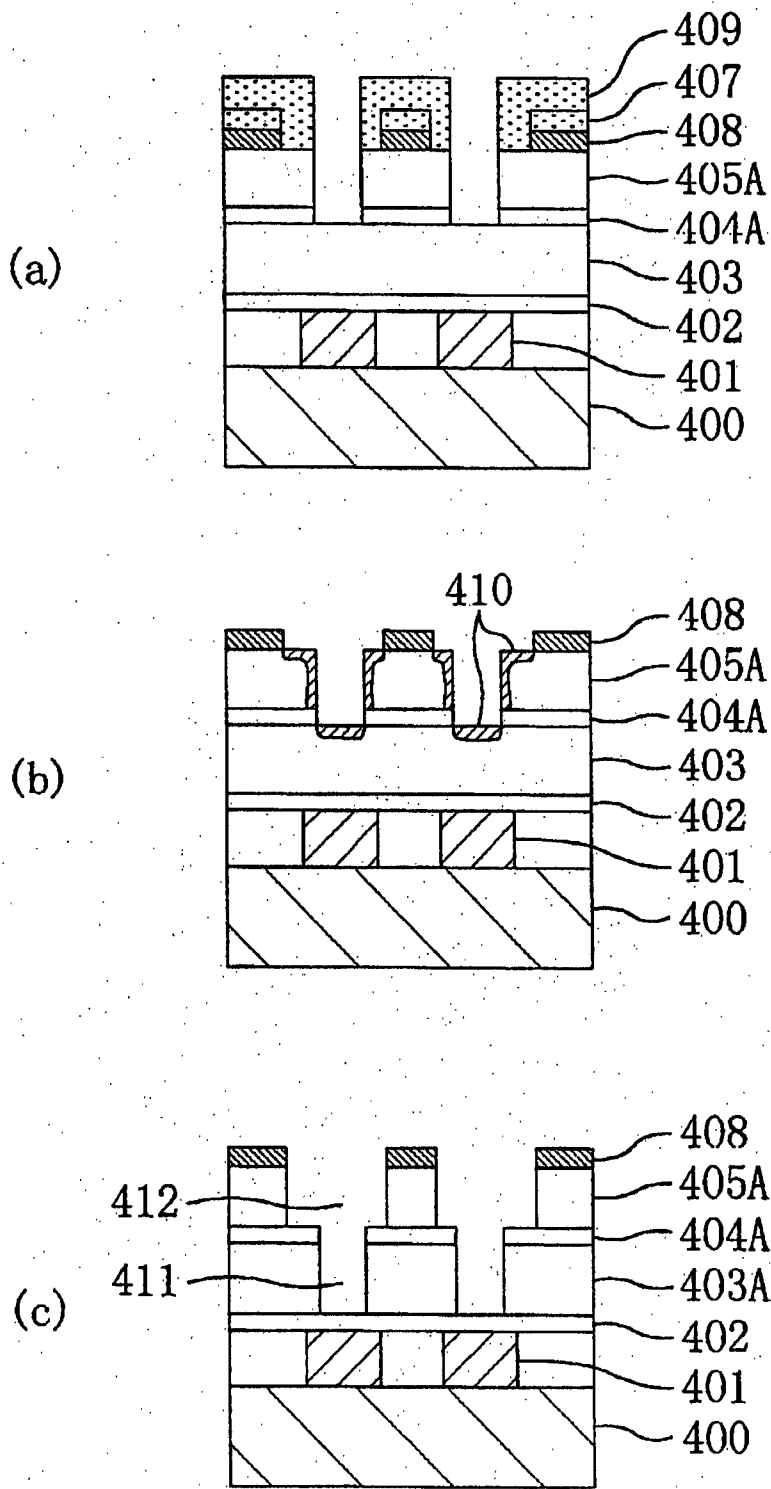
【图 17】



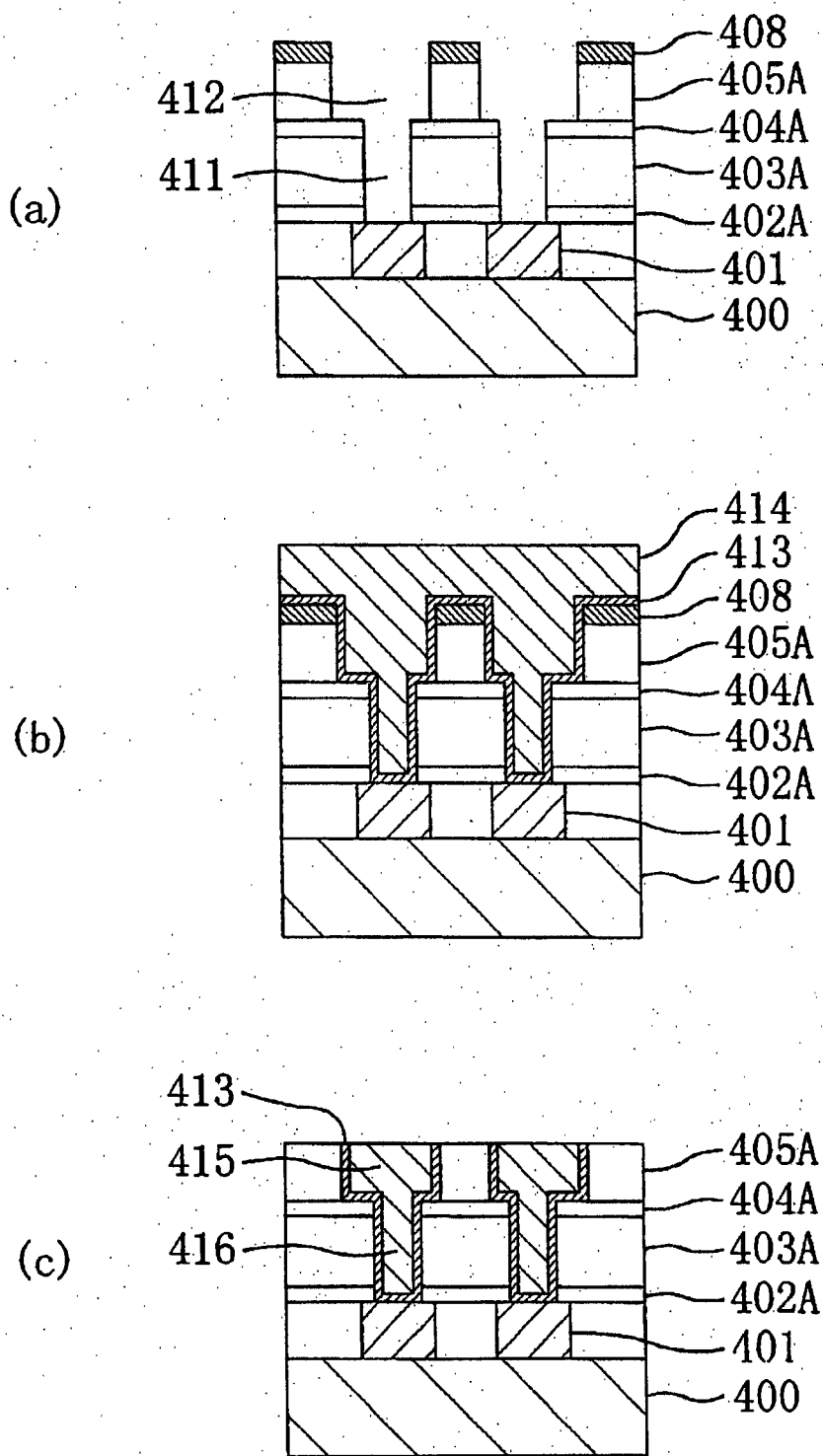
【図18】



【図19】



【図20】



特平10-079371

【書類名】 要約書

【要約】

【課題】 通常のレジストプロセスを採用して、比誘電率が低い層間絶縁膜を形成できるようにする。

【解決手段】 半導体基板100上の第1の金属配線101の上に、シリコン窒化膜102、第1の有機膜103、有機含有シリコン酸化膜104、第2の有機膜105及び窒化チタン膜106を順次堆積した後、窒化チタン膜106の上に形成された第1のレジストパターン107をマスクとして窒化チタン膜106に対してエッチングを行なってマスクパターン108を形成し、その後、第2の有機膜105の上に第2のレジストパターン109を形成する。第2の有機膜105に対して第2のレジストマスク109をマスクとしてエッチングを行なって、第2の有機膜105をパターン化すると共に第1及び第2のレジストパターン107、109を除去する。第2の有機膜105に対してマスクパターン108をマスクとしてエッチングして配線溝を形成すると共に、第1の有機膜103に対してパターン化された有機含有シリコン酸化膜104をマスクとしてエッチングしてコンタクトホールを形成する。

【選択図】 図1

特平10-079371

【書類名】 職権訂正データ  
【訂正書類】 特許願

<認定情報・付加情報>

【特許出願人】

【識別番号】 000005821

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特平10-079371

出願人履歴情報

識別番号 [000005821]

1. 変更年月日 1990年 8月28日  
[変更理由] 新規登録  
住所 大阪府門真市大字門真1006番地  
氏名 松下電器産業株式会社

Transaction History Date 1999-08-09

Date information retrieved from USPTO Patent

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GP 1763



Docket: 0819-0226

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of )  
 NOBUO AOI )  
 Serial No. 09/274,114 ) Group Art Unit: 1763  
 Filed: March 23, 1999 ) Examiner: Unassigned  
 For: METHOD FOR FORMING )  
 INTERCONNECTION STRUCTURE )

RECEIVED  
AUG 11 1999  
TC 1700 MAIL ROOM

Honorable Assistant Commissioner of Patents

Washington, D.C. 20231

Sir:

Transmitted herewith is an Information Disclosure Statement in the above-identified application.

[ X ] In the event applicant(s) has overlooked the need for any petition to effect the entry of the documents submitted herewith, it is respectfully requested that this be treated as such petition and that any necessary fees associated with this petition be charged to Deposit Account No. 19-2380.

[ X ] In the event applicant(s) has overlooked the need for any petition and fee for extension of time, and such extension is required, applicant(s) requests that this be considered a petition therefor and that such fee be charged to Deposit Account No. 19-2380.

[ X ] The Commissioner is hereby authorized to charge fees under 37 CFR 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c) and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment, to Deposit Account No. 19-2380. A duplicate copy of this sheet is attached.

CERTIFICATE OF MAILING

Respectfully submitted,

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 8-4-99

Oliver M. Fisher

Eric J. Robinson  
 Eric J. Robinson  
 Reg. No. 38,285  
 Sixbey, Friedman, Leedom & Ferguson, P.C.  
 8180 Greensboro Drive, Suite 800  
 McLean, Virginia 22102  
 (703) 790-9110

Docket: 0819-0226

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
NOBUO AOI	)	
Serial No. 09/274,114	)	Group Art Unit: 1763
Filed: March 23, 1999	)	Examiner: Unassigned
For: METHOD FOR FORMING	)	
INTERCONNECTION STRUCTURE	)	



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Washington, D.C. 20231

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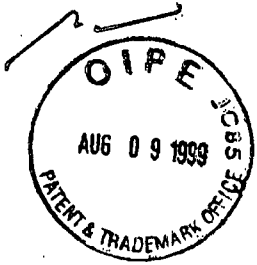
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Respectfully submitted,

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*H3*



- 1 -

Docket: 0819-0226

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of )  
 NOBUO AOI )  
 Serial No. 09/274,114 ) Group Art Unit: 1763  
 Filed: 03/23/1999 ) Examiner: Unassigned  
 For: METHOD FOR FORMING )  
 INTERCONNECTION STRUCTURE )

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INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner of Patents  
 Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith attached Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 19-2380. A duplicate copy of this sheet is attached.

Respectfully submitted,

*Eric J. Robinson*

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 Reg. No. 38,285

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 (703) 790-9110

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*Rose M. S. [Signature]*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of )  
 NOBUO AOI )  
 Serial No. 09/274,114 ) Group Art Unit: 1763  
 Filed: 03/23/1999 ) Examiner: Unassigned  
 For: METHOD FOR FORMING )  
 INTERCONNECTION STRUCTURE )



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INFORMATION DISCLOSURE STATEMENT


Honorable Assistant Commissioner of Patents  
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Sir:

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The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 19-2380. A duplicate copy of this sheet is attached.

Respectfully submitted,

  
 Eric J. Robinson  
 Reg. No. 38,285

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 (703) 790-9110

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Carol M. Fichth



Form PTO-1449  
(Rev. 8-83)

U.S. Department of Commerce  
Patent and Trademark Office

Atty. Docket No.:

Serial No.

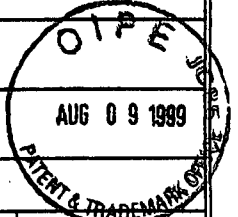
**INFORMATION DISCLOSURE STATEMENT**

(Use several sheets if necessary)

Applicant:

Filing Date:

Group:



**U.S. PATENT DOCUMENTS**

Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if approp.)
	5,651,855	07/29/97	Dennison et al.			
	5,110,712	05/05/92	Kessler et al.			

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**FOREIGN PATENT DOCUMENTS**

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	0 680 085 A1	11/02/95	EPO				
	0 425 787 A2	05/08/91	EPO				

**OTHER DOCUMENTS (Including Author, Title, Relevant Pages, Date, Place of Publication)**

	European Search Report dated July 1, 1999

Examiner \_\_\_\_\_ Date Considered \_\_\_\_\_

\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

# File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 1999-08-09

Document Title - List of References cited by applicant and considered by examiner

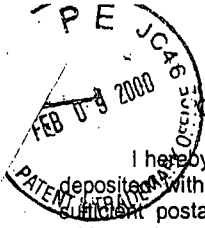
Page(s) - 2 of 2



## Other Prior Art

According to the information contained in form PTO-1449 or PTO-892, there are one or more other prior art/non-patent literature documents missing from the original file history record obtained from the United States Patent and Trademark Office. Upon your request we will attempt to obtain these documents from alternative resources. Please note that additional charges will apply for this service.

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Rose M. Fichtel

*Gen 176 #*  
*2-17-0*  
*Leifer*  
*B*

Docket No. 0819-226

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re PATENT Application of )  
Nobuo AOI )  
Serial No. 09/274,114 ) Group Art Unit: 1763  
Filed: March 23, 1999 ) Examiner: Unassigned  
For: METHOD FOR FORMING )  
INTERCONNECTION STRUCTURE )

**INFORMATION DISCLOSURE STATEMENT**


Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith attached Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above-identified application. Copies of the references are submitted herewith in accordance with 37 C.F.R. 1.98(a).

The Commissioner is hereby authorized to charge fees under 37 CFR 1.17 which may be required now or hereafter, or credit any overpayment, to Deposit Account No. 19-2380. A duplicate copy of this paper is attached.

Respectfully submitted,

  
Eric J. Robinson  
Registration No. 38,285  
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McLean, Virginia 22102  
(703) 790-9110  
(703) 883-0370 (Fax)





<b>Notice of Allowability</b>	Application No. <b>09/274,114</b>	Applicant(s) <b>AOI</b>
	Examiner <b>Lynette T. Umez-Eronini</b>	Group Art Unit <b>1765</b>

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

- This communication is responsive to \_\_\_\_\_.
- The allowed claim(s) is/are 1-15.
- The drawings filed on Mar 23, 1999 are acceptable.
- Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
  - All  Some\*  None of the CERTIFIED copies of the priority documents have been
    - received.
    - received in Application No. (Series Code/Serial Number) \_\_\_\_\_.
    - received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
  - \*Certified copies not received: \_\_\_\_\_.
- Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

- Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
- Applicant MUST submit NEW FORMAL DRAWINGS
  - because the originally filed drawings were declared by applicant to be informal.
  - including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. \_\_\_\_\_.
  - including changes required by the proposed drawing correction filed on \_\_\_\_\_, which has been approved by the examiner.
  - including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

- Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

**Attachment(s)**

- Notice of References Cited, PTO-892
- Information Disclosure Statement(s), PTO-1449, Paper No(s). 3 & 4
- Notice of Draftsperson's Patent Drawing Review, PTO-948
- Notice of Informal Patent Application, PTO-152
- Interview Summary, PTO-413
- Examiner's Amendment/Comment
- Examiner's Comment Regarding Requirement for Deposit of Biological Material
- Examiner's Statement of Reasons for Allowance

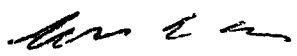
Art Unit: 1765

**REASONS FOR ALLOWANCE**

1. The following is an examiner's statement of reasons for allowance: Prior art lacks the steps of forming an interconnection structure as recited in the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is (703) 306-9074.

  
BENJAMIN L. UTECH  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 1700

ltue

October 6, 2000

**Notice of References Cited**

Application No. 09/274,114	Applicant(s) AOI
Examiner Lynette T. Umez-Eronini	Group Art Unit 1765

Page 1 of 1

**U.S. PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	5,518,963	5/1996	PARK	438	624
B	5,635,423	6/1997	HUANG ET AL.	438	638
C	5,702,982	12/1997	LEE ET AL.	438	620
D					
E					
F					
G					
H					
I					
J					
K					
L					
M					

**FOREIGN PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

**NON-PATENT DOCUMENTS**

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U		
V		
W		
X		

**NOTICE OF DRAFTPERSON'S  
PATENT DRAWING REVIEW**

The drawing filed (insert date) 03/23/99 are:

- A.  not objected to by the Draftperson under 37 CFR 1.84 or 1.152.  
 B.  objected to by the Draftperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings where necessary. Corrected drawings must be submitted according to the instructions on the back of this notice.

<p><b>1. DRAWINGS.</b> 37 CFR 1.84(a): Acceptable categories of drawings:                  Black ink. Color.  <input type="checkbox"/> Color drawing are not acceptable until petition is granted.                  Fig.(s) _____  <input type="checkbox"/> Pencil and non black ink is not permitted. Fig(s) _____</p> <p><b>2. PHOTOGRAPHS.</b> 37 CFR 1.84(b)  <input type="checkbox"/> Photographs are not acceptable until petition is granted,  <input type="checkbox"/> 3 full-tone sets are required. Fig(s) _____  <input type="checkbox"/> Photographs not properly mounted (must bristol board or photographic double-weight paper). Fig(s) _____  <input type="checkbox"/> Poor quality (half-tone). Fig(s) _____</p> <p><b>3. TYPE OF PAPER.</b> 37 CFR 1.84(e)  <input type="checkbox"/> Paper not flexible, strong, white and durable.                  Fig.(s) _____  <input type="checkbox"/> Erasures, alterations, overwritings, interlineations, folds, copy machine marks not acceptable. (too thin)  <input type="checkbox"/> Mylar, vellum paper is not acceptable (too thin).                  Fig(s) _____</p> <p><b>4. SIZE OF PAPER.</b> 37 CFR 1.84(F): Acceptable sizes:  <input type="checkbox"/> 21.0 cm by 29.7 cm (DIN size A4)  <input type="checkbox"/> 21.6 cm by 27.9 cm (8 1/2 x 11 inches)  <input type="checkbox"/> All drawings sheets not the same size.                  Sheet(s) _____</p> <p><b>5. MARGINS.</b> 37 CFR 1.84(g): Acceptable margins:                  Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm                  SIZE: A4 Size                  Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm                  SIZE: 8 1/2 x 11  <input type="checkbox"/> Margins not acceptable. Fig(s) _____  <input type="checkbox"/> Top (T) _____ Left (L)  <input type="checkbox"/> Right (R) _____ Bottom (B)</p> <p><b>6. VIEWS.</b> CFR 1.84(h)                  REMINDER: Specification may require revision to correspond to drawing changes.  <input type="checkbox"/> Views connected by projection lines or lead lines.                  Fig.(s) _____                  Partial views. 37 CFR 1.84(h)(2)  <input type="checkbox"/> Brackets needed to show figure as one entity.                  Fig.(s) _____  <input type="checkbox"/> Views not labeled separately or properly.                  Fig.(s) _____  <input type="checkbox"/> Enlarged view not labeled separately or properly.                  Fig.(s) _____</p>	<p><b>7. SECTIONAL VIEWS.</b> 37 CFR 1.84(h)(3)  <input type="checkbox"/> Hatching not indicated for sectional portions of an object.                  Fig.(s) _____  <input type="checkbox"/> Sectional designation should be noted with Arabic or Roman numbers. Fig.(s) _____</p> <p><b>8. ARRANGEMENT OF VIEWS.</b> 37 CFR 1.84(i)  <input type="checkbox"/> Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned, so that the top becomes the right side, except for graphs. Fig.(s) _____  <input type="checkbox"/> Views not on the same plane on drawing sheet. Fig.(s) _____</p> <p><b>9. SCALE.</b> 37 CFR 1.84(k)  <input type="checkbox"/> Scale not large enough to show mechanism with crowding when drawing is reduced in size to two-thirds in reproduction.                  Fig.(s) _____</p> <p><b>10. CHARACTER OF LINES, NUMBERS, &amp; LETTERS.</b> 37 CFR 1.84(l)  <input type="checkbox"/> Lines, numbers &amp; letters not uniformly thick and well defined, clean, durable and black (poor line quality).                  Fig.(s) _____</p> <p><b>11. SHADING.</b> 37 CFR 1.84(m)  <input type="checkbox"/> Solid black areas pale. Fig.(s) _____  <input type="checkbox"/> Solid black shading not permitted. Fig.(s) _____  <input type="checkbox"/> Shade lines, pale, rough and blurred. Fig.(s) _____</p> <p><b>12. NUMBERS, LETTERS, &amp; REFERENCE CHARACTERS.</b> 37 CFR 1.48(p)  <input type="checkbox"/> Numbers and reference characters not plain and legible.                  Fig.(s) _____  <input type="checkbox"/> Figure legends are poor. Fig.(s) _____  <input type="checkbox"/> Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(3) Fig.(s) _____  <input type="checkbox"/> English alphabet not used. 37 CFR 1.84(p)(3) Fig.(s) _____  <input type="checkbox"/> Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig.(s) _____</p> <p><b>13. LEAD LINES.</b> 37 CFR 1.84(q)  <input type="checkbox"/> Lead lines cross each other. Fig.(s) _____  <input type="checkbox"/> Lead lines missing. Fig.(s) _____</p> <p><b>14. NUMBERING OF SHEETS OF DRAWINGS.</b> 37 CFR 1.48(t)  <input type="checkbox"/> Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Fig.(s) _____</p> <p><b>15. NUMBERING OF VIEWS.</b> 37 CFR 1.84(u)  <input type="checkbox"/> Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig.(s) _____</p> <p><b>16. CORRECTIONS.</b> 37 CFR 1.84(w)  <input type="checkbox"/> Corrections not made from PTO-948 dated _____</p> <p><b>17. DESIGN DRAWINGS.</b> 37 CFR 1.152  <input type="checkbox"/> Surface shading shown not appropriate. Fig.(s) _____  <input type="checkbox"/> Solid black shading not used for color contrast.                  Fig.(s) _____</p>
-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------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COMMENTS

Draftsman: **Son Lam**  
 (703)308-0366

REVIEWER \_\_\_\_\_ DATE 10/06/00 TELEPHONE NO. \_\_\_\_\_

ATTACHMENT TO PAPER NO. \_\_\_\_\_





UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office

**NOTICE OF ALLOWANCE AND ISSUE FEE DUE**

IM61/1010

GERALD J FERGUSON JR.  
SIXBEY FRIEDMAN LEEDOM & FERGUSON  
8180 GREENSBORO DRIVE  
SUITE 800  
MCLEAN VA 22102

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/274,114	03/23/99	015	UMEZ BRONINI, L	1765 10/10/00
First Named Applicant	AOI,		35 USC 154(b) term ext. =	0 Days.

TITLE OF INVENTION: METHOD FOR FORMING INTERCONNECTION STRUCTURE

ATTY'S DOCKET NO.	CLASS/SUBCLASS	BATCH NO.	APPL. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
1 0819-226	438-700,000	T53	UTILITY	NO	\$1240.00	01/10/01

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.**

**THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.**

**HOW TO RESPOND TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status; or
- B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- A. Pay FEE DUE shown above, or
- B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

PATENT AND TRADEMARK OFFICE COPY

**AT B—ISSUE FEE TRANSMITTAL**

Fee, to: **Box ISSUE-FEE  
 Assistant Commissioner for Patents  
 Washington, D.C. 20231**



B #

ed for transmitting the ISSUE FEE. Blocks 1  
 of further correspondence including the Issue Fee  
 of maintenance fees will be mailed to the current  
 correspondence address as indicated below or directed otherwise in Block 1; by (a)  
 specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for  
 maintenance fee notifications.

Note: The certificate of mailing below is not valid for domestic  
 mailings of the Issue Fee Transmittal. This certificate cannot be used  
 for any other accompanying papers. Each additional paper, such as an  
 assignment or formal drawing, must have its own certificate of mailing.

**Certificate of Mailing**

I hereby certify that this Issue Fee Transmittal is being deposited with  
 the United States Postal Service with sufficient postage for first class  
 mail in an envelope addressed to the Box Issue Fee address above on  
 the date indicated below.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly make-up with any corrections or use Block 1)

IM51/1010

**GERALD J FERGUSON JR  
 SIXBEY FRIEDMAN LEEDOM & FERGUSON  
 8180 GREENSBORO DRIVE  
 SUITE 800  
 MCLEAN VA 22102**

Rose M. Fichtel (Depositor's name)

*Rose M Fichtel* (Signature)

January 8, 2001 (Date)

APPLICATION NO.	FILED DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/274,114	03/23/99	015	UMEZ KRONINI, L	1765 10/10/00
First Named Applicant	AOI,		35 USC 154(b) term ext. = 0 Days.	

TITLE OF INVENTION **METHOD FOR FORMING INTERCONNECTION STRUCTURE**

01/16/2001 EEKUBAY2 00000201 09274114  
 01 FC:142 1240.00 OP

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
1	0819-226	438-700.000	T53 UTILITY	NO	\$1240.00	01/10/01

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).  
 Use of PTO form(s) and Customer Number are recommended, but not required.

- Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- "Fee Address" indication (or "Fee Address" indication form PTO/SB/47) attached.

2. For printing on the patent front page, list  
 (1) the names of up to 3 registered patent  
 attorneys or agents OR, alternatively, (2)  
 the name of a single firm (having as a  
 member a registered attorney or agent)  
 and the names of up to 2 registered patent  
 attorneys or agents. If no name is listed, no  
 name will be printed.

- 1 Eric J. Robinson
- 2 Nixon Peabody LLP
- 3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type).  
 PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent.  
 Inclusion of assignee data is only appropriate when an assignment has been previously submitted to  
 the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for  
 filing an assignment.

(A) NAME OF ASSIGNEE  
Matsushita Electric Industrial Co., Ltd.  
 (B) RESIDENCE: (CITY & STATE OR COUNTRY)  
Osaka, Japan  
 Please check the appropriate assignee category indicated below (will not be printed on the patent)  
 Individual  corporation or other private group entity  government

4a. The following fees are enclosed (make check payable to Commissioner  
 of Patents and Trademarks):

- Issue Fee
- Advance Order - # of Copies 10

4b. The following fees or deficiency in these fees should be charged to:

- DEPOSIT ACCOUNT NUMBER 19-2380  
 (ENCLOSE AN EXTRA COPY OF THIS FORM)
- Issue Fee
- Advance Order - # of Copies \_\_\_\_\_

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) [Signature] (Date) \_\_\_\_\_  
 Reg. No. 38,285

NOTE: The Issue Fee will not be accepted from anyone other than the applicant, a registered attorney  
 or agent, or the assignee or other party in interest as shown by the records of the Patent and  
 Trademark Office.

**Burden Hour Statement:** This form is estimated to take 0.2 hours to complete. Time will vary  
 depending on the needs of the individual case. Any comments on the amount of time required  
 to complete this form should be sent to the Chief Information Officer, Patent and Trademark  
 Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS  
 ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for  
 Patents, Washington D.C. 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection  
 of information unless it displays a valid OMB control number.

01/11/2001 EEKUBAY2 00000030 09274114  
~~01 FC:141~~ 1240.00 OP  
 02 FC:561 30.00 OP

Adjustment date: 01/16/2001 EEKUBAY2  
 01/11/2001 EEKUBAY2 00000030 09274114  
 01 FC:141 -1240.00 OP

TRANSMIT THIS FORM WITH FEE

# File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2001-03-06

Document Title - USPTO Grant

(staple to front of application)

USPTO

1700 INTERNAL TRANSFER REQUEST FOR S.N.

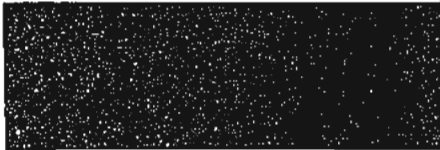
09/274,114

DATE: <u>10/5/00</u>	FROM: <u>ANITA ALANKO</u> (print name)
FORWARD TO: A. Art Unit: <u>1765</u> B. Class: <u>438</u> C Subclass: <u>689+</u>	REASON(S): A. You had Parent <input type="checkbox"/> (check box) B. See Spec. page(s) _____ C. See Claims _____

REASONS *forming interconnect for semiconductor*

DATE: _____	FROM: _____ (print name)
FORWARD TO: A. Art Unit: _____ B. Class: _____ C Subclass: _____	REASON(S): A. You had Parent <input type="checkbox"/> (check box) B. See Spec. page(s) _____ C. See Claims _____

REASONS

DATE: _____	FROM: _____ (print name)
FORWARD TO: 1700 CLASSIFICATION UNIT 	REASON(S): A. You had Parent <input type="checkbox"/> (check box) B. See Spec. pages(s) _____ C. See Claims _____

REASONS

DISPOSITION BY 1700 CLASSIFICATION UNIT

DATE: _____	CLASSIFIER: _____
FORWARD TO: A. Art Unit: _____ B. Class: _____ C Subclass: _____	REASON(S): A. You had Parent <input type="checkbox"/> (check box) B. See Spec. page(s) _____ C. See Claims _____

REASONS

**PATENT APPLICATION FEE DETERMINATION RECORD**  
Effective November 10, 1998

Application or Docket Number

**CLAIMS AS FILED - PART I**

(Column 1) (Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	15 minus 20 = *	
INDEPENDENT CLAIMS	4 minus 3 = *	1
MULTIPLE DEPENDENT CLAIM PRESENT		

\* If the difference in column 1 is less than zero, enter "0" in column 2.

SMALL ENTITY TYPE

OR OTHER THAN SMALL ENTITY

RATE	FEE	OR	RATE	FEE
	380.00			760.00
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	78
+130=		OR	+260=	
TOTAL		OR	TOTAL	858

**CLAIMS AS AMENDED - PART II**

(Column 1) (Column 2) (Column 3)

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

SMALL ENTITY

OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

(Column 1) (Column 2) (Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

RATE ADDITIONAL FEE

RATE ADDITIONAL FEE

X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

(Column 1) (Column 2) (Column 3)

AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

RATE ADDITIONAL FEE

RATE ADDITIONAL FEE

X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

\*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Table of Contents

---

1. US6197696B1 Method for forming interconnection structure
-

**Family 1/1**

13 record(s) per family, collapsed by 7 record(s)

**Record 1/7** JP03062491B2 The formation method of a wiring structure

**Publication Number:**

JP03062491B2 20000710

JP2000003913A 20000107

**Title:**

The formation method of a wiring structure

**Title - DWPI:**

**Priority Number:**

JP199879371A

**Priority Date:**

1998-03-26

**Application Number:**

JP199975519A

**Application Date:**

1999-03-19

**Publication Date:**

2000-07-10

**IPC Class Table:**

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

**IPC Class Table - DWPI:**

**Assignee/Applicant:**

**JP F Terms:**

| 5F033HH07 | 5F033HH08 | 5F033HH11 | 5F033HH12 | 5F033HH13 | 5F033HH14 |  
5F033HH15 | 5F033HH19 | 5F033HH33 | 5F033JJ01 | 5F033JJ07 | 5F033JJ08 | 5F033JJ11 |  
5F033JJ12 | 5F033JJ13 | 5F033JJ14 | 5F033JJ15 | 5F033JJ19 | 5F033JJ33 | 5F033MM02 |  
5F033MM12 | 5F033MM13 | 5F033NN06 | 5F033NN07 | 5F033PP06 | 5F033PP15 | 5F033PP26 |  
5F033QQ08 | 5F033QQ09 | 5F033QQ10 | 5F033QQ11 | 5F033QQ21 | 5F033QQ27 | 5F033QQ28  
| 5F033QQ29 | 5F033QQ37 | 5F033QQ48 | 5F033RR04 | 5F033RR06 | 5F033RR09 | 5F033RR21  
| 5F033RR25 | 5F033SS01 | 5F033SS02 | 5F033SS03 | 5F033SS15 | 5F033TT04 | 5F033TT07 |  
5F033XX12 | 5F033XX15 | 5F033XX24 | 5F058AA10 | 5F058AD02 | 5F058AD04 | 5F058AD05 |  
5F058AD09 | 5F058AD11 | 5F058AF02 | 5F058AF04 | 5F058AH01 | 5F058AH02 | 5F058BA20 |  
5F058BD02 | 5F058BD10 | 5F058BD19 | 5F058BF07 | 5F058BH20 | 5F058BJ01 | 5F058BJ02

**JP FI Codes:**

| H01L0021312-N | H01L002188-K | H01L002190-S

**Assignee - Original:**

**Any CPC Table:**

**ECLA:**

**Abstract:**

**Language of Publication:**

JA

**INPADOC Legal Status Table:**

Gazette Date	Code	INPADOC Legal Status Impact
2015-03-17	R250	+
<b>Description:</b> RECEIPT OF ANNUAL FEES JAPANESE INTERMEDIATE CODE: R250		
2014-01-17	R350	-
<b>Description:</b> WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		



2014-01-08	S111	-
<b>Description:</b> REQUEST FOR CHANGE OF OWNERSHIP OR PART OF OWNERSHIP JAPANESE INTERMEDIATE CODE: R313113		
2013-11-18	R350	-
<b>Description:</b> WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		
2013-11-08	S533	-
<b>Description:</b> WRITTEN REQUEST FOR REGISTRATION OF CHANGE OF NAME JAPANESE INTERMEDIATE CODE: R313533		
2013-04-02	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20140428		
2013-03-28	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20130428		
2012-05-08	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20130428		
2012-04-05	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120428		
2011-04-05	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120428		
2010-04-06	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20110428		
2009-03-31	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100428		
2008-04-22	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20090428		
2008-03-27	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20080428		

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:

The image shows the front page of a patent document in Chinese. It features a header with the patent number '1171' and the title '一种...的方法'. Below the header is a table with columns for 'Inventor', 'Applicant', 'Attorney', and 'Agent'. The text is in Chinese and includes details about the patent application, such as the title '一种...的方法' and the applicant '华为技术有限公司'. The table contains the following information:

发明人	申请人	代理人	代理人
任正非	华为技术有限公司	北京...律师事务所	...

Below the table, there is a section for '代理人' (Attorney) and '代理人' (Agent), followed by a section for '代理人' (Attorney) and '代理人' (Agent). The text is in Chinese and includes details about the patent application, such as the title '一种...的方法' and the applicant '华为技术有限公司'.

**Record 2/7** JP2000294643A METHOD FOR FORMATION OF WIRING STRUCTURE | The formation method of a wiring structure

**Publication Number:**

JP2000294643A 20001020  
JP03078811B1 20000821

**Title:**

METHOD FOR FORMATION OF WIRING STRUCTURE | The formation method of a wiring structure

**Title - DWPI:**

Interconnection structure for a semiconductor integrated circuit

**Priority Number:**

JP199879371A

**Priority Date:**

1998-03-26

**Application Number:**

JP200066163A

**Application Date:**

1999-03-19

**Publication Date:**

2000-10-20

**IPC Class Table:**

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

**IPC Class Table - DWPI:**

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205

H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

**Assignee/Applicant:**

MATSUSHITA ELECTRIC IND CO LTD

**JP F Terms:**

| 5F004DB00 | 5F004DB03 | 5F004DB23 | 5F004DB25 | 5F004EA03 | 5F004EA06 |  
5F004EA07 | 5F004EB01 | 5F004EB03 | 5F033HH08 | 5F033HH09 | 5F033HH11 | 5F033HH12 |  
5F033HH13 | 5F033HH14 | 5F033HH15 | 5F033HH19 | 5F033HH33 | 5F033JJ08 | 5F033JJ09 |  
5F033JJ11 | 5F033JJ12 | 5F033JJ13 | 5F033JJ14 | 5F033JJ15 | 5F033JJ19 | 5F033JJ33 |  
5F033KK08 | 5F033KK09 | 5F033KK11 | 5F033KK12 | 5F033KK13 | 5F033KK14 | 5F033KK15 |  
5F033KK19 | 5F033KK33 | 5F033MM02 | 5F033NN06 | 5F033PP06 | 5F033PP15 | 5F033PP26 |  
5F033QQ10 | 5F033QQ11 | 5F033QQ12 | 5F033QQ21 | 5F033QQ24 | 5F033QQ25 | 5F033QQ27  
| 5F033QQ28 | 5F033QQ35 | 5F033QQ37 | 5F033QQ48 | 5F033RR06 | 5F033RR09 |  
5F033RR12 | 5F033RR21 | 5F033RR25 | 5F033RR26 | 5F033SS03 | 5F033SS11 | 5F033SS15 |  
5F033SS22 | 5F033TT04 | 5F033TT07 | 5F033XX24

**JP FI Codes:**

| H01L0021302-105A | H01L0021302-301N | H01L0021302-301S | H01L0021302-J |  
H01L002188-B | H01L002190-A | H01L002190-B | H01L002190-S

**Assignee - Original:**

MATSUSHITA ELECTRIC IND CO LTD

**Any CPC Table:**

**ECLA:**

**Abstract:**

**PROBLEM TO BE SOLVED:** To obtain a method for formation of wiring structure by which an interlayer insulating film having a low specific inductive capacity can be formed by adopting an ordinary resist process.

**SOLUTION:** In the method for formation of wiring structure, a first organic film 603, a silicon oxide film 604, and a second organic film 605 are sequentially deposited on a semiconductor substrate 600, and then, a mask pattern 608 is formed on the second organic film 605. Then the organic film 605 is patterned by etching the film 605 by using a second resist pattern 609 and the mask pattern 608 as a mask and, at the same time, the second resist pattern 609 is removed. In addition, the silicon oxide film 604 is patterned by etching the film 604 by using the patterned second organic film 605A as a mask. Thereafter, a wiring groove is formed in the second organic film 605A by etching the film 605A by using the mask pattern 608 as a mask and the first organic film 603 by using the silicon oxide film 604 as a mask and, at the same time, a contact hole is formed in the first organic film 603.

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## SUBJECT of the Invention

A normal resist process is employ|adopted and it enables it to form an interlayer insulation film with a low dielectric constant.

## PROBLEM to be solved

After depositing the 1st organic membrane 603, the silicon oxide film 604, and the 2nd organic membrane 605 one by one on the semiconductor substrate 600, the mask pattern 608 is formed on the 2nd organic membrane 605.

It etches with respect to organic insulating film 605 by setting the 2nd resist pattern 609 and the mask pattern 608 as a mask, and while patterning the 2nd organic membrane 605, the 2nd resist pattern 609 is removed.

It etches by setting as a mask 2nd organic membrane 605A patternized with respect to the silicon oxide film 604, and the silicon oxide film 604 is patternized.

While etching by setting the mask pattern 608 as a mask with respect to the 2nd organic membrane 605A,

A contact hole is formed in the 1st organic membrane 603, while etching by setting a silicon oxide film as a mask with respect to the 1st organic membrane 603 and forming a wiring groove|channel in the 2nd organic membrane 605A.

[MAT\_IMAGE 000002]

**PROBLEM TO BE SOLVED:** To obtain a method for formation of wiring structure by which an interlayer insulating film having a low specific inductive capacity can be formed by adopting an ordinary resist process. **SOLUTION:** In the method for formation of wiring structure, a first organic film 603, a silicon oxide film 604, and a second organic film 605 are sequentially deposited on a semiconductor substrate 600, and then, a mask pattern 608 is formed on the second organic film 605. Then the organic film 605 is patterned by etching the film 605 by using a second resist pattern 609 and the mask pattern 608 as a mask and, at the same time, the second resist pattern 609 is removed. In addition, the silicon oxide film 604 is patterned by etching the film 604 by using the patterned second organic film 605A as a mask. Thereafter, a wiring groove is formed in the second organic film 605A by etching the film 605A by using the mask pattern 608 as a mask and the first organic film 603 by using the silicon oxide film 604 as a mask and, at the same time, a contact hole is formed in the first organic film 603.

## Language of Publication:

JA

## INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2014-01-17	R350	-
<b>Description:</b> WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		
2014-01-08	S111	-
<b>Description:</b> REQUEST FOR CHANGE OF OWNERSHIP OR PART OF OWNERSHIP JAPANESE INTERMEDIATE CODE:		

R313113		
2013-11-18	R350	-
<b>Description:</b> WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		
2013-11-08	S533	-
<b>Description:</b> WRITTEN REQUEST FOR REGISTRATION OF CHANGE OF NAME JAPANESE INTERMEDIATE CODE: R313533		
2012-06-05	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20130616		
2012-05-31	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120616		
2011-05-31	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120616		
2010-06-01	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20110616		
2010-05-27	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100616		
2009-06-02	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100616		
2008-06-10	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20090616		
2008-06-05	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20080616		

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

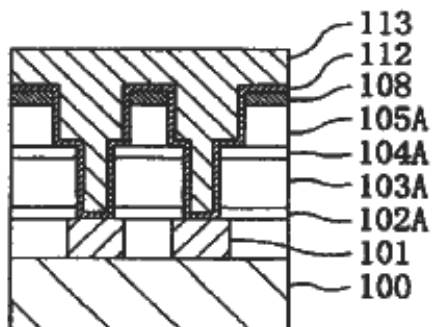
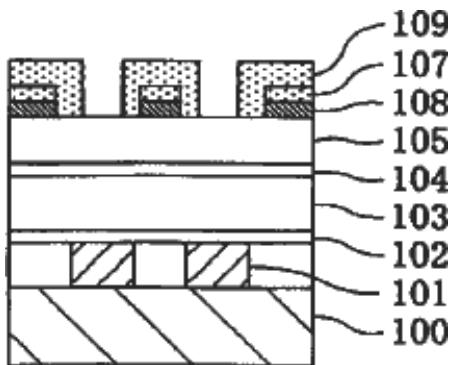
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



**Record 3/7** JP2000294644A METHOD FOR FORMATION OF WIRING STRUCTURE | The formation method of a wiring structure

**Publication Number:**

JP2000294644A 20001020  
JP03078812B1 20000821

**Title:**

METHOD FOR FORMATION OF WIRING STRUCTURE | The formation method of a wiring structure

**Title - DWPI:**

Interconnection structure for a semiconductor integrated circuit

**Priority Number:**

JP199879371A

**Priority Date:**

1998-03-26

**Application Number:**

JP200066179A

**Application Date:**

1999-03-19

**Publication Date:**

2000-10-20

**IPC Class Table:**

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

**IPC Class Table - DWPI:**

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205



H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

**Assignee/Applicant:**

MATSUSHITA ELECTRIC IND CO LTD

**JP F Terms:**

| 5F004AA08 | 5F004AA16 | 5F004DA00 | 5F004DB00 | 5F004DB03 | 5F004DB07 |  
5F004DB23 | 5F004DB25 | 5F004EA03 | 5F004EB01 | 5F004EB03 | 5F004EB08 | 5F033HH08 |  
5F033HH09 | 5F033HH11 | 5F033HH12 | 5F033HH13 | 5F033HH14 | 5F033HH15 | 5F033HH19 |  
5F033HH33 | 5F033JJ08 | 5F033JJ09 | 5F033JJ11 | 5F033JJ12 | 5F033JJ13 | 5F033JJ14 |  
5F033JJ15 | 5F033JJ19 | 5F033JJ33 | 5F033KK08 | 5F033KK09 | 5F033KK11 | 5F033KK12 |  
5F033KK13 | 5F033KK14 | 5F033KK15 | 5F033KK19 | 5F033KK33 | 5F033MM02 | 5F033NN06 |  
5F033PP06 | 5F033PP15 | 5F033PP26 | 5F033QQ10 | 5F033QQ11 | 5F033QQ12 | 5F033QQ21 |  
5F033QQ25 | 5F033QQ27 | 5F033QQ28 | 5F033QQ35 | 5F033QQ37 | 5F033QQ48 | 5F033RR06  
| 5F033RR09 | 5F033RR12 | 5F033RR21 | 5F033RR25 | 5F033RR26 | 5F033SS03 | 5F033SS11 |  
5F033SS15 | 5F033SS22 | 5F033TT04 | 5F033TT07 | 5F033XX24

**JP FI Codes:**

| H01L0021302-105A | H01L0021302-301N | H01L0021302-301S | H01L0021302-301Z |  
H01L0021302-J | H01L002188-B | H01L002190-A | H01L002190-B | H01L002190-S

**Assignee - Original:**

MATSUSHITA ELECTRIC IND CO LTD

**Any CPC Table:**

**ECLA:**

**Abstract:**

**PROBLEM TO BE SOLVED:** To provide a method for formation of wiring structure by which an interlayer insulating film having a low specific inductive capacity can be formed by adopting an ordinary resist process.

**SOLUTION:** In the method for formation of wiring structure, a first organic matter-bearing silicon oxide film 303, an SOG film 304 having a low specific inductive capacity, and a second organic matter-containing silicon oxide film 305 are sequentially deposited on a semiconductor substrate 300, and then, a mask pattern 308 is formed on the silicon oxide film 305. Then contact holes 310 are formed in the silicon oxide film 303 by etching the silicon oxide film 305, SOG film 304, and silicon oxide film 303 by using a second resist pattern 309 as a mask. After the pattern 309 is removed thereafter, wiring grooves 311 are formed in the SOG film 304 by etching the silicon oxide film 305 and SOG film 304 by using a mask pattern 308 as a mask.

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SUBJECT of the Invention

A normal resist process is employ|adopted and it enables it to form an interlayer insulation film with a low dielectric constant.

**PROBLEM to be solved**

On the semiconductor substrate 300, the 1st organic containing silicon oxide film 303, low dielectric constant SOG film 304, and the 2nd organic containing silicon oxide film 305 were deposited one by one,

Then, the mask pattern 308 is formed on the 2nd organic containing silicon oxide film 305.

It etches by setting the 2nd resist pattern 309 as a mask with respect to the 2nd organic containing silicon oxide film 305, low dielectric constant SOG film 304, and the 1st organic containing silicon oxide film 303, and the contact hole 310 is formed in the 1st organic containing silicon oxide film 303.

The 2nd resist pattern 309 was removed,

Then, it etches by setting the mask pattern 308 as a mask with respect to the 2nd organic containing silicon oxide film 305 and low dielectric constant SOG film 304, and the wiring groove|channel 311 is formed in low dielectric constant SOG film 304.

[MAT\_IMAGE 000002]

**PROBLEM TO BE SOLVED:** To provide a method for formation of wiring structure by which an interlayer insulating film having a low specific inductive capacity can be formed by adopting an ordinary resist process. **SOLUTION:** In the method for formation of wiring structure, a first organic matter-bearing silicon oxide film 303, an SOG film 304 having a low specific inductive capacity, and a second organic matter-containing silicon oxide film 305 are sequentially deposited on a semiconductor substrate 300, and then, a mask pattern 308 is formed on the silicon oxide film 305. Then contact holes 310 are formed in the silicon oxide film 303 by etching the silicon oxide film 305, SOG film 304, and silicon oxide film 303 by using a second resist pattern 309 as a mask. After the pattern 309 is removed thereafter, wiring grooves 311 are formed in the SOG film 304 by etching the silicon oxide film 305 and SOG film 304 by using a mask pattern 308 as a mask.

**Language of Publication:**

JA

**INPADOC Legal Status Table:**

Gazette Date	Code	INPADOC Legal Status Impact
2014-01-17	R350	-
<b>Description:</b> WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		
2014-01-08	S111	-
<b>Description:</b> REQUEST FOR CHANGE OF OWNERSHIP OR PART OF OWNERSHIP JAPANESE INTERMEDIATE CODE: R313113		
2013-11-18	R350	-
<b>Description:</b> WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		

2013-11-08	S533	-
<b>Description:</b> WRITTEN REQUEST FOR REGISTRATION OF CHANGE OF NAME JAPANESE INTERMEDIATE CODE: R313533		
2012-06-05	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20130616		
2012-05-31	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120616		
2011-05-31	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120616		
2010-06-01	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20110616		
2010-05-27	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100616		
2009-06-02	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100616		
2008-06-10	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20090616		
2008-06-05	FPAY	+
<b>Description:</b> RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20080616		

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

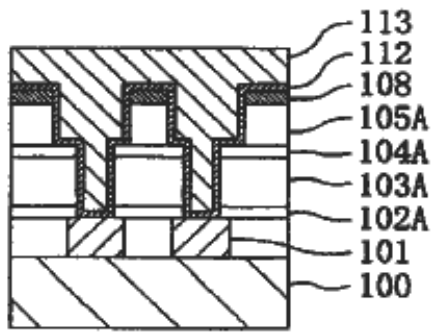
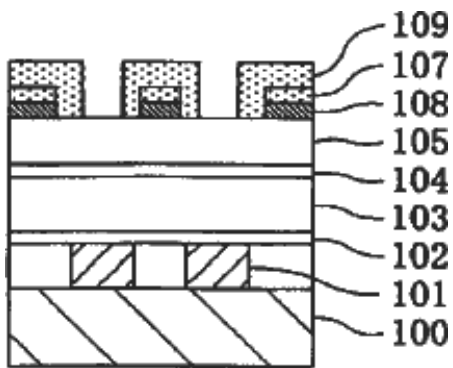
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



**Record 4/7** US6197696B1 Method for forming interconnection structure

**Publication Number:**

US6197696B1 20010306

**Title:**

Method for forming interconnection structure

**Title - DWPI:**

Interconnection structure for a semiconductor integrated circuit

**Priority Number:**

JP199879371A

**Priority Date:**

1998-03-26

**Application Number:**

US1999274114A

**Application Date:**

1999-03-23

**Publication Date:**

2001-03-06

**IPC Class Table:**

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021768	H	H01	H01L	H01L0021	H01L0021768

**IPC Class Table - DWPI:**

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

**Assignee/Applicant:**

Matsushita Electric Industrial Co. Ltd., Osaka, JP

**JP F Terms:**

**JP FI Codes:****Assignee - Original:**

Matsushita Electric Industrial Co. Ltd.

**Any CPC Table:**

Type	Invention	Additional	Version	Office
Current	H01L 21/76835	-	20130101	EP
Current	H01L 21/76811		20130101	EP
Current	H01L 21/76813		20130101	EP
Current	H01L 21/76814		20130101	EP
Current	H01L 21/76826		20130101	EP
Current	H01L 21/76829		20130101	EP
Current	H01L 21/76831		20130101	EP
Current	H01L 21/76895		20130101	EP

**ECLA:**

H01L0021768B12 | H01L0021768B2D6 | H01L0021768B2D8 | H01L0021768B2F |  
H01L0021768B8P | H01L0021768B10 | H01L0021768B10B | H01L0021768C10

**Abstract:**

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film is masked with the third insulating film and dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films are masked with the mask pattern and the second insulating film, respectively, and dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.

**Language of Publication:**

EN

**INPADOC Legal Status Table:**

Gazette Date	Code	INPADOC Legal Status Impact
2014-02-03	AS	-
<b>Description:</b> ASSIGNMENT GODO KAISHA IP BRIDGE 1, JAPAN ASSIGNMENT OF ASSIGNORS INTEREST;		

ASSIGNOR: PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.);  
 REEL/FRAME: 032152/0514 2014-01-17

2012-08-20	FPAY	+
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**Description:** FEE PAYMENT

2008-08-27	FPAY	+
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**Description:** FEE PAYMENT

2004-08-04	FPAY	+
------------	------	---

**Description:** FEE PAYMENT

1999-03-23	AS	-
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**Description:** ASSIGNMENT MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., JAPAN ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR: AOI, NOBUO; REEL/FRAME: 009862/0097 1999-03-19

**Post-Issuance (US):**

**Reassignment (US) Table:**

Assignee	Assigner	Date Signed	Reel/Frame	Date
GODO KAISHA IP BRIDGE 1, TOKYO, JP	PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.)	2014-01-17	032152/0514	2014-02-03
<b>Conveyance:</b> ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
<b>Correspondent:</b> SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVE. NW SUITE 800 WASHINGTON, DC 20037-3213				
MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD., OSAKA 571-8501, JP	AOI, NOBUO	1999-03-19	009862/0097	1999-03-23
<b>Conveyance:</b> ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
<b>Correspondent:</b> SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, ERIC J. ROBINSON 8180 GREENSBORO DRIVE SUITE 800 MCLEAN, VA 22102				

**Maintenance Status (US):**

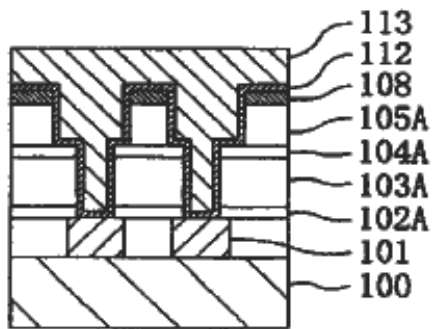
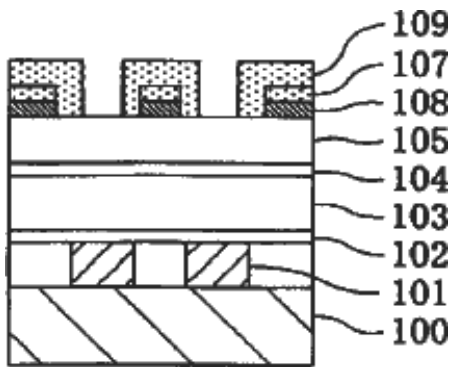
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:





**Record 5/7** US6287973B2 Method for forming interconnection structure

**Publication Number:**

US6287973B2 20010911  
US20010001739A1 20010524

**Title:**

Method for forming interconnection structure

**Title - DWPI:**

Interconnection structure for a semiconductor integrated circuit

**Priority Number:**

JP199879371A | US1999274114A

**Priority Date:**

1998-03-26 | 1999-03-23

**Application Number:**

US2001756242A

**Application Date:**

2001-01-09

**Publication Date:**

2001-09-11

**IPC Class Table:**

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021768	H	H01	H01L	H01L0021	H01L0021768

**IPC Class Table - DWPI:**

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

**Assignee/Applicant:**

Matsushita Electric Industrial Co. Ltd., Osaka, JP

**JP F Terms:**

**JP FI Codes:****Assignee - Original:**

Matsushita Electric Industrial Co. Ltd.

**Any CPC Table:**

Type	Invention	Additional	Version	Office
Current	H01L 21/76835	-	20130101	EP
Current	H01L 21/76811		20130101	EP
Current	H01L 21/76813		20130101	EP
Current	H01L 21/76814		20130101	EP
Current	H01L 21/76826		20130101	EP
Current	H01L 21/76829		20130101	EP
Current	H01L 21/76831		20130101	EP
Current	H01L 21/76895		20130101	EP

**ECLA:**

H01L0021768B12 | H01L0021768B2D6 | H01L0021768B2D8 | H01L0021768B2F |  
H01L0021768B8P | H01L0021768B10 | H01L0021768B10B | H01L0021768C10

**Abstract:**

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film is masked with the third insulating film and dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films are masked with the mask pattern and the second insulating film, respectively, and dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.

**Language of Publication:**

EN

**INPADOC Legal Status Table:**

Gazette Date	Code	INPADOC Legal Status Impact
2014-02-03	AS	-

**Description:** ASSIGNMENT GODO KAISHA IP BRIDGE 1, JAPAN ASSIGNMENT OF ASSIGNORS INTEREST;  
 ASSIGNOR: PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.);  
 REEL/FRAME: 032152/0514 2014-01-17

2013-02-19

FPAY

+

**Description:** FEE PAYMENT

2009-02-11

FPAY

+

**Description:** FEE PAYMENT

2005-02-17

FPAY

+

**Description:** FEE PAYMENT

**Post-Issuance (US):**

**Reassignment (US) Table:**

Assignee	Assignor	Date Signed	Reel/Frame	Date
GODO KAISHA IP BRIDGE 1, TOKYO, JP	PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.)	2014-01-17	032152/0514	2014-02-03
<b>Conveyance:</b> ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
<b>Correspondent:</b> SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVE. NW SUITE 800 WASHINGTON, DC 20037-3213				

**Maintenance Status (US):**

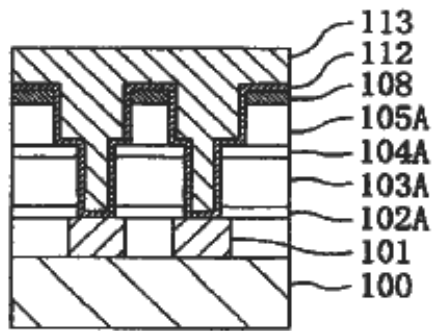
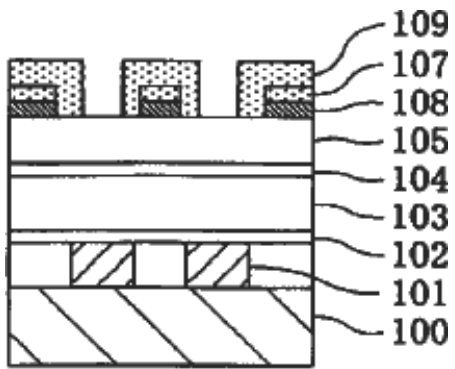
**Litigation (US):**

**Opposition (EP):**

**License (EP):**

**EPO Procedural Status:**

**Front Page Drawing:**



**Record 6/7** EP945900B1 Method for forming interconnection structure | Verfahren zur Herstellung einer Verbindungsstruktur | Méthode de formation d'une structure d'interconnexion

**Publication Number:**

EP945900B1 20060809

EP945900A1 19990929

**Title:**

Method for forming interconnection structure | Verfahren zur Herstellung einer Verbindungsstruktur | Méthode de formation d'une structure d'interconnexion

**Title - DWPI:**

Interconnection structure for a semiconductor integrated circuit

**Priority Number:**

JP199879371A

**Priority Date:**

1998-03-26

**Application Number:**

EP1999105946A

**Application Date:**

1999-03-24

**Publication Date:**

2006-08-09

**IPC Class Table:**

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021768	H	H01	H01L	H01L0021	H01L0021768

**IPC Class Table - DWPI:**

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

**Assignee/Applicant:**

MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD,Kadoma shi, Osaka 571 8501,JP,01855508  
JP F Terms:

JP FI Codes:

Assignee - Original:

MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD

Any CPC Table:

Type	Invention	Additional	Version	Office
Current	H01L 21/76835	-	20130101	EP
Current	H01L 21/76811		20130101	EP
Current	H01L 21/76813		20130101	EP
Current	H01L 21/76814		20130101	EP
Current	H01L 21/76826		20130101	EP
Current	H01L 21/76829		20130101	EP
Current	H01L 21/76831		20130101	EP
Current	H01L 21/76895		20130101	EP

ECLA:

H01L0021768B12 | H01L0021768B2D6 | H01L0021768B2D8 | H01L0021768B2F |  
H01L0021768B8P | H01L0021768B10 | H01L0021768B10B | H01L0021768C10

Abstract:

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film masked with the third insulating film is dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films masked with the mask pattern and the second insulating film, respectively, are dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.

Language of Publication:

EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact

2015-03-31	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2014-08-29	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
2014-06-30	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
2014-05-30	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2014-04-30	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2013-08-30	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2013-04-30	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
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<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2013-04-30	PGFP	+
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2012-07-31	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
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2012-06-29	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		

2012-04-30	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2011-07-29	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
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2010-08-31	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
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2010-06-30	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
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2009-10-30	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2009-08-31	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
2009-06-30	PGFP	+
<b>Description:</b> POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		



USPTO Maintenance Report

Patent Bibliographic Data			05/12/2015 12:56 PM		
Patent Number:	6197696	Application Number:	09274114		
Issue Date:	03/06/2001	Filing Date:	03/23/1999		
Title:	METHOD FOR FORMING INTERCONNECTION STRUCTURE				
Status:	4th, 8th and 12th year fees paid		Entity:	LARGE	
Window Opens:	N/A	Surcharge Date:	N/A	Expiration:	N/A
Fee Amt Due:	Window not open	Surchg Amt Due:	Window not open	Total Amt Due:	Window not open
Fee Code:					
Surcharge Fee Code:					
Most recent events (up to 7):	08/20/2012 07/05/2012 07/05/2012 08/27/2008 08/04/2004 09/12/2001	Payment of Maintenance Fee, 12th Year, Large Entity. Payor Number Assigned. Payer Number De-assigned. Payment of Maintenance Fee, 8th Year, Large Entity. Payment of Maintenance Fee, 4th Year, Large Entity. Payor Number Assigned. --- End of Maintenance History ---			
Address for fee purposes:	PANASONIC PATENT CENTER 20000 Mariner Avenue, Suite 200 Torrance CA 90503				