Lett., **edl-1**, 217 (1980).
5. K. Mochiji, Y. Maruyama, F. Murai, S. Okazaki, Y. Takeda, and S. Asai, *Jpn. J. Appl. Phys.*, **20**, Suppl. 20-1, 63 (1981).
6. J. M. Shaw and M. Hatzakis, *IEEE Trans. Electron Dev.*, **ed-25**, 425 (1978).
7. T. D. Berker and D. D. Casey, *ibid.*, **ed-29**, 524 (1982).

A Three-Layer Resist System for Deep U.V. and RIE Microlithography on Nonplanar Surfaces

E. Bassous,*[1] L. M. Ephrath,* G. Pepper, and D. J. Mikalsen

IBM, Thomas J. Watson Research Center, Yorktown Heights, New York 10598

ABSTRACT

The three-layer resist system AZ1350J/Si/PMMA was used to define high-resolution patterns on nonplanar surfaces with topographical features typically encountered in the fabrication of VLSI circuits. The substrate was coated successively with a thick layer of polymethyl methacrylate (PMMA) for planarization, a thin layer of amorphous silicon for masking, and a thin AZ1350J resist layer in which the optical or electron beam exposed pattern was defined. Transfer of the resist image pattern into the amorphous silicon film was performed anisotropically by reactive ion etching (RIE) in a CF_4 plasma. The pattern in the Si layer was then replicated in the underlying PMMA layer either by blanket deep u.v. exposure (200-300 nm) and solvent development or by *in situ* RIE in an O_2 plasma. Both patterning techniques were comparable in defining submicrometer features in PMMA films 1-3 μm thick with good linewidth control and high aspect ratio over steps 1 μm high. Experimental details are described and the complexity of deep u.v. and RIE patterning techniques are discussed with particular emphasis on the planarizing characteristics of PMMA.

High-resolution submicrometer resist patterns for VLSI applications are often difficult to generate on nonplanar surfaces due primarily to the nonuniform thickness of the resist layer covering topographical structures. Good linewidth control with high resolution requires, ideally, a uniform resist film less than 1 μm thick on a perfectly planar surface. Good step coverage and large height-to-width aspect ratio over 1 μm high topography demand, however, the use of a resist layer substantially thicker than 1 μm (1).

To overcome the conflicting requirements imposed on the resist film thickness, multilayer resist systems have been developed which separate the imaging and step-coverage functions in different layers. Sensitivity of the imaging process and definition of resist patterns could thus be enhanced independently, without sacrificing step coverage or aspect ratio (1-33). In two-layer systems (4-18), a thick resist film is first applied over the surface to cover vertical features and to planarize its topography. The thick layer is then overcoated with a thin resist film in which the image pattern is defined. The small thickness of the top imaging layer, and its relatively large distance from the substrate surface, enhance the resolution of patterns obtained by optical and electron beam exposure. This is due to a reduction of diffraction effects in the optical case and a decrease of electron scattering effects in the latter. Transfer of the top image pattern to the underlying thick layer has been accomplished by the use of solvents (7-9), selective developers (10, 34, 35), deep u.v. exposure and development (4, 15-18), and by dry etching in an oxygen plasma (11-14, 19-29).

One of the drawbacks of two-layer resist systems is the nonuniform mixing which sometimes occurs at the interface between the layers, resulting in processing difficulties and poor pattern definition. To minimize this effect, and to improve processing selectivity, three-layer resist systems have been introduced which incorporate a barrier film sandwiched between the two resist layers (17-32). The barrier film prevents mixing between the top and bottom layers, and thus, permits a wider choice of resist materials and pattern transfer techniques. The increased processing flexibility serves to enhance imaging sensitivity, and to achieve better control of pattern geometry. The pattern transfer processes in two-layer and three-layer resist systems are similar and their selectivity determines how faithfully the exposed image is replicated.

This study was undertaken to explore the feasibility and processing complexity associated with the use of a silicon barrier layer in a three-layer system for patterning submicrometer features over 1 μm topography employing wet and dry processes. The imaging layer used was AZ1350J, and the planarizing layer was polymethyl methacrylate (PMMA). Silicon was selected as the barrier material (23, 25, 26) in the AZ1350J/Si/PMMA three-layer system because of its compatibility with Si integrated circuit fabrication processes, its very low etch rate in an oxygen plasma, and its opacity in the deep u.v. region of the spectrum (200-300 nm). Amorphous Si barrier layers with smooth uniform surfaces are readily deposited as doped or undoped films on resist surfaces (36-38). The use of doped Si films is advantageous in electron beam exposures because an electrically conducting layer is less subject to surface charging, and thus, misregistration associated with this effect is significantly reduced (25).

The pattern in AZ1350J resist was defined by either optical or electron beam exposure, and then replicated in the Si film by RIE. Amorphous Si films were obtained by plasma CVD of silane or by electron-gun evaporation of silicon (38). Pattern transfer to the PMMA planarizing layer was accomplished either by blanket deep u.v. exposure and solvent development or by *in situ* RIE in an oxygen plasma. Processing details will first be described, followed by a discussion of the experimental results.

Experimental Procedure

High-resolution test patterns in the AZ/Si/PMMA system were defined on 57 mm diameter Si wafers patterned with surface steps 1 μm high. The steps were repetitive grating structures of different size, defined photolithographically in an SiO_2 film 1 μm thick. The stepped surface was first coated with a layer of PMMA 1.5-3 μm thick followed by a thin silicon film ~100 nm thick and finally a film of AZ1350J photoresist ~0.5 μm thick to serve as the top imaging layer.

The high-resolution line/space test pattern which ranged from 0.5 to 5 μm was defined in the AZ imaging

* Electrochemical Society Active Member.
[1] Present address: IBM Corporation, White Plains, NY 10604.
Key words: multilayer lithography, submicron lithography, trilevel resist, planarization, topography.

Downloaded on 2017-06-19 to IP 65.207.2.2 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

layer perpendicular to the underlying grating structures. Exposures were performed either with a direct write Vector Scan electron beam system (39) or with a 5× step-and-repeat optical projection printer (40). The exposed and developed image pattern in the AZ resist layer was replicated in the sandwiched Si film by RIE in a CF_4 plasma (41). Transfer of the Si pattern to the underlying PMMA layer was performed either by flood exposure to deep u.v. radiation (200-260 nm) followed by development of the image pattern in organic solvents, or by *in situ* RIE in an oxygen plasma (11-14, 19-29). A typical process sequence is outlined below and is illustrated schematically in Fig. 1. Typical patterns of PMMA resist lines crossing over SiO_2 steps are shown in Fig. 2.

Process sequence.—Spin-coat HMDS. Spin-coat 1 μm PMMA. (Dupont Elvacite 2041, 10% by weight in 2-methoxyethyl ether). Bake 15 min at 85°C. Repeat, spin-coat 1 μm PMMA. Bake 1 hr at 160°C. Deposit amorphous Si 30-200 nm by plasma CVD of SiH_4 or by electron gun evaporation of Si. Bake 1 hr at 100°C in air. Spin-coat HMDS. Spin-coat 0.45 μm AZ1350J using 2 AZ1350J:1 AZ thinner. Bake 15 min at 85°C. Expose test pattern either by (*i*) electron beam at 30 $\mu C/cm^2$, 20 keV, or (*ii*) on a 5× optical projection printer at 15 mJ/cm^2 using 405 nm monochromatic radiation. Develop image in AZ developer, then bake 30 min at 100°C. RIE Si in CF_4. RIE patterning: (*i*) *In situ* RIE PMMA in O_2 plasma, and (*ii*) dip etch 5-10 sec in buffered HF to clean off residues. Deep u.v. patterning: (*i*) flood expose to deep u.v. at 0.5-1 J/cm^2, and (*ii*) develop image in either chlorobenzene or methyl isobutyl ketone (MIBK).

Resist films.—Although resist films other than PMMA were used for planarization, PMMA was selected for

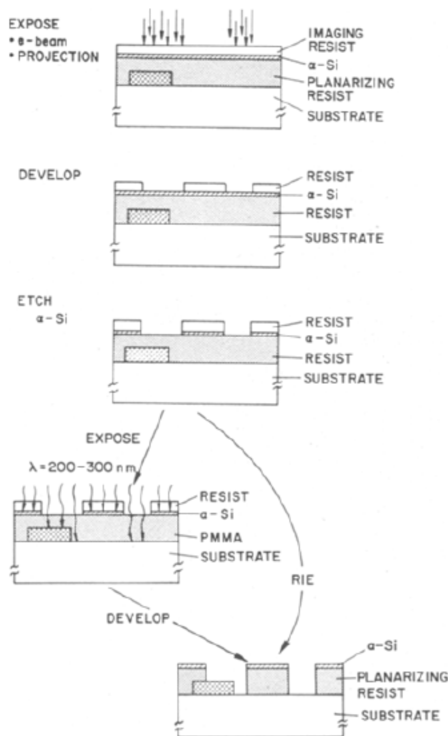


Fig. 1. Deep u.v. and RIE processes for patterning over topography using the three-layer resist system AZ1350J/Si/PMMA. The electron beam or optically exposed pattern is generated in the thin top AZ layer, and then replicated in the sandwiched amorphous silicon film by RIE in CF_4. The Si pattern is transferred to the thick bottom PMMA planarizing layer by deep u.v. exposure and solvent development or by RIE in oxygen.

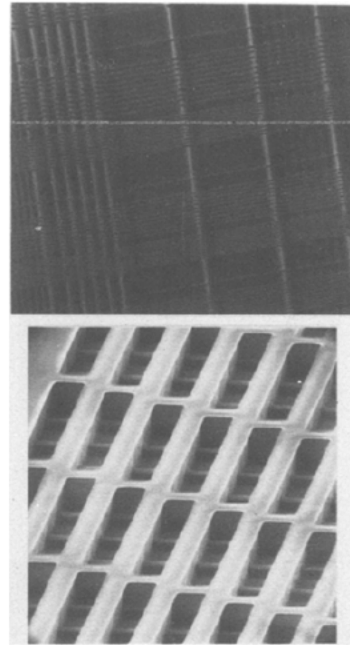


Fig. 2. Typical high resolution line/space test patterns in the three-layer system AZ/Si/PMMA defined over 1 μm high grating structures etched in an SiO_2 film. Top: Optical micrograph of part of the test pattern showing line/space features ranging between 0.5-5 μm. Bottom: SEM of equal line/space features 3 μm wide in 3 μm thick PMMA generated by RIE in oxygen.

detailed study because of its deep u.v. sensitivity (42) and its high etching rate in an O_2 plasma. PMMA films >1 μm thick were obtained by applying multiple coatings in order to avoid cracking, and to promote better planarization of the substrate surface as discussed below. Adhesion of PMMA to Si and SiO_2 surfaces was enhanced by prior coating with the adhesion promoter hexamethyl disilazane (HMDS). However, the use of HMDS was essential to ensure adequate adhesion of AZ1350J photoresist to the Si surface.

Despite its low sensitivity, AZ1350J resist was selected as an imaging layer because it offered the convenience of both optical and electron beam sensitivity. The initial thickness of AZ1350J resist was reduced by ~0.1 μm after development to a final nominal thickness of 0.4 μm. The latter was quite adequate to mask the underlying Si layer in a CF_4 plasma during the pattern transfer process.

Silicon films.—Plasma CVD silicon films were deposited in the plasma reactor illustrated in Fig. 3 using a mixture of SiH_4 and He at 4 and 65 mTorr partial pressures, respectively. The wafers were placed on the 125 mm diameter lower electrode, and after pumping to a pressure of 5×10^{-7} Torr, the deposition was performed at 50°C substrate temperature, at a rate of 15 nm/min using a power density of 0.6 W/cm^2. Films deposited under these conditions were hydrogenated amorphous silicon containing as much as 30% H_2 (43-46). Films obtained by electron gun evaporation of pure silicon on substrates maintained at or slightly above room temperature were functionally indistinguishable from CVD Si films.

Thin films obtained by plasma CVD of silane and electron gun evaporation of silicon were particularly well suited for lithographic processing because the films were clear, smooth, and amorphous. The optimum thickness for most patterning applications was 90 ± 20 nm although patterns were defined in films 30-200 nm thick. Silicon films were transparent in the visible spectrum as shown in Fig. 4, but more importantly,

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

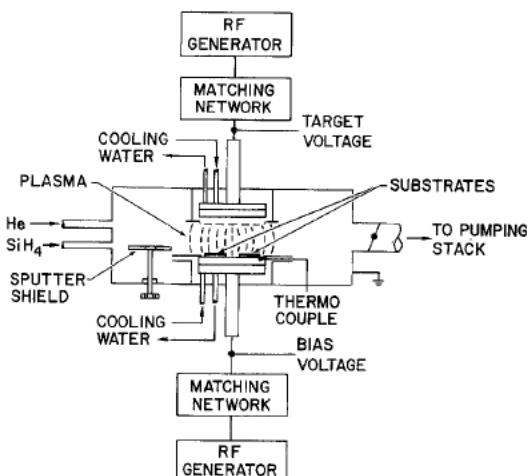


Fig. 3. Sketch of plasma CVD system for the deposition of hydrogenated amorphous silicon films from a silane/helium mixture. The 14 cm diameter electrodes 6 cm apart operated at 13.56 MHz. Typical conditions: SiH_4 4 mTorr, He 65 mTorr, upper electrode 850V, lower (substrate) electrode 0V, power 0.6 W/cm^2, deposition rate 15 nm/min.

they were totally opaque in the deep u.v. region below 300 nm. The films were excellent blocking layers for deep u.v. pattern transfer applications as suggested by the PCM techniques discussed by Lin (1, 4, 16-18).

Pattern replication.—Transfer of the image pattern from the top AZ layer to the Si film was performed by RIE in a diode reactor with a perforated grounded aluminum catcher plate positioned between the electrodes to minimize backscattering of sputtered aluminum (47). The system was first pumped down to 10^{-6} Torr, and Si was then etched in CF_4 at 2.5 mTorr pressure, 0.25 W/cm^2 rf power density at 13.56 MHz. Using end-point laser detection (48) and 50% overetching beyond end point ensured complete and uniform removal of the Si layer.

Etching of the underlying PMMA or polymer layer was performed in an oxygen plasma at 20 mTorr pressure and 0.06 W/cm^2 rf power density. Overetching varied between 50 and 100% depending on the topography present and the maximum thickness of resist. The etch rates of the 3 layers viz., Si, AZ1350J, and PMMA in CF_4 were 40, 50, and 70 nm/min, respectively, while in O_2 the etch rates of the same films were 0, 35, and 70 nm/min, respectively. Replication of the AZ image pattern in an Si film 100 nm thick resulted in an AZ film loss of 200 nm, while replication into a PMMA layer $\leq$1 μm resulted in the total loss of the AZ film.

Transfer of the Si image pattern to the PMMA layer was also performed by flood exposure to deep u.v. radiation, followed by development in either chlorobenzene or MIBK at room temperature. A 1 kW Hg-Xe deep u.v. source manufactured by Hanovia was used to expose individual wafers in air. The exposure time varied between 2-10 min depending on the sensitivity and thickness of the planarizing resist as well as on the composition of the developing solvent. To obtain the same dissolution rate of PMMA, the deep u.v. exposure necessary for MIBK development was approximately twice that required for chlorobenzene.

Results and Discussion

High-resolution line/space features over 1 μm topography were defined in the three-layer system AZ/Si/PMMA using RIE and deep u.v. patterning techniques. The minimum dimension defined in PMMA layers 1-3 μm thick was 0.5 μm using electron beam exposure of the top AZ layer. Optical exposure on a 5× step-and-repeat projection system using 405 nm monochromatic radiation produced minimum line/space features of 1 μm. Figure 5 shows 1 μm and 0.75 μm line/space features defined in the Si layer, and replicated in 2 μm thick PMMA by deep u.v. exposure, and development in chlorobenzene. Similar test patterns 1 μm/0.5 μm

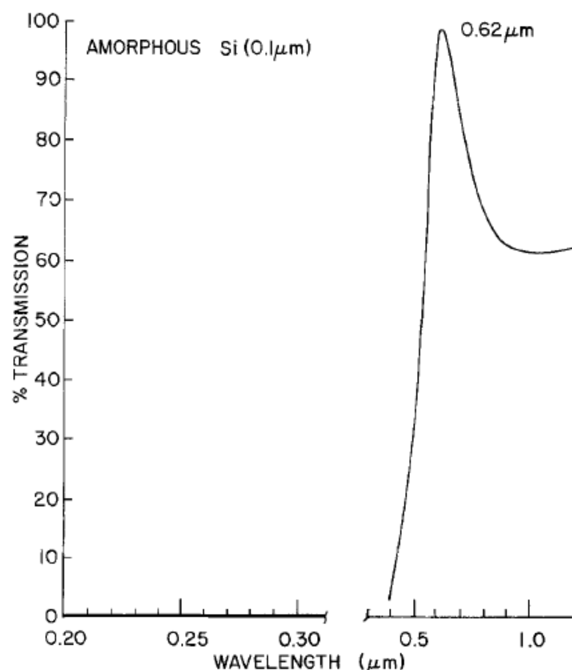


Fig. 4. Transmission spectrum of a 100 nm thick film of hydrogenated amorphous silicon deposited by plasma CVD of a silane/helium mixture on a quartz (suprasil) substrate. The film is transparent in the visible region with a peak at 620 nm and is totally opaque below 400 nm. Similar spectra are exhibited by films as thin as 20 nm including those obtained by electron-gun evaporation.

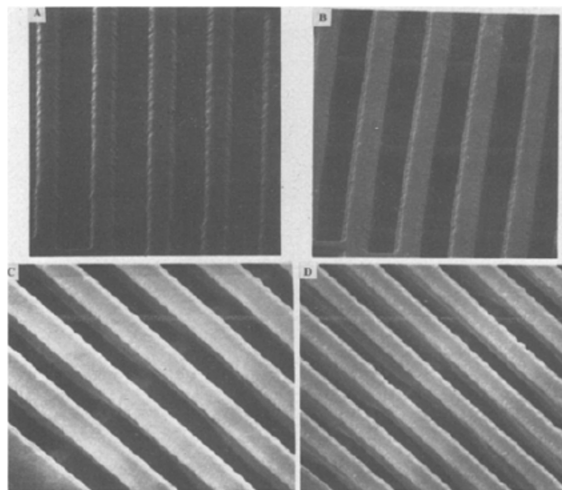


Fig. 5. SEM micrographs of high resolution line/space test patterns defined in the AZ/Si/PMMA system over 1 μm high topography. A: Equal 1 μm line/space features in AZ1350J and Si obtained by electron beam exposure followed by RIE etching of Si. B: Same pattern after deep u.v. exposure and development of PMMA 2 μm thick. C: Same as B showing vertical sidewalls of PMMA crossing over an oxide step 1 μm high. D: Equal 0.75 μm line/space features similar to C.

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

and 1 μm/1 μm were obtained by RIE of PMMA in an oxygen plasma as shown in Fig. 6.

The RIE and deep u.v. patterning techniques were equally capable of generating uniform resist features with good linewidth control, quasi-vertical sidewalls, and high aspect ratio over 1 μm topography as illustrated in Fig. 2, 5, and 6. Such patterns are highly desirable for subtractive and additive processes in VLSI fabrication. The differences between the RIE and deep u.v. patterning techniques were mainly determined by the characteristics of the planarizing layer as discussed below.

RIE patterning.—RIE processing was more tolerant of variations in thickness and composition of the planarizing layer by virtue of the anisotropy of RIE, and the high etch rate of organic resist materials relative to Si in an oxygen plasma. Radiation sensitivity of the planarizing layer was also not a requirement in RIE processing. The selection of useful organic coatings was, therefore, wider, and the processing flexibility, for example with respect to high-temperature baking and thermal cycling, was greater than deep u.v. processing.

Undesirable resist residues, which appeared on surfaces after etching by RIE, were removed by a cleaning procedure such as dip-etching in dilute HF solution. Figure 7 illustrates the effectiveness of the HF dip-etching technique in cleaning off all traces of residues from RIE-patterned surfaces. Where exposure to HF was incompatible with the materials on the wafer surface, alternate cleaning procedures were used in conjunction with modified RIE conditions. Potential contamination from metals sputtered from the substrate holder and radiation damage from energetic photons could be drawbacks in some applications, but their

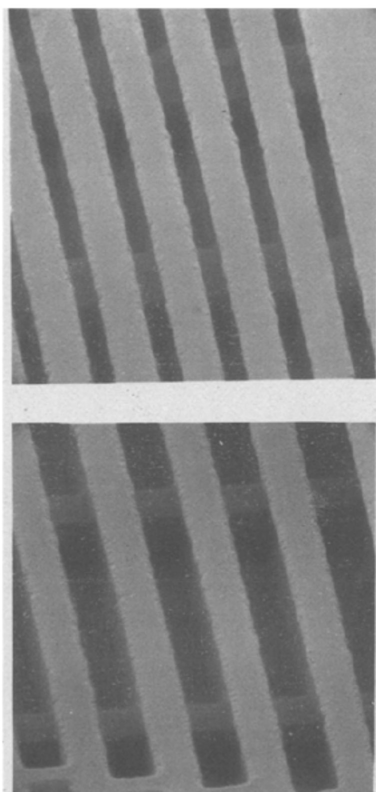


Fig. 6. SEM micrographs of line/space patterns defined in the AZ/Si/PMMA three-layer system over 0.8 μm high topography. Top: Line/space pattern 1 μm/0.5 μm obtained by RIE of PMMA 2.5 μm thick. Bottom: Similar pattern with line/space features 1 μm/1 μm. Decrease in linewidth is less than 0.1 μm.

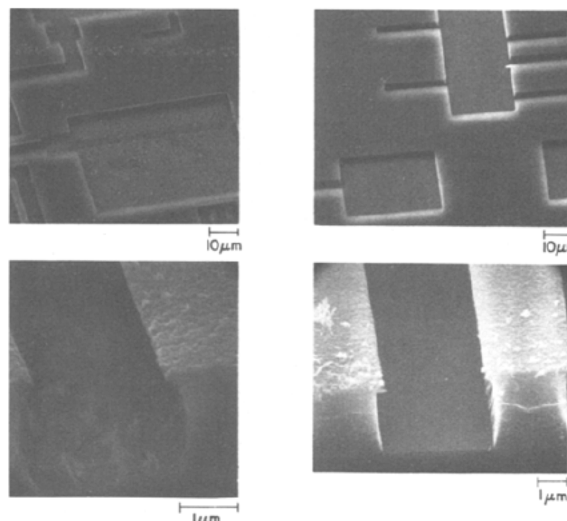


Fig. 7. SEM micrographs of patterns defined in a PMMA film 2 μm thick by RIE in oxygen. Resist residues on etched surfaces were cleaned off by dip etching in buffered HF for 10-15 sec. A,C: After RIE. B,D: After cleaning.

effects could be eliminated or minimized by adjusting RIE conditions (47).

Deep u.v. patterning.—In deep u.v. patterning, resist residues seldom appeared after solvent development of adequately exposed PMMA. Residues tended to appear when the overall PMMA thickness was excessive, or the thickness variation over steps was large. This could be attributed to the strong attenuation of the deep u.v. intensity in thick layers, resulting from the strong absorption of PMMA in the spectral region between 200-260 nm (42). As the solubility of PMMA was a strong function of the energy absorbed, the attenuation from top to bottom of thick PMMA layers resulted in a corresponding decrease in development rate. This phenomenon influenced residue-formation, as well as the cross-sectional profile and aspect ratio of resist features. Where PMMA thickness variations due to topography were large, development in chlorobenzene resulted in better linewidth control than undiluted MIBK. Development in chlorobenzene could also be used to retain the top imaging resist film, and generate a three-layer structure which is potentially useful in lift-off applications (49-51). Similar structures could also be generated by RIE using a top imaging resist film which is stable in an oxygen plasma.

An advantage of the deep u.v. patterning process was its relative insensitivity to pinholes or cracks in the barrier layer when the top imaging film was intact and opaque in the deep u.v. In the absence of the Si barrier layer, a film of AZ1350J photoresist 0.3 μm thick is sufficient to block deep u.v. radiation from exposing the PMMA layer (4). Despite the infinite solubility of exposed PMMA relative to silicon, the maximum useful thickness of PMMA was limited to 3 μm due to the severe attenuation of the deep u.v. intensity, and the tendency of thicker layers to crack after baking or pattern development.

Film integrity.—Successful patterning of the AZ/Si/PMMA system required careful optimization of the film thicknesses and the experimental conditions which affected the integrity of the 3 layers. In particular, the stress, the adhesion, and defect levels in one layer affected directly the integrity of the two other layers during processing. The film characteristics and the processing tolerances varied with the horizontal and vertical geometry of the underlying topography.

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

Hydrogenated amorphous Si films deposited by plasma CVD often formed blisters (Fig. 8) on poorly planarized PMMA surfaces. Such blister formation was presumably due to excessive stress induced in the Si film by the underlying topography. Silicon films deposited at room temperature by electron gun evaporation were more susceptible to loss of adhesion than plasma CVD Si films. The evaporated films were more specular and uniform, resulting in better defined patterns. The etching and deep u.v. blocking characteristics of evaporated and CVD films were identical.

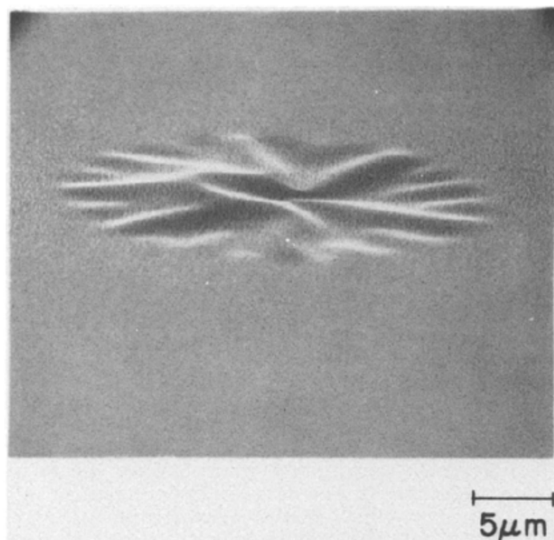
Poorly adhering and highly stressed silicon films often cracked and peeled after the imaging layer was patterned. Deposition above room temperature and annealing of the films prior to the application of the top imaging layer alleviated this problem. Similar behavior was observed with evaporated films of Al and Ti used as barrier layers between PMMA and AZ1350J.

The thickness of the top imaging resist layer and the baking conditions also influenced the integrity of the silicon barrier layer. Resist films ≤ 0.5 μm thick baked at about 100°C were readily processed over a wide range of PMMA and Si film thicknesses. Good step coverage and adequate planarization were essential to obtain a uniformly thick imaging layer. Inadequate planarization resulted in variations in thickness of the imaging layer with corresponding variations in linewidth and profile geometry. Multiple reflections at the resist-silicon interface also contribute to linewidth variations in the case of optically exposed patterns. The effect is clearly illustrated in Fig. 9 which shows the systematic variation in linewidth of 5 parallel resist lines nominally 2 μm wide crossing over 2 raised oxide steps 1 μm thick and 2 μm wide.

Planarization.—Due to the importance of the planarizing function of PMMA, an empirical evaluation of the coating characteristics of a variety of films was made using single and multiple coatings on stepped surfaces. Oxidized wafers, with sets of periodic line/space structures 2.5-25 μm wide, were coated by conventional resist spinning and baking methods. The undulations of the resist surface profile conforming to the substrate topography were scanned with a mechanical stylus to determine the planarization or leveling accomplished by a coating layer.

The curves in Fig. 10 show the peak-to-valley amplitude of the resist surface profile covering surface steps 0.8 μm high. The degree of planarization, represented by the amplitude, varied with the molecular weight of PMMA, the thickness and number of PMMA layers, the line/space dimensions of the substrate topography, and their periodicity or pitch. As the average molecular weight of PMMA decreased, the amplitude of the surface undulations decreased indicating enhanced planarization. This effect is illustrated in Fig. 10(a) with three PMMA compositions of average molecular weight 500,000, 150,000, and 33,000. The films were nominally 2 μm thick coated on sets of parallel steps 5 μm wide and varying pitch.

The expected improvement in planarization with increasing PMMA thickness is illustrated in Fig. 10(b) for the same sets of steps 5 μm wide and 0.8 μm high. The amplitude of the surface undulations also progressively decreased as the number of PMMA layers increased. It is interesting to note that better planar-



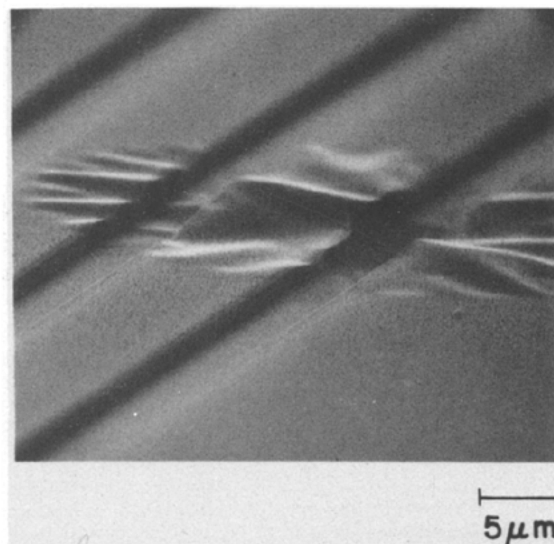


Fig. 8. Hydrogenated amorphous silicon films 100 nm thick deposited on PMMA at room temperature. Blisters indicative of compressive stress in the film are randomly distributed on the surface. Top: Single blister after film deposition. Bottom: Appearance of blister after patterning.

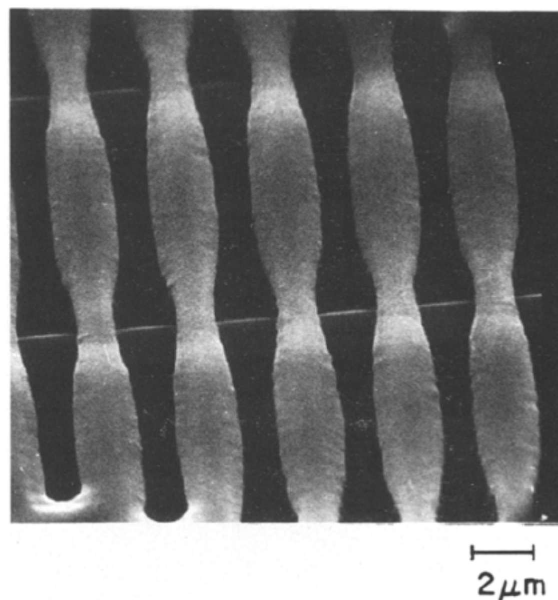


Fig. 9. Linewidth variation of PMMA resist lines that run from top to bottom of the micrograph traversing two 1 μm high SiO_2 steps. Narrowing of the resist lines occurs at the top of the steps where the resist is thinnest.

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

WHAT WILL YOU BUILD? | sales@docketalarm.com | 1-866-77-FASTCASE

fastcase®
Smarter legal research.