

# **Silicon VLSI Technology**

## **Fundamentals, Practice and Modeling**

**James D. Plummer**

**Michael Deal**

**Peter B. Griffin**

*Department of Electrical Engineering  
Stanford University*



**Prentice Hall**  
**Upper Saddle River, NJ 07458**

**Library of Congress Cataloging-in-Publication Data**

Silicon VLSI technology

p. cm.

ISBN 0-13-085037-3

1. Integrated circuits—Very large scale integration—Design and construction. 2. Silicon. 3. Silicon oxide films. 4. Metal oxide semiconductors. 5. Silicon technology.

TK7874.75.S54 2000

621.39'5—dc21

99-42745

CIP

*Publisher:* Tom Robbins

*Associate Editor:* Alice Dworkin

*Editorial/Production Supervision:* Rose Kernan

*Vice President and Editorial Director, ECS:* Marcia Horton

*Vice President of Production and Manufacturing:* David W. Riccardi

*Executive Managing Editor:* Vince O'Brien

*Marketing Manager:* Danny Hoyt

*Managing Editor:* David A. George

*Manufacturing Buyer:* Pat Brown

*Manufacturing Manager:* Trudy Pisciotti

*Art Director:* Jayne Conte

*Cover Design:* Bruce Kenselaar

*Editorial Assistant:* Jesse Power

*Copy Editor:* Martha Williams

*Composition:* D&G Limited, LLC



©2000 by Prentice Hall, Inc.  
Upper Saddle River, New Jersey 07458

All rights reserved. No part of this book may be reproduced, in any form or by any means, without permission in writing from the publisher.

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of the theories and programs to determine their effectiveness. The author and publisher make no warranty of any kind, expressed or implied, with regard to these programs or the documentation contained in this book. The author and publisher shall not be liable in any event for incidental or consequential damages in connection with, or arising out of, the furnishing, performance, or use of these programs.

Printed in the United States of America

10 9 8 7 6 5 4 3 2

**ISBN 0-13-085037-3**

Prentice Hall International (UK) Limited, *London*

Prentice Hall of Australia Pty. Limited, *Sydney*

Prentice Hall Canada Inc., *Toronto*

Prentice Hall Hispanoamericana, S.A., *Mexico*

Prentice Hall of India Private Limited, *New Delhi*

Prentice Hall of Japan, Inc., *Tokyo*

Pearson Education Pte., Ltd., *Singapore*

Editora Prentice Hall do Brasil, Ltda., *Rio de Janeiro*

# Contents

Preface.....	xi
<b>Chapter 1      Introduction and Historical Perspective</b>	<b>1</b>
1.1      Introduction .....	1
1.2      Integrated Circuits and the Planar Process—Key Inventions That Made It All Possible.....	7
1.3      Semiconductors.....	13
1.4      Semiconductor Devices .....	33
1.4.1      PN Diodes .....	33
1.4.2      MOS Transistors .....	36
1.4.3      Bipolar Junction Transistors .....	39
1.5      Semiconductor Technology Families.....	41
1.6      Modern Scientific Discovery—Experiments, Theory, and Computer Simulation .....	43
1.7      The Plan For This Book .....	45
1.8      Summary of Key Ideas .....	46
1.9      References .....	46
1.10      Problems .....	47
<b>Chapter 2      Modern CMOS Technology</b>	<b>49</b>
2.1      Introduction .....	49
2.2      CMOS Process Flow.....	50
2.2.1      The Beginning—Choosing a Substrate .....	51
2.2.2      Active Region Formation .....	52
2.2.3      Process Option for Device Isolation—Shallow Trench Isolation .....	57
2.2.4      N and P Well Formation .....	60
2.2.5      Process Options for Active Region and Well Formation .....	63
2.2.6      Gate Formation .....	71
2.2.7      Tip or Extension (LDD) Formation .....	76
2.2.8      Source/Drain Formation .....	80
2.2.9      Contact and Local Interconnect Formation .....	82
2.2.10      Multilevel Metal Formation .....	84
2.3      Summary of Key Ideas .....	90
2.4      Problems .....	91

<b>Chapter 3</b>	<b>Crystal Growth, Wafer Fabrication and Basic Properties of Silicon Wafers</b>	<b>93</b>
3.1	Introduction.....	93
3.2	Historical Development and Basic Concepts .....	93
3.2.1	Crystal Structure.....	94
3.2.2	Defects in Crystals .....	97
3.2.3	Raw Materials and Purification .....	101
3.2.4	Czochralski and Float-Zone Crystal Growth Methods .....	102
3.2.5	Wafer Preparation and Specification.....	105
3.3	Manufacturing Methods and Equipment.....	109
3.4	Measurement Methods.....	111
3.4.1	Electrical Measurements.....	111
3.4.1.1	Hot Point Probe.....	112
3.4.1.2	Sheet Resistance .....	113
3.4.1.3	Hall Effect Measurements .....	115
3.4.2	Physical Measurements .....	117
3.4.2.1	Defect Etches.....	117
3.4.2.2	Fourier Transform Infrared Spectroscopy (FTIR).....	118
3.4.2.3	Electron Microscopy .....	119
3.5	Models and Simulation.....	121
3.5.1	Czochralski Crystal Growth .....	122
3.5.2	Dopant Incorporation during CZ Crystal Growth.....	125
3.5.3	Zone Refining and FZ Growth.....	128
3.5.4	Point Defects.....	131
3.5.5	Oxygen in Silicon .....	138
3.5.6	Carbon in Silicon .....	142
3.5.7	Simulation .....	143
3.6	Limits and Future Trends in Technologies and Models .....	144
3.7	Summary of Key Ideas.....	146
3.8	References .....	147
3.9	Problems .....	148
<b>Chapter 4</b>	<b>Semiconductor Manufacturing—Clean Rooms, Wafer Cleaning, and Gettering</b>	<b>151</b>
4.1	Introduction.....	151
4.2	Historical Development and Basic Concepts .....	154
4.2.1	Level 1 Contamination Reduction: Clean Factories.....	157
4.2.2	Level 2 Contamination Reduction: Wafer Cleaning.....	159
4.2.3	Level 3 Contamination Reduction: Gettering.....	161
4.3	Manufacturing Methods and Equipment.....	165
4.3.1	Level 1 Contamination Reduction: Clean Factories.....	165
4.3.2	Level 2 Contamination Reduction: Wafer Cleaning.....	166
4.3.3	Level 3 Contamination Reduction: Gettering.....	167
4.4	Measurement Methods.....	169

4.4.2	Level 2 Contamination Reduction: Wafer Cleaning.....	173
4.4.3	Level 3 Contamination Reduction: Gettering.....	176
4.5	Models and Simulation.....	180
4.5.1	Level 1 Contamination Reduction: Clean Factories.....	181
4.5.2	Level 2 Contamination Reduction: Wafer Cleaning.....	184
4.5.3	Level 3 Contamination Reduction: Gettering.....	186
	4.5.3.1 Step 1: Making the Metal Atoms Mobile .....	186
	4.5.3.2 Step 2: Metal Diffusion to the Gettering Site.....	187
	4.5.3.3 Step 3: Trapping the Metal Atoms at the Gettering Site.....	190
4.6	Limits and Future Trends in Technologies and Models .....	193
4.7	Summary of Key Ideas .....	196
4.7	References .....	196
4.9	Problems .....	198

5.1	Introduction . . . . .	201
5.2	Historical Development and Basic Concepts . . . . .	203
5.2.1	Light Sources . . . . .	206
5.2.2	Wafer Exposure Systems . . . . .	208
	5.2.2.1 Optics Basics—Ray Tracing and Diffraction . . . . .	209
	5.2.2.2 Projection Systems (Fraunhofer Diffraction) . . . . .	212
	5.2.2.3 Contact and Proximity Systems (Fresnel Diffraction) . . . . .	219
5.2.3	Photoresists . . . . .	221
	5.2.3.1 g-line and i-line Resists . . . . .	223
	5.2.3.2 Deep Ultraviolet (DUV) Resists . . . . .	225
	5.2.3.3 Basic Properties and Characterization of Resists . . . . .	227
5.2.4	Mask Engineering—Optical Proximity Correction and Phase Shifting . . . . .	230
5.3	Manufacturing Methods and Equipment . . . . .	234
5.3.1	Wafer Exposure Systems . . . . .	234
5.3.2	Photoresists . . . . .	238
5.4	Measurement Methods . . . . .	241
5.4.1	Measurement of Mask Features and Defects . . . . .	242
5.4.2	Measurement of Resist Patterns . . . . .	244
5.4.3	Measurement of Etched Features . . . . .	244
5.5	Models and Simulation . . . . .	246
5.5.1	Wafer Exposure Systems . . . . .	247
5.5.2	Optical Intensity Pattern in the Photoresist . . . . .	253
5.5.3	Photoresist Exposure . . . . .	259
	5.5.3.1 g-line and i-line DNQ Resists . . . . .	259
	5.5.3.2 DUV Resists . . . . .	263
5.5.4	Postexposure Bake (PEB) . . . . .	264
	5.5.4.1 g-line and i-line DNQ Resists . . . . .	264
	5.5.4.2 DUV Resists . . . . .	266
5.5.5	Photoresist Developing . . . . .	267
5.5.6	Photoresist Postbake . . . . .	270

# Explore Litigation Insights



Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

## Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

## Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

## Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

### API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

### LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

### FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

### E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.