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(Dr. A. Pfau)

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IN THE MATTER OF
Patent Application

C E R T I F I C A T E

I, Yoshiharu IWASAKA, residing at 2-12, Nakazaki 2-chome, Kita-ku, Osaka, Japan, hereby declare that the document attached hereto is a translation made by me of the Japanese Patent Application number **10-079371** and certify that it is a true translation to the best of my knowledge and belief.

Dated this **31st** day of **May** , **1999** .

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[Title of Invention] METHOD FOR FORMING INTERCONNECTION STRUCTURE

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[Title of the Invention] METHOD FOR FORMING INTERCONNECTION STRUCTURE

[Claims]

[Claim 1] A method for forming an interconnection structure, characterised by comprising:

a first step of forming a first insulating film over lower-level metal interconnects;

a second step of forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

a third step of forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

a fourth step of forming a conductive film over the third insulating film;

a fifth step of forming a first resist pattern on the conductive film, the first resist pattern having openings for forming wiring grooves;

a sixth step of etching the conductive film using the first resist pattern as a mask, thereby forming a mask pattern out of the conductive film to have the openings for forming wiring grooves;

a seventh step of forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;

an eighth step of dry-etching the third insulating film under such conditions that the third insulating film and the first and

second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left;

a ninth step of dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;

a tenth step of dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and

an eleventh step of filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

[Claim 2] The method for forming an interconnection structure of Claim 1, characterised by further comprising the step of forming a metal adhesion layer over part of the third insulating film exposed

inside the wiring grooves and part of the first insulating film exposed inside the contact holes between the tenth and eleventh steps.

[Claim 3] The method for forming an interconnection structure of Claim 1, characterised in that the third insulating film is mainly composed of an organic component.

[Claim 4] The method for forming an interconnection structure of Claim 3, characterised in that the third step includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin.

[Claim 5] The method for forming an interconnection structure of Claim 3, characterised in that the first insulating film is mainly composed of an organic component.

[Claim 6] The method for forming an interconnection structure of Claim 5, characterised by further comprising the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process using a reactive gas containing nitrogen between the tenth and eleventh steps.

[Claim 7] The method for forming an interconnection structure of Claim 3, characterised in that the first step includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin.

[Claim 8] A method for forming an interconnection structure, characterised by comprising:

a first step of forming a first insulating film over lower-level metal interconnects;

a second step of forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

a third step of forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

a fourth step of forming a conductive film over the third insulating film;

a fifth step of forming a first resist pattern on the conductive film, the first resist pattern having openings for forming wiring grooves;

a sixth step of etching the conductive film using the first resist pattern as a mask, thereby forming a mask pattern out of the conductive film to have the openings for forming wiring grooves;

a seventh step of forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;

an eighth step of dry-etching the third insulating film using the first and second resist patterns as a mask under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes;

a ninth step of dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions that the second insulating film is etched at a relatively high rate

and that the first and third insulating films and the first and second resist patterns are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;

a tenth step of removing the first and second resist patterns;

an eleventh step of dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and

a twelfth step of filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

[Claim 9] The method for forming an interconnection structure of Claim 8, characterised in that the third insulating film is a low-dielectric-constant SOG film with a siloxane skeleton.

[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention relates to a method for forming an interconnection structure in a semiconductor integrated circuit.

[Prior Art]

As the number of devices integrated within a single semiconductor integrated circuit has been tremendously increasing, line-to-line capacitance as parasitic capacitance between metal

interconnects has become larger. This increases wiring delay, thereby interfering with the performance improvement of a semiconductor integrated circuit. The wiring delay is so-called "RC delay", which is proportional to the product of the resistance of metal interconnection and the line-to-line capacitance.

Therefore, to reduce the wiring delay, either the resistance of metal interconnection or the line-to-line capacitance should be reduced.

In order to reduce the interconnection resistance, IBM Corp., Motorola, Inc., etc. have reported semiconductor integrated circuits using copper, not aluminium alloy, as a material for metal interconnects. A copper material has a specific resistance about two-thirds as high as that of an aluminium alloy material. Accordingly, in accordance with simple calculation, the wiring delay involved with the use of a copper material for metal interconnects can be reduced to about two-thirds of that involved with the use of an aluminium alloy material therefor. That is to say, the operating speed can be increased by about 1.5 times.

However, if the number of devices integrated within a single semiconductor integrated circuit further increases, the wiring delay is considerably increased. Therefore, it is concerned that even if copper is used as an alternate metal interconnection material, the improvement in the operating speed will reach its limit. Also, the specific resistance of copper as a metal interconnection material is just a little higher than, but almost equal to, that of gold or silver. Accordingly, even if gold or silver is used instead of copper as a metal interconnection

material, the wiring delay can be reduced only slightly.

Under these circumstances, not only reducing interconnection resistance but also suppressing line-to-line capacitance play a key role in further increasing the number of devices that can be integrated within a single semiconductor integrated circuit. And, the relative dielectric constant of an interlevel insulating film should be reduced to suppress the line-to-line capacitance. A silicon dioxide film has heretofore been used as an interlevel insulating film. The relative dielectric constant of a silicon dioxide film is, however, about 4 to about 4.5. Therefore, it would be difficult to apply a silicon dioxide film to a semiconductor integrated circuit incorporating an even larger number of devices.

In order to solve such a problem, fluorine-doped silicon dioxide film, low-dielectric-constant spin-on-glass (SOG) film, organic polymer film and so on have been proposed as alternate interlevel insulating films with respective relative dielectric constants smaller than that of a silicon dioxide film.

[Problems that the Invention is to solve]

The relative dielectric constant of a fluorine-doped silicon dioxide film is about 3.3 to about 3.7, which is about 20 percent lower than that of a conventional silicon dioxide film. Nevertheless, a fluorine-doped silicon dioxide film is highly hygroscopic, and easily absorbs water in the air, resulting in various problems in practice. For example, when the fluorine-doped silicon dioxide film absorbs water, SiOH groups, having a high relative dielectric constant, are introduced into the film. As a result, the relative dielectric constant of the

fluorine-doped silicon dioxide film adversely increases, or the SiOH groups react with the water during a heat treatment to release H_2O gas. In addition, fluorine free radicals, contained in the fluorine-doped silicon dioxide film, segregate near the surface thereof during a heat treatment and react with Ti, contained in a TiN layer formed thereon as an adhesion layer, to form a TiF film, which easily peels off.

An exemplary low-dielectric-constant SOG film is an HSQ (hydrogen silsesquioxane) film, composed of Si atoms, O atoms and H atoms the number of which is about two-thirds of that of the O atoms. However, the HSQ film releases a larger amount of water than a conventional silicon dioxide film. Accordingly, since it is difficult to form a buried interconnection line in the HSQ film, a patterned metal film should be formed as metal interconnects on the HSQ film.

Also, since the HSQ film cannot adhere so strongly to metal interconnects, a CVD oxide film should be formed between the metal interconnects and the HSQ film to improve the adhesion therebetween. However, in such a case, if the CVD oxide film is formed on the metal interconnects, the substantial line-to-line capacitance is equal to the serial capacitance formed by the HSQ and CVD films because the CVD oxide film with a high dielectric constant exists between the metal interconnects. Accordingly, the resulting line-to-line capacitance is larger as compared with using the HSQ film alone.

An organic polymer film, as well as the low-dielectric-constant SOG film, cannot adhere strongly to metal interconnects,

either. Accordingly, a CVD oxide film should be formed as an adhesion layer between the metal interconnects and the organic polymer film, too.

Moreover, an etch rate, at which an organic polymer film is etched, is approximately equal to an ash rate, at which a resist pattern is ashed with oxygen plasma. Accordingly, a usual resist application process is not applicable in such a situation, because the organic polymer film is likely to be damaged during ashing and removing the resist pattern. Therefore, a proposed alternate process includes: forming a CVD oxide film on an organic polymer film; forming a resist film on the CVD oxide film; and then etching the resist film using the CVD oxide film as an etch stopper (i.e., a protective film).

However, during the step of forming the CVD oxide film on the organic polymer film, the surface of the organic polymer film is exposed to a reactive gas containing oxygen. Accordingly, the organic polymer film reacts with oxygen to take in polar groups such as carbonyl groups and ketone groups. As a result, the relative dielectric constant of the organic polymer film disadvantageously increases.

Also, in forming inlaid copper interconnects in the organic polymer film, an adhesion layer, formed of for example TiN, should be formed around wiring grooves formed in the organic polymer film, because the organic polymer film cannot adhere strongly to the metal interconnects. However, since the TiN film has a high resistance, the effective cross-sectional area of the metal interconnects decreases. Consequently, the intended effect

attainable by the use of the copper lines, i.e., reduction in resistance, would be lost.

In view of the above problems, an object of the present invention is to enable the forming of an interlevel insulating film with a low dielectric constant through an ordinary resist application process.

[Means for Solving the Problems]

A first method for forming an interconnection structure according to the present invention includes: a first step of forming a first insulating film over lower-level metal interconnects; a second step of forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; a third step of forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; a fourth step of forming a conductive film over the third insulating film; a fifth step of forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the conductive film; a sixth step of etching the conductive film using the first resist pattern as a mask, thereby forming a mask pattern out of the conductive film to have the openings for forming wiring grooves; a seventh step of forming a second resist pattern, having a plurality of openings for forming contact holes, on the third insulating film; an eighth step of dry-etching the third insulating film under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby

patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left; a ninth step of dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes; a tenth step of dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and an eleventh step of filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the first method for forming an interconnection structure, the third insulating film is dry-etched under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film and removing the first and second resist patterns in the eighth step. Accordingly, it is not necessary to perform the step of ashing and removing the first and second

resist patterns with oxygen plasma.

Furthermore, the composition of the second insulating film is different from that of the third insulating film. Thus, the second insulating film can be used as an etch stopper while the wiring grooves are formed by dry-etching the third insulating film using the mask pattern as a mask in the tenth step.

The first method for forming an interconnection structure preferably further includes the step of forming a metal adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes between the tenth and eleventh steps.

In the first method for forming an interconnection structure, the third insulating film is preferably mainly composed of an organic component.

In this case, the third step preferably includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin.

Further, the first insulating film is also preferably mainly composed of an organic component.

In the case where the first and second insulating films are both mainly composed of organic components, the first method preferably further includes the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process using a reactive gas containing nitrogen between the tenth and eleventh steps.

In the case where the first insulating film is mainly composed

of an organic component, the first step preferably includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin.

A second method for forming an interconnection structure according to the present invention includes: a first step of forming a first insulating film over lower-level metal interconnects; a second step of forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; a third step of forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; a fourth step of forming a conductive film over the third insulating film; a fifth step of forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the conductive film; a sixth step of etching the conductive film using the first resist pattern as a mask, thereby forming a mask pattern out of the conductive film to have the openings for forming wiring grooves; a seventh step of forming a second resist pattern, having a plurality of openings for forming contact holes, on the third insulating film; an eighth step of dry-etching the third insulating film using the first and second resist patterns as a mask under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes; a ninth step of dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions

that the second insulating film is etched at a relatively high rate and that the first and third insulating films and the first and second resist patterns are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes; a tenth step of removing the first and second resist patterns; an eleventh step of dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and a twelfth step of filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the second method for forming an interconnection structure, even if a damaged layer is formed in respective parts of the first and third insulating films that are exposed inside the openings for forming contact holes in the second insulating film during the tenth step of removing the first and second resist patterns, the third and first insulating films are dry-etched using the mask pattern and the patterned second insulating film as respective masks in the eleventh step under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact

holes in the third and first insulating films, respectively. Accordingly, the damaged layer can be removed without fail.

In the second method for forming an interconnection structure, the third insulating film is preferably a low-dielectric-constant SOG film with a siloxane skeleton.

[Embodiments of the Invention]

(First Embodiment)

Hereinafter, an exemplary method for forming an interconnection structure according to the first embodiment of the present invention will be described with reference to Figures 1(a) through 1(c), Figures 2(a) through 2(c) and Figures 3(a) through 3(c).

First, as shown in Figure 1(a), a silicon nitride film 102 is formed over first metal interconnects 101 formed on a semiconductor substrate 100. The silicon nitride film 102 is formed to be, for example, 50 nm thick, and used to protect the first metal interconnects 101 during a subsequent etching process step. Thereafter, a first organic film 103, mainly composed of an organic component, is formed to be, for example, 1μm thick on the silicon nitride film 102. Next, an organic-containing silicon dioxide film 104, containing an organic component in silicon dioxide, is formed to be, for example, 50 nm thick on the first organic film 103. Then, a second organic film 105, mainly composed of an organic component, is formed to be, for example, 400 nm thick on the organic-containing silicon dioxide film 104. And, a titanium nitride film 106 is formed to be, for example, 50 nm thick on the second organic film 105.

The first and second organic films 103 and 105 may be deposited

by any arbitrary technique. For example, these films 103 and 105 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films 103 and 105.

Moreover, the first organic film 103 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin and organic silane such as hexamethyl disiloxane, arylalkoxy silane or alkylalkoxy silane. In such a case, an organic/inorganic hybrid film can be obtained.

Similarly, the organic-containing silicon dioxide film 104 may also be deposited by any arbitrary technique. For instance, the film 104 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. In such a case, an organic-containing silicon dioxide film 104, having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide, can be obtained.

Next, as shown in Figure 1(b), a first resist pattern 107, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 106. Thereafter, the titanium nitride film 106 is dry-etched using the first resist pattern 107 as a mask, thereby forming a mask pattern 108 out of the titanium nitride film 106 as shown in Figure 1(c).

Subsequently, a second resist pattern 109, having openings for forming contact holes, is formed by lithography on the second organic film 105 without removing the first resist pattern 107. Then, the

second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the openings for forming contact holes as shown in Figure 2(a). In this case, since the second organic film 105 and the first and second resist patterns 107 and 109 are all mainly composed of organic components, the second organic film 105 is etched at a substantially equal rate to that of the first and second resist patterns 107 and 109. Thus, when the second organic film 105 is dry-etched, the first and second resist patterns 107 and 109 are also removed simultaneously.

It should be noted that part of the second resist pattern 109 may be left in the process step of dry-etching the second organic film 105. This is because the residual second resist pattern 109 can be removed during a subsequent process step of forming wiring grooves 111 in the patterned second organic film 105A (see Figure 2(c)).

Then, the organic-containing silicon dioxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic-containing silicon dioxide film 104A having the openings for forming contact holes as shown in Figure 2(b). In this process step, by selecting such etching conditions that the organic-containing silicon dioxide film 104 is etched at a rate higher than that of the patterned second organic film 105A, it is possible to prevent the patterned second organic film 105A from being erroneously etched.

Next, the patterned second organic film 105A is dry-etched using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in Figure

2(c). At the same time, the first organic film 103 is also dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes as shown in Figure 2(c).

Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes 110 as shown in Figure 3(a).

Then, as shown in Figure 3(b), an adhesion layer 112, made of titanium nitride, is deposited to be, for example, 50 nm thick on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film 113 is deposited over the entire surface of the substrate to completely fill in the contact holes 110 and the wiring grooves 111. In this embodiment, the metal film 113 may be made of any arbitrary metal. For example, copper, aluminium, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 113 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure 3(c), respective portions of the adhesion layer 112, the metal film 113 and the mask pattern 108, which are deposited on the patterned second organic film 105A, are removed by, for example, a CMP technique. As a result, second metal interconnects 114 and contacts 115, connecting the first and second metal interconnects 101 and 114, are formed out of the metal film 113.

It should be noted that a multilevel interconnection structure

may be formed by forming respective films, interconnects and contacts on the second metal interconnects 114 through the same process steps as those described above.

In the first embodiment, the organic-containing silicon dioxide film 104 is formed by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Accordingly, the film 104 has a structure in which a phenyl group (i.e., an exemplary organic group), bonded to a silicon atom, is introduced into silicon dioxide. Thus, the film 104 can be processed as well as a conventional CVD oxide film, and the relative dielectric constant of the film 104 is as low as that of the conventional CVD oxide film. In addition, the film 104 can adhere strongly to organic film, oxide film and metal film.

After the mask pattern 108 has been formed out of the titanium nitride film 106, the second resist pattern 109 is formed without removing the first resist pattern 107, and the first and second resist patterns 107 and 109 are removed while the second organic film 105 is dry-etched. Thus, it is no longer necessary to ash and remove the first and second resist patterns 107 and 109 with oxygen plasma. That is to say, it is possible to prevent the second organic film 105 from being damaged during the step of ashing and removing a resist pattern. Accordingly, although the second organic film 105 with a low relative dielectric constant is used as an interlevel insulating film, an ordinary resist application process is applicable to this embodiment.

Moreover, the wiring grooves 111 are formed by dry-etching the patterned second organic film 105A using the mask pattern 108 as a

mask and using the patterned organic-containing silicon dioxide film 104A as an etch stopper. Accordingly, the depth of the wiring grooves 111 matches with the thickness of the second organic film 105. That is to say, the depth of the wiring grooves 111 can be defined by self-alignment.

Hereinafter, problems caused by the misalignment of the second resist pattern 109 with the first resist pattern 107 and the measured taken to solve the problems will be described.

First, it will be described with reference to Figures 4(a) through 4(c), Figures 5(a) through 5(c) and Figures 6(a) through 6(c) what problems are caused if the second resist pattern 109 has misaligned.

As in the first embodiment, a silicon nitride film 102 is first formed to be, for example, 50 nm thick over first metal interconnects 101 formed on a semiconductor substrate 100 as shown in Figure 4(a). Thereafter, a first organic film 103, mainly composed of an organic component, is formed to be, for example, 1μm thick on the silicon nitride film 102.

Next, an organic-containing silicon dioxide film 104, containing an organic component in silicon dioxide, is formed to be, for example, 50 nm thick on the first organic film 103. Then, a second organic film 105, mainly composed of an organic component, is formed to be, for example, 400 nm thick on the organic-containing silicon dioxide film 104. And a titanium nitride film 106 is formed to be, for example, 50 nm thick on the second organic film 105.

Next, as shown in Figure 4(b), a first resist pattern 107, having openings for forming wiring grooves, is formed on the titanium

nitride film 106. Thereafter, the titanium nitride film 106 is dry-etched using the first resist pattern 107 as a mask, thereby forming a mask pattern 108 out of the titanium nitride film 106 as shown in Figure 4(c).

Subsequently, as shown in Figure 5(a), a second resist pattern 109, having openings for forming contact holes, is formed on the second organic film 105 without removing the first resist pattern 107. As can be seen if Figures 5(a) and 1(c) are compared with each other, the second resist pattern 109 has misaligned with the first resist pattern 107 in this case.

Then, the second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the openings for forming contact holes as shown in Figure 5(b). As in the first embodiment, since the second organic film 105 and the first and second resist patterns 107 and 109 are all mainly composed of organic components, the first and second resist patterns 107 and 109 are removed simultaneously with the dry-etching of the second organic film 105. In this case, since the second resist pattern 109 has misaligned with the first resist pattern 107, the diameter of the openings for forming contact holes, which are provided in the second organic film 105A, is smaller than desired.

Then, the organic-containing silicon dioxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic-containing silicon dioxide film 104A having the openings for forming contact holes as shown in Figure 5(c).

Next, the patterned second organic film 105A is dry-etched

using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in Figure 6(a). At the same time, the first organic film 103 is also dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes 110 as shown in Figure 6(a). Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes 110 as shown in Figure 6(b).

Then, an adhesion layer 112, made of titanium nitride, is deposited to be, for example, 50 nm thick on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer 112, the metal film and the mask pattern 108, which are deposited on the patterned second organic film 105A, are removed by, for example, a CMP technique. As a result, second metal interconnects 114 are certainly formed. However, since the diameter of the contact holes 110 is smaller than desired, the contact holes 110 cannot be completely filled in with the metal film, and the first and second metal interconnects 101 and 112 cannot be connected to each other, resulting in a contact failure.

Next, it will be described with reference to Figures 7(a) through 7(c) and Figures 8(a) through 8(c) what measures should be taken to solve the problems caused by the misalignment of the second resist

pattern 109.

First, a second resist pattern 109, having openings for forming contact holes, is formed through the same process steps as those described with reference to Figures 4(a) through 4(c) and Figure 5(a). In this case, the second resist pattern 109 has also misaligned with the first resist pattern 107 (see Figure 5(a)).

Thus, as shown in Figure 7(a), the first resist pattern 107 and the mask pattern 108 are dry-etched using the second resist pattern 109 as a mask. In this manner, portions of the first resist pattern 107, not overlapping with the second resist pattern 109, are removed and each opening of the mask pattern 108 is expanded to be equal to or larger than each opening for forming wiring grooves or each opening for forming contact holes. As a result, the pattern for the openings of the second resist pattern for forming contact holes 109 can be transferred to the first resist pattern 107 and the mask pattern 108.

Then, the second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the openings for forming contact holes as shown in Figure 7(b). In this case, since the second organic film 105 and the first and second resist patterns 107 and 109 are all mainly composed of organic components, the first and second resist patterns 107 and 109 are removed simultaneously with the dry-etching of the second organic film 105.

Then, the organic-containing silicon dioxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic-containing silicon dioxide film 104A having the openings for forming contact holes as shown in Figure

7(c).

As described above, the second resist pattern 109 has misaligned with the first resist pattern 107. However, in this case, the pattern for the openings of the second resist pattern for forming contact holes 109 has been successfully transferred to the first resist pattern 107 and the mask pattern 108. Thus, the diameter of the openings for forming contact holes, which have been formed in the patterned second organic film 105A and the patterned organic-containing silicon dioxide film 104A, is a predetermined size.

Next, the patterned second organic film 105A is dry-etched using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in Figure 8(a). At the same time, the first organic film 103 is also dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes 110 as shown in Figure 8(a). Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes 110 as shown in Figure 8(b).

Then, an adhesion layer 112, made of titanium nitride, is deposited to be, for example, 50 nm thick on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer 112, the metal film and the mask pattern 108, which are deposited on the patterned second

organic film 105A, are removed by, for example, a CMP technique. As a result, second metal interconnects 114 and contacts 115 are formed out of the titanium nitride film 112 and the metal film as shown in Figure 8(c).

(Second Embodiment)

Next, an exemplary method for forming an interconnection structure according to the second embodiment of the present invention will be described with reference to Figures 9(a) through 9(c), Figures 10(a) through 10(c) and Figures 11(a) through 11(c).

First, as shown in Figure 9(a), a silicon nitride film 202 is formed to be, for example, 50 nm thick over first metal interconnects 201 formed on a semiconductor substrate 200. Thereafter, a first organic film 203, mainly composed of an organic component, is formed to be, for example, 1μm thick on the silicon nitride film 202. Next, an organic-containing silicon dioxide film 204, containing an organic component in silicon dioxide, is formed to be, for example, 50 nm thick on the first organic film 203. Then, a second organic film 205, mainly composed of an organic component, is formed to be, for example, 400 nm thick on the organic-containing silicon dioxide film 204. And, a titanium nitride film 206 is formed to be, for example, 50 nm thick on the second organic film 205.

The first and second organic films 203 and 205 may be deposited by any arbitrary technique. For example, these films 203 and 205 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic

films 203 and 205.

Similarly, the organic-containing silicon dioxide film 204 may also be deposited by any arbitrary technique. For instance, the film 204 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

Next, as shown in Figure 9(b), a first resist pattern 207, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 206. Thereafter, the titanium nitride film 206 is dry-etched using the first resist pattern 207 as a mask, thereby forming a mask pattern 208 out of the titanium nitride film 206 as shown in Figure 9(c).

Subsequently, a second resist pattern 209, having openings for forming contact holes, is formed by lithography on the second organic film 205 without removing the first resist pattern 207. Then, the second organic film 205 is dry-etched, thereby forming a patterned second organic film 205A having the openings for forming contact holes as shown in Figure 10(a). In this case, since the second organic film 205 and the first and second resist patterns 207 and 209 are all mainly composed of organic components, the second organic film 205 is etched at a rate substantially equal to that of the first and second resist patterns 207 and 209. Accordingly, when the second organic film 205 is dry-etched, the first and second resist patterns 207 and 209 are also removed simultaneously.

If the second resist pattern 209 may have been misaligned with the first resist pattern 207, then the first resist pattern 207 and the mask pattern 208 should be dry-etched using the second resist pattern 209 as a mask. In this manner, parts of the first resist

pattern 207, not overlapping with the second resist pattern 209, are removed and the openings of the mask pattern 208 are expanded to be equal to or larger than the openings for forming wiring grooves and contact holes as described in the first embodiment.

Then, the organic-containing silicon dioxide film 204 is dry-etched using the patterned second organic film 205A as a mask, thereby forming a patterned organic-containing silicon dioxide film 204A having the openings for forming contact holes as shown in Figure 10(b). Next, the patterned second organic film 205A is dry-etched using the mask pattern 208 as a mask, thereby forming the wiring grooves 211 in the patterned second organic film 205A as shown in Figure 10(c). At the same time, the first organic film 203 is also dry-etched using the patterned organic-containing silicon dioxide film 204A as a mask, thereby forming a patterned first organic film 203A having the contact holes 210 as also shown in Figure 10(c).

Subsequently, the silicon nitride film 202 is dry-etched using the patterned organic-containing silicon dioxide film 203A as a mask, thereby forming a patterned silicon nitride film 202A and exposing the first metal interconnects 201 within the contact holes 210 as shown in Figure 11(a).

Then, the patterned first and second organic films 203A and 205A are subjected to plasma processing using ammonium gas. As a result, as shown in Figure 11(b), an adhesion layer 212, including amino and amide groups, is deposited on the wall faces of the patterned first organic film 203A exposed inside the contact holes 210 and on the wall faces of the patterned second organic film 205A exposed inside the wiring grooves 211. Thereafter, a metal film 213

is deposited over the entire surface of the substrate to completely fill in the contact holes 210 and the wiring grooves 211. In this embodiment, the metal film 213 may be made of any arbitrary metal. For example, copper, aluminium, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 213 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure 11(c), respective portions of the metal film 213 and the mask pattern 208, which are deposited on the patterned second organic film 205A, are removed by, for example, a CMP technique. As a result, second metal interconnects 214 and contacts 215 are formed out of the metal film 213.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 214 through the same process steps as those described above.

(Third Embodiment)

Next, an exemplary method for forming an interconnection structure according to the third embodiment of the present invention will be described with reference to Figures 12(a) through 12(c), Figures 13(a) through 13(c) and Figures 14(a) through 14(c).

First, as shown in Figure 12(a), a silicon nitride film 302 is formed over first metal interconnects 301 formed on a semiconductor substrate 300. The silicon nitride film 302 is formed to be, for example, 50 nm thick and to protect the first metal interconnects 301 during a subsequent etching process step. Thereafter, a first organic-containing silicon dioxide film 303,

containing an organic component in silicon dioxide, is formed to be, for example, 1μm thick on the silicon nitride film 302. Next, a low-dielectric-constant SOG film 304, having a siloxane skeleton, is deposited to be, for example, 400 nm thick on the first organic-containing silicon dioxide film 303. Then, a second organic-containing silicon dioxide film 305, containing an organic component in silicon dioxide, is formed to be, for example, 50 nm thick on the low-dielectric-constant SOG film 304. And, a titanium nitride film 306 is formed to be, for example, 50 nm thick on the second organic-containing silicon dioxide film 305.

The first and second organic-containing silicon dioxide films 303 and 305 may be deposited by any arbitrary technique. For example, these films 303 and 305 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Also, an HSQ film may be used as the low-dielectric-constant SOG film 304 with a siloxane skeleton.

Next, as shown in Figure 12(b), a first resist pattern 307, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 306. Thereafter, the titanium nitride film 306 is dry-etched using the first resist pattern 307 as a mask, thereby forming a mask pattern 308 out of the titanium nitride film 306 as shown in Figure 12(c).

Subsequently, as shown in Figure 13(a), the first resist pattern 307 is removed and then a second resist pattern 309, having openings for forming contact holes, is formed on the second organic-containing silicon dioxide film 305. Then, the second organic-containing silicon dioxide film 305, the low-dielectric-constant SOG film 304

and the first organic-containing silicon dioxide film 303 are sequentially dry-etched using the second resist pattern 309 as a mask. As a result, a patterned second organic-containing silicon dioxide film 305A, a patterned low-dielectric-constant SOG film 304A and a patterned first organic-containing silicon dioxide film 303A having contact holes 310 are formed as shown in Figure 13(b).

Next, as shown in Figure 13(c), the second resist pattern 309 is removed and the patterned second organic-containing silicon dioxide film 305A is dry-etched using the mask pattern 308 as a mask, thereby forming openings for forming wiring grooves in the patterned second organic-containing silicon dioxide film 305A. Thereafter, the patterned low-dielectric-constant SOG film 304A is dry-etched using the mask pattern 308 and the patterned second organic-containing silicon dioxide film 305A having the openings for wiring grooves as a mask, thereby forming the wiring grooves 311. In forming the wiring grooves 311, by selecting such etching conditions that the first organic-containing silicon dioxide film 303A is etched at a rate sufficiently lower than that of the low-dielectric-constant SOG film 304A, sufficient selectivity can be secured for the patterned first organic-containing silicon dioxide film 303A. Accordingly, the depth of the wiring grooves 311 can be determined univocally at the sum of the thicknesses of the second organic-containing silicon dioxide film 305 and the low-dielectric-constant SOG film 304.

If the second resist pattern 309 may have been misaligned with the first resist pattern 307, the mask pattern 308 should be dry-etched using the second resist pattern 309 as a mask before the second organic-containing silicon dioxide film 305 is dry-etched

using the second resist pattern 309 as a mask. That is to say, if the mask pattern 308 is partially exposed inside the openings of the second resist pattern 309 for forming contact holes because of the misalignment of the second resist pattern 309 with the first resist pattern 307, then the mask pattern 308 is dry-etched using the second resist pattern 309 as a mask. In this manner, the openings of the mask pattern 308 are expanded to include the openings for forming wiring grooves and contact holes.

Subsequently, the silicon nitride film 302 is dry-etched using the patterned first organic-containing silicon dioxide film 303A as a mask, thereby forming a patterned silicon nitride film 302A and exposing the first metal interconnects 301 within the contact holes 310 as shown in Figure 14(a).

Then, as shown in Figure 14(b), an adhesion layer 312, made of titanium nitride, is deposited to be, for example, 50 nm thick on the wall faces of the contact holes 310 and the wiring grooves 311. Thereafter, a metal film 313 is deposited over the entire surface of the substrate to completely fill in the contact holes 310 and the wiring grooves 311. In this embodiment, the metal film 313 may be made of any arbitrary metal. For example, copper, aluminium, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 313 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure 14(c), respective portions of the adhesion layer 312, the metal film 313 and the mask pattern 308, which are deposited on the patterned second organic-containing silicon dioxide film 305A, are removed by, for example, a CMP

technique. As a result, second metal interconnects 314 and contacts 315, connecting the first and second metal interconnects 301 and 314, are formed out of the metal film 313.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 314 through the same process steps as those described above.

In the third embodiment, while the first resist pattern 307 is ashed and removed with oxygen plasma, the low-dielectric-constant SOG film 304 is not exposed to the oxygen plasma, because the second organic-containing silicon dioxide film 305 exists on the low-dielectric-constant SOG film 304.

Also, in this embodiment, after the second organic-containing silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic-containing silicon dioxide film 303 have been sequentially dry-etched using the second resist pattern 309 as a mask, the second resist pattern 309 is ashed and removed with oxygen plasma. Accordingly, the regions of the patterned low-dielectric-constant SOG film 304A, which are exposed inside the openings for forming contact holes, are exposed to oxygen plasma and damaged. However, the damaged layer, formed in the patterned low-dielectric-constant SOG film 304A, can be removed when the wiring grooves 311 are formed in the patterned low-dielectric-constant SOG film 304A, and does not have harmful effects on subsequent process steps.

Accordingly, the low-dielectric-constant SOG film 304 may be made of a material degradable with oxygen plasma. For example, in general, if an HSQ film is exposed to oxygen plasma, the Si-H bonds

thereof are oxidised and the content of water and the relative dielectric constant thereof both increase to deteriorate the reliability and performance of the device. However, according to the third embodiment, the patterned low-dielectric-constant SOG film 304A, in which the wiring grooves 311 have already been formed, is not affected by oxygen plasma. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

(Modified Example of Third Embodiment)

Next, an exemplary method for forming an interconnection structure according to a modified example of the third embodiment of the present invention will be described with reference to Figures 15(a) through 15(c), Figures 16(a) through 16(c) and Figures 17(a) through 17(c).

First, as shown in Figure 15(a), a silicon nitride film 352 is formed over first metal interconnects 351 formed on a semiconductor substrate 350. The silicon nitride film 352 is formed to be, for example, 50 nm thick and to protect the first metal interconnects 351 during a subsequent etching process step. Thereafter, a first silicon dioxide film 353 is formed to be, for example, 1μm thick on the silicon nitride film 352. Next, an organic film 354 is deposited to be, for example, 400 nm thick on the first silicon dioxide film 353. Then, a second silicon dioxide film 355 is formed to be, for example, 50 nm thick on the organic film 354. And, a titanium nitride film 356 is formed to be, for example, 50 nm thick on the second silicon dioxide film 355.

The first and second silicon dioxide films 353 and 355 may

be deposited by any arbitrary technique. For example, these films 353 and 355 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

Next, as shown in Figure 15(b), a first resist pattern 357, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 356. Thereafter, the titanium nitride film 356 is dry-etched using the first resist pattern 357 as a mask, thereby forming a mask pattern 358 out of the titanium nitride film 356 as shown in Figure 15(c).

Subsequently, as shown in Figure 16(a), the first resist pattern 357 is removed and then a second resist pattern 359, having openings for forming contact holes, is formed on the second silicon dioxide film 355. Then, the second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask, thereby forming a patterned second silicon dioxide film 355A and a patterned organic film 354A having openings 360 for forming contact holes as shown in Figure 16(b). In this case, the second resist pattern 359 is removed during the step of etching the organic film 354.

Next, as shown in Figure 16(c), the first silicon dioxide film 353 is dry-etched using the patterned second silicon dioxide film 355A and the patterned organic film 354A as a mask, thereby forming a patterned first silicon dioxide film 353A having contact holes 361. In this etching process step, the mask pattern 358 is transferred to the patterned second silicon dioxide film 355A. Accordingly, openings for forming wiring grooves are formed in the patterned second silicon dioxide film 355A.

Thereafter, as shown in Figure 16(d), the patterned organic film 354A is dry-etched using the mask pattern 358 and the patterned second silicon dioxide film 355A having the openings for forming wiring grooves as a mask, thereby forming the wiring grooves 362. In forming the wiring grooves 362, by selecting such etching conditions that the first silicon dioxide film 353A is etched at a rate sufficiently lower than that of the organic film 354A, sufficient selectivity can be secured for the patterned first silicon dioxide film 353A. Accordingly, the depth of the wiring grooves 362 can be determined univocally at the sum of the thicknesses of the second silicon dioxide film 355 and the organic film 354.

If the second resist pattern 359 may have been misaligned with the first resist pattern 357, then the mask pattern 358 should be dry-etched using the second resist pattern 359 as a mask before the second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask. That is to say, if the mask pattern 358 is partially exposed inside the openings of the second resist pattern 359 for forming contact holes because of the misalignment of the second resist pattern 359 with the first resist pattern 357, then the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask. In this manner, the openings of the mask pattern 358 are expanded to include the openings for forming wiring grooves and contact holes.

Subsequently, the silicon nitride film 352 is dry-etched using the patterned first silicon dioxide film 353A as a mask, thereby forming a patterned silicon nitride film 352A and exposing the first metal interconnects 351 within the contact holes 361 as shown in Figure

17(a).

Then, as shown in Figure 17(b), an adhesion layer 363, made of titanium nitride, is deposited to be, for example, 50 nm thick on the wall faces of the contact holes 361 and the wiring grooves 362. Thereafter, a metal film 364 is deposited over the entire surface of the substrate to completely fill in the contact holes 361 and the wiring grooves 362. In this embodiment, the metal film 364 may be made of any arbitrary metal. For example, copper, aluminium, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 364 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure 17(c), respective portions of the adhesion layer 363, the metal film 364 and the mask pattern 358, which are deposited on the patterned second silicon dioxide film 355A, are removed by, for example, a CMP technique. As a result, second metal interconnects 365 and contacts 366, connecting the first and second metal interconnects 351 and 365, are formed out of the metal film 364.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 365 through the same process steps as those described above.

In this modified example of the third embodiment, while the first resist pattern 357 is ashed and removed by oxygen plasma, the organic film 354 is not exposed to the oxygen plasma, because the second silicon dioxide film 355 exists on the organic film 354.

Also, in this example, the second resist pattern 359 is removed

while the second silicon dioxide film 355 and the organic film 354 are dry-etched using the second resist pattern 359 as a mask. Accordingly, since there is no need to ash and remove the second resist pattern 359 with oxygen plasma, the organic film 354 is not exposed to oxygen plasma.

(Fourth Embodiment)

Next, an exemplary method for forming an interconnection structure according to the fourth embodiment of the present invention will be described with reference to Figures 18(a) through 18(c), Figures 19(a) through 19(c) and Figures 20(a) through 20(c).

First, as shown in Figure 18(a), a silicon nitride film 402 is formed over first metal interconnects 401 formed on a semiconductor substrate 400. The silicon nitride film 402 is formed to be, for example, 50 nm thick and to protect the first metal interconnects 401 during a subsequent etching process step. Thereafter, a first low-dielectric-constant SOG film 403, having a siloxane skeleton, is formed to be, for example, 1μm thick on the silicon nitride film 402. Next, an organic-containing silicon dioxide film 404, containing an organic component in silicon dioxide, is deposited to be, for example, 50 nm thick on the first low-dielectric-constant SOG film 403. Then, a second low-dielectric-constant SOG film 405, having a siloxane skeleton, is formed to be, for example, 400 nm thick on the organic-containing silicon dioxide film 404. And, a titanium nitride film 406 is formed to be, for example, 50 nm thick on the second low-dielectric-constant SOG film 405.

The first and second low-dielectric-constant SOG films 403

and 405 may be, for example, HSQ films. The organic-containing silicon dioxide film 404 may be deposited by any arbitrary technique. For example, the film 404 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Then, an organic-containing silicon dioxide film 404, having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide, can be obtained.

Next, as shown in Figure 18(b), a first resist pattern 407, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 406. Thereafter, the titanium nitride film 406 is dry-etched using the first resist pattern 407 as a mask, thereby forming a mask pattern 408 out of the titanium nitride film 406 as shown in Figure 18(c).

Subsequently, a second resist pattern 409, having openings for forming contact holes, is formed by lithography on the second low-dielectric-constant SOG film 405 without removing the first resist pattern 407. Then, the second low-dielectric-constant SOG film 405 and the organic-containing silicon dioxide film 404 are sequentially dry-etched using the second resist pattern 409 as a mask, thereby forming a patterned second low-dielectric-constant SOG film 405A and a patterned organic-containing silicon dioxide film 404A as shown in Figure 19(a).

Next, the first and second resist patterns 407 and 409 are ashed and removed with oxygen plasma. As a result, a damaged layer 410 is unintentionally formed in respective portions of the patterned second low-dielectric-constant SOG film 405A and the first low-dielectric-constant SOG film 403, which are exposed inside the

openings for forming contact holes, as shown in Figure 19(b).

Then, the patterned second low-dielectric-constant SOG film 405A is dry-etched using the mask pattern 408 as a mask, thereby forming wiring grooves 412 in the patterned second low-dielectric-constant SOG film 405A as shown in Figure 19(c). At the same time, the first low-dielectric-constant SOG film 403 is dry-etched using the patterned organic-containing silicon dioxide film 404A as a mask, thereby forming a patterned first low-dielectric-constant SOG film 403A having contact holes 411 as shown in Figure 19(c). By performing this dry-etching process step, the damaged layer 410 can be removed from the patterned second low-dielectric-constant SOG films 405A and the first low-dielectric-constant SOG film 403.

Subsequently, the silicon nitride film 402 is dry-etched using the patterned organic-containing silicon dioxide film 404A as a mask, thereby forming a patterned silicon nitride film 402A and exposing the first metal interconnects 401 within the contact holes 411 as shown in Figure 20(a).

Then, as shown in Figure 20(b), an adhesion layer 413, made of titanium nitride, is deposited to be, for example, 50 nm thick on the wall faces of the contact holes 411 and the wiring grooves 412. Thereafter, a metal film 414 is deposited over the entire surface of the substrate to completely fill in the contact holes 411 and the wiring grooves 412. In this embodiment, the metal film 414 may be made of any arbitrary metal. For example, copper, aluminium, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 414 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure 20(c), respective portions of the adhesion layer 413, the metal film 414 and the mask pattern 408, which are deposited on the patterned second low-dielectric-constant SOG film 405A, are removed by, for example, a CMP technique. As a result, second metal interconnects 415 and contacts 416, connecting the first and second metal interconnects 401 and 415, are formed out of the metal film 414.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects 114 through the same process steps as those described above.

In the fourth embodiment, while the first and second resist patterns 407 and 409 are ashed and removed with oxygen plasma, a damaged layer 410 is formed in the first low-dielectric-constant SOG film 403 and the patterned second low-dielectric-constant SOG film 405A. But, the damaged layer 410 can be removed while the contact holes 411 and the wiring grooves 412 are formed.

Accordingly, the first and second low-dielectric-constant SOG films 403 and 405 may be made of a material degradable with oxygen plasma. For example, in general, if an HSQ film is exposed to oxygen plasma, Si-H bonds thereof are oxidised and the content of water and the relative dielectric constant thereof both increase to deteriorate the reliability and performance of the device. However, according to the fourth embodiment, the patterned first low-dielectric-constant SOG film 403A, in which the contact holes 411 have already been formed, and the patterned second low-dielectric-constant SOG film 405A, in which the wiring grooves 412

have already been formed, are not affected by oxygen plasma any more. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

[Effects of the Invention]

According to the first method for forming an interconnection structure, it is not necessary to perform the step of ashing and removing the first and second resist patterns with oxygen plasma. Since this enables to prevent the third insulating film from being damaged during ashing and removing a resist pattern, a low-dielectric-constant insulating film, which would otherwise be damaged easily by oxygen plasma, may be used as the third insulating film. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In addition, the second insulating film can be used as an etch stopper while the wiring grooves are formed by dry-etching the third insulating film using the mask pattern as a mask in the tenth step. Accordingly, the depth of each wiring groove can be equalised with the thickness of the third insulating film. That is to say, the depth of the wiring grooves can be defined by self-alignment.

If the first method for forming an interconnection structure further includes the step of forming a metal adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes between the tenth and eleventh steps, the adhesion between the upper-level metal interconnects and the third insulating film and

between the contacts and the first insulating film can be ensured.

In the first method for forming an interconnection structure, if the third insulating film is mainly composed of an organic component, the conditions, employed in the eighth step, that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, are realised with reliability.

In this case, if the third step includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the third insulating film with reliability.

Further, in this case, if the first insulating film is also mainly composed of an organic component, the conditions, employed in the ninth step, that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, are realised with reliability. At the same time, the conditions, employed in the tenth step, that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, are also realised with reliability.

In the case where the first and second insulating films are both mainly composed of organic components, if the first method further includes the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process

using a reactive gas containing nitrogen between the tenth and eleventh steps, the adhesion between the upper-level metal interconnects and the third insulating film mainly composed of an organic component, and between the contacts and the first insulating film mainly composed of an organic component can be ensured without fail.

In the case where the first insulating film is mainly composed of an organic component, if the first step includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the first insulating film with reliability.

According to the second method for forming an interconnection structure, even if a damaged layer is formed in respective parts of the first and third insulating films that are exposed inside the openings for forming contact holes in the second insulating film during the tenth step of removing the first and second resist patterns, the damaged layer can be removed without fail in the eleventh step. Accordingly, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In the second method for forming an interconnection structure, if the third insulating film is a low-dielectric-constant SOG film with a siloxane skeleton, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist

application process.

[Brief Description of the Drawings]

[Fig. 1]

(a) through (c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the first embodiment of the present invention.

[Fig. 2]

(a) through (c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

[Fig. 3]

(a) through (c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

[Fig. 4]

(a) through (c) are cross-sectional views illustrating problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

[Fig. 5]

(a) through (c) are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

[Fig. 6]

(a) through (c) are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern

during the process of forming the interconnection structure of the first embodiment.

[Fig. 7]

(a) through (c) are cross-sectional views illustrating measures to solve the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

[Fig. 8]

(a) through (c) are cross-sectional views illustrating the measures to solve the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

[Fig. 9]

(a) through (c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the second embodiment of the present invention.

[Fig. 10]

(a) through (c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

[Fig. 11]

(a) through (c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

[Fig. 12]

(a) through (c) are cross-sectional views illustrating respective process steps for forming an interconnection structure

according to the third embodiment of the present invention.

[Fig. 13]

(a) through (c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

[Fig. 14]

(a) through (c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

[Fig. 15]

(a) through (c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to a modified example of the third embodiment.

[Fig. 16]

(a) through (d) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the modified example of the third embodiment.

[Fig. 17]

(a) through (c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the modified example of the third embodiment.

[Fig. 18]

(a) through (c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the fourth embodiment of the present invention.

[Fig. 19]

(a) through (c) are cross-sectional views illustrating

respective process steps for forming the interconnection structure of the fourth embodiment.

[Fig. 20]

(a) through (c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fourth embodiment.

[Explanation of References]

100 semiconductor substrate
101 first metal film
102 silicon nitride film
102A patterned silicon nitride film
103 first organic film
103A patterned first organic film
104 organic-containing silicon dioxide film
104A patterned organic-containing silicon dioxide film
105 second organic film
105A patterned second organic film
106 titanium nitride film
107 first resist pattern
108 mask pattern
109 second resist pattern
110 contact hole
111 wiring groove
112 adhesion layer
113 metal film
114 second metal interconnect
115 contact

200 semiconductor substrate

201 first metal film

202 silicon nitride film

202A patterned silicon nitride film

203 first organic film

203A patterned first organic film

204 organic-containing silicon dioxide film

204A patterned organic-containing silicon dioxide film

205 second organic film

205A patterned second organic film

206 titanium nitride film

207 first resist pattern

208 mask pattern

209 second resist pattern

210 contact hole

211 wiring groove

212 adhesion layer

213 metal film

214 second metal interconnect

215 contact

300 semiconductor substrate

301 first metal film

302 silicon nitride film

302A patterned silicon nitride film

303 first organic-containing silicon dioxide film

303A patterned first organic-containing silicon dioxide film

304 low-dielectric-constant SOG film

305 second organic-containing silicon dioxide film

305A patterned second organic-containing silicon dioxide film

306 titanium nitride film

307 first resist pattern

308 mask pattern

309 second resist pattern

310 contact hole

311 wiring groove

312 adhesion layer

313 metal film

314 second metal interconnect

315 contact

350 semiconductor substrate

351 first metal film

352 silicon nitride film

352A patterned silicon nitride film

353 first silicon dioxide film

353A patterned first silicon dioxide film

354 organic film

355 second silicon dioxide film

355A patterned second silicon dioxide film

356 titanium nitride film

357 first resist pattern

358 mask pattern

359 second resist pattern

360 opening for forming a contact hole

361 contact hole

362 wiring groove

363 adhesion layer

364 metal film

365 second metal interconnect

366 contact

400 semiconductor substrate

401 first metal interconnect

402 silicon nitride film

402A patterned silicon nitride film

403 first low-dielectric-constant SOG film

403A patterned first low-dielectric-constant SOG film

404 organic-containing silicon dioxide film

404A patterned organic-containing silicon dioxide film

405 second low-dielectric-constant SOG film

405A patterned second low-dielectric-constant SOG film

406 titanium nitride film

407 first resist pattern

408 mask pattern

409 second resist pattern

410 damaged layer

411 contact hole

412 wiring groove

413 adhesion layer

414 metal film

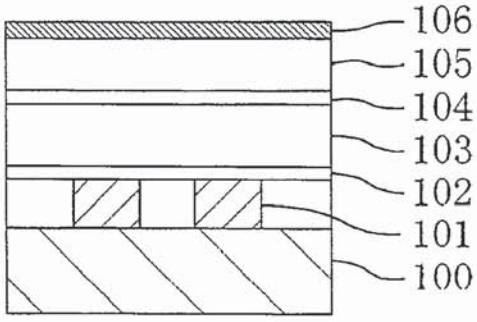
415 second metal film

416 contact

【書類名】 図面
[Name of the Document] DRAWINGS

【図１】
[Fig. 1]

(a)



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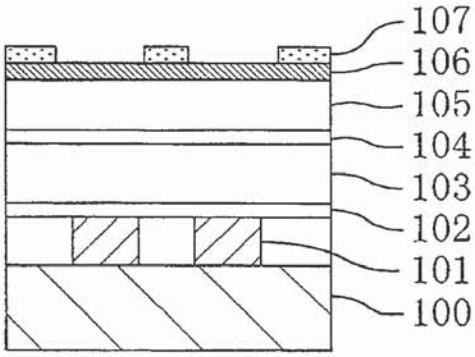

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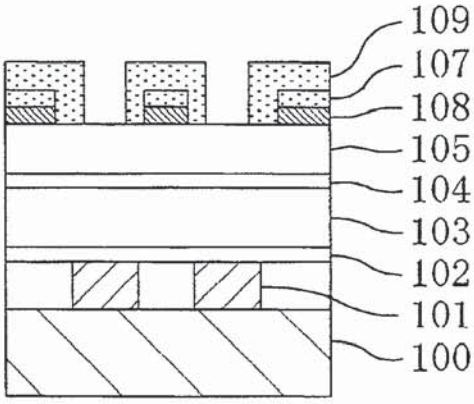

【図２】
[Fig. 2]

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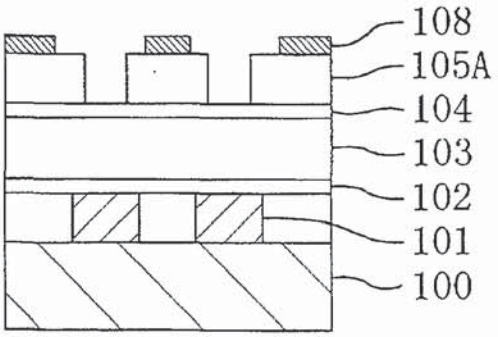
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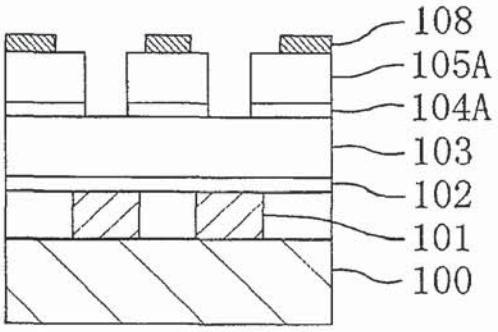
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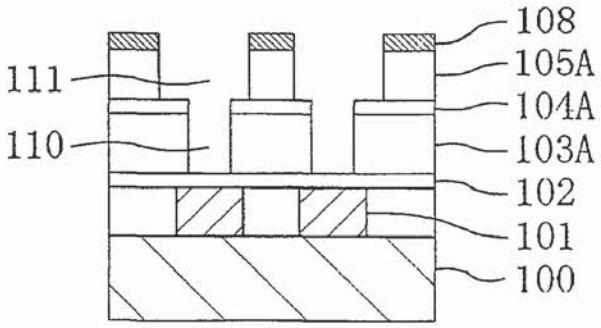
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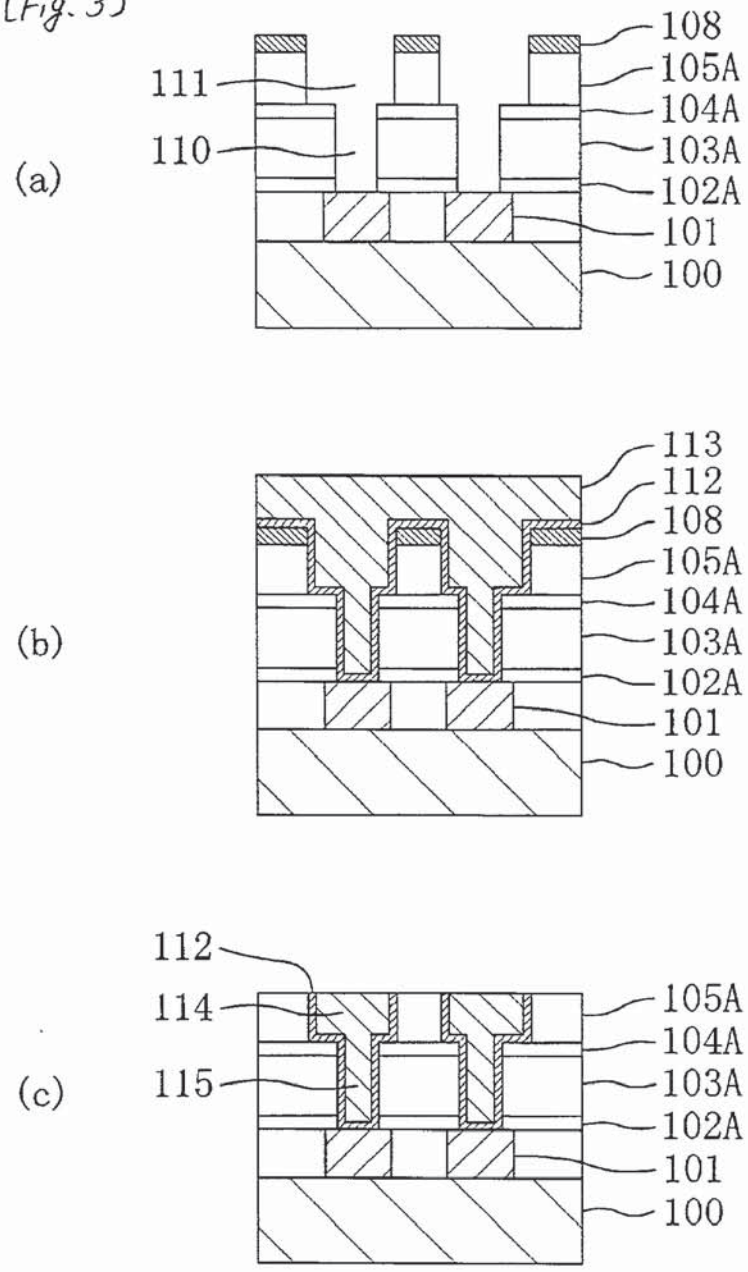
【図３】
[Fig. 3]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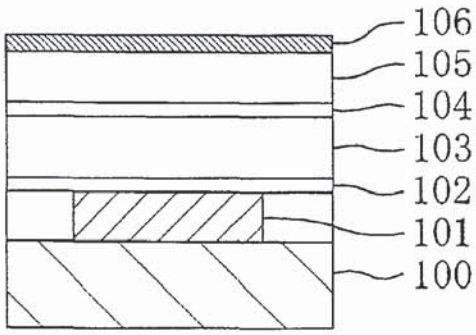
【図４】
[Fig. 4]

(a)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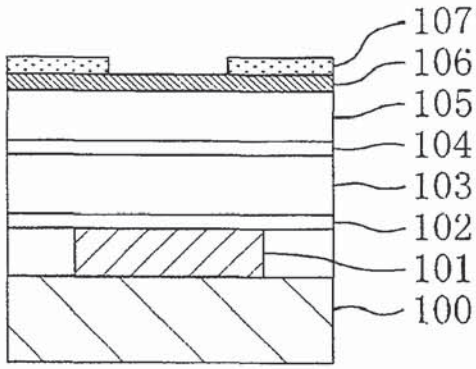
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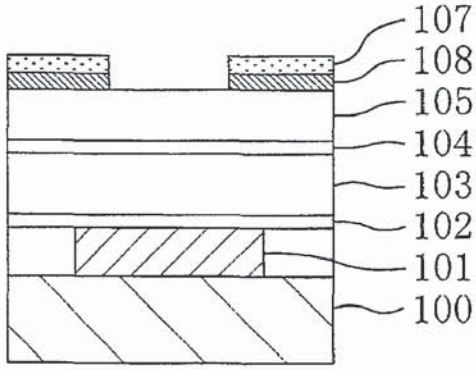
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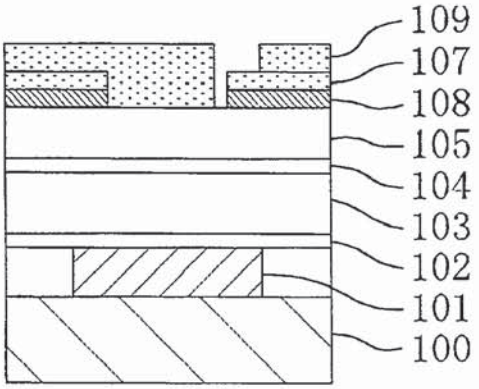
【図５】
[Fig. 5]

(a)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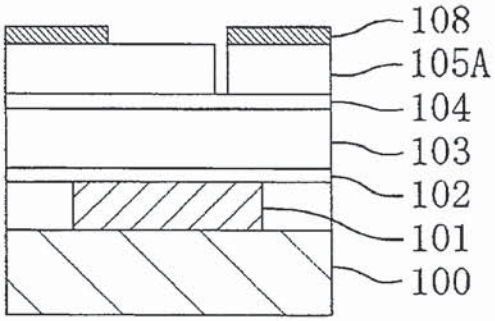
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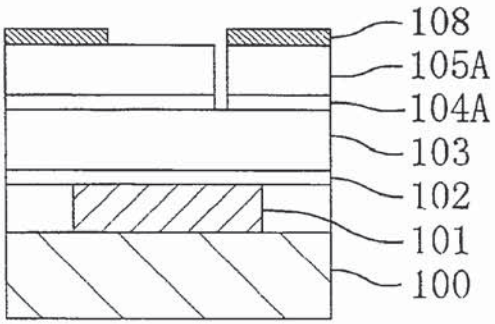
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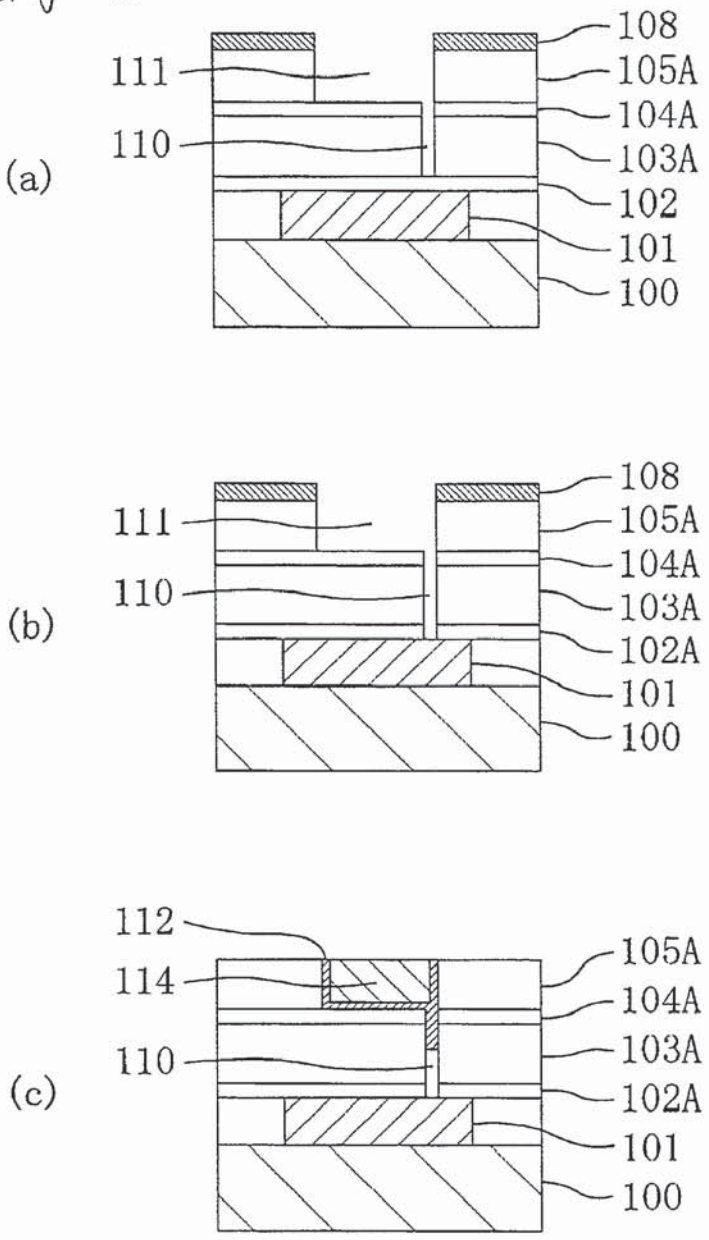
【図６】
[Fig. 6]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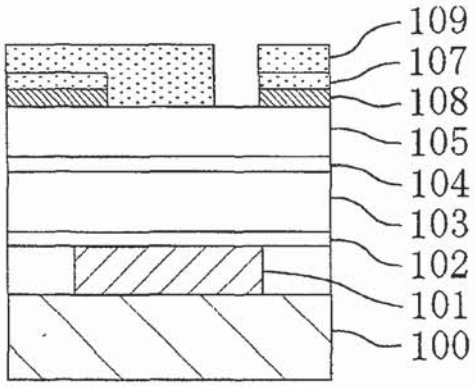
【図７】
[Fig. 7]

(a)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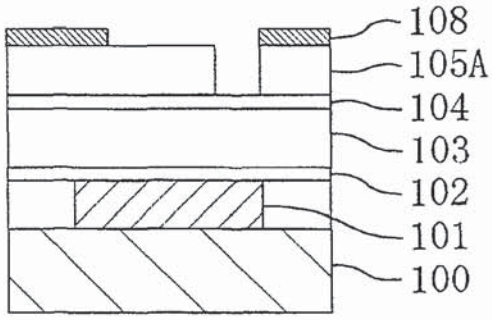
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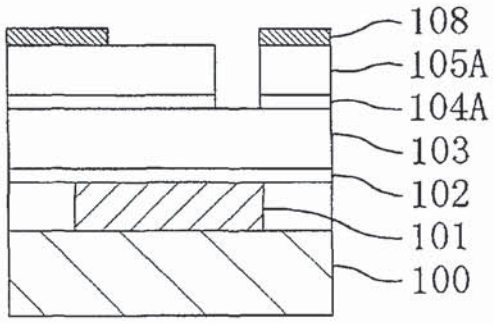
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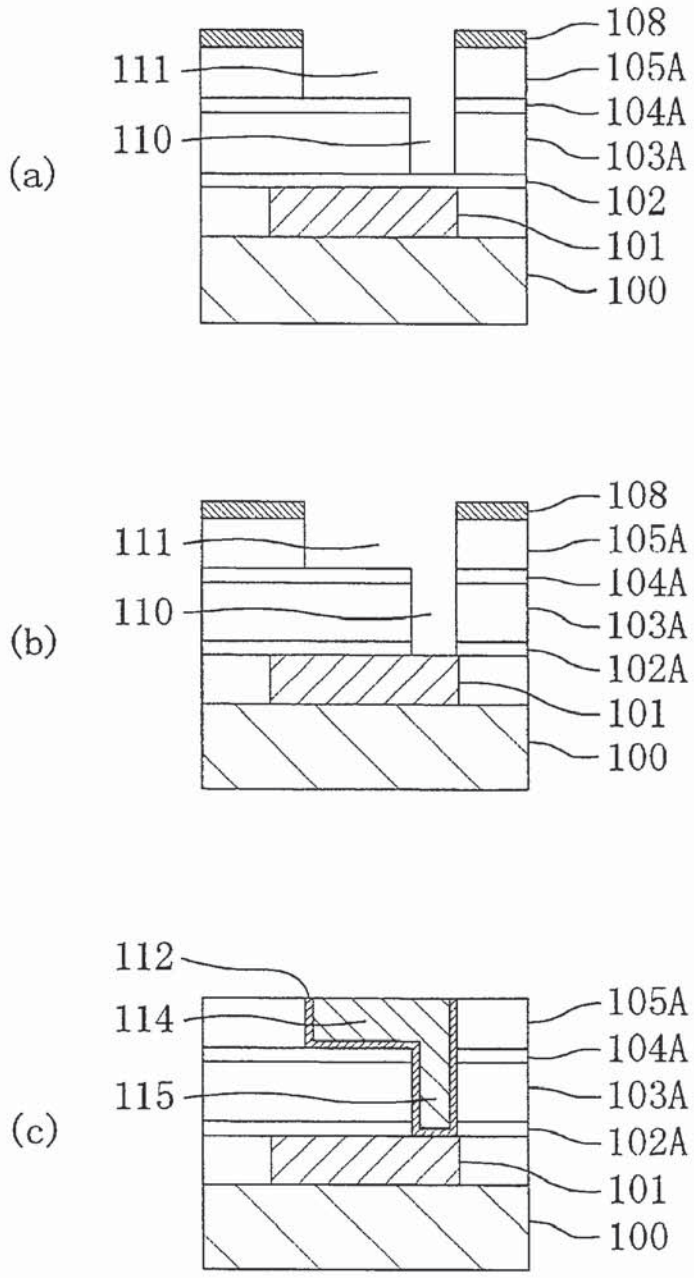
【図８】
[Fig. 8]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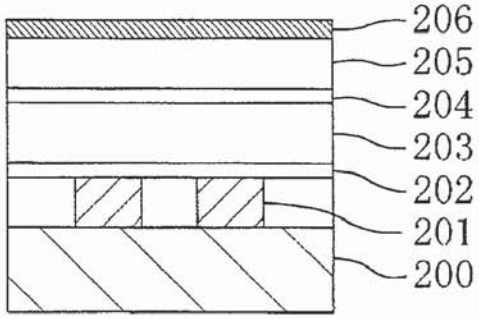
【図９】
[Fig. 9]

(a)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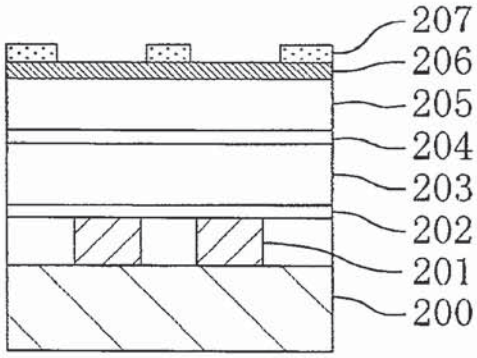
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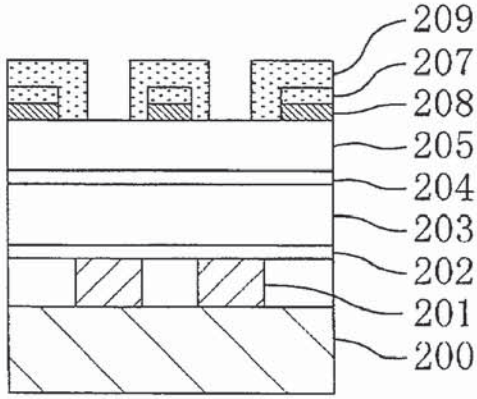
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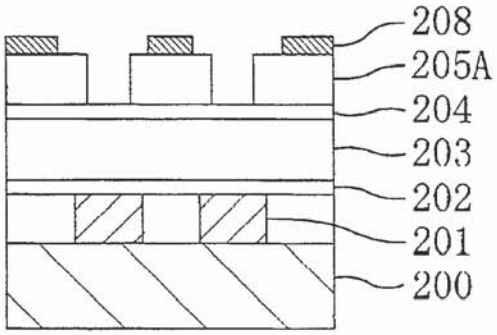
【図１０】
[Fig. 10]

(a)



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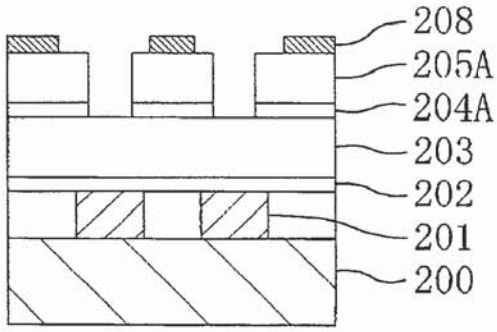

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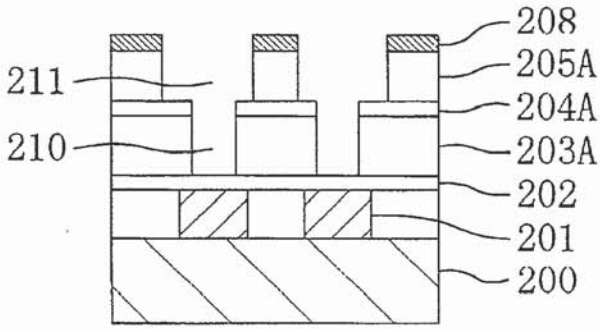

【図１１】
[Fig. 11]

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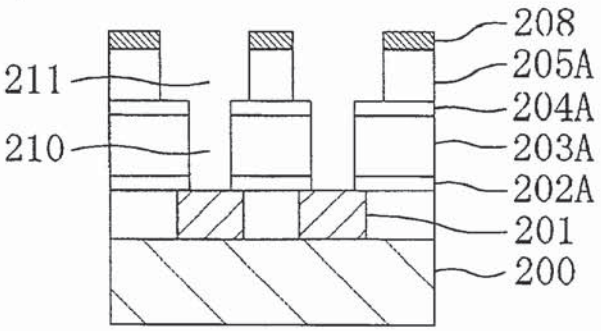

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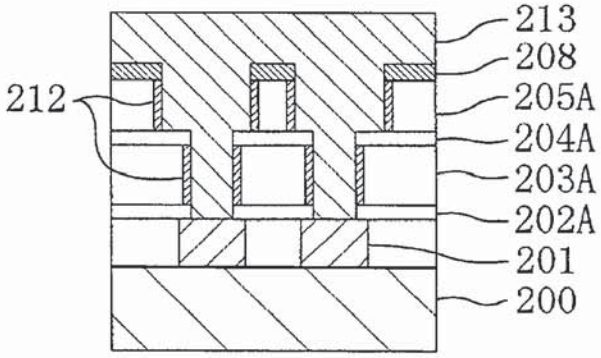

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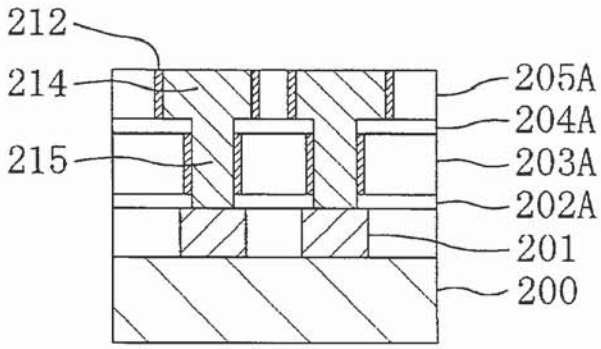

【図１２】
[Fig. 12]

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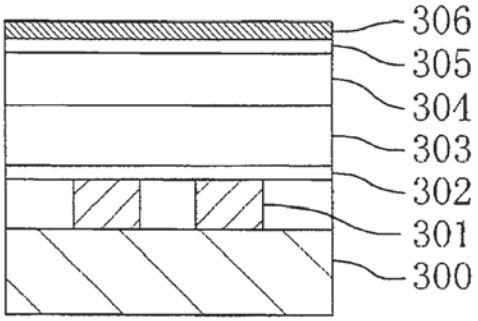

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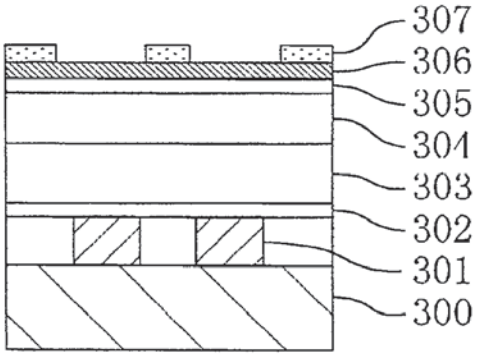

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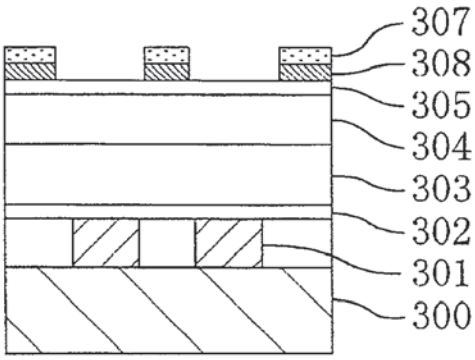
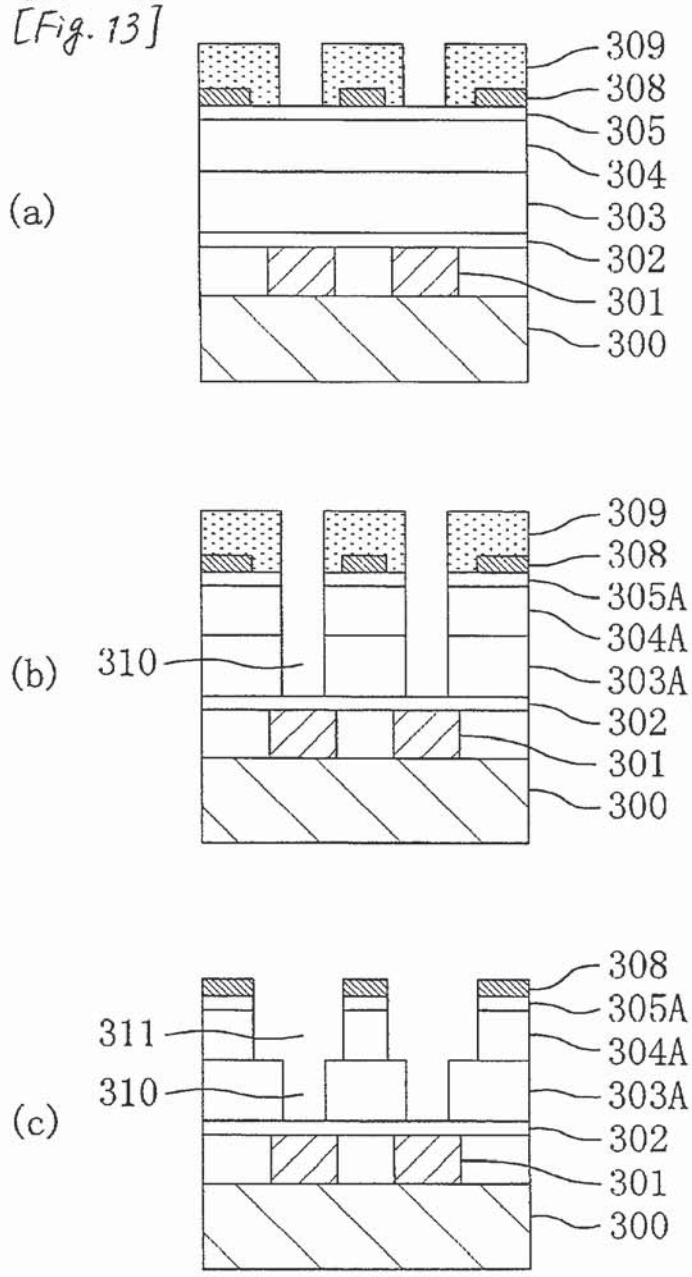


【図１３】
[Fig. 13]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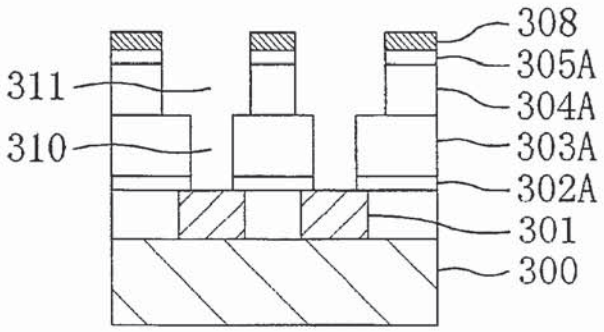
【図１４】
[Fig. 14]

(a)



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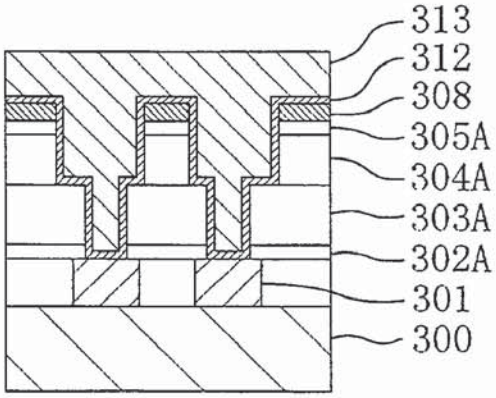

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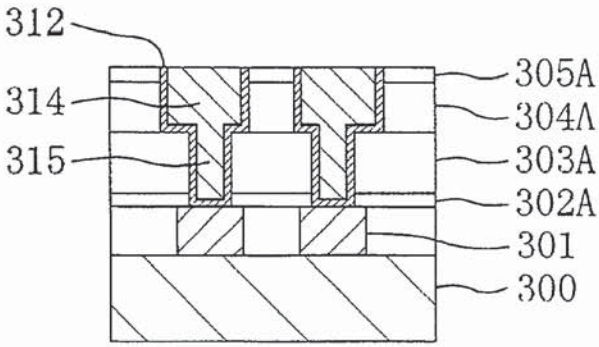

【図１５】
[Fig. 15]

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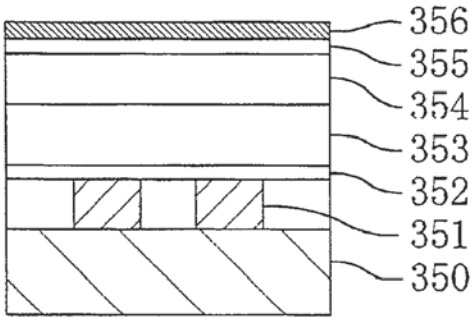

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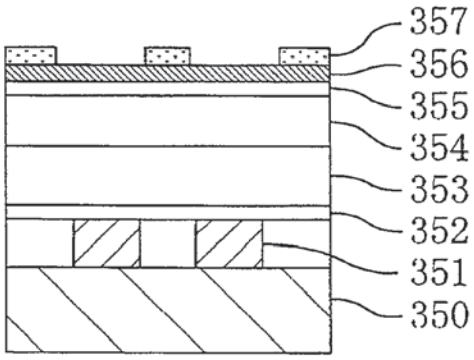

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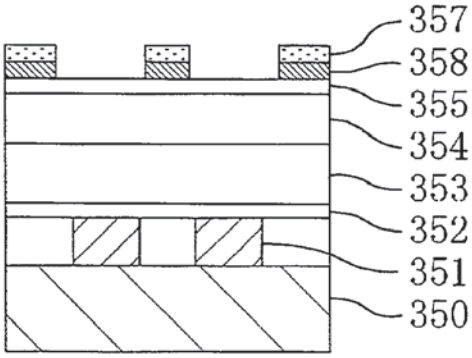
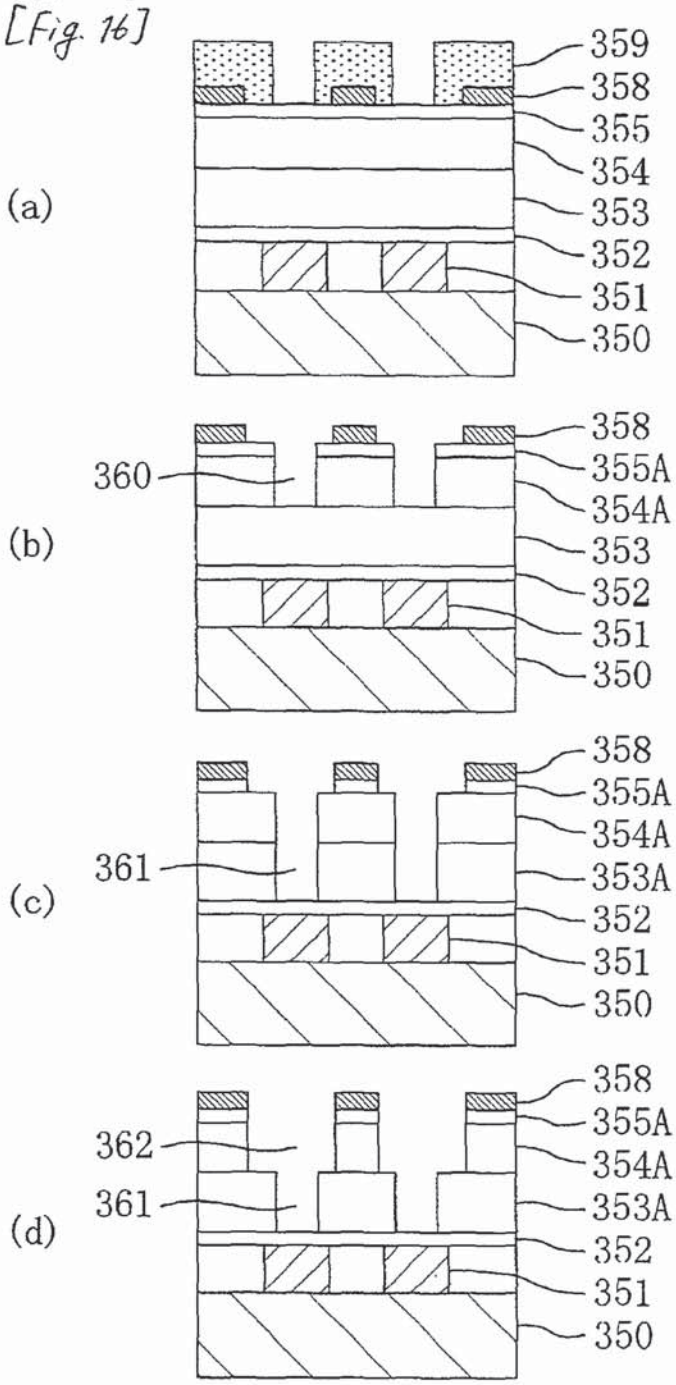


【図１６】
[Fig. 16]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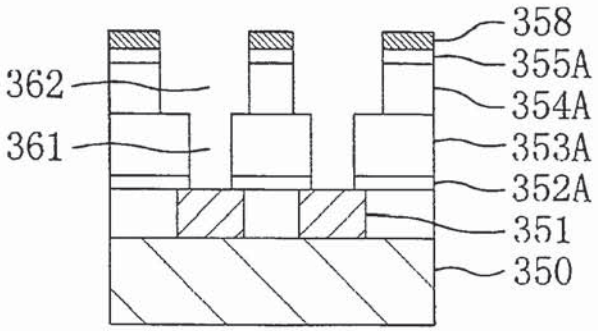
【図１７】
[Fig. 17]

(a)



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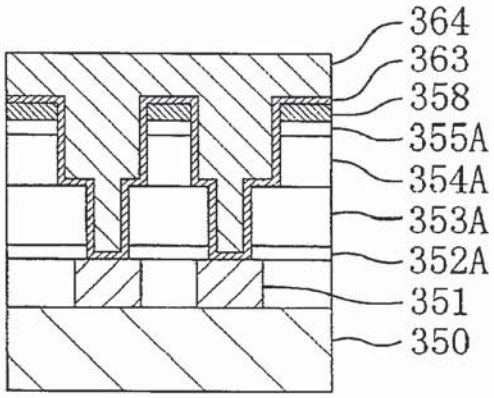

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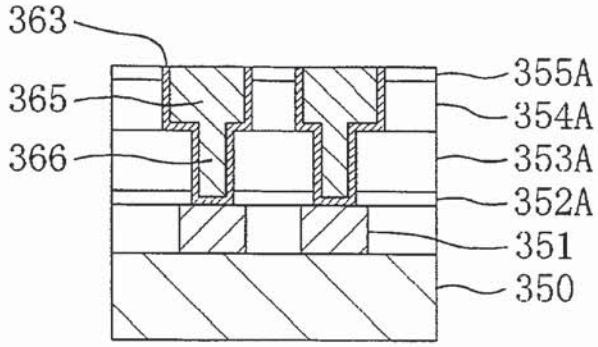
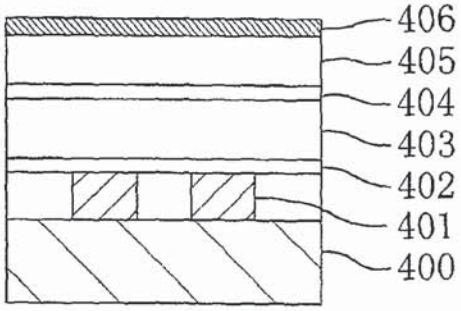


【図１８】
[Fig. 18]

(a)



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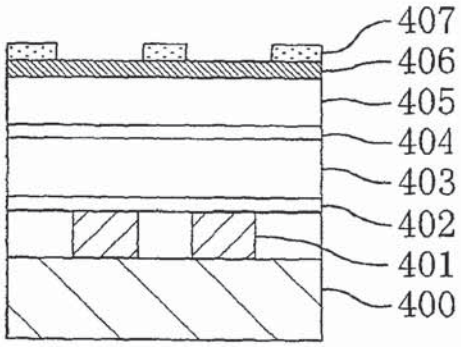
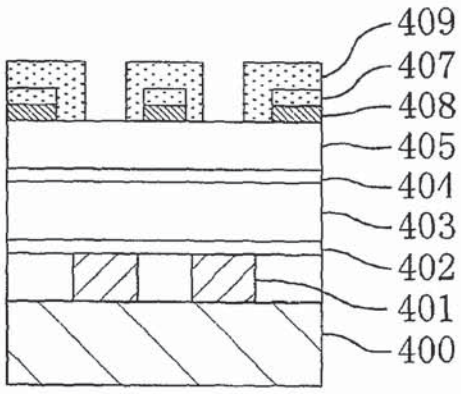
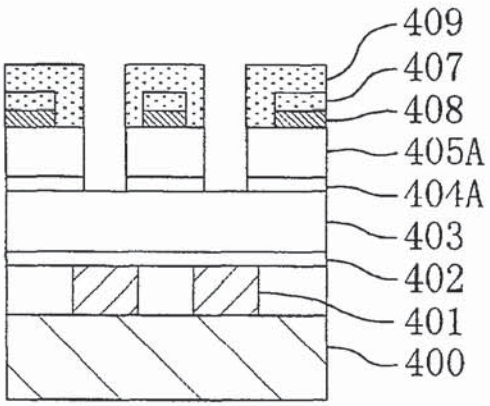


(c)

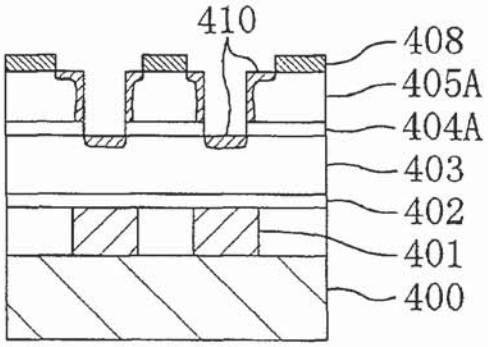


【図１９】
[Fig. 19]

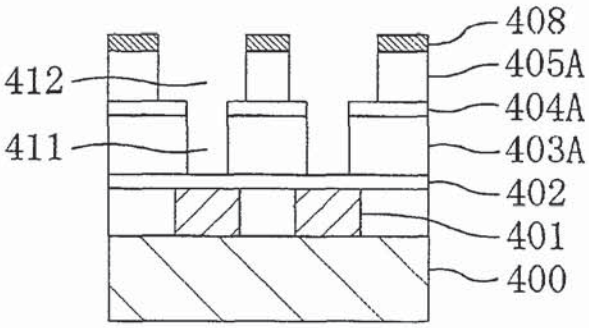
(a)



(b)

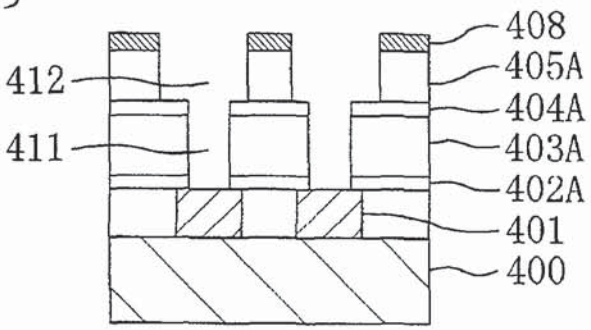


(c)

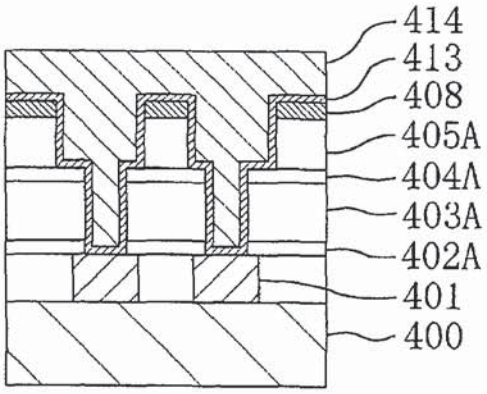


【図２０】
[Fig. 20]

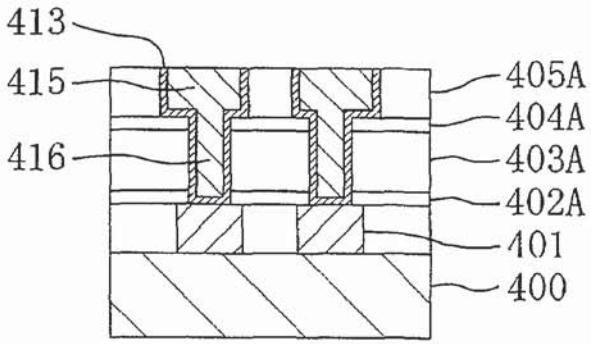
(a)



(b)



(c)



[Name of the Document] ABSTRACT

[Abstract]

[Purpose] To enable the forming of an interlevel insulating film with a low dielectric constant through an ordinary resist application process.

[Solution] Over first metal interconnects 101 formed on a semiconductor substrate 100, a silicon nitride film 102, a first organic film 103, an organic-containing silicon dioxide film 104, a second organic film 105, and a titanium nitride film 106 are deposited sequentially. Then, the titanium nitride film 106 is etched using as a mask the first resist pattern 107 formed on the titanium nitride film 106, thereby forming a mask pattern 108. Thereafter, a second resist pattern 109 is formed on the second organic film 105. Then, the second organic film 105 is etched using the second resist pattern 109 as a mask, thereby patterning the second organic film 105 and removing the first and second resist patterns 107 and 109. Next, the second organic film 105 is etched using the mask pattern 108 as a mask, thereby forming wiring grooves, and concurrently the first organic film 103 is etched using the patterned organic-containing silicon dioxide film 104 as a mask, thereby forming contact holes.

[Selected Figure] Figure 1