UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD., Petitioner,

v.

GODO KAISHA IP BRIDGE 1, Patent Owner.

Case IPR2016-01377 Patent 6,197,696 B1

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE



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| Bayer CropScience AG v. Dow Agro Sciences LLC, 728 F.3d 1324 (Fed. Cir. 2013)9 |
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| Dynamic Drinkware, LLC v. Nat'l Graphics, Inc., 800 F.3d 1375 (Fed. Cir. 2015) |
| In re Applied Materials, Inc., 692 F.3d 1289 (Fed. Cir. 2012)27 |
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| Lucent Techs., Inc. v. Gateway, Inc., 543 F.3d 710 (Fed. Cir. 2008)2 |
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| Trs. of Columbia Univ. v. Symantec Corp., 811 F.3d 1359 (Fed. Cir. 2016)9 |
| TurboCare Div. of Demag Delaval Turbomachinery Corp. v. General Elec. Co., 264 F.3d 1111 (Fed. Cir. 2001) |
| Other Authorities |
| Core Survival, Inc. v. S&S Precision, LLC, PGR2015-00022, Paper 8 (P.T.A.B. Feb. 19, 2016) |
| Rules |
| 37 C.F.R. §42.24 |



LIST OF EXHIBITS

Exhibit 1001: U.S. Patent No. 6,197,696 to Aoi et al.

Exhibit 1002: Expert Declaration of Dr. Bruce W. Smith, Ph.D.

Exhibit 1003: U.S. Patent No. 3,617,824 to Shinoda et al.

Exhibit 1004: U.S. Patent No. 3,838,442 to Humphreys.

Exhibit 1005: U.S. Patent No. 6,140,226 to Grill et al.

Exhibit 1006: U.S. Patent No. 5,635,423 to Huang et al.

U.S. Patent No. 5,741,626 to Jain et al. Exhibit 1007:

C. Akrout et al., "A 480-MHz Microprocessor in a $0.12\mu m L_{eff}$ Exhibit 1008:

CMOS Technology with Copper Interconnects," IEEE J. of

Solid-State Circuits, Vol. 33, no. 11 (November 1998).

Exhibit 1009: J.N. Burghartz et al., "Monolithic Spiral Inductors Fabricated

> Using a VLSI Cu-Damascene Interconnect Technology and Low-Loss Substrates," International Electron Devices Meeting

(December 1996).

Exhibit 1010: U.S. Patent No. 6,100,184 to Zhao et al.

Exhibit 1011: U.S. Patent No. 6,103,616 to Yu et al.

Exhibit 1012: File History of U.S. Patent No. 6,197,696 to Aoi et al.

Exhibit 1013: Japanese Patent Application No. 10-079371 to Aoi.

Exhibit 1014: Certified Translation of Japanese Patent Application No. 10-

079371 to Aoi.

Exhibit 1015: Japanese Patent Application No. 11-075519 to Aoi.

Exhibit 1016: Certified Translation of Japanese Patent Application No. 11-

075519 to Aoi.

Exhibit 1017: U.S. Provisional Patent Application No. 60/071,628.



Exhibit 1018: U.S. Patent No. 5,592,024 to Aoyama et al.

Exhibit 1019: U.S. Patent No. 5,920,790 to Wetzel et al.

Exhibit 1020: Transcript of Teleconference with the Board, dated November

16, 2016.

Exhibit 1021: http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=

4251.

Exhibit 1022: IEEE, "Technical Digest of the International Electron Devices,"

1996 International Electron Devices Meeting at San Francisco,

CA, Table of Contents (December 8-11, 1996).

Exhibit 1023: J.N. Burghartz et al., "Monolithic spiral inductors fabricated

using a VLSI Cu-damascene interconnect technology and low-loss substrates," 1996 International Electron Devices Meeting at San Francisco, CA, pp. 99-102 (December 8-11, 1996).

Exhibit 1024: http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=15684.

Exhibit 1025: G. Gerosa, "Introduction to the Digital Section," IEEE Journal

of Solid-State Circuits, vol. 33, no. 11, p. 1599 (Nov. 1998).

Exhibit 1026: J. Dreibelbis, "Introduction to the Memory Section," IEEE

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Number=2.

Exhibit 1029: C. Akrout et al., "A 480-MHz RISC Microprocessor in a 0.12-

μm L_{eff} CMOS Technology with Copper Interconnects," IEEE



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