UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01377
Patent 6,197,696 B1

**DECLARATION OF DR. BRUCE W. SMITH, PH.D.
IN SUPPORT OF PETITIONER'S REPLY**

# TABLE OF CONTENTS

I, Dr. Bruce W. Smith, Ph.D., declare as follows:

## I. Introduction

1.     My name is Dr. Bruce W. Smith. I previously signed a declaration in relation to these proceedings on July 11, 2016, which I understand is Exhibit 1002. My qualifications, a summary of my opinions, a list of materials reviewed, and an explanation of the relevant legal standards I was asked to apply appear at paragraphs 1 through 31 of Exhibit 1002, which I incorporate herein by reference for brevity.

## II. Materials Reviewed

2.     In addition to the references listed in Exhibit 1002, I have reviewed the following references in forming the opinions expressed in this declaration:

- Declaration of Dr. Bruce W. Smith, Ph.D. dated July 11, 2016 (which I understand is Exhibit 1002);

- U.S. Provisional Patent Application No. 60/071,628 with line numbers appended (which I have been told is Exhibit 1049);

- IPB's Translation of Japanese Patent Application No. 10-079371 to Aoi (which I have been told is Exhibit 2012);

- Excerpts from James D. Plummer et al., "Silicon VLSI Technology: Fundamentals, Practice, and Modeling" (2000) ("*Plummer*," which I have been told are Exhibits 1031 and 2016);

- Excerpts from C.Y. Chang & S. M. Sze, "ULSI Technology" (1996) ("*Chang & Sze*," which I have been told is Exhibit 1032);

- Excerpts from S. Wolf & R.N. Tauber, "Silicon Processing for the VLSI Era: Volume 1: Process Technology" (1986) ("*Wolf & Tauber*," which I have been are Exhibits 1033 and 2020);

- U.S. Patent No. 5,091,047 to Cleeves et al. ("*Cleeves*," which I have been told is Exhibit 1034);

- U.S. Patent No. 6,287,973 to Aoi et al. ("the '973 patent," which I have been told is Exhibit 1035);

- U.S. Patent No. 4,560,436 to Bukhman et al. ("*Bukhman*," which I have been told is Exhibit 1036);

- U.S. Patent No. 6,091,081 to Matsubara et al. ("*Matsubara*," which I have been told is Exhibit 1037);

- U.S. Patent No. 4,473,437 to Higashikawa et al. ("*Higashikawa*," which I have been told is Exhibit 1038);

- U.S. Patent No. 5,880,018 to Boeck et al. ("*Boeck*," which I have been told is Exhibit 1039);

- U.S. Patent No. 4,832,789 to Cochran et al. ("*Cochran*," which I have been told is Exhibit 1040);

- U.S. Patent No. 4,855,252 to Peterman et al. ("*Peterman*," which I have been told is Exhibit 1041);

- U.S. Patent No. 5,786,276 to Brooks et al. ("*Brooks*," which I have been told is Exhibit 1042);

- U.S. Patent No. 5,756,216 to Becker et al. ("*Becker*," which I have been told is Exhibit 1043);

- U.S. Patent No. 5,821,168 to Jain ("*Jain 168*," which I have been told is Exhibit 1044);

- J.M. Moran & D. Maydan, "High Resolution, Steep Profile Resist Patterns," J. Vac. Sci. & Tech., vol. 16, no. 6 (Nov./Dec. 1979) ("*Moran & Maydan*," which I have been told is Exhibit 1045);

- M.M. O'Toole et al., "Linewidth Control in Projection Lithography Using a Multilayer Resist Process," IEEE Transactions on Electron Devices, vol. ED-28, no. 11 (Nov. 1981) ("*O'Toole*," which I have been told is Exhibit 1046);

- E. Bassous et al., "A Three-Layer Resist System for Deep U.V. and RIE Microlithography on Nonplanar Surfaces," J. Electrochem. Soc.: Solid-State Sci. & Tech. (Feb. 1983) ("*Bassous*," which I have been told is Exhibit 1047);

- Transcript of the Deposition of Dr. A. Glew (June 30, 2017) ("*Glew Deposition*," which I have been told is Exhibit 1048);

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