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I Roger P. Lewis, whose address is 42 Bird Street North, Martinsburg WV 25401, declare and state the following:

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I hereby certify that the Japanese translation of the attached document identified as:

JP Hei. 11 [1999] – 075519 Part I

is true, and that all statements of information and belief are believed to be true, and that these and similar statements are punishable by fines or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

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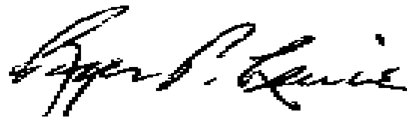

ROGER P. LEWIS

Date: June 30, 2016

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【Name of Item】 Abstract 1

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Required

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【Document Name】 Specifications
【Name of Invention】 Formation Method of Wiring Structure
【Scope of the Patent Claims】
【Claim 1】A formation method of wiring structure that is characterized by the following:

Process 1, by which a 1st insulating film is formed over the lower layer of metal wiring, and Process 2, by which a 2nd insulating film that differs in composition from the afore described 1st insulating film is formed over this 1st insulating film, and

Process 3, by which a 3rd insulating film that differs in composition from the afore described 2nd insulating film is formed over this 2nd insulating film, and

Process 4, by which a thin film is formed over the afore described 3rd insulating film, and

Process 5, by which a 1st resist pattern that has opening(s) for forming wiring is formed over the afore described thin film, and

Process 6, by which etching is performed vis-à-vis the afore described thin film whilst using the afore described 1st register pattern as a mask, thus forming from the afore described thin film a mask pattern that has opening(s) for forming wiring, and

Process 7, by which a 2nd resist pattern that has opening(s) for contact hole formation is formed over the afore described 3rd insulating film, and

Process 8, by which dry etching is performed vis-à-vis the afore described 3rd insulating film so that the etching conditions for the etching rate for the afore described 3rd insulating film vis-à-vis the 1st resist pattern and the 2nd resist patter is high whilst the etching rate vis-à-vis the afore described 2nd insulating film is low, so that together with pattern formation on the afore described 3rd insulating film of opening(s) for contact hole formation on this 3rd insulating film, and the total or partial removal of the afore described 1st resist pattern and the 2nd resist pattern, and

Process 9, by which the etching conditions are such that the etching rate vis-à-vis the afore described 2nd insulating film is high, the etching rate vis-à-vis the 3rd insulating film is low, the patterning is in such a way as to form on the afore described 2nd insulating film contact hole formation opening(s) on this 2nd insulating film, with, as a mask, the afore described 3rd insulating film that has been patterned vis-à-vis the afore described 2nd insulating, and

Process 11, by which, under etching […]

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[…] conditions such that the etching rate vis-à-vis the afore described 1st insulating film and 3rd insulating film is high whilst the etching rate vis-à-vis the afore described mask pattern and 2nd insulating pattern is low, are conducted dry etching vis-à-vis the afore described 3rd insulating film as the afore described mask pattern and also conducting dry etching vis-à-vis the afore described 1st insulating pattern as the patterned afore described 2nd insulating film, resulting in the formation of the wiring groove(s) in the afore described 3rd insulating film together with the contact hole(s) in the afore described 1st insulating film, and

Process 11, by which the filling of the afore described wiring groove(s) and contact hole(s) with a metal film so as to form the contact that connects the upper level metal wiring & the afore described lower level metal wiring and the afore described lower level metal wiring & the afore described upper level metal wiring.

【Claim 2】The formation method of wiring structure of Claim 1 that is characterized by the fact that it is further equipped with a process between the afore described Process 10 and Process 11 of the formation of an adhesive layer consisting of a metal film that is formed in the exposed portion(s) of the afore described wiring groove(s) in the afore describe 3rd insulating film and the exposed portion(s) of the afore described contact hole(s) of the afore described 1st insulating film.

【Claim 3】The formation method of wiring structure described in Claim 1 that is characterized by the fact that the afore described 3rd insulating film is mainly composed of organic component(s).

【Claim 4】The formation method of wiring structure described in Claim 3 that is characterized by the fact it includes the formation of the afore described 3rd insulating film by means of the CVD method wherein a perfluorodecalin containing reactive gas is used.

【Claim 5】The formation method of wiring structure described in Claim 3 that is characterized by the fact that the afore described 1st insulating film is mainly composed of organic component(s).

【Claim 6】The formation method of wiring structure of Claim 5 that is characterized by the fact that it is further equipped with a process between the afore described Process 10 and Process 11 of the formation of an adhesive layer by the plasma processing wherein nitrogen-containing reactive gas(es) is/are used on the exposed portion(s) of the afore described wiring groove(s) in the afore describe 3rd insulating film and the exposed portion(s) of the afore described contact hole(s) of the afore described 1st insulating film.

【Claim 7】The formation method of wiring structure described in Claim 3 that is characterized by the fact it includes the formation of the afore described 1st insulating film by means of the CVD method wherein a perfluorodecalin containing reactive gas is used.

【Claim 8】A formation method of wiring structure that is characterized by the following:

Process 1, by which a 1st insulating film is formed over the lower layer of metal wiring, and […]

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