United States Patent [19]

Humphreys

[11] **3,838,442**

[45] **Sept. 24, 1974**

[54] **SEMICONDUCTOR STRUCTURE HAVING METALLIZATION INLAID IN INSULATING LAYERS AND METHOD FOR MAKING SAME**

[75] Inventor: **Charles B. Humphreys,** Pleasant Valley, N.Y.

[73] Assignee: **International Business Machines Corporation,** Armonk, N.Y.

[22] Filed: **June 9, 1972**

[21] Appl. No.: **261,348**

Related U.S. Application Data

[63] Continuation of Ser. No. 28,891, April 15, 1970, abandoned.

[52] **U.S. Cl.** **357/54,** 357/68, 357/71

[51] **Int. Cl.** **H01l 29/34**

[58] **Field of Search** 317/234, 235

[56] **References Cited**

UNITED STATES PATENTS

3,461,347	8/1969	Lemelson	317/101
3,461,357	8/1969	Mutter et al.	317/234
3,479,237	11/1969	Bergh et al.	156/11
3,584,264	6/1971	McLouski et al.	317/234
3,597,834	8/1971	Lathrop et al.	29/576
3,622,384	11/1971	Davey et al.	117/212
3,649,888	3/1972	Pitzer et al.	317/235

OTHER PUBLICATIONS

1EEE Transactions on Elec. Devices, Oct. 1969, pp. 876–877.

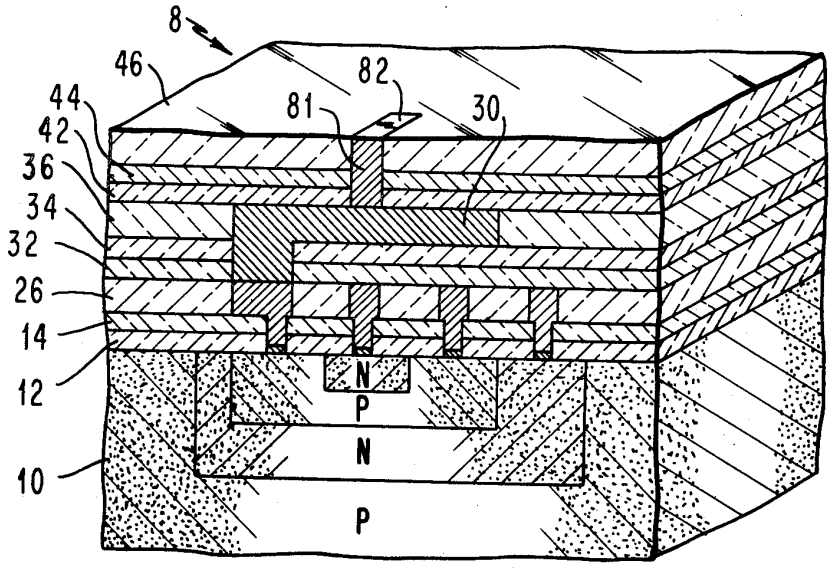
IBM (TDB), Vol. 8, No. 11, April 1966, p. 1687.

Primary Examiner—Rudolph V. Rolinec
Assistant Examiner—E. Wojciechowicz
Attorney, Agent, or Firm—Thomas F. Galvin

[57] **ABSTRACT**

In a semiconductor structure with multiple levels of metallization on the surface, each metallization pattern is inlaid in trenches formed in an insulating layer. The surface of the metallization is flush with or somewhat lower than the surface of its associated insulating layer. In a preferred embodiment, the different etching characteristics of glass and silicon nitride are utilized to form the trenches in the glass layer. The glass comprises the insulating layer and the nitride forms the bottom of the trench.

5 Claims, 12 Drawing Figures



PATENTED SEP 24 1974

3,838,442

SHEET 1 OF 2

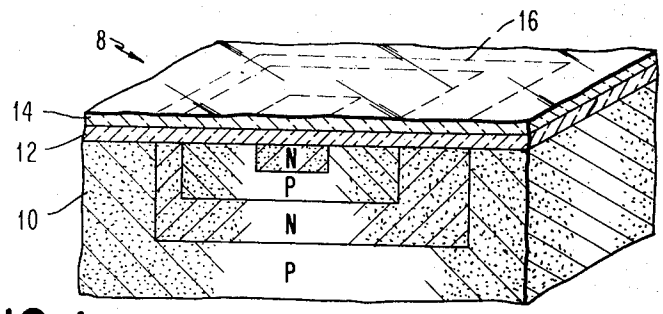


FIG. 1

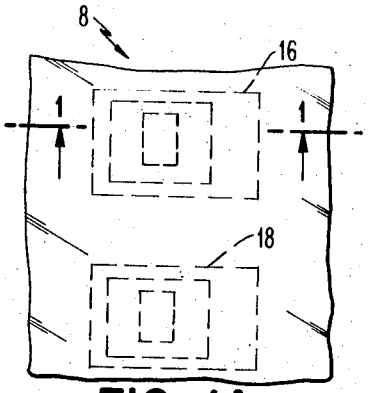


FIG. 1A

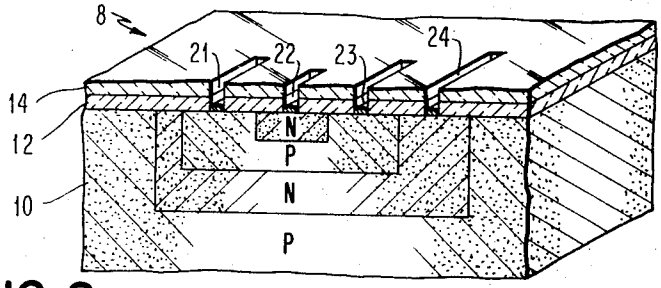


FIG. 2

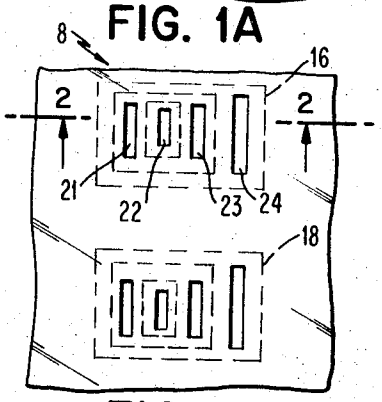


FIG. 2A

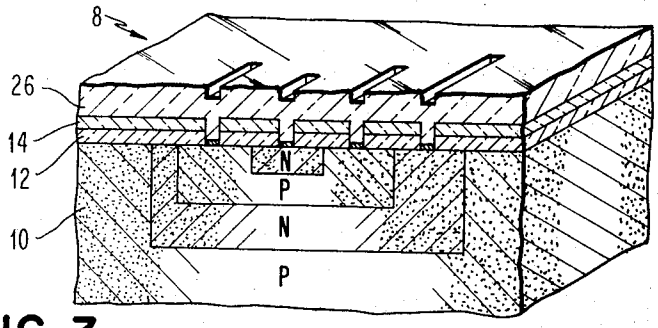


FIG. 3

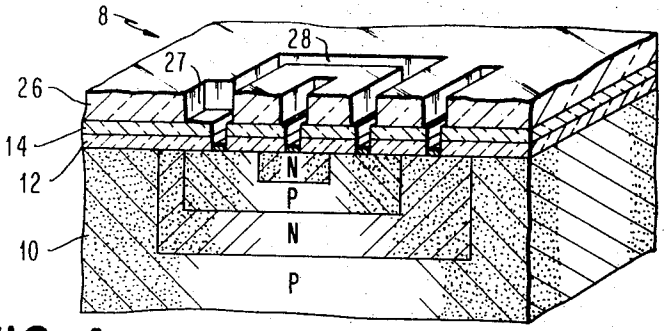


FIG. 4

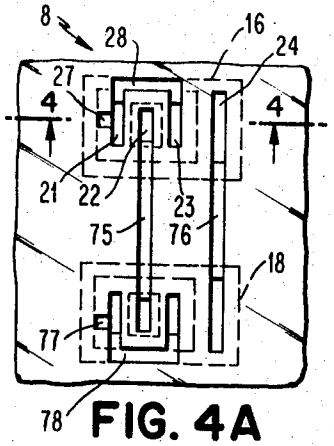


FIG. 4A

INVENTOR
CHARLES B. HUMPHREYS

BY Maurice H. Klitzman

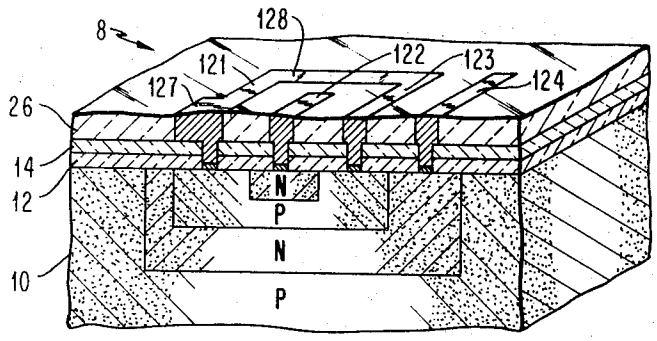


FIG. 5

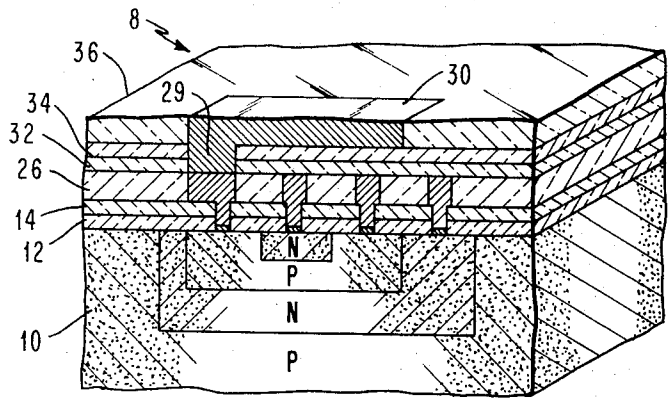


FIG. 6

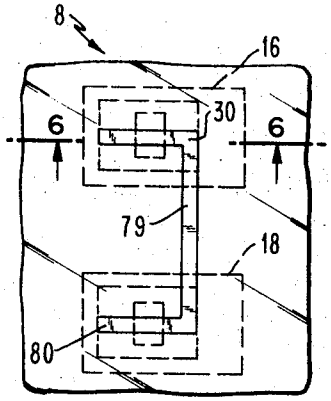


FIG. 6A

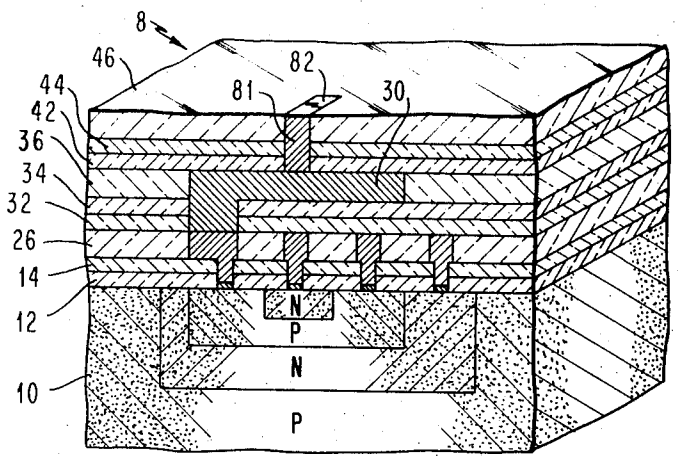


FIG. 7

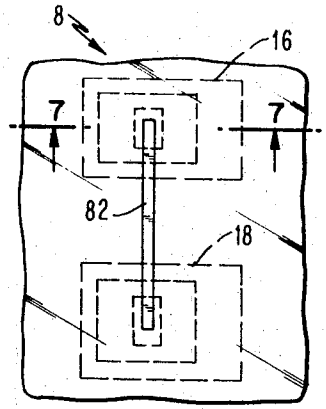


FIG. 7A

SEMICONDUCTOR STRUCTURE HAVING METALLIZATION INLAID IN INSULATING LAYERS AND METHOD FOR MAKING SAME

This is a continuation of application Ser. No. 28,891 filed Apr. 15, 1970 and now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to semiconductor structures wherein crossover connections between active devices within the structure, external leads and power buses are formed on the surface of the semiconductor body.

2. Description of the Prior Art

Recent technological advances have enabled transistor manufacturers to place more and more active and passive elements into the body of a semiconductor chip. For example, it is possible to form more than 500 such elements into a chip having an area of less than 100 by 100 mils. This has presented a serious problem in interconnecting the devices within the chip to form circuits and in providing external connections from the chip.

Several alternative techniques have been advanced, none of which have met with great success.

In one method, the connections are formed separately on multilayered ceramic substrates. With this method, many of the interconnections between individual devices as well as substantially all of the external connections to other sources are formed on the various layers of the laminated ceramic structure. However, this method has the basic flaw of consuming a large area as compared to the size of the semiconductor chip mounted thereon. In addition to the basic flaw, there is a problem of the length of the connection between the device within the chip and the connection on the ceramic. The longer the lead, other factors being equal, the longer it will take a signal to propagate. This has led to the rather anomalous result of having the transistor "package" cause a considerable portion of the total delay in signal propagation. Of course, as the art has advanced in forming a device within a smaller area of the semiconductor chip, this problem has grown steadily worse, relatively speaking.

A second technique which has received considerable publicity is the bonding of external connections at the periphery of the chip itself or on a ceramic substrate which holds the chip. These connections, in the form of wires of minute diameter, jump over the active areas of the chip, very similarly to conventional wiring. The problems with this technique are the fragility of the wires and the great difficulty in bonding the wires to small contact areas.

A third technique, to which the present invention is directed, is to produce most of the conductive connections in multiple levels on the surface of the chip itself. In circuits requiring relatively few interconnections between devices and few power connections, all of the metallization may be confined to one level. However, the art has progressed to having such increased density of devices per chip that more than one metallization level is required. In general, the prior art multilevel metallization technique has comprised:

(1) the deposition of ohmic contacts and certain device interconnections on a first level; (2) depositing one or more insulation layers atop the first metallization; (3) producing via holes within the insulation; (4) depositing a second pattern of metallization atop the insulation; (5) simultaneously connecting selectively the first level of metallization with the second level through the via holes; and reproducing steps 2, 3, 4, and 5 to form a third level. This technique, and the many variations of it which have been suggested in the prior art, has resulted in a commercially acceptable transistor structure. However, in production the ratio of acceptable finished circuits to the total number of circuits started initially, i.e., the yield, has remained lower than desired. The basic problem lies in the humps formed by the conductive lands at the locations where an insulation layer passes over or under the conductive lands which form the metallization pattern. These humps are present in all techniques which appear in patents and technical publications directed to insulating the multilevel metallization patterns printed on top of the chip. They are not evident in many drawings, probably for reasons of clarity and because they had not caused noticeable problems in the particular processes or structures involved. However, these humps have been found to be a principal cause of the formation of pinholes and stress cracks in the insulation layer and pinholes in the metallization. One reason for this lies in the discontinuity present in the otherwise smooth insulation layer where it passes over the conductive metallization pattern. The stress on the insulation layer is greatest at that location. In addition, there are locations in a non-planar insulation layer where its thickness is less than the average thickness. These locations will have more pinholes than average. These pinholes and stress cracks may cause one portion of a metallization pattern to "short" with another; or cause one portion of one level of metallization to short with another level. Pinholes and stress cracks in the insulation layer may also cause pinholes in the metallization. During an etching process on the metallization, the etchant may seep through the insulation and attack the metal at an undesired location, resulting in the pinhole. Pinholes in the metal may, in turn, cause pinholes in the insulation layer if an insulation etchant seeps through the metal. Any of these occurrences can cause a defective chip.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide an improved semiconductor structure with multilevel metallization on the surface thereof and a method for making it.

A further object is to provide an improved method for eliminating humps occurring at crossover points of insulation and metallization patterns.

Another object is to substantially eliminate pinholes and stress cracks commonly occurring in semiconductor structures having multilevel metallization.

Another object is to provide a method for accurately forming trenches in an insulating layer which allows an accurate deposition of metallization in the trenches.

The preset invention accomplishes these and other objects by providing a structure in which each level of metallization is inlaid within an associated insulating layer and bottomed on a passivating layer. In each laminated section formed by the passivating and insulating layers and the metallization, the surface of the metallization is flush with or somewhat lower than the surface of the insulating layer. However, good results are obtained if the surface of the metallization lies within the

range of 50A higher than the surface of the insulating layer and 2500A lower than the surface of the insulating layer. This range as defined is termed "substantially flush" in this application and the term will be understood to mean that range.

The preferred method is to etch a trench in the insulating layer and then deposit the metallization into the trench. The bottom of the trench comprises the upper surface of a passivating layer which is insensitive to the etchant used to etch the insulating layer. Preferrably, the insulating layer is glass and the passivating layer is a conjoint layer of silicon oxide and silicon nitride; the nitride is the upper portion of the conjoint layer.

IN THE DRAWING

FIG. 1 is a sectional perspective view of the junctions of a single active device within a passivated planar semiconductor chip.

FIG. 1A is a view of the top surface of a portion of the chip showing two active device areas.

FIG. 2–5 show various stages of producing ohmic contacts and the first metallization level of active devices in accordance with the invention.

FIGS. 6 and 7 show an active device with second and third levels of metallization, respectively, in accordance with the invention.

FIGS. 6A and 7A are views of the top surface of the chip showing the metallization patterns connecting the active devices.

All of the figures are not necessarily to scale. In some instances, the dimensions have been exaggerated for clarity and to show particular aspects of the invention.

Referring now to FIG. 1 and FIG. 1A, a semiconductor chip **8** is shown having a substrate **10** which is covered by two passivating coatings **12** and **14.** The chip is one section of perhaps **50** or **60** such chips which together form a semiconductor wafer. Within the substrate **10** are areas, generally denoted as **16** and **18,** containing surface junctions which form active devices. The bulk of substrate **10** may comprise a monocrystalline p-type silicon semiconductor body having an oriented surface and exhibiting relatively high resistivity, e.g., in the order of 10 ohm-cm.

Typically, chip **8** is around 100 by 100 mils, and, of course, contains many active areas of which areas **16** and **18** are merely illustrative. In addition, the chip may contain regions which are passive, i.e., resistive and capacitive, which may also be connected on top of the chip in accordance with the present invention.

FIG. 1 is a sectional perspective view of area **16,** taken along line 1—1 of FIG. 1A. Area **16** is totally within chip **8** except for the upper surface, which initially is completely covered by conjoint passivating coatings **12** and **14** which together form a passivating layer. For simplicity and ease of understanding, area **16** is depicted as a segment removed from chip **8.** Furthermore, it will be understood that each of the processes to be performed on area **16** is also performed, preferably simultaneously, on area **18.** Within area **16,** there is shown a planar N-P-N junction device. The fabrication of this kind of device is well known to those skilled in the art. It will be recognized that the invention is not confined to a particular type of device or process of forming the device. For instance, the device could be a P-N-P type with an N type substrate **10.** Also, germanium instead of silicon could be used as the semiconductor material. It is important only that the ohmic contacts be formed at the surface of the device, the surface being substantially planar.

Coating **12** is preferrably an oxide of silicon. Any conventional technique may be used to form the silicon oxide layer. The particular choice will depend on the nature of the semiconductor material. In the case of a silicon wafer, a silicon dioxide coating is formed preferrably as a genetic coating formed by thermal growth from the silicon body itself. One preferred technique is to heat the body to between 900° C. to 1400° C. in an oxidizing atmosphere of air saturated with water vapor or in an atmosphere of steam, thus forming a silicon dioxide coating. Alternately, an R.F. sputtering method may be used to form the silicon dioxide coating. If the semiconductor material is germanium rather than silicon, a silicon oxide coating may be formed by pyrolytic decomposition of ethyl silicate vapor. In the present embodiment, coating **12** is silicon dioxide with a depth of 600a. The thickness preferrably ranges from 2000A to 8000A. In the remainder of the specification, the term silicon oxide will be understood to also include silicon dioxide. The silicon nitride coating **14** is contiguous with silicon oxide coating **12.** The silicon nitride coating may be formed by known techniques such as R.F. sputtering, as described in co-pending application Ser. No. 494,789, filed Oct. 11, 1965, or by reactive sputtering, as described in co-pending application Ser. No. 583,175, filed Sept. 30, 1966. Both of these applications are assigned to the assignee of the present invention. A third technique which could be used to form the silicon nitride coating is the pyrolytic decomposition of a gaseous mixture of silane and ammonia which is heated to around 900° C. The preferred technique is to R.F. sputter the silicon nitride coating to a thickness of around 1000A, but preferrably below 2000A.

The ranges of thickness of silicon oxide coating **12** and silicon nitride coating **14** may vary from the preferred thickness. However, in the preferred embodiment of this invention, it is important that the total thickness of the conjoint layer be precisely controlled or measured after deposition, as the metallization layer to be applied will be substantially flush with a glass layer which will be applied in a later step. In place of the conjoint passivating layer **12**/14 of oxide and nitride, a single layer of silicon nitride might be used. However, the nitride layer alone may not insure the requisite passivation for structures with extensive metallurgy.

The precise depth of the oxide and nitride coatings may be calculated by standard techniques. For example, the thicknesses may be measured by means of a technique described in "Non-Destructive Technique for Thickness and Refractive Index Measurements of Transparent Films," W. A. Pliskin and E. E. Conrad, IBM Techincal Disclosure Bulletin, Vol. 5, No. 10, March 1963, pp. 6–8. Preferrably, this technique is augmented with a spectrophotometer as described in "Transparent Thin-Film Measurements by Visible Spectrophotometry," A. Decobert and M. Lachaud, IBM Technical Disclosure Bulletin, Vol. 10, No. 11, April 1968, p. 1799. Besides this non-destructive method of testing the thickness of transparent thin films, any well-known destructive method using a test wafer could be used. One known destructive method is the so-called angle-lap technique. One end of the test wafer is beveled at a very small angle to expose a rela-

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.