Dual Damascene Processing for Semiconductor Chip Interconnects

FIELD OF THE INVENTION

The present invention relates to lithographic methods for forming a dual relief pattern in a substrate, and the application of such methods to fabricating multilevel interconnect structures in semiconductor chips.

BACKGROUND OF THE INVENTION

Device interconnections in Very Large Scale Integrated (VLSI) or Ultra-Large Scale Integrated (ULSI) semiconductor chips are typically effected by multilevel interconnect structures containing patterns of metal wiring layers called traces. Wiring structures within a given trace or level of wiring are separated by an intralevel dielectric, while the individual wiring levels are separated from each other by layers of an interlevel dielectric. Conductive vias are formed in the interlevel dielectric to provide interlevel contacts between the wiring traces.

By means of their effects on signal propagation delays, the materials and layout of these ~~inter- connect~~interconnect structures can substantially impact chip speed, and thus chip performance. Signal propagation delays are due to RC time constants wherein R is the resistance of the on-chip wiring, and C is the effective capacitance between the signal lines and the surrounding conductors in the multilevel interconnection stack. RC time constants are reduced by lowering the specific resistance of the wiring material, and by using interlevel and intralevel dielectrics with lower dielectric constants.

A preferred metal/dielectric combination for low RC interconnect structures might be Cu metal with a carbon-based dielectric such as diamond-like-carbon (DLC) or an organic polymer. Due to difficulties in subtractively patterning copper,

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however, interconnect structures containing copper are typically fabricated by a Damascene process. In a Damascene process, metal patterns inset in a layer of dielectric are formed by the steps of

etching holes (for vias) or trenches (for wiring) into the interlevel or intralevel dielectric,

optionally lining the holes or trenches with one or more adhesion or diffusion barrier layers,

overfilling said holes and trenches with a conductive wiring material, by a process such as physical vapor deposition (for example, sputtering or evaporation), chemical vapor deposition, or plating, and

removing the metal overfill by planarizing the metal to be even with the upper surface of the dielectric.

This process is repeated until the desired number of wiring and via levels have been fabricated.

Fabrication of interconnect structures by Damascene processing can be substantially simplified by using a process variation known as Dual Damascene, in which a wiring level and its underlying via level are filled in with metal in the same deposition step. However, fabrication by this route requires transferring two patterns to one or more layers of dielectric in a single block of lithography and/or etching steps. This has previously been accomplished by using a layer of masking material that is patterned twice, the first time with a via pattern and the second time with a wiring pattern. This procedure typically comprises the steps of:

forming one or more layers of dielectric having a total thickness equal to the sum of the via level and wiring level thicknesses,

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applying a layer of a hard mask material such as SiO2 or Si3N4 having different etch characteristics than the underlying dielectric,

patterning the hard mask material with the via level pattern, typically by etching through a photoresist stencil,

transferring said via level pattern into a first upper thickness of said one or more layers of dielectric by a process such as etching,

repatterning the same layer of hard mask material with the wiring level pattern,

transferring the wiring level pattern into a second upper thickness of said one or more layers of dielectric in such a manner as to simultaneously transfer the previously etched via pattern to a bottom thickness of said one or more layers of dielectric, said second upper and bottom thicknesses closely approximating the wiring and via level thicknesses, respectively.

While this "twice patterned single mask layer" process has the virtue of simplicity, difficulties in reworking the second lithography step may occur if the interconnect dielectric and the photoresist stencil used to pattern the hard mask have similar etch characteristics. Such would be the case with an organic photoresist and a carbon-based interconnect dielectric such as DLC. A typical cause for rework ~~would~~might be a misalignment between the via-patterned hard mask/upper dielectric layers and the wiring-patterned resist layer. However, lithographic rework at this stage is a problem because the sidewalls of the via-patterned dielectric are not protected from the resist stripping steps necessary for removing a misaligned wiring-patterned resist layer.

SUMMARY OF THE INVENTION

The present invention relates to improved methods for defining and transferring two patterns (or a single dual relief pattern) to one or more layers of dielectric in a

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single block of lithography and/or etching steps. The invention comprises two preferred modifications of a prior art "twice patterned single mask layer." Dual Damascene process and two preferred embodiments of a fabrication process for a dual pattern hard mask which may be used to form dual relief cavities for Dual Damascene applications.

The first and second preferred modifications of a prior art "twice patterned single mask layer" process introduce an easy-to-integrate sidewall liner which protects organic interlevel and intralevel dielectrics from potential damage induced by photoresist stripping steps which may be needed, for example, during rework processing to correct for lithographic misalignment. In the first modification, the liner may be permanent, in which case portions of the liner can remain in the final structure. In the second modification, the liner may be disposable, in which case the liner would be removed from the finished structure. Use of these inventive modifications allows problem-free rework with minimal impact on processing.

The two preferred embodiments of a dual pattern hard mask fabrication process provide a mask wherein the lithographic alignment for both via and wiring levels is completed before any pattern transfer into the underlying interlevel/intralevel dielectric. The dual pattern hard mask might preferably comprise a bottom layer of silicon nitride with a first pattern and a top layer of SiO_2 with a second pattern. The two embodiments differ by the order in which said first and second patterns are transferred into the hard mask layers.

It is thus an object of the present invention to improve the existing "twice patterned single mask layer" Dual Damascene process by adding a protective sidewall liner which may or may not remain in the final structure.

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It is a further object of the present invention to teach the use of a Dual Damascene process in which a dual pattern hard mask containing both via and wiring level patterns is fabricated on a substrate comprising at least one layer of an interlevel/intralevel dielectric, prior to any pattern transfer into the interlevel/intralevel dielectric.

It is a further object of the present invention to provide a general method for forming a dual pattern hard mask, said dual pattern hard mask comprising a first set of one or more layers with a first pattern, and a

second set of one or more layers with a second pattern.

It is a further object of the present invention to teach a method for transferring said first and second patterns of said dual pattern hard mask to an underlying substrate to form a dual relief patterned structure.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, objects, and advantages of the present invention will become apparent upon a consideration of the following detailed description of the invention when read in conjunction with the drawings, in which:

FIGS. 1A-1L show in cross section view the prior art "twice patterned single mask layer" Dual Damascene process flow for forming a wiring layer and its associated underlying via layer;

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