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HANDBOOK OF VLSI MICROLITHOGRAPHY

GLENDINNING
HELBERT

HANDBOOK OF VLSI MICROLITHOGRAPHY

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Principles, Technology and Applications

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PREFACE

The chapter topics of this lithography handbook deal with the critical and enabling aspects of the intriguing task of printing very high resolution and high density integrated circuit (IC) patterns into thin resist process pattern transfer coatings. Circuit pattern density or resolution drives Dynamic Random Access Memory (DRAM) technology, which is the principal circuit density driver for the entire Very Large Scale Integrated Circuit (VLSI) industry. The book's main theme is concerned with the special printing processes created by workers striving to achieve volume high density IC chip production, with the long range goal being pattern features sizes near 0.25 μm or 256 Mbit DRAM lithography. The text is meant for a full spectrum of reader types spanning university, industrial, and government research and development scientists and production-minded engineers, technicians, and students. Specifically, we have attempted to consider the needs of the lithography-oriented student and practicing industrial engineers and technicians in developing this handbook.

The leadoff chapter focusses on the view that lithography methods (printing patterns) are pursued for the singular purpose of manufacturing IC chips in the highly competitive commercial sector, and attempts to delineate the factors determining lithographic tool selection. The reader's perspective is drawn to consider IC device electrical performance criteria versus plausible and alternative energetic, or circuit density limited, particle printing methods--visible or shorter UV optical, electron, X-ray, and ion beams. The criteria for high quality micrometer and submicrometer lithography is very simply defined by the three major patterning parameters: line/space resolution, line edge and pattern feature dimension control, which when combined with pattern to pattern alignment capability determine lithographic overlay accuracy. Patterning yield and throughput further enter in as dependent economic factors.

Resist technology has a logical, prominent, second-chapter position indicative of resist's overall importance in lithography, i.e., the end product of any IC lithography process is the patterned resist masking layer needed to delineate the VLSI circuit level. Example coverage of optical resist process optimization assures the reader a grasp of the most commonly and widely used (world-

wide) lithographic process technologies. The basic resist design concepts and definitions are thoroughly covered as well as advanced lithographic processes.

Basic metrology considerations (Chapter 3) are absolutely imperative to rendering a total description of lithography methodology. The task of precisely measuring printed linewidth, or, space artifacts at submicron dimensions must be performed at present without the use of a traceable reference source--National Institute of Standards and Technology. These desirable and necessary standards must be made available in the future. However, critical and sufficient physical modelling of varied resist and IC material topological structures requires funding support and completion. Nevertheless, elucidation of optical, scanning-electron-microscope (SEM), and electrical test device linewidth measurements data present the reader with key boundary conditions essential for obtaining meaningful linewidth characterization.

The portrayal of energetic particle microlithography is totally incomplete without some detail of the actual printing tool concepts, design, construction, and performance. The printing tools are presented and described in chapters 4-7 as to their usage in the IC manufacturing world. Clearly optical lithography has been the backbone and mainstay of the world's microchip production activity and will most likely continue in this dominant role until about 1997. In the optical arena, it is found that 1X, 5X, and 10X reduction printers of the projection scanned and unscanned variety must be described in subsets according to coherent and non-coherent radiation, as well as, by wavelengths ranging from visible to deep ultraviolet. Higher resolution or more energetic sourced tools are also well described.

Next in world manufacturing usage, electron beam (e-beam) pattern printing has been vital, mostly because of its application in a pattern generation capacity for making photo masks and reticles, but also because of direct-write on-wafer device prototyping usage. The writing strategy divides e-beam printers, in general, into two groups: Gaussian beam raster scan, principally for pattern generation, and fixed or variable-shaped beam vector scan for direct-write-on-wafer applications. Subsets of the latter groups depend upon site-by-site versus write-on-the-fly substrate movements. The sophistication and complexity of e-beam printers requires diverse expertise in many technical areas such as: electrostatic and electromagnetic beam deflection, high speed beam blanking, intense electron sources, precise beam shapers, and ultra fast data flow electronics and storage. Interestingly, important special beam relationships

of maximum current, density, and writing pattern path-speed require the observance of unique boundary conditions in meeting printing criteria.

On a worldwide basis, X-ray printing does not yet have high volume IC device production background examples, but high density prototype CMOS devices have been fabricated by IBM and feasibility demonstrated. The X-ray chapter presents X-ray lithography as a system approach with source, mask, aligner, and resist components. Of the competing volume manufacturing printing methods (optical and X-ray), the X-ray process is unique as a proximity and 1:1 method. As such, in order to meet the IC patterning quality criteria, extreme demands are placed on the mask fabrication process, much more so than for masks or reticles produced for the optical analogue. For economically acceptable IC production, laser/diode plasma and synchrotron ring X-ray sources must be presented as high density photon emitters. In the second part of Chapter 6, synchrotron is given special attention and presented as a unique X-ray generator with an X-ray flux collimation feature. In spite of the synchrotron's massive size and very large cost, it's multiport throughput capacity makes it viable for the very high production needs of certain industrial IC houses or possibly for multi-company or shared-company situations.

In the last of the printing tool chapters, Chapter 7, the energetic ion is depicted in a controllable, steerable, particle beam serial pattern writer performing lithography at a high mass ratio compared to an e-beam writer. The focussed ion beam not only can deposit energy to form IC pattern latent resist images, but offers as another application the direct implant of impurity ions into semiconductor wafers, obviating completely the need for any resist whatsoever and greatly simplifying the IC chip processing sequence. The versatile energetic ion plays yet another and possibly its most significant role in a "steered-beam" tool, indispensable for optical and X-ray mask repair through the precise localized oblation and/or deposition of mask absorber material.

The goal of establishing 0.35 μm IC chip production by 1995 is plagued by the constraints of yield-defect models. A small fractional-submicron mask defect population is adversely catastrophic to the mask-and-reticle-dependent energetic lithographies (optical, X-ray), and especially so for the case of 1:1 parallel reduction printing. The modernization of photo mask and reticle fabrication methods and facilities paves the way for achieving extremely accurate and defect free optical masks and

reticles ($<0.1/cm^2$). With defects of fractional-submicron sizes, mask and reticle repairs require fully automated "steered-beam" inspection/mapping equipment to work under full computer automation with compatible focussed ion beam repair tools.

One of the editors' purposes in assembling this book has been to accurately disseminate the results of many and varied microlithography workers. Since it is not possible in any one book to satisfy enough detail for every reader's full curiosity, we consider at least that the reader is enabled to perform his own valid analysis and make some meaningful conclusions regarding the status and trends of the vital technical thrust areas of submicron IC pattern printing technology. The editors wish to extend appreciation to various colleagues for helpful discussions and encouragement: A. Oberai, J.P. Reekstin, M. Peckerar, and many others as the lengthy lists of chapter references attest.

In addition, many individuals representing industrial, government, and university sectors have been extremely helpful in providing technical discussions, data, and figures to the chapter authors of this book. Gratitude is further extended here to those persons and their organizations. Gratitude also has been expressed via courtesy annotations in the figure captions. Finally, we commend and thank Judy Walsh for her compilation and editing skills.

Nobleboro, Maine — William B. Glendinning
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CONTENTS

2

RESIST TECHNOLOGY - DESIGN, PROCESSING AND APPLICATIONS

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CHAPTER PREFACE

The objective of this chapter is to provide a user's view of resist technology. Other notable authors have previously provided insightful views of resist technology(1-4), but from a research or resist inventor's point of view. My intent, here, is to supplement these excellent works, not to reproduce them in another source. Some material must be rehashed for completeness, but hopefully from another complementary perspective. The emphasis of this chapter will be placed on applications of this technology to the manufacturing of prototype and production integrated circuit devices. Furthermore, a greater emphasis will be placed upon empirical resist process development to achieve reproducible and statistically controlled resist manufacturing processes.

1.0 INTRODUCTION

Organic resist technology is vital to integrated circuit(5), or more generally semiconductor device, manufacturing. Nearly every device fabrication step requires a process compatible masking layer, which is capable of providing a desired circuit level pattern. This indirect patterning is required because either the layer is not directly patternable technologically or it cannot be accomplished economically. Resist layers, as their name implies, "resist" individual layer processing steps to enable electronic devices to be fabricated vertically layer by layer on a thin silicon crystal wafer (see Figure 1)(5). These individual layers can be insulating dielectrics, semiconducting active device elements, or metallic interconnects.

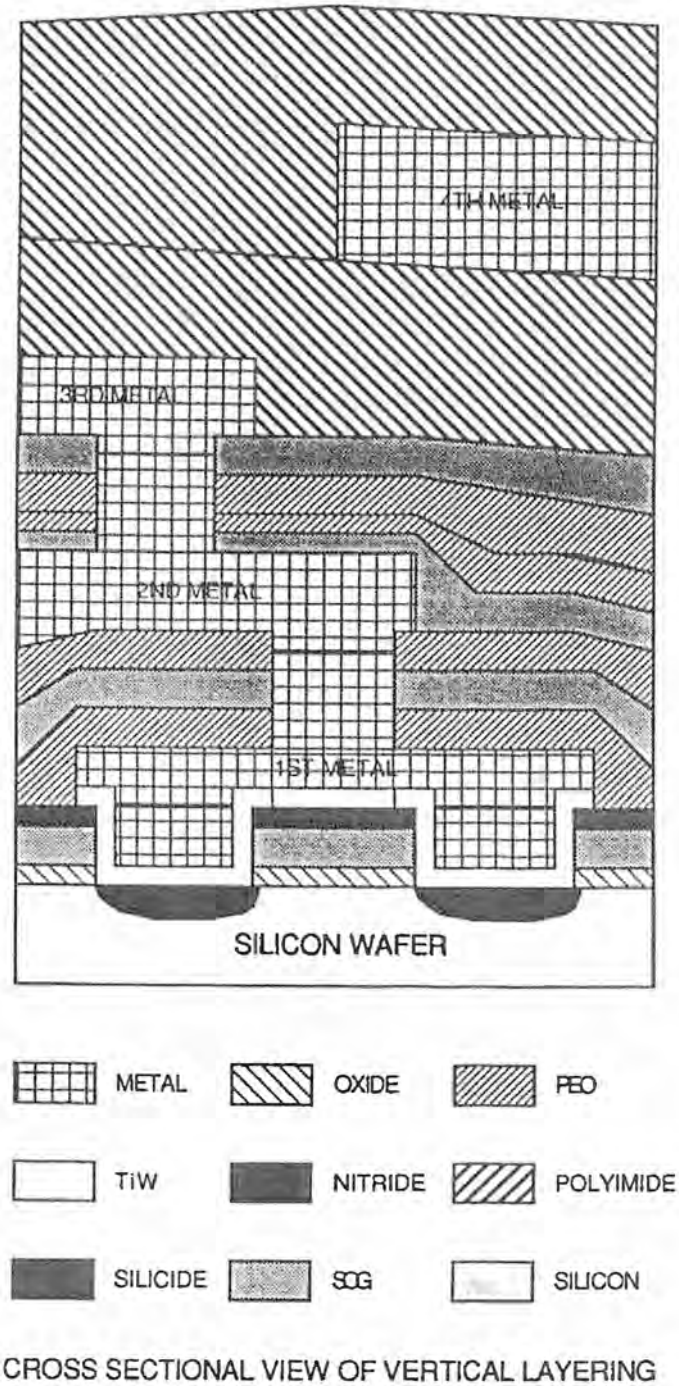


Figure 1. Cross sectional view of vertical layering in the manufacturing of silicon VLSI circuits.

In addition to providing device manufacturability from a circuit element delineation view(5), the resist process is capable of influencing device performance. The resist lithographic resolution and critical dimension (CD) control, for example, can directly influence device turn- on threshhold, speed and/or circuit density. Historically, the resist CD requirements have reduced approximately 20-30% every two years(3), thus pushing some older lithographic tools to their limits and making them obsolete. The dramatic time evolution of memory chip storage capability presents an adequate testimonial. Dynamic random access memory element counts have gone from 1-256 kilobits in about six years, and four megabit chips are being sampled at the time of this book preparation.

The lithographic capability of the resist is determined to a large degree by the wavelength of the electromagnetic energy source used to carry out the selective patterning process. Typically, visible light is used of wavelengths ranging from 300-420 nm. The light is imaged on the wafer through chromium metal patterned transparent glass masks using either reflective or refractive optics(3). Electromagnetic energy sources of wavelengths <310 nm can be provided by deep UV (DUV) producing systems such as high pressure mercury arc lamps or laser systems(4). Further reductions in wavelength are achieved by employing focused electron beam sources, like those found in scanning electron microscopy(i.e., 10-30 keV), or those found in soft X-ray systems (2-20 Å wavelength). Most importantly, the wavelength in most cases determines what type of resist can be employed, because the energy of the lithographic tool must be coupled to the resist to insure a conversion of electromagnetic energy to radiation chemical energy occurs. In the next section, the design of resist materials for specific radiation sources will be described. Furthermore, resist systems or processes will be described which actually extend the useful resolution or lifetime of certain lithographic aligners.

Although the lithographic properties of resists can determine circuit density and performance, the resist must first of all be device layer process compatible, or it is of academic importance only. Unfortunately, the literature abounds with resist systems of great lithographic capability, but they cannot be employed in the commercial fabrication of semiconductor devices because they are not capable of withstanding or "resisting" certain required processes. The most widely studied e-beam resist, namely poly(methyl methacrylate) (PMMA), falls into this category due to an inferior dry etch(6) capability. In the process and process applications sections of this chapter, process

compatible processes will be highlighted. In this sense, the perspective is a practical user's view as opposed to a resist inventor's view, where typically little actual device fabrication experience exists and the process and manufacturing issues are not as well realized.

2.0 RESIST DESIGN

2.1 Conventional Photoresists

2.1.1 Positive Resists. These resist materials(1-4) are the workhorses of modern integrated circuit (IC) manufacturing technology. All new very large scale IC (VLSIC) fabrication lines employ high resolution positive toned material, while the older lines with more mature products still rely heavily on negative toned resists. Positive toned resists develop away to create recessed relief images in the exposed areas (see Figure 2) with safely-disposing dilute aqueous base solutions. When employed, they can be used at all device levels by simply changing the density of the Cr patterned mask or reticle by the mask shop, but the pattern information is usually digitized positive by the design group regardless of final density.

Positive photoresists are composed or formulated from several components: polymeric resins of molecular weight of the order of 1-10K, photoactive molecular organic additives (PAC), leveling agents (SLA), optional dyes to reduce substrate reflectivity effects, sensitizers and organic spinning solvents. The resin molecular weights are intentionally chosen to be low to insure solubility in the polar basic developers. The photoactive species also acts as a dissolution inhibitor, that is, it prevents development in the unirradiated regions of the film needed to resist (i.e., mask) further processes. The leveling agents prevent undulations on the resist surface by presumably plasticizing the resin or by providing a resist solution with lower surface tension to improve wetting at wafer spin.

2.1.2 PAC Influence. Photoactive compounds, or sensitizers, are usually naphthoquinone diazides (i.e., PACs) like those pictured in Figure 3(7)(8). The diazide (DAQ) moiety of this molecule absorbs in the visible region of the spectrum, but most importantly, it undergoes a photochemically-induced radiation chemical reaction, the photoelimination of the azo nitrogen, that results in a solubility change in the dissolution inhibitor photoproduct (Ref. 1-4 and references therein). It is this energy

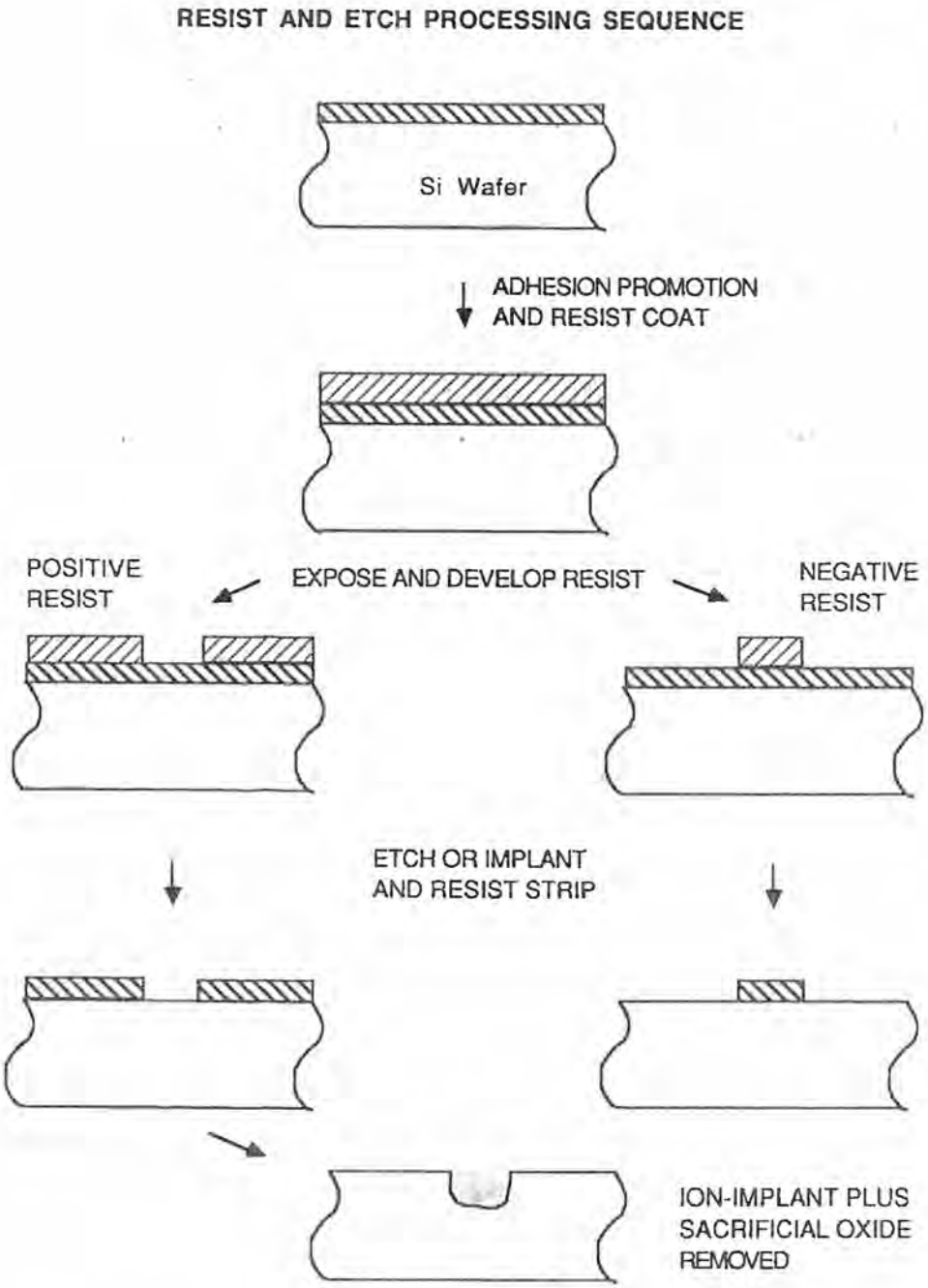


Figure 2. Resist and etching processing sequence relevant to the fabrication of VLSI circuits.

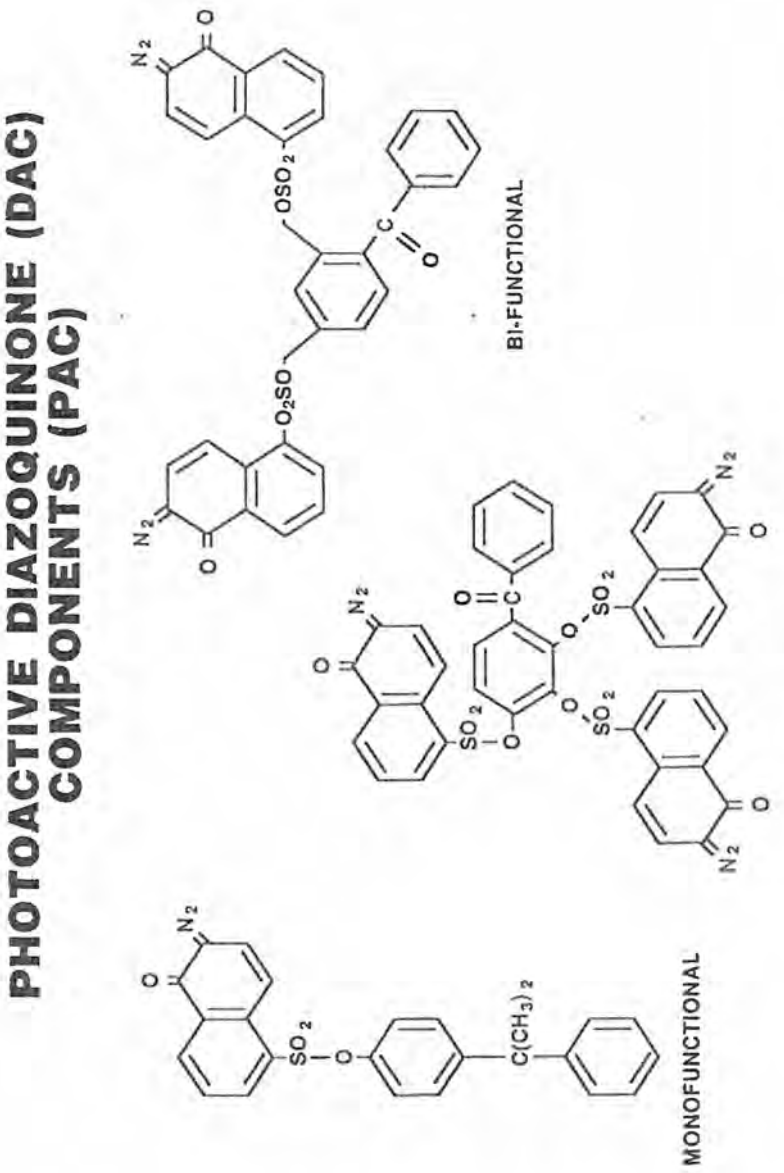


Figure 3. Structural formulae for photoactive diazoquinone (DAC) components of positive photoresist.

conversion process from electromagnetic energy to chemical reaction product which results in the observed resist behavior.

It turns out that this conversion process is fairly efficient as determined by basic quantum efficiency measurements for some PAC's. This quantity, defined as the ratio of the number of molecules reacting to photoproduct to the number of photons absorbed, Ø, can be as large as 10^6. Values larger than 1 are usually associated with a free radical chain reaction mechanism, while most photoresist photochemical reactions have values ranging from a few hundredths to a few tenths. The quantum efficiency for acetone, a model carbonyl-containing compound (i.e., C=O containing PAC) like those of Figure 3, was measured to be 0.17(9). The quantum efficiencies for the PAC's of Figure 3 were determined to all be about 0.3 at the typical optical exposure wavelengths(8). Actually, these values are quite high when compared to other energy conversion processes, thus, these photoprocesses are very energy efficient, roughly 30%. Even greater efficiency , 50%, has been observed for some resists by other researchers(10).

In the acetone example above, the light is being absorbed by the specific carbonyl chromophore group, which in turn leads to the chemical reaction. The first law of photochemistry, "only the light absorbed by the molecule (e.g., the PAC) can result in a chemical change in the molecule"(11), applies for this example and for PAC absorption in photolithography. The light, which is merely absorbed in the resin or the substrate and not at the specific chromophore, does not provide contributions to Ø. In other words, only the bleachable absorption of the resist over the exposure spectrum is important in the lithography (see Figure 4). Further, the sum of the quantum efficiencies must be 1, the second law of photochemistry(11), unless a chain reaction is involved. This definition stipulates the absorption of energy is a one-quantum process.

Absorption of light in the resist is given by the Beer-Lambert law: $I/I_0=10^{-Ecl}$, where E is the molar extinction coefficient, c the chromophore concentration, and l the resist film thickness. Arden et al.(12) have shown high E can lead to poor resist image edge walls and larger CD variation, and should be judiciously chosen in designing the positive photoresist.

It is pretty clear the photochemical quantities of interest to photoresist design are Ø and E. Both quantities can be measured empirically, as outlined in ref. 11. Resist sensitivity is influenced by phi, but E is merely a measure of the film absorption, and may not reflect absorption which leads to useful

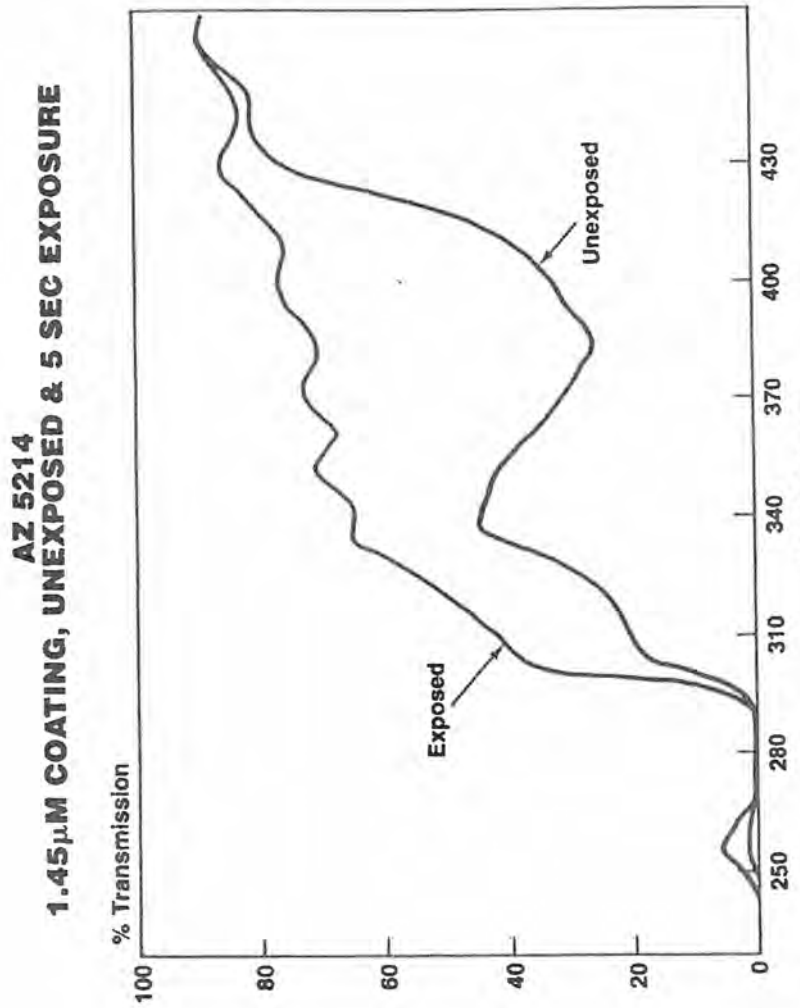


Figure 4. Bleaching curves for AZ 5214 mid -UV resists. (Courtesy of AZ Photoresists).

radiation chemical change in the resist as a result of a photochemical reaction. For example, conventional photoresists have large E at wavelengths less than 300 nm, but are very poor resists at those wavelengths due to the high absorption of the novolac resin alone, regardless of the phi value of the PAC involved. Obviously, E must not approach 1 or the system is useless at those wavelengths, but must have some value intermediate (i.e., 0.3-0.5) so the "skin absorption effect" can be avoided. This ensures the resist image will be cleared to the substrate, and that the resist image edge wall will not be severely degraded (i.e., undercut) from normal due to the high resist absorptivity(4)(12).

The composition of the PAC can influence both the spectral response and the contrast or resolution of the resist. This is important because mask/reticle aligners operate at different wavelengths, therefore, the PAC must be designed for the wavelength characteristic of that particular aligner tool. Willson and coworkers (ref. 4 and references therein) have written key papers in the area of PAC design and have demonstrated successful PAC wavelength tuning through chemical synthesis. By adding chemical substituents to the PAC molecules at specific molecular bonding sites and by blending PAC's, they were successful at formulating a resist designed to be used with a Perkin-Elmer Micralign 500 lithographic exposure system operating at the mid UV (UV-3; 310 nm) region of the Hg lamp emission spectrum. It had bleachable absorption at the mid UV region, which was an indication the radiation chemical reaction of the diazonaphthoquinone molecule to the acid soluble product was occurring as required for image formation (see Figure 5).

Daniels and coworkers(13) have also shown the importance of PolyDAQ substitution (see Figure 3) of the PAC upon resist contrast or effective aerial image of the total resist system. In Figure 6, the theoretical polyphotolysis photoproduct modulation transfer function is compared to that provided by the phototool. The resist can be designed to provide image resolution better than the resolution limited tool performance, a result which is becoming more prevalent, that is, photolithography has gone from aligner limited with low contrast resists to resist performance or contrast limited. Furthermore, higher contrast resists and special resist processes are being developed to extend tool lifetimes in some cases.

Successful or high contrast positive resist design requires a non-linear response between exposed and unexposed resist. For any degree of polyphotolysis, q, the general dissolution rate is given by:

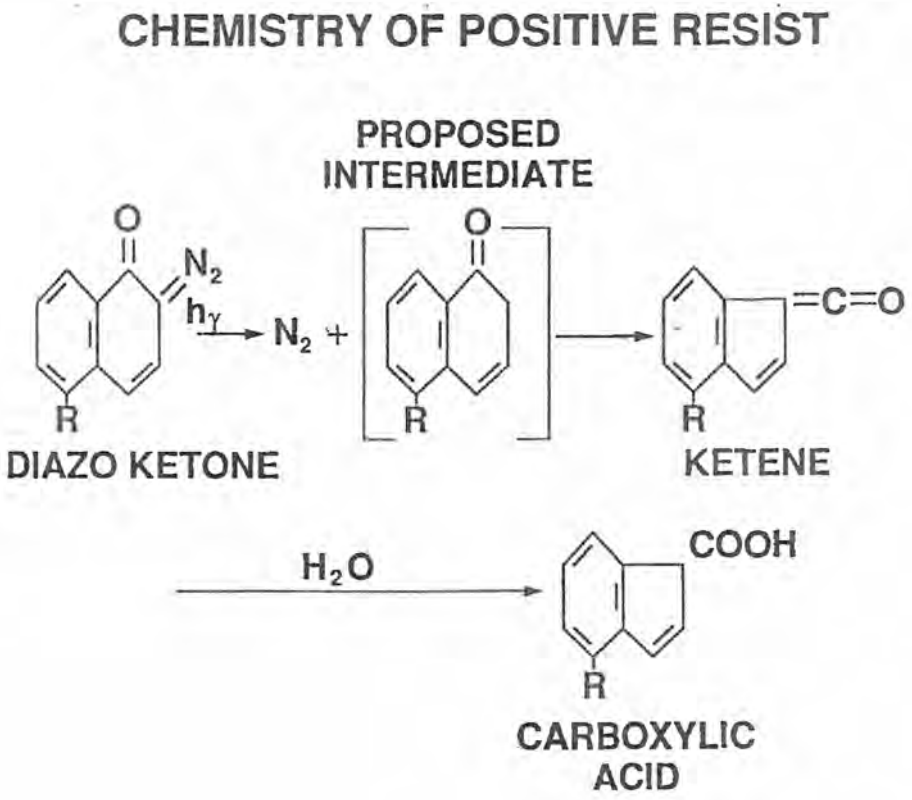


Figure 5. Chemical reactions of positive photoresists photoactive component during the UV exposure of positive photoresists.

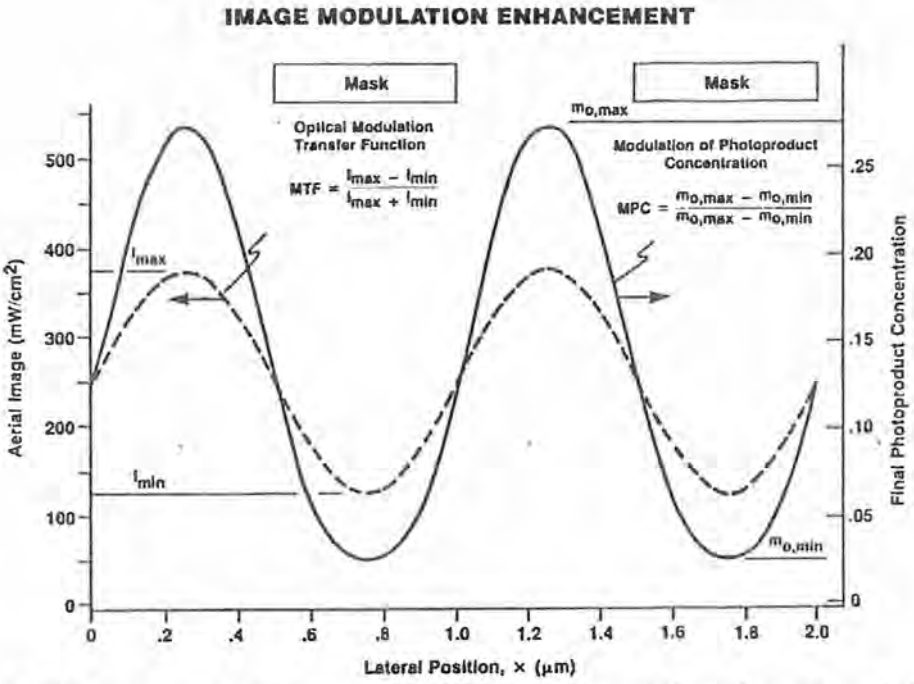


Figure 6. Image modulation enhancement function or aerial image vs. lateral position for positive photoresist exposure. (Courtesy of Shipley Co. and SPIE ref. 13).

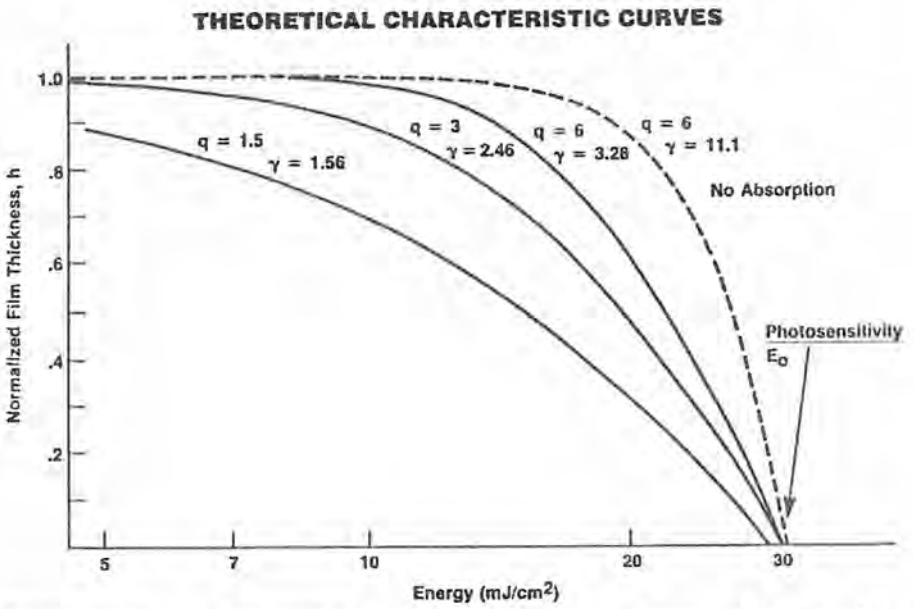


Figure 7. Theoretical characteristic curves for positive photoresist assuming a polyphotolysis mechanism. (Courtesy of Shipley Co. and SPIE ref. 13).

$$R = r_o(1- e^{-Ec})^q \quad [1]$$

where, r_o is the fully photolyzed dissolution rate. The potential influence of polyphotolysis upon resist contrast is demonstrated in Figure 7, where it is seen that as q increases the resist contrast increases. Of course, these theoretical limits are rarely obtained due to the complexity of the total system, but over the last three years significant gains in resist contrast have been achieved by several commercial positive resist manufacturers (e.g., Shipley [Aspect] Systems 8 and 9, MacDermid 1024, AZ 5214, and others).

The preceding two paragraphs point out that the resist and alignment tool make up a total lithographic system; both can influence the final result, but since the tool aerial image(14), or the light contrast across the mask edge, is fixed at the wafer plane by the manufacturer, the process engineer is left with only the resist process optimization as a primary variable of influence.

2.1.3 Influence of Resin Composition. The novolac resin composition of the positive photoresist formulation has been shown to influence resist contrast performance by Hanabata et al.(15) Templeton et al.(16) and Pampalone(17). This task is accomplished through resin conformational effects upon the dissolution rates at image development created by isomeric compositional effects which occur at resin synthesis. Not just the unexposed development rate is important, but the compositional effect of the resin upon the exposed to unexposed rates in the photoresist.

Novolac resins are polymers synthesized via a condensation reaction between substituted phenols, o,m, and p-cresols, and formaldehyde (see Figure 8)(15). Due to the poor reproducibility of feedstock and resin compositions, the normally high polydispersity novolac resins are usually custom blended to achieve a better confidence level in the final formulated product for improved lot-to-lot photoresist performance reproducibility(17). Their dissolution rates in aqueous base developers are determined primarily by isomer composition, methlyene bond position in the resin, and/or molecular weight; for example, high molecular weight fractions are synthesized most easily from m-cresols(18), and these resins would have lower dissolution rates. High resin molecular weights (i.e., ≥9000) lead to development resistance, an attractive property in the unexposed area of resist, but also may lead to film residues under conditions of low humidity(18) and reduced contrast(17). Low molecular

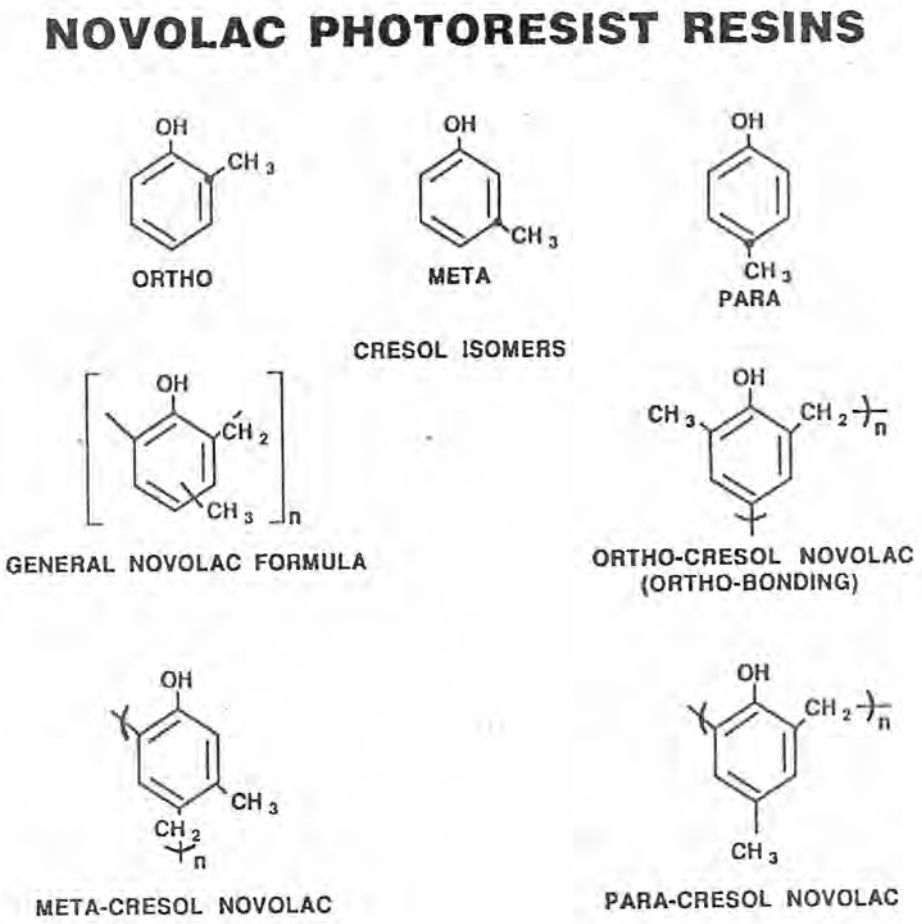


Figure 8. Novolac photoresist resin structural formulae for representative novolac resins found in conventional photoresist materials.

weight resins, such as those for pure para-cresol resins, similarly lead to poor photoresist formulations due to increased development rates, therefore, resin molecular weight and dispersity must be optimized in positive photoresist design.

Hanabata et al.(15) finds the dissolution rate of "high ortho-bonding" (i.e., ortho to ortho' methylene bonding; see Figure 8) unexposed resist to be strongly inhibited; this contrast enhancing property is hypothesized by Hanabata to result from a azo coupling interaction between this type of resin and the diazide dissolution inhibitor, and ultimately results in higher resist contrast without sacrificing resist speed. Similarly, Templeton et al.(16) found novolac resin solubility rates to be highly methylene bonding position (i.e., structurally) dependent, but they emphasize the intra- and intermolecular hydrogen bonding effects upon isomeric composition to be performance dominating. Regardless of mechanism, however, resin structural composition, molecular weight and molecular weight distribution can be performance limiting and their influence upon dissolution rates (i.e., exposed vs. unexposed) taken into account for successful resist design.

2.1.4 Positive Photoresist Summary. All of the positive photoresist design effects discussed above have one thing in common. They all lead to non-linear dissolution characteristics, which creates high contrast resist imagery. Furthermore, these effects also lead to improved latitude in dimensional control(19), a desirable resist characteristic in semiconductor device manufacturing.

2.1.5 Negative Toned Photoresist. Negative photoresist, the mainstay of semiconductor manufacturing production from the 60's to late 70's, is also basically a two component resist formulation like conventional positive systems. The resist mechanism, however, is quite different. Here, the photoactive species is a difunctional photocrosslinking azide, abbreviated as N_3-X-N_3, where X is a conjugated aromatic moiety. The bisazide efficiently absorbs visible light to form a very reactive nitrene, -N:, which is capable of chemically inserting into any C-H or C=C bond of the partially cyclized rubber resin to form an intermolecular crosslink between resin molecules. This crosslinking reaction creates a large increase (i.e., 2X) in the cyclized rubber binder polymer molecular weight every time two azide crosslinks occur, thus, decreasing the solubility rate of the optically exposed image substantially. The image is negative toned where the light strikes and remains following development, because of increased molecular weight due

to the photocrosslinking reaction vs. the unexposed area which is completely developed away (see Figure 2).

Negative resists are designed by controlling the degree of partial cyclization of the resin and by extending the conjugation of the bis-arylazide sensitizer(3). Control of the resin cyclization reaction is thought to influence the resin molecular weight distribution which in turn influences resist contrast, while the degree of conjugation of the azide-chalcone chromophore determines the spectral wavelength absorption chacteristics of the crosslinking azide sensitizer. These photoresist formulations are generally very sensitive, because the bisarylazides have high quantum efficiency, where Ø~0.4 to 0.7 and is a biphotonic average (i.e., $Ø_1+Ø_2/2$)(20).

Unfortunately, negative resists do not withstand advanced dry etch processing (e.g., Applied Materials' reactive ion etchers) very well (see Figure 9), therefore, negative photoresists remain in use only in older production lines, where large design rules (i.e., large image sizes) are called for and wet isotropic etching is still acceptable from a process image dimension bias view. Negative photoresists suffer from low contrast generally (i.e., usually have contrast values ≤1.0), created at least partially by resist swelling effects which occur during development. The highest contrast negative photoresist tested at Motorola is Merck Selectilux with a contrast value of 1.7(21). Negative resists also suffer from oxygen sensitivity or reciprocity failure, which is manifested by a thinner resist image than expected due to a competing nitrene/oxygen reaction instead of the desired nitrene/resin reaction.

2.2 Deep UV Resists

Deep UV (DUV) resists, materials responsive to light with 100-248 nm wavelength, will be needed now. Lithographic alignment tools are being designed with excimer laser light sources, and beta-site machines are currently being delivered. Current photoresists are largely ineffective at these wavelengths due to the strong absorbance of the novolac resins and PAC's involved. Work on new resists has ocurred mainly in Japan(22), at AT&T Bell Labs(23) and IBM(24), but serious reservations about the device fabrication process compatibility of these new DUV model systems exists. Work with conventional positive resists has focused upon minimization of absorption through isomer resin synthesis(25). Recently, IBM workers have reported negative DUV Si-containing systems with very good properties, but

Figure 9. Illustration of poor etch compatibility (reticulation or frying) of negative photoresist under AME etch conditions.

unfortunately, they require bi-layer RIE development and concerns of resist removal following etch processing remain. No commercial system has emerged to meet the projected device fabrication needs yet, but design activity for these materials at resist vendor labs is on the rise.

2.3 Radiation Resists

2.3.1 Introduction. The term radiation resist refers generically to materials that function under exposure to ionizing radiation, that is, radiation with short wavelegths such as soft X-rays, electron beams, and ion beams. Since only the relative sensitivities are changed when the radiation source is changed and not the resist process, the text in this entire chapter will be restricted to e-beam resists only. The basic resist mechanisms are unaffected by ionizing radiation source change even though the energy absorption mechanisms may change significantly. The main demand for these resists is in the area of e-beam fabrication of Cr- patterned glass or quartz photomasks and reticles(26).

For these resists, the energy is absorbed much differently than for photoresists. Here, enough energy is available to cleave any bond in the resist and initiate any possible reaction, where for photoresists only absorption at specific chromophoric sites in the resist can result in chemical reactivity. Even though the energy absorption is more uniform with depth for radiation resists and seemingly nonspecific, the radiation chemistry results are surprisingly very specific, hence, design criteria exist and will be reviewed.

2.3.2 Energy Absorption Considerations. Resist atomic composition can infuence both resolution and energy absorption. For electrons with 10-30 keV energies typical to e-beam lithography, the energy loss per unit path length is linear with resist density, the quantity Z/A (where Z and A are the average atomic and mass numbers for the resist) and the term ln E(27). The energy absorbed depends primarily upon the energy of the beam, but resist compositional effects are best for resists with the greatest H content, where Z/A is greatest. Since Z/A approaches 0.5 rapidly for elements with Z>5, resists with high atomic numbered compositions actually may have reduced energy transfer per unit length penetrated vertically by up to ~ 30%. More importantly, lateral scattering and backscattering effects, effects which ultimately limit resolution in e-beam lithography, increase dramatically for higher atomic numbered substituents and hence they should be avoided by resist designers(28)(29).

2.3.3 Positive resists. Positive resists have historically been designed as single component polymer type systems. The most classic examples are poly(methyl methacrylate) and poly(butene sulfone), PMMA and PBS, respectively. Their radiation chemistry was well known previous to their application as resists. Both were known to degrade, that is, produce large quantities of gaseous radiation byproducts, CO and CO_2 and SO_2, as well as exhibit reduced molecular weights under gamma-ray and e-beam exposure. In fact, both do function as positive e-beam resists(30) and(31), and the latter material is the major positive e-beam resist in use today, mostly in mask shop applications. In both resists, the design principle is the incorporation of groups that are thermodynamically favored to be split out of the molecule when irradiated; for PBS that group is in the main polymer chain while for PMMA it is in the ester side chain of the molecule. Later positive resist molecular designs involved derivatives of PMMA, namely substituted acrylates and methacrylates. These systems are represented by the general vinyl polymer structural formula:

[2] $$-[CH_2\text{-}CX(CO_2Y)]-$$

where, X could be CH_3 as in PMMA or any electron-withdrawing group such as a halogen or CN group, and Y could be any alkyl or halogenated alkyl group.

When polymers with this general structural formula are employed, their G_S values, polymer main chain bond scission yields/100 eV exposure dose, for degradation are large and their G_X values, intermolecular bonds formed (i.e., crosslinking) between polymer molecules/100 eV dose, are nearly zero in many cases(32)(33). This term, G_S, is analogous to Ø for photoresists. It determines to first order the sensitivity of the resist and is approximately inversely proportional to the e-beam sensitivity(28). Actually, the most important parameter for determining resist tone is G_S/G_X. When G_S/G_X is ≥4, the resist will predominantly degrade and hence be a positive resist.

The ultimate in substituted acrylates was designed/synthesized, and is currently being manufactured, by Toray in Japan as EBR-9, where X is Cl and Y is CH_2CF_3. This resist rivals PBS as a sensitive positive e-beam resist for mask making purposes, because both the X and Y substituents increase the radiation susceptibility of the resist(28).

The methacrylate polymer resist materials are characterized by fair to good sensitivity, and poor to good contrast

or resolution. Unfortunately, all of these resists suffer from poor dry etch compatibility and their use in lithography is restricted to mask-making only (see Table I). This market is, however, reasonably large since most masks require a master reduction reticle for stepper repeater fabrication or are MEBES master plates themselves .

Direct-write e-beam positive resists, resists used to fabricate devices directly on silicon wafers, must be heartier or more dry process compatible(6) than the mask making resists above. As such, they have been restricted to two basic resist types: conventional positive photoresists and novolac/sulfone copolymer blends. Table II contains a representative list of these systems and their resist characteristics. Generally, these resists are less sensitive but are dry process compatible, and semiconductor devices can actually be made directly with them on silicon wafers.

Fahrenholz et al. of AT&T(34) and Hunt Chemical researchers(35) have been actively involved in designing novolac-based positive e-beam resists for direct-write circuit fabrication. The AT&T activity has focused upon two component polymer blend systems where the dissolution inhibitor is a poly (alkene sulfone) like PBS(36) and the novolac binder resin is designed to actually degrade with the inhibitor and have minimal concomitant crosslinking(34). The idea here is to minimize the competing crosslinking reaction from the resin which tends to counteract the positive action occurring in the degrading sulfone. Novolacs with bulky sustituents on the phenyl ring, n-propyl, sec-butyl, and phenyl, all produce positive acting novolac resins without any dissolution inhibitor at all. Although images of these uninhibited resins do not clear to the substrate without extensive resist loss in the unexposed areas, they provide a substantial advantage over more conventional resins that crosslink extensively over the entire dose range, which tends to conteract the positive behavior in the two component resist. Other conditions which promote positive behavior are post exposure pre-develop exposure to air (oxygen), higher resin molecular weights (i.e., limited due to solubility), and stronger base developers. As with the AT&T resists, the Hunt system also contains a proprietary resin which participates significantly to the positive e-beam behavior.

2.3.4 Negative E-beam Resists. Like positive resists, these resists can be conveniently classified between mask-making and direct-write (see Tables III and IV). Basically, these resists are direct-write compatible when they are aromatic in nature, that is, when they are polystyrenes or naphthalenes or their derivatives, and mask-making compatible when they are

TABLE I: METHACRYLATE-BASED POSITIVE E-BEAM RESISTS

RESIST	SENSITIVITY	CONTRAST	DRY-PROCESS COMPATIBILITY
PMMA (IBM)	80 MicroC/cm^2	4	NO (see Table IX)
EBR-9 (JAPAN)	12	1.4	NO
FBM-120 (JAPAN)	5	2	NO
HP POS CROSSLINKED PMMA	40	3	NO
PBS (AT&T)	1	2	NO
PMCN (ARMY)	12	1	OK
PMCA (ARMY/HONEYWELL)	16	NOT MEASURED	NO

TABLE II: NOVOLAK-BASED POSITIVE E-BEAM RESISTS

RESIST	SENSITIVITY	CONTRAST	DRY-PROCESS COMPATIBILITY
HUNT-204	50 MicroC/cm^2	2.9	YES(0.5)
PC-129	200	4	YES(0.2)
HITACHI NPR	14	0.7-0.9	YES
AZ-2400(IBM)	10	-	YES IF DUV
	25	2.5	
	50	1.6	
HUNT-1182	25	1.3-1.6	UNKNOWN
ALLIED-6010	25	1.2-4	YES
HUNT WX-214	15	2.5-4	YES IF DUV

TABLE III: MASK-MAKING NEGATIVE E-BEAM RESISTS

RESIST	SENSITIVITY	CONTRAST	DRY-PROCESS COMPATIBILITY
AT&T COP	0.8 MicroC/cm^2	1.0	NO AND SWELLING
SEL-N (JAPAN)	2	1.2	NO AND SWELLING
KODAKS	0.5	0.8-1.3	NO PLUS SOME SWELLING PLUS EDGE-SCALING
CONVENTIONAL PHOTORESISTS	1-3	0.7-1.2	NO AND SWELLING

TABLE IV: DRY-PROCESS COMPATIBLE NEGATIVE E-BEAM RESISTS

RESIST	SENSITIVITY	CONTRAST	DRY-PROCESS COMPATIBILITY
POLYSTYRENE	80 MicroC/cm^2	2.0	YES(0.05)
CMS-EX-S (JAPAN)	1.7	1.6	YES(<0.1)
MES-E (JAPAN	1.5	1.5	YES(<0.1)
CMS-EX-R (JAPAN)	17	2.2	YES
ALPHA-M-CMS-S (JAPAN)	10	2.0	YES
AZ-1450	100	1.4	YES(<0.5)
-1450(+300)	160	2.4	
-1350(+300)	60	3.2	
GMC (AT&T)	4	1.6	YES

vinyl polymers without any unsaturated bonding except at the polymer crosslinking site.

Mask-making resists generally possess very good sensitivity, but low contrast or resolution (see Table III for examples). Their applications are restricted to making 5X or 10X reduction reticles where larger features (>4-5) microns are required. These resists withstand wet etching of thin chromium films, but also require descum processing prior to etch. These resists are basically useless for device fabrication applications using direct-write e-beam due to their poor plasma etch resistance(6). This is due to a general lack of selectivity to harsh RIE treatments and swelling behavior exhibited by these materials at feature sizes below 1 micron, the size domain where direct-write e-beam techniques are of need to improve circuit packing density.

The dry-process compatible resists shown in Table IV generally possess reduced sensitivily, but with higher contrast and resolution. The sensitivity trade-off, however, is not completely prohibitive (i.e., reasonable exposure levels $<10X10^{-6}$ Coul/cm^2 can be employed). Most importantly, these materials are less susceptible to pattern swelling during development, and submicron images are easily obtained. As for the mask-making resists, these materials must also be descummed after development for best resolution performance. Figure 10 illustrates the effect of the oxygen RIE descum on the negative resist image foot at the base of the example image. The alpha-M-CMS, CMS, polystyrene, and AZ tone-reversed positive photoresist systems have all been used in direct-write applications to fabricate high performance MOS and Bipolar circuits.

Negative e-beam resists are designed by incorporating radiation crosslinking groups into usually single component vinyl polymer resists(1)(2). These appendage groups range typically from alpha hydrogen or halogen, to side chain epoxy(37) and allyl(38), to halogenated alkyl groups attached to styrene(39) or acrylate esters(40) (see Figure 11). These groups are all very radiation susceptible and design incorporation into the resist leads to easily crosslinkable polymers with high G_X values, and hence, good e-beam sensitivities($\leq 5X10^{-6}$ C/cm^2).

Recent advances in negative E-beam resist design have been in the areas of polymer blending(41) and chemical amplification(42). The blending technique, similar to that for two-component positive e-beam resists, allows the preparation of a sensitive high contrast resist from a polymer with poor

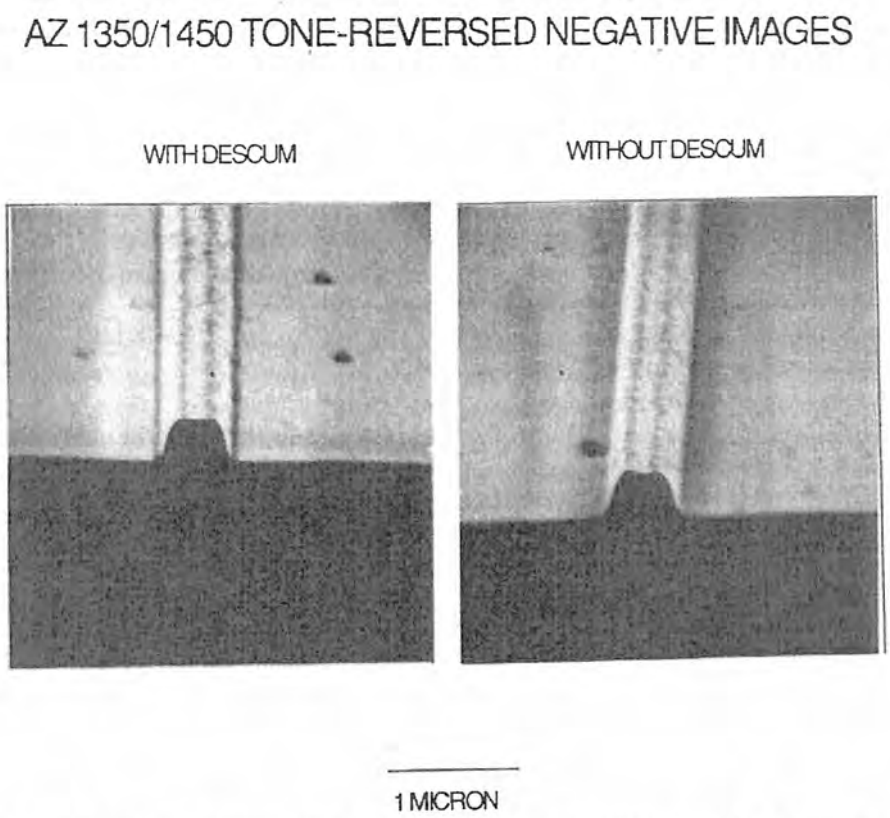


Figure 10. Illustration of line edge improvement via reactive-ion-etch oxygen descum processing on negative e-beam resist images.

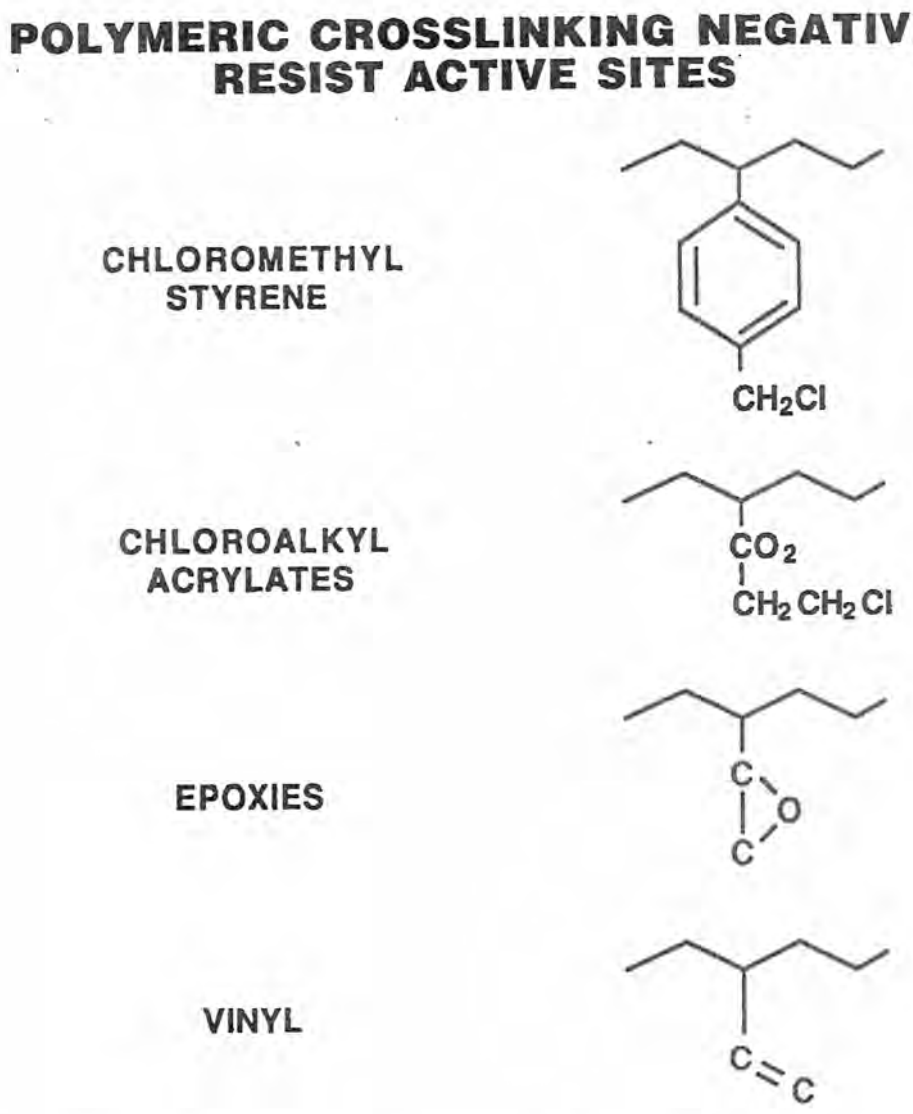


Figure 11. Polymeric crosslinking active sites for negative e-beam (or radiation) resists.

sensitivity. The sensitivity requirement for the insensitive material is that it possess a good electron donating ring substituent for improved H-abstraction induced crosslinking efficiency with the coblended chloromethylstyrene. The latter technique developed at IBM involves radiation induced acid formation in the resist to catalyze crosslinking or induce degradation, hence, positive and negative behavior can both be designed. An example negative behaving system is now marketed by Shipley as SAL 601 EBR-7 or later improved derivatives(43).

The limitation of negative e-beam systems stems primarily from their advantage. Sensitive crosslinked or gelled polymers are also very susceptible to developer solvent swelling (see Figure 12) due to the three dimensional crosslinked networks formed in the irradiated polymer regions. Hence, these resists generally suffer from reduced resolution and are highly susceptible to proximity effects (cooperative exposures which occur due to backscattered electrons from adjacent lines). As a result, these systems will probably always be limited to high pattern area coverage layers requiring somewhat lower resolution as is typical of many metal layer interconnect requirements. The new Shipley acid-catalyzed resists, however, are less susceptible to this resolution limiting effect because they are base developed novolac systems (recall: positive novolac resists are non-swelling).

2.4 Future Resists

Conventional positive photoresist technology combined with multi-level processing techniques (see applications and special processes section) will inevitably allow the lithographic community to achieve 0.5 micron or below design rules without the extensive use of resists responsive to ionizing radiation(44). The future of optical lithography beyond 0.5 micron will require extensive development in the areas of Deep UV resists, where new resin and PAC or single component resists, and even new resist mechanisms will be required. New advances, such as those demonstrated in DUV binder resin design by Turner et al.(45) and the chemical amplification resist mechanism by Willson et al.(42) or combinations of theoretical lithographic simulation(46) and statistical design of experiments(47) to achieve the ultimate resist design as proposed by Monohan et al., will evolve to provide the 4th or 5th generation photoresists for the 1990's. These new resists will probably be employed as top layer imaging systems for multi-layer resist processes, emphasized due to the sharp

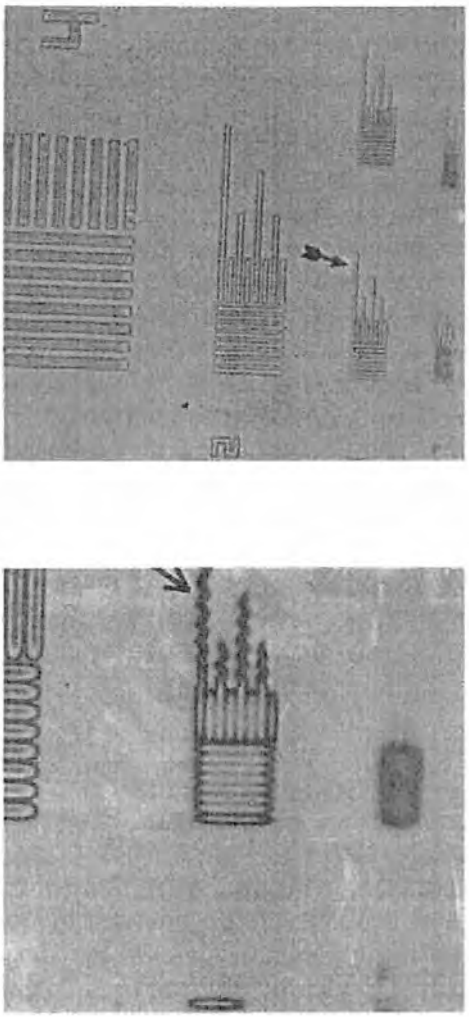


Figure 12. Optical micrographs illustrating snaking behavior, solvent developer, swelling behavior, of negative e-beam resists.

increase in numerical aperture or decreased depth of focus of proposed advanced optical lithographic systems(44).

3.0 RESIST PROCESSING

3.1 Resist Parameter Screening

Before a resist, commercial or otherwise, can be instituted into a device fabrication process flow, it must demonstrate high performance characteristics to a battery of fundamental tests. Completing these tests by no means provides an optimized resist process to be plugged into the production line. That comes later, but the results do provide the processing engineer on the IC fab line a basis for selecting one resist over another in a quantitative impartial way. Usually, the results for a new material are compared to those of an existing baseline process, whose capability may have become insufficient at one or more critical levels.

Usually, the resist vendor has spent a lot of time selecting a suitable developer for the resist to be tested, and that recommendation should be used at least initially for performance screening purposes. The investigating engineer, however, should make clear to the vendor what performance is actually being sought, that is, high contrast, speed, metal-ion free base developer or not, thermal stability, whatever. The device requirement will usually dictate the type of developer selected for testing.

3.1.1 Sensitivity and Contrast. Actual sensitivity curves are found in Figures 13 and 14 for example negative and positive systems, respectively. For these curves to have meaning, the experimental data of developer type or composition and concentration, development time and conditions, image dimension size, and the resist characteristics such as thickness must be known. The resist sensitivity for the negative system in Figure 13 is defined by that dose where 50-80% (i.e., the data may be fit to any point between 0 and 50 to 80% film retention but should be explicitly specified) of the original resist thickness is maintained; of course, the unexposed areas of resist are completely developed away and only the exposed images remain. For the positive system, sensitivity is defined as the dose where the image is cleared to the substrate (i.e., dose where $I_O - I_d/I_O = 0$), a unique point from the data plot.

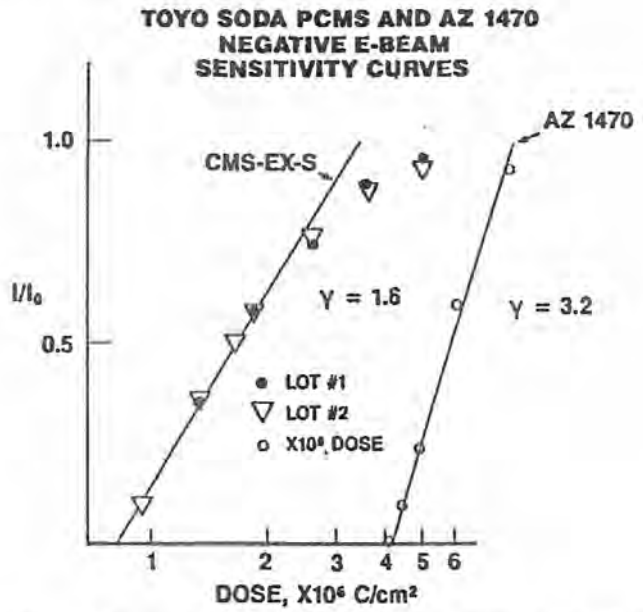


Figure 13. Characteristic sensitivity curve for two negative e-beam resists. The AZ resist is imaged density reversed with high e-beam exposure combined with a 300 mJ/cm^2 uv-4 flood exposure prior to development.

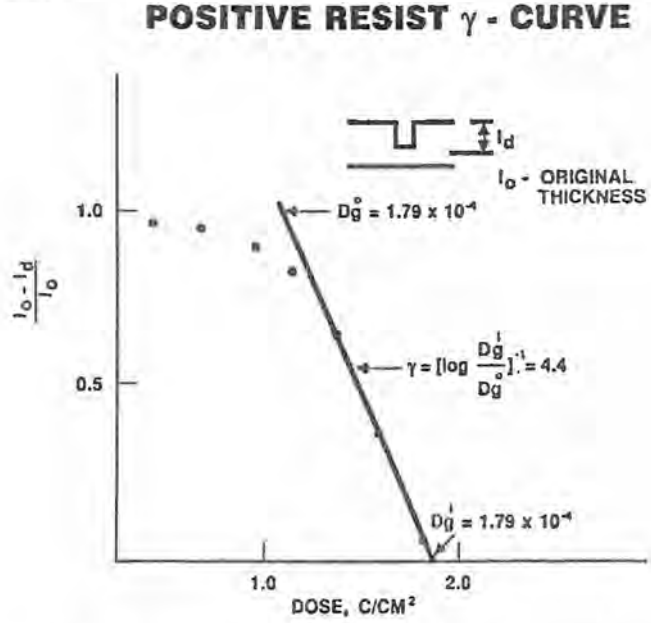


Figure 14. Characteristic sensitivity contrast curve for a positive e-beam resist example.

It should be noted here the negative resist sensitivity curve is essentially invariant with development time, where for the positive system a series of curves is obtained when the development time is changed. These curves will remain fairly parallel until appreciable unexposed resist loss begins to occur. The resulting curve never reaches I_o-I_d/I_o values of 1.0, even at low exposure. Both negative and positive sensitivity curves shift on the exposure axis when the image CD is changed. Most lithographic tools allow for exposure to be varied across the wafer, so this data can be generated on a single wafer if desired.

Resist process contrast is given by the slope of the least squares fit of the data in Figures 13 &14. The contrast of the process is obtained by simply subtracting the log values as depicted on the figures and taking the mathematical inverse. These values are of importance because they can be used to predict edge wall angles and resist resolution(48).

To better clarify positive resist sensitivity, researchers at IBM(30) have adopted a modified sensitivity plot where I(unexposed)/Io is plotted vs. exposure (see Figure 15). Here, each data point represents an entirely different wafer and development time combination for the chosen CD to develop. Note, it would take a series of exposure response curves like Figure 14 to generate a single curve like Figures 15a and b. Since for positive resists, the full resist thickness is usually required for further process masking requirements, this method of resist sensitivity measurement is of great value. The slope of these curves, however, is not a direct measure of the image dose response and cannot be used as a measure of resist process contrast.

3.1.2 Resist Image Edge Wall. When reactive-ion etching (RIE) dry etching techniques are employed, the resist image edge wall becomes an important evaluation characteristic and should be measured. A vertical resist image edge wall is essential to RIE to minimize etch bias even for the more anisotropic processes. Unfortunately, angle measurement requires a Scanning Electron Microscopy (SEM) picture be taken edge-on with a cleaved and mounted wafer piece, which is a tedious procedure. The edge wall can be preliminarily estimated from the bulk contast as measured above(48), but in the final analysis the edge wall must be verified. Near vertical resist image edge walls (i.e.,87-90°) are specified in nearly all modern facilities, thus necessitating this resist process characteristic be known to be employed as a criterion for resist/process selection (see Figure 16 for examples).

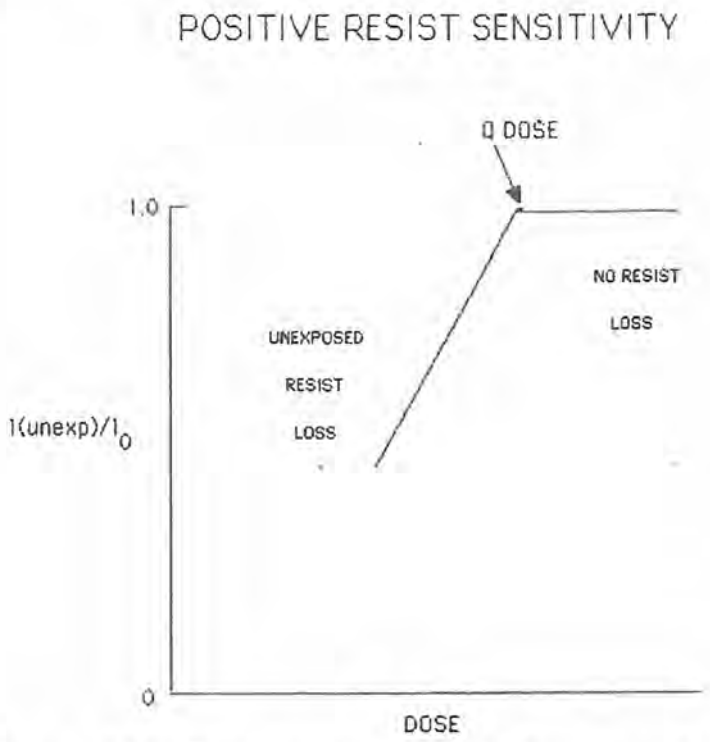


Figure 15a. Positive resist sensitivity curve for positive e-beam resists.

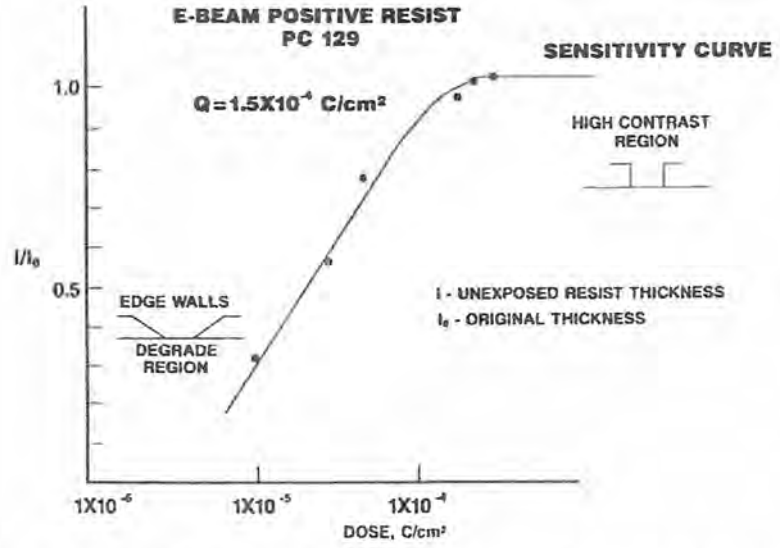


Figure 15b. Actual e-beam positive resist sensitivity curve for PC-129 positive photoresist.

Figure 16. SEM micrographs of positive and negative resist images illustrating the results of image edge wall profile angle measurement.

3.1.3 Resist CD Latitude. The most important resist process parameter to a photoengineer is image critical dimension control or CD latitude(20). This parameter can be quantitatively measured for a resist/developer combination as set forth by Walker and Helbert(49). In this method, a quantity called Δ, which is a measure of the difference of the resist image CD from that nominally exposed, is plotted vs. exposure and development time to obtain a series of characteristic curves. Figure 17 illustrates this for a positive photoresist example. Each point on this graph represents a different exposure and development time combination, which results in a cleared or fully developed image to the substrate. The solid uppermost line of Figure 17 is a least squares fit of data where the resist image just clears to the substrate; there is no data above this line because it would represent images that did not fully develop. The largest exposure on the horizontal Δ=0 line is an equivalence sensitivity condition for every plot, where sensitivities for resists can be compared on the basis of equivalent CD transfer. The |slope| of the just clearing line, called RPL, is a measure of the exposure/development latitude of the resist process being evaluated.

In Figure 18, a strong developer has been intentionally employed to illustrate the effect upon RPL and sensitivity; here an undesirably large value for RPL is obtained. Obviously, the flatest Δ, or CD, vs. dose curve is most attractive from a process stability view, and the resist process yielding that performance characteristic should be implemented onto the IC fab line.

Tables of RPL results for representative first, second and third generation resists are found in Tables V-VIII. Since these results are dependent upon testing conditions, they are not meant to be absolute as to the performance of the resists tabulated, but they are of interest for gathering some general performance trends. Second generation resists tend to be more sensitive than first generation materials, while third generation resists tend to have greater contrast as well as sensitivity without sacrificing CD latitude in the process. The effects of developer concentration and development method upon sensitivity and CD control are also evident from these tables. Developer concentration increases can lead to greater sensitivity (Table V), but usually at the expense of latitude. Development method (see Table VIII and Figure 19) can influence process contrast and should be investigated when feasible.

Figure 20 compares two real e-beam gate processes actually employed to make CMOS transistors. The process on the left had a severe exposure latitude problem, and as a result

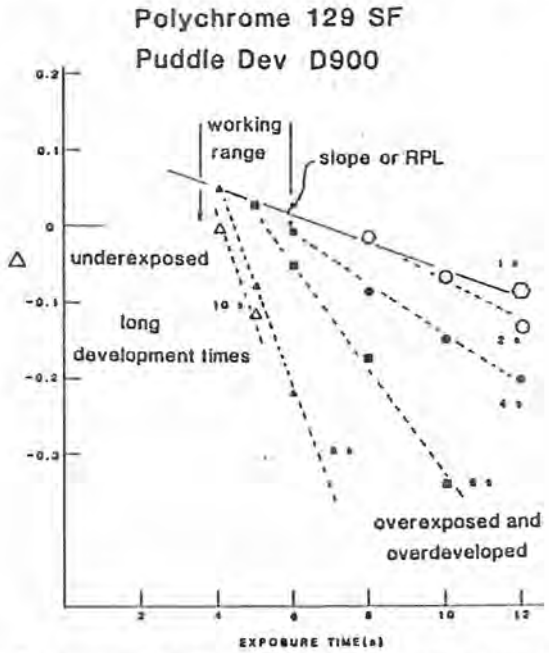


Figure 17. Characteristic sensitivity curve for positive photoresist employing CD transfer as a criterion.

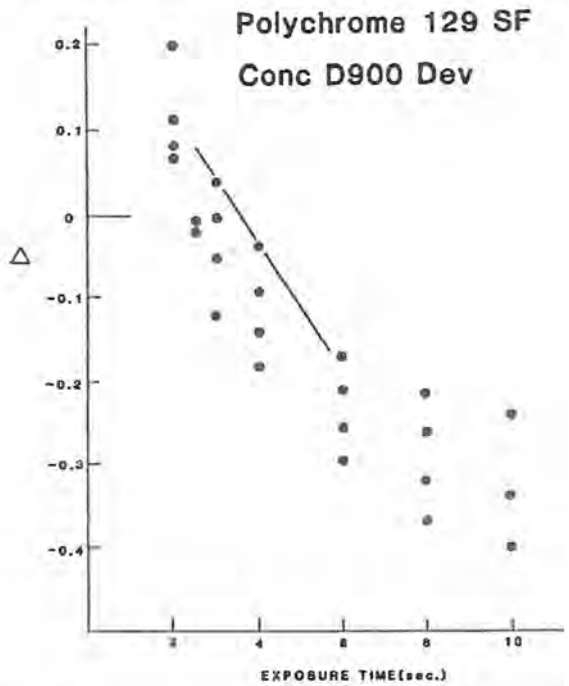


Figure 18. Delta vs. exposure characteristic curve for positive photoresist with a concentrated developer.

TABLE V: PHOTORESIST PERFORMANCE DATA FOR FIRST GENERATION RESISTS

Resist	γ	RPL	Q,[a] mJ/cm^2	Developer /Method
PC-129 (Allied P2025)	2.0	1.0	110±20	D900/DIP
		1.6	102	D900/PUDDLE
		1.6	119	D910/DIP
		4-8	50	CONC 900/DIP
AZ-1350	1.5	1.4	81	1:1 MF 312/DIP
KTI-II	1.8	2.1	105	DE-3/SPIN-SPRAY
		1.0	132	DE-3/DIP
Kodak-809	1.6	0.4	100-160	809 Developer
HPR-204	1.7	2.7	91	1:1 LSI/DIP
		3.5	60	1:1 LSI/PUDDLE

a Data for nominally 3 microns line and space mask images.

TABLE VI: PHOTORESIST PERFORMANCE DATA FOR SECOND GENERATION RESISTS

Resist	γ	RPL	Q,mJ/cm^2	Developer/Method
Allied P-5019	2.5-3.8	1.0	13	2:1 D100/DIP
		3.9	72	D150/DIP
		3.0	95	LM1500/DIP
AZ-1470	1.8	2.3	40	1:1 MF312/DIP
-4110	1.6	1.5	43	1:1 MF312/DIP
OFPR-800-1	1.4	1.3	74	NMD3-1/DIP
-800-2		2.7	75	NMD3-2/DIP
-800-1		0.5	37	1:1 MF312/DIP
KMPR-820-AA	1.2	1.6	18	AA-0980-52 /DIP
-820		2.2	17	AA-0980-52/DIP
HUNT-159	1.5-1.6	0.9	73	1:3 LSI/PUDDLE
-118		1.4	62	1:3 LSI/PUDDLE
MAC-9564	1.1	3.8	24	1:1 9562(MF)/DIP
		4.2	24	1:1 9564/DIP
-9574		1.9	12	1:1 9571/DIP

TABLE VII: 3RD GENERATION RESIST RESULTS

RESIST	Q, mJ/cm^2	RPL	γ	DEVELOPER
ALLIED 6010	83	1.1	1.3	LMI-600/DIP
	89	2.3	2.3	D-360/DIP
AZ 4110	45	1.0	1.5	1:1 MF 312/DIP
5214	62	2.1	2.3	1:1 MF 312/DIP
DYNACHEM				
XPR 1000	52	2.2	2.4	NMD-3/PUDDLE
1501	120	1.2	1.9	
MACDERMID 914	250	1.5	2.4	1:1 MF-62/DIP
KTI 9000	72	2.1	1.7	DE-3/SPRAY
JSR 3003A	60	0.8	1.6	JSR DEV/DIP
TOKYO OKA ONPR 830	40	0.6	1.7	NMD-3/DIP
KTI 9000	72	1.2	1.7	DE-3 Spray
Monsanto RX7	94	2.0	1.9	MFD Dip
Sumitomo PF6200	80	0.9	1.5	SOPD Dip
OFPR 800	75	1.3	1.4 (1.6)*	NMD-3/PUDDLE

*DYNACHEM DATA

TABLE VIII: DEVELOPMENT METHOD EFFECT

RESIST	METHOD	RPL (mJ/cm^2)$^{-1}$
KTI-II	SPIN/SPRAY	2.1
	DIP	1.0
HUNT-204	SPIN/SPRAY	SURFACE SPOTS
	DIP	2.7
	PUDDLE	3.5
PC-129SF	SPIN/SPRAY	SEVERE SURFACE SPOTS
	DIP	1.0
	PUDDLE	1.6

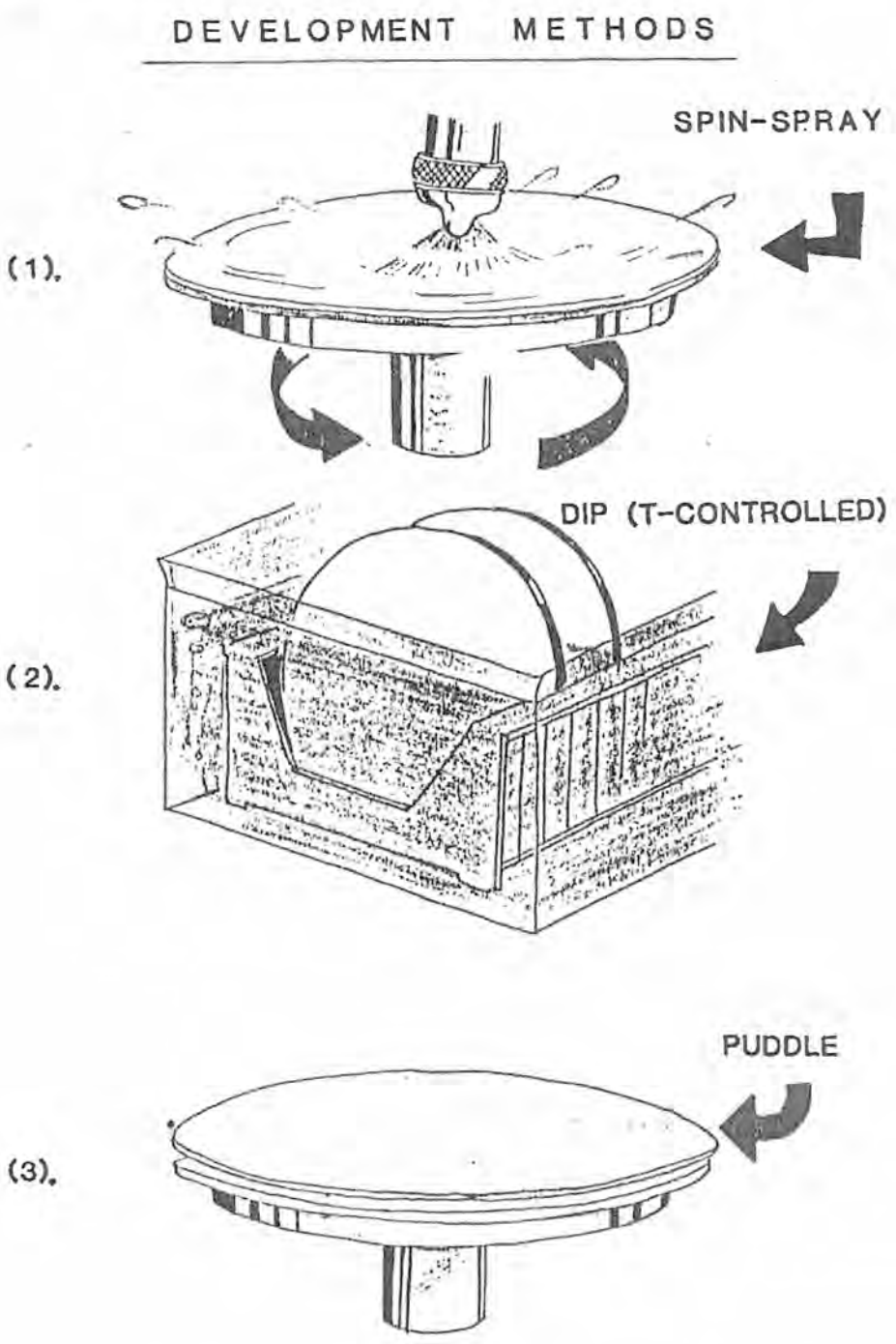


Figure 19. Development methods used to create relief images in photoresist materials.

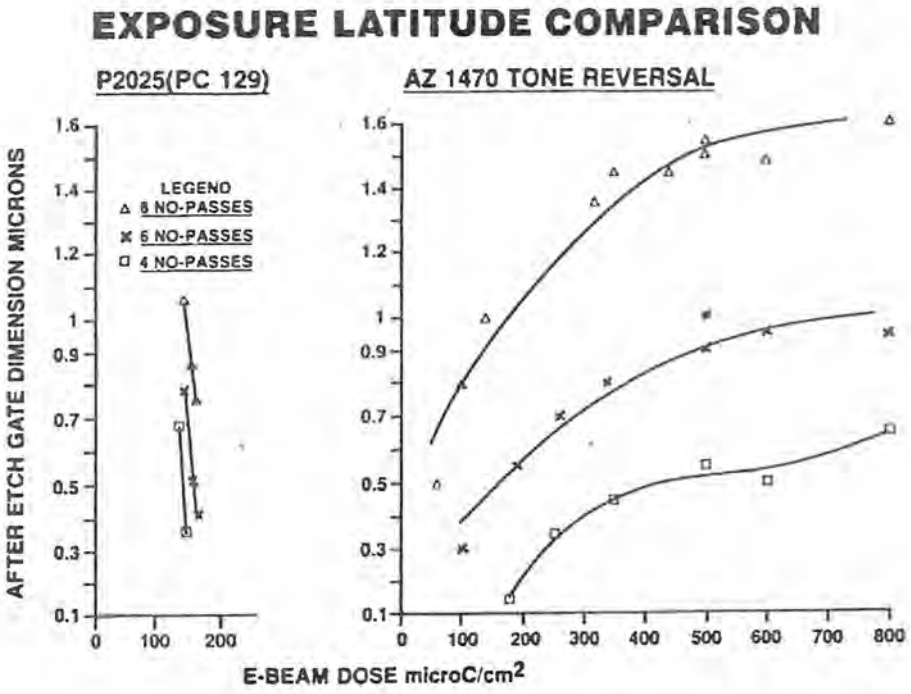


Figure 20. Exposure latitude comparison for two electron beam gate processes. The process to the left employed positive resist with unexposed pattern islands, while the process to the right is the same as that for the Figure 13 AZ process.

rework rates for this process were between 40-60%; due to this poor latitude, the process to the left was never fully implemented.

Sometimes CD vs dose curves are flat (i.e., have latitude like that shown in Figure 21), but are not flat at the CD required. When this occurs, a process bias is applied to the process to achieve the CD specification. This is done by shaving the e-beam directly written image by software or by biasing the Cr image on the reticle or photomask, and is fairly routine to all fabs.

3.1.4 Process Compatibility. All the measurements described above are of academic interest only if the resist is not device fabrication process compatible. It must be able to withstand Ion-implantation (II) or RIE processes, for example, without loosing CD integrity, that is, it must resist these processes from both a thermal flow and radiation degradation point of view. RIE selectivity, a component of RIE compatibility, for example, can be measured as shown in Figure 22. The measured selectivity must be << 1, or the lower the better. If S is 1 or larger, the resist does not possess the required process compatibility, and cannot be used. Typical values are found in Tables IX & X.

Thermal image flow/degradation resistance, the second part of process compatibility, can be estimated from polymer or resin differential scanning calorimetry (DSC) measured glass transition temperatures (tg) and thermal gravimetric analysis (TGA) measured decomposition temperatures, respectively(50). See Figures 23 and 24 for examples for pure novolac resin polymer. Resist manufacturers usually list these parameters in their technical brochures, and this additional data forms the rest of the data base required to make a resist process decision.

3.2 Resist Adhesion Requirements

Before spinning resist onto the IC wafer in process, resist adhesion promotion is typically accomplished. This process, involving either liquid or vapor phase treatment of the wafer with hexamethyldisilazane(HMDS), has become an industrial standard. It is typically used at every lithographic step in the IC fab process, whether it accomplishes surface modification or not. HMDS processing can be carried out on automatic wafer tracks with liquid or vapor HMDS modules (e.g., GCA or SVG) or in stand alone microprocessor-controlled all stainless-steel commmercial reactor chambers (e.g., IMTEC or YES); these processes are proven for high volume production.

Resist image adhesion is of paramount importance, because if IC circuit patterns are missing or are not the right dimension, the device will simply not function as designed. The resist systems

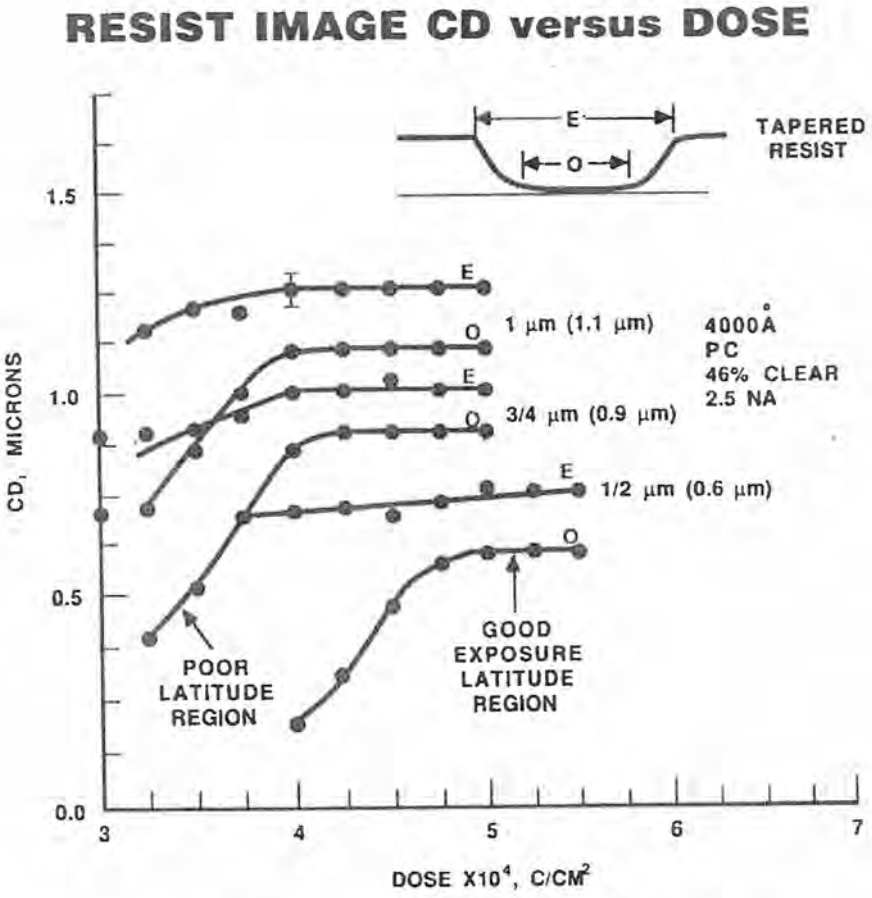


Figure 21. Resist image CD vs. dose for an example e-beam positive photoresist process.

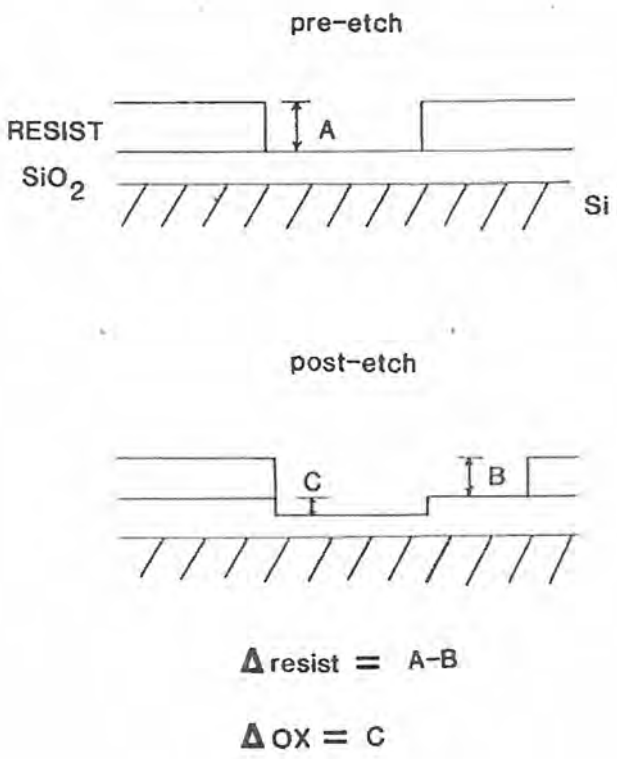


Figure 22. Etch rate ratio measurement methodology and calculations method.

TABLE IX: PLASMA ETCH RATIOS VS SiO_2 REFERENCE AND THERMAL PARAMETERS FOR VINYL POLYMERS

Polymer or Copolymer	Mole % ratio	T_g °C	TGA °C	Plasma etch Rate Ratio
PMCN	100	120	335	0.3
PVDCN	100	165	260/500	insoluble
PVDCN-CO-MMA	52/48	155	330/500	0.4
	38/62	135	270/400	1.0
PMMA	100	107	275	0.9-1.2
PACAN-CO-MCN	50/50	131	210/500	1.0
	39/61	128	223/500	0.5
	11/89	123	216/500	0.4
PACAN	100	-	-	1.3
PCMMA	100	115	250	0.4-1.1
PCEMA	100	105	250/400	2.1
PCEMA-CO-MMA	50/50	102	293	1.4
PTFMAN-CO-MCN	12/88	123	357	0.3
PTFMAN-CO-MMA	32/68	98	295	0.3
PMCA	100	130;151	-	1.8
PTCEMA	100	123	305	2.3
PTCEMA-CO-MCA	66/34	137	286	3.5
PTCEMA-CO-MCN	50/50	130	310	0.4
PTCEMA-CO-TCECA	90/10	123	290	2.0
PTCECA	100	147	290	2.0
PTCECA-CO-MMA	29/71	130	325	1.6
PACTFEMA (EBR-9)	100	133	277	2.1
PMFA	100	131	404	0.4
PMBA	100	130	170	2.0
PBCEE	100	100	293	1.7
PBCEE-CO-MMA	25/75	78	275	1.0
	50/50	92	292	1.1
PBCME	100	72	320	2
PBCME-CO-MMA	50/50	100	310	0.9
PEMA	100	65	-	1.7
PAMBL	100	83	363	0.3
PCMS (Toyo Soda)	100	105	350	0.06
PS	100	103	322	0.1

Abbreviations and Structural Formulae:

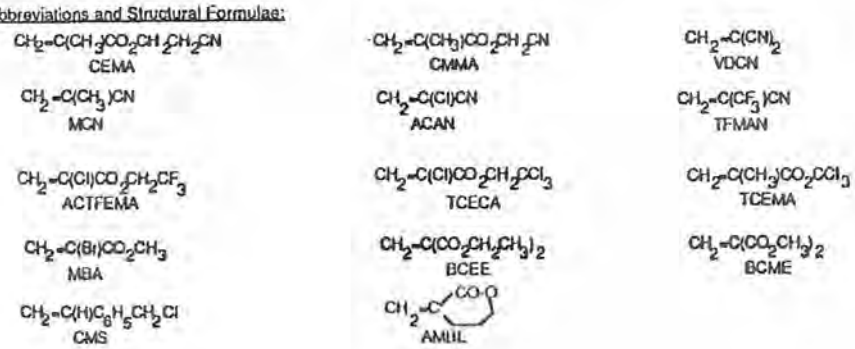


TABLE X: POSITIVE PHOTORESIST THERMAL FLOW AND PLASMA ETCH RATE RATIO CHARACTERISTICS

Resist	TGA, °C	Image Flow Temperature, °C	PE
PC-129SF	125	140	0.2
KTI-II	133	160-170	0.4
OFPR-800	150	160-170	0.3
AZ-1350	140	140-160	0 5
AZ-2400*	145	140	0.5
KODAK-809*	-	120-130	0.3
HUNT-204	-	180	0.5

*AZ-2400, and K-809 "fry" (see Figure 9).

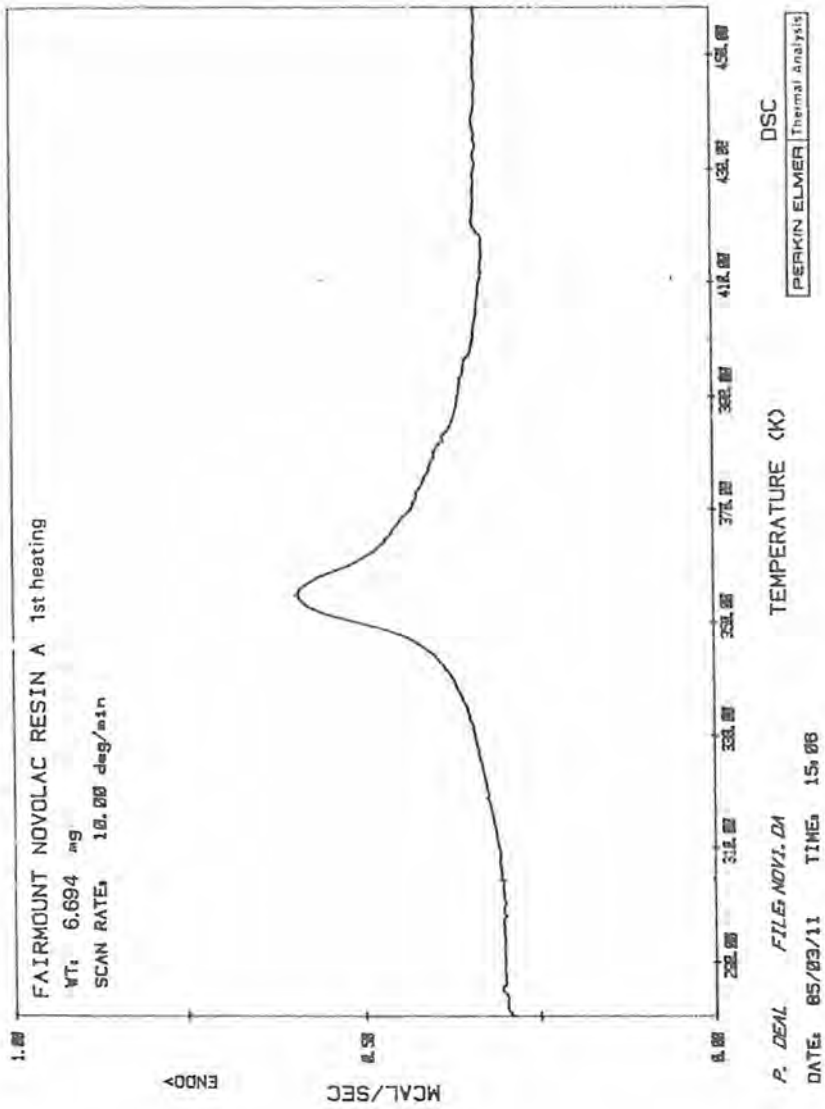


Figure 23. Differential Scanning Calorimetric (DSC) thermo-analysis curve for an example novolac resin.

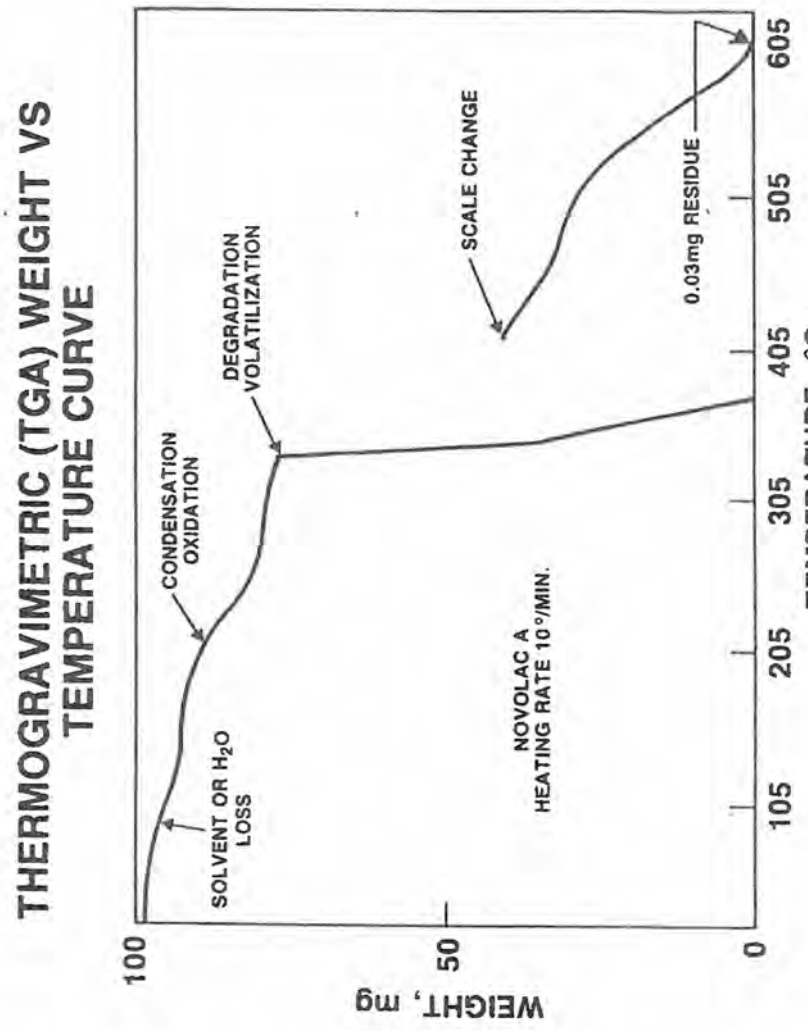


Figure 24. Thermogravimetric Analysis (TGA) curve for example novolac system.

most susceptible to resist image lifting at the development stage of processing are positive e-beam and conventional photo- resists (51). Historically, negative photoresists also have required adhesion promotion, but in that case the goal was reduced undercut from wet etch processing and not the prevention of simple image lifting at develop(52)(51). Undercutting is less of a consideration for positive photoresists, because they are used primarily in conjunction with anisotropic dry etching processes. Examples of negative resist wet etch undercut and positive lifting at develop are shown in Figures 25 and 26.

What is accomplished by adhesion promotion treatments in IC manufacturing should actually be referred to as wafer substrate preparation, and not adhesion. Adhesion in the structural sense, as found in airplane composite material part attachment, is not accomplished in HMDS processing treatments. The term adhesion, as it is used here, refers to a more practical definition, that is, resist image adhesion. Figure 27 demonstates what is actually accomplished when a Si wafer is treated with HMDS. The ESCA(53) spectra shown clearly illustrate the removal of carbon containing adsorption species at lower binding energies in favor of the monolayer of trimethylsilyl surface reaction product(see Figures 27a and b)(54). In addition the surface is dehydrated in-situ as verified by increased water contact angle(55) and a lower O/Si ratio as measured by ESCA. Furthermore, this converted surface is stabilized for days against recontamination, therefore, the HMDS process provides a very stable surface for resist adherence. The Si 2p ESCA spectrum of Figures 27c and d verify the appearance of the trimethylsilyl silanol reaction species.

Substrate nonwetting, another adhesion problem, has been observed most frequently with mistakenly overpromoted wafers. It occurs after repeated treatments, when the wrong liquid treatment has been applied, or when vapor times exceed the optimum time for that respective substrate. It also can occur in selected circuit pattern areas and not for the whole layer, and can be characterized by higher water droplet contact angle. Although it is not generally well understood, it can be prevented by reducing prime times for vapor treatments, corrected by ion treatment of the wafer(56), and be prevented by using resist containing a spinning solvent of lower surface tension or by double resist application under dynamic spin conditions. The silicon based substrate layers, nearly all the layers encountered in IC device production except metal layers, can usually be successfully promoted against lifting by treatment with liquid silanes or silane vapor treatments at reduced pressures(52)(54)(56) (see Figure 28).

Figure 25. Wet etching adhesion test of silicon-illustrating wet etch undercutting at the silicon resist interface during the etch process.

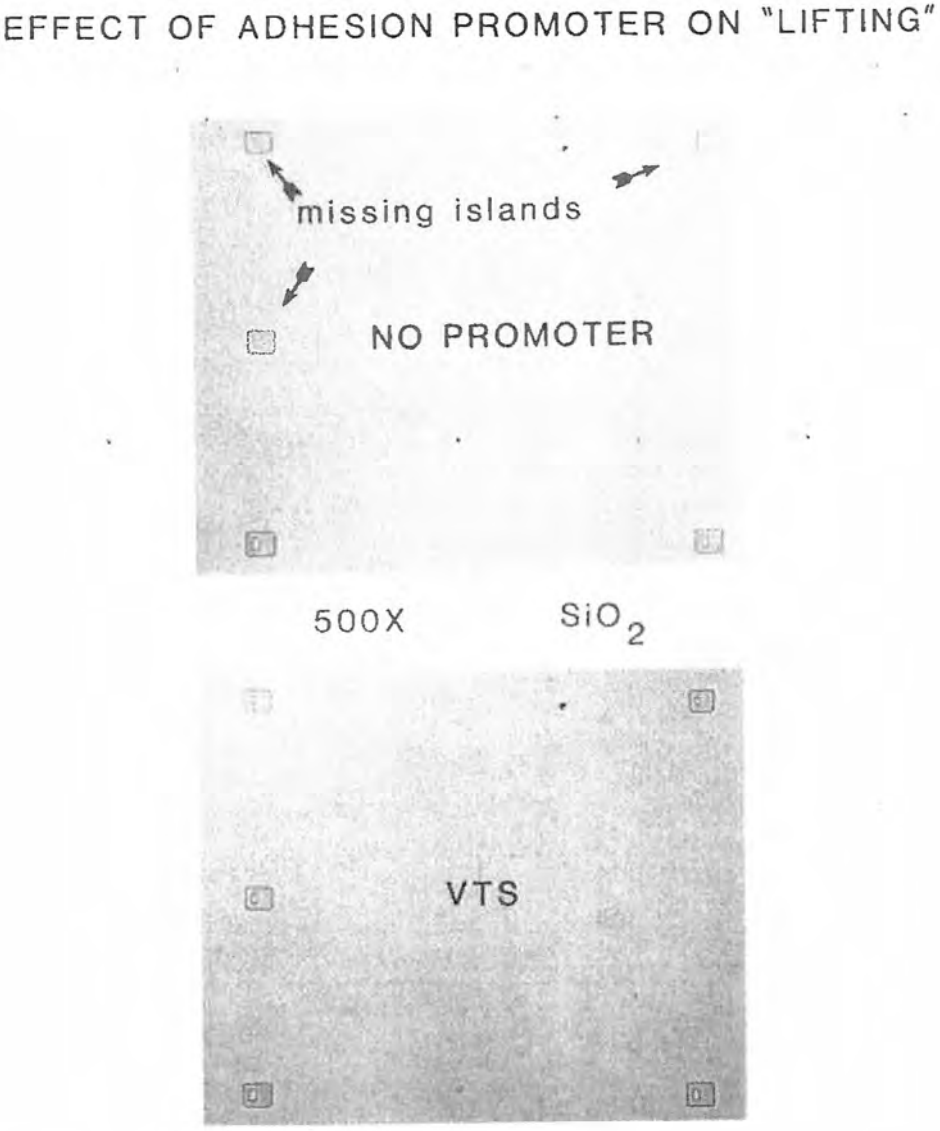


Figure 26. "Image Lifting" phenomena observed with and without adhesion promoter on SiO_2 test surfaces. This type of lifting occurs at development prior to etch processing.

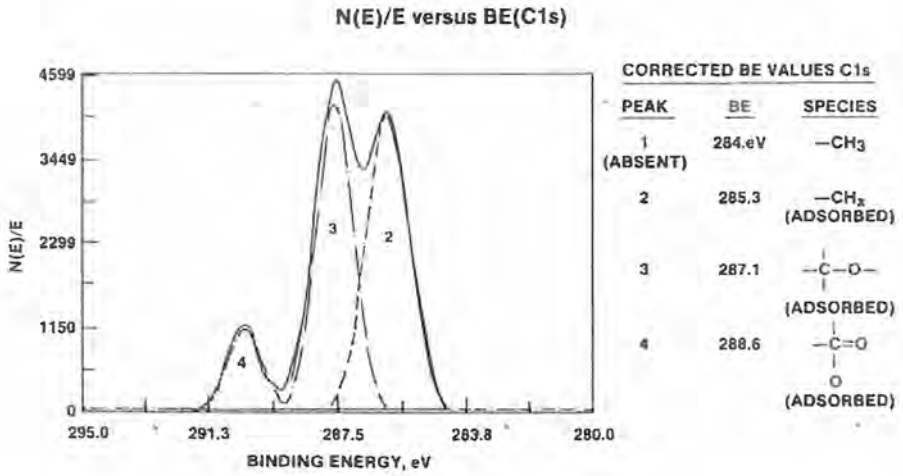


Figure 27a. N(E)/E vs. BE for carbon 1s bare silicon wafer.

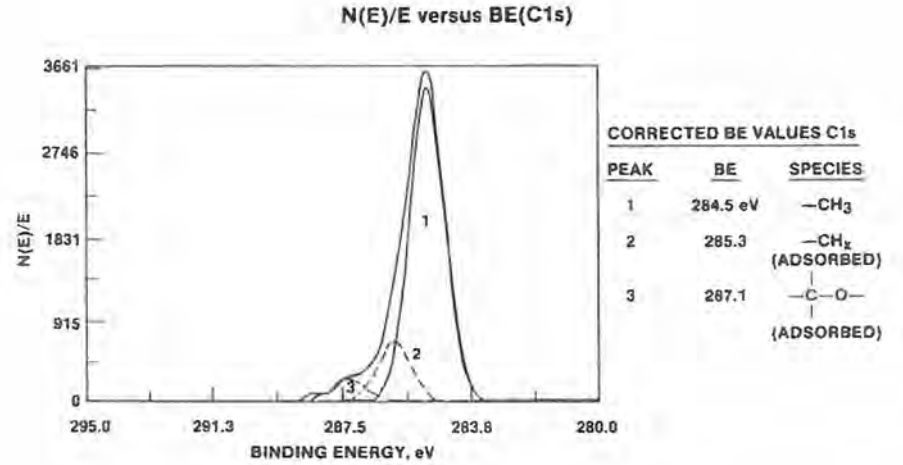


Figure 27b. N(E)/E vs. BE carbon 1s for HMDS vapor (Star 2000) treated silicon wafer.

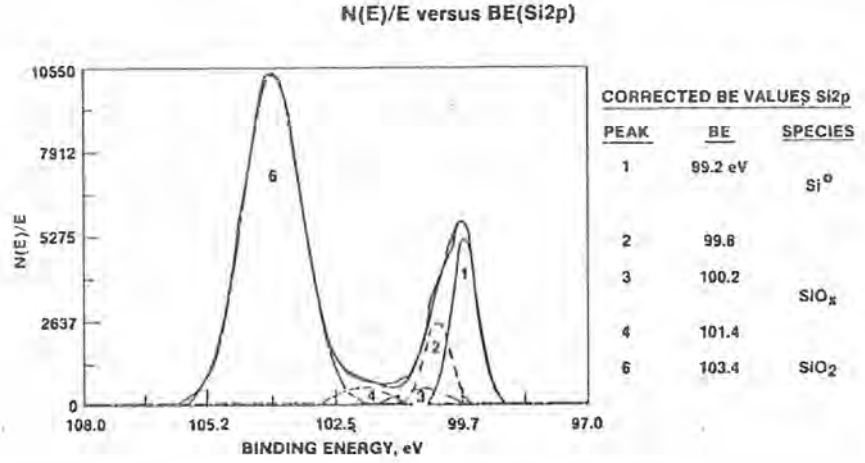


Figure 27c. N(E)/E vs. BE silicon 2p for untreated silicon wafer.

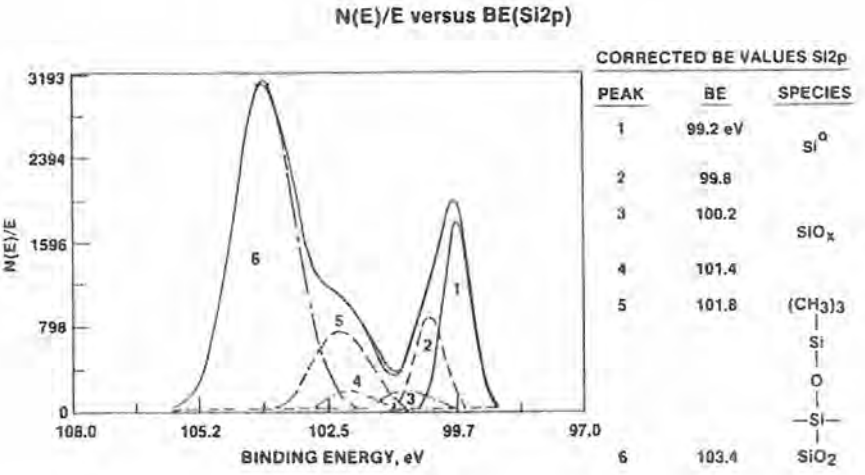


Figure 27d. N(E) vs. BE vs. for silicon 2p of HMDS treated silicon wafer.

CHEMICAL REACTIONS:

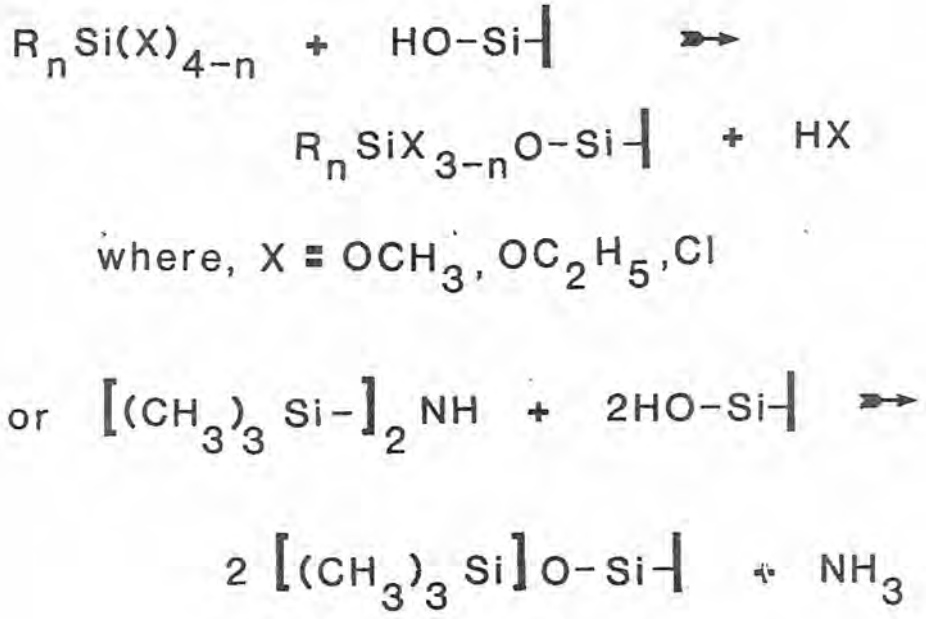


Figure 28. Chemical reactions for different silicon-based adhesion promoter systems.

The carbon 1s ESCA spectra are shown for a Si(100) substrate with native oxide (<50 A) in Figure 29 to illustrate the surface chemical changes between liquid and vapor promoter processes. The LPIII process, a vapor HMDS process, efficiently removes the carboxylic, etheral, and hydrocarbon impurities from the surface and replaces them with a blanket of trimethylsilyl groups comprising a monolayer (also see Figures 27 c and d).

The Mallinckrodt system, a model liquid primer with both amine and alkoxy silane molecular moieties, replaces the carbon surface species with CH_x species resulting from the condensation polymerization reaction on the surface, which produced a 20-50 Å thick adhesion promoting layer. When the Si 2p spectrum is observed, a new signal appears at 101.8 eV (see Figures 27c and d) from the $Si(CH)_3$ groups for the vapor treated HMDS substrates, while no such signal appears for the Mallinckrodt system. Hence, the two comparison systems differ in the basic method of adhesion lifting prevention even though they are both successful "lift preventing" processes. In Table XI, the ESCA results and water droplet contact angle (CA) measurements are listed for a range of representative processes. Total surface C/Si ratios from ESCA are also listed because lifting has been shown to occur when that parameter is found to be from 30-100% larger than that for primed wafers(54).

The CA measurements of Table XI indicate these treaments are also very successful at removing wafer surface water contamination, as has been verified by others (see ref. 55 and references therein). It is notable, however, that there is a correlation between CA, resist image lifting results and ESCA surface condition. If CA is less than 60 degrees, the ESCA C 1s carboxylic peak at 290 eV present, and there is a high relative total C/Si ratio, lifting or poor resist image adhesion is very likely to occur, either intermittantly or quite frequently. For semiconductor manufacturing or any manufacturing process this kind of processing uncertainty is unacceptable, and the vapor processes and some liquid treatments have created better process reproducibility. HMDS SVG, a wafer track applied liquid HMDS process, is an example of a process that worked most of the time, but provided only marginal resist image lift prevention reproducibility. Vapor temperature is seen in the Table to make little difference to the measured parameters, while time of prime does provide more attractive, i.e., higher CA values. Multiple priming and long prime times can also lead to overpromoted or

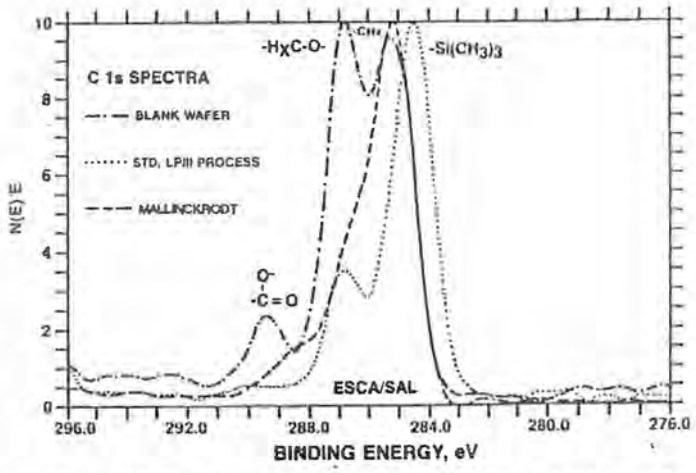


Figure 29. N(E)/E carbon 1s spectra for blank wafer and two comparison photoresist adhesion promoter processes, standard LP 3 vapor and vs. Mallinckrodt (liquid silane).

TABLE XI: ADHESION PRIME METHODS COMPARISON

		ESCA			
METHOD	TYPE	CARBOXYLIC	TRIMETHYLSILYL	C/SI	CA
STAR 2002(5 MIN)	VAPOR(100 C)	NO	YES	0.64/NA	75
STAR 2002(90 SEC)	VAPOR(100 C)	NO	YES	0.58/NA	69
STAR 2000	VAPOR(150 C)	NO	YES	NA/0.8	77
YES LP-3	VAPOR(120 C)	NO	YES	0.54/NA	76
SVG	VAPOR(RT;760 MM)	YES; CA<70 NO; CA>70	YES	0.46/NA	75
HMDS SVG	LIQUID	YES	SMALLER	NA/1.1	58
MALLINCKRODT	LIQUID	SMALL	NO	NA/1.5	60
VIRGIN CONTROL	NA	YES	NO	1.0/1.1	24

nonwetting (i.e., at coat) wafers, therefore, the prime time should be optimized for each substrate.

After silicon wafers have been fabricated to a certain level, they become too valuable to terminate fabrication when misprocessed. Sometimes either the wrong mask is used, the resist exposure is adjusted improperly, or the resist is improperly developed. At lithography, since the pattern is just a thin polymer layer and not an integral part of the circuit, by simply removing the misprocessed layer, the wafer can be saved and completed. A good rework process, sometimes referred to as recycle or redo, is required to accomplish this task. For device implantation, etch, or deposited layers, this flexibility is lost. As a result, rework or redo is quite common in fabrication frontends. Unfortunately, Deckert(57) has found silicon oxide wafer surfaces exhibit random photoresist adhesion variation, which is very much affected by previous chemical treatments, such as those for rework. Of course, these effects can cause defects, and the additional wafer processing required is known to statistically increase defect levels, which in turn decreases circuit electrical yield. Obviously, original and rework processes which prevent adhesion failure and are clean from a surface point of view, are very important economically. The best case situation occurs when the rework process is also the resist removal process, the one which removes the resist following layer patterning completion, thus only one process would be required.

When considering adhesion effects with rework wafers, we must first look at the effect upon substrate surface chemistry of a representative group of resist strip or removal processes. This is done in Table XII. The same wafer parameters are used as for Table XI. Oxygen plasma and sulphuric acid/peroxide are both oxidizing carbon removal techniques, Carbitol is a commercial mildly alkaline organic solvent stripper, and acetone is simply a representative organic resist solvent stripper. All but the acetone treatment restore the wafer to a state close to the original before prime and coat, but the simple acetone dissolution strip leaves the substrate in the primed, ready for recoat, state, thus saving a reprime processing step. Importantly, the other processes tend to leave the substrate less clean and with larger CA values than the virgin wafers. These observations are consistent with those reported by Deckert(57), where greater lifting or poorer adhesion was reported to occur for sulphuric/peroxide reworked wafers. Obviously, reworking wafers is not desirable, but when economically necessary, simple solvent treatments on a particle filtered wafer track like the acetone treatment are attractive and can be effective.

TABLE XII: REWORK METHOD WAFER CHARACTERIZATION

	ESCA			
REWORK PROCESS	CARBOXYLIC	TRIMETHYLSILYL	C/SI	CA
ACETONE DISSOLUTION	-	+	NA/0.48	70
OXYGEN PLASMA	+	-	NA/0.7	39
ACETONE/PLASMA	+	-	NA/0.8	26
SULPHURIC/PEROXIDE	+	-	0.6-0.8/NA	25
CARBITOL STRIP	+	-	0.6-0.8/NA	48
VIRGIN CONTROL	+	-	0.6/1.0	25

Rework/reprimed wafer results are found in Table XIII. Here it is seen that all the rework processes return the substrate to a primed condition, but they are all a little less properly conditioned than the virgin wafer controls. Either the CA or the ESCA data are a little worse than those values for the virgin controls. Most importantly, these processes must all be concluded to provide a more particulated wafer simply due to the increased handling and processsing involved and this most likely will result in reduced circuit yield.

3.3 Resist Application

Resists are applied by wafer spinning modules either integral to a wafer track system (eg, GCA or SVG) or as individual units like those sold by Headway Research. The resist solutions with an optimally volatile spinning solvent, are applied dynamically (i.e., with the wafer spinning at 2-100 rpm) or statically to the wafer using 1-4 cc's of resist, spread across the wafer by a low frequency spin (e.g., 500 rpm), followed by a high rpm/sec ramp (e.g., 5000-40000 rpm/sec) to the final thickness determining rpm usually at ~ 5000 rpm.

The film thickness for positive photoresists can usually be approximated by:

$$[3] \qquad t = K(C)^2 / SS^{0.5}$$

where, C is the concentration of solids and SS the spin frequency in rpm. Stein(58) of Hunt Chemical has shown that K increases with the average molecular weight of the resin. The more general form of this empirical equation is:

$$[4] \qquad t = K(C)^{\beta}(v)^{g}/(SS)^{a}$$

where v is the solution viscosity. Log-log plots of t vs C, v, and SS provide the constants ß, g, and a from the slopes of the least squares data fits, empirically. More typically, technicians in fab lines simply run a curve of t vs. SS and fit the curve with an exponential function as shown in Figure 30 . Due to differences in coating equipment and fab ambient conditions, these curves must always be run, and vendor-provided spin curves used only as rough thickness guides. Resist vendors also adjust resist solutions to achieve the approximate thickness desired to be obtained at roughly 4-5K rpm, because thickness variation is often minimized at mid-range rpm values.

TABLE XIII: REWORK REPRIME CHARACTERIZATION

REWORK PROCESS	ESCA CARBOXYLIC	ESCA TRIMETHYLSILYL	C/SI	CA
ACETONE DISSOLUTION ONLY	NO	YES	0.48	70
SULPHURIC/PEROXIDE/SVG	NO	YES	0.48	68
SULPHURIC/PEROXIDE/2000	VERY SMALL	YES	0.59	77
CARBITOL/SVG	VERY SMALL	YES	0.56	77
CARBITOL/2000	NO	YES	0.60	70
VIRGIN/SVG	NO	YES	0.43	73
VIRGIN/2000	NO	YES	0.46	78

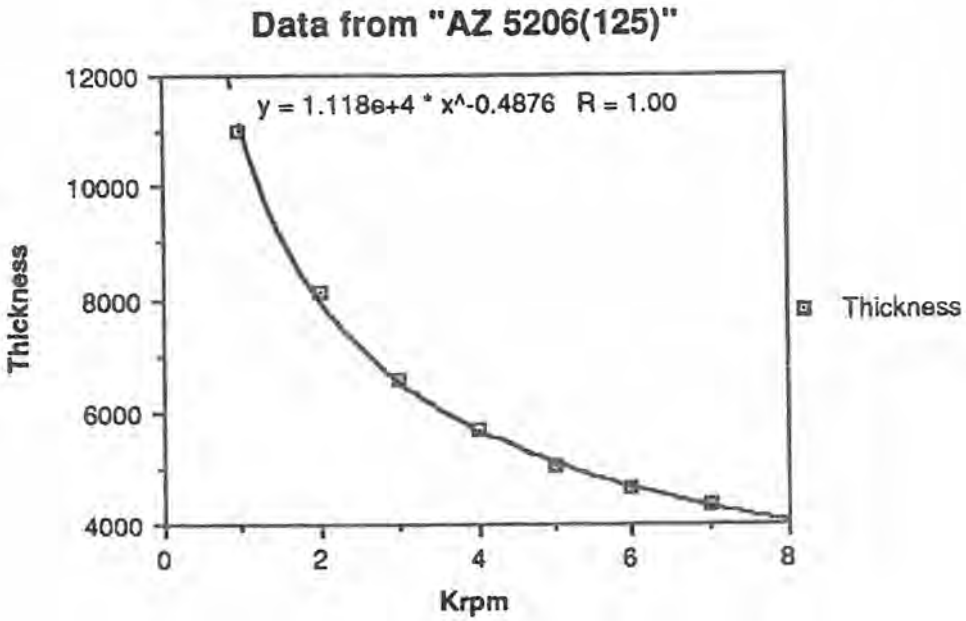


Figure 30. Thickness vs. RPM for AZ 5206 prebaked at 125°. The solid curve is an exponential fit of the experimental data.

Meyerhofer(59) has theoretically treated wafer spinning application of resist and accounted for thickness and drying times considering only centrifugal force, linear shear forces, and uniform evaporation as variables. Middleman(60a) has further shown that air flow induced by disc or wafer rotation provides the required shear stress at the liquid/air interface to enhance the rate of resist thinning on the wafer.

Of more importance than average film thickness across the wafer is the film thickness variation across the wafer measured radially from the center of the wafer. This is important, because resist image critical dimensions can vary beyond specification limits due to the resist film thickness variation. Film thickness variation depends upon the spin frequency, and an optimum frequency is usually measurable at a given solution viscosity. Typical thickness variation within wafer and wafer to wafer for 1986 vintage wafer track spinners is of the order of 20-100Å and 50-200Å, respectively which is more than adequate for CD uniformity requirements of most lithography areas. Control charts are typically used (see Figure 31) to monitor coat processes and if values for monitor wafers fall out of specification, the wafer tracks are shut down for maintenance or engineering adjustment.

Film nonuniformity, visually observed as radial stripes in the resist called striations, is prevalent when either the resist solvent is too volatile, dynamic dispense is employed, wetting additives are omitted, or at high resist concentrations. Striations are easily measured using interferometric or profilometric techniques. Orange peel, another spin problem, occurs due to rapid evaporation of volatile spinning solvents, and cloudy resist films sometimes occur when hygroscopic solvents are employed(60b).

Machine variables which have been observed to influence resist coating uniformity and average thickness are exhaust flow thru the coat module, motor frequency control and acceleration precision, dispenser type, and of course possible interactions which may occur between these and the resist variables already mentioned.

Optimizing coating processes is a complex time-consuming empirical task. It involves screening the many potentially material dependent variables through statistically designed experiments(61) to reduce or minimize process variability to achieve manufacturing success.

3.4 Prebake/Exposure/Development Processing

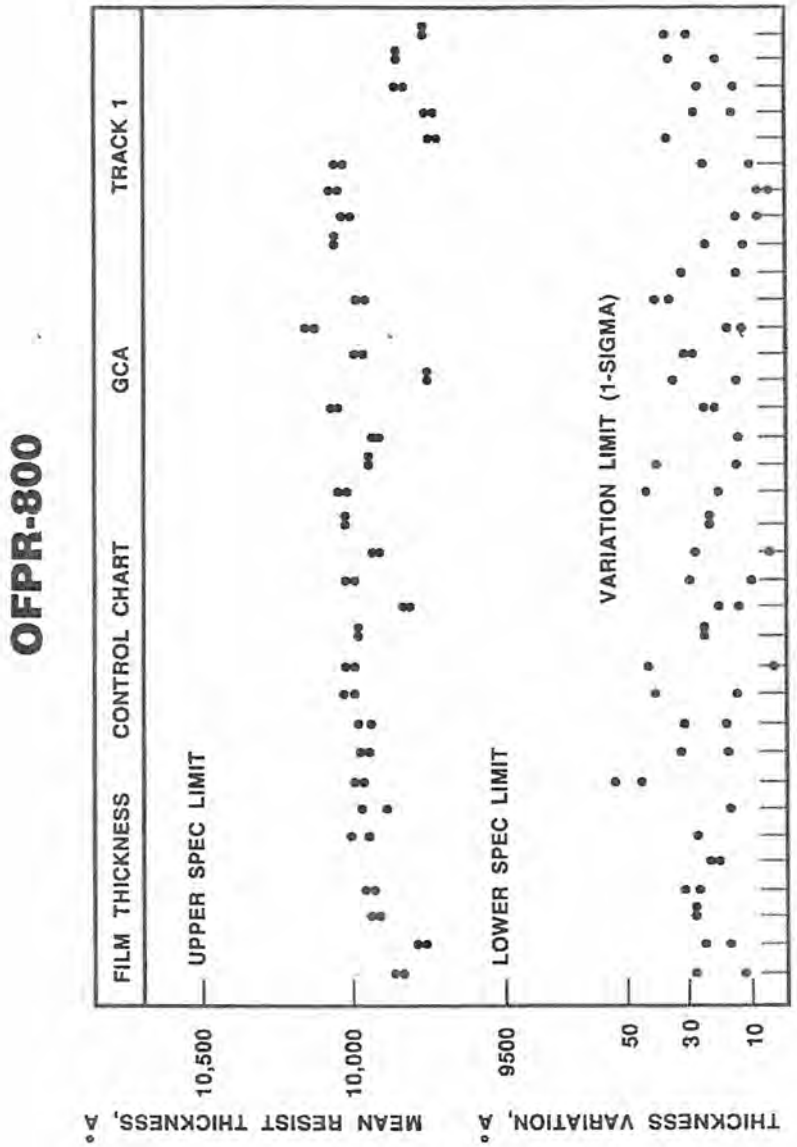


Figure 31. Thickness control chart for OFPR-800.

For positive resists, the prebake conditions, exposure and development conditions are inseparable, and together can critically determine the performance of the overall resist process. For example, sometimes interactions occur between prebake and development variables; a 2-factor interaction between prebake temperature and development method has been observed for Shipley 1400 resist. Due to this interaction, both of these variables would have to be changed in parallel to optimize this resist process. Prebake is almost always a primary variable for positive resists, because their development rates are influenced strongly by residual solvent content and the thermal history of the film. For negative resists, this is not the case--prebake and developer compositions have less influence over resist contrast, but they can impact resist swelling behavior and hence resolution performance. Since positive resists are the evolutional choice of most new fab lines and they are most affected by these variable combinations, this section primarily addresses positive resist effects.

Variables which can influence resist image edge wall, critical dimension control, and resist sensitivity are prebake temperature and time, exposure level, developer composition and conditions, rinse composition, and fab ambient. The effect of developer composition upon CD RPL, sensitivity and contrast were demonstrated earlier in this section. All of these parameters can potentially interact, therefore, statistical engineering methods and experimental designs are invaluable in optimizing the overall resist process.

3.4.1 Statistical Process Optimization Characterization Example. The best way to illustrate a statistically oriented resist process optimization and its efficiency is to provide an example. In this section, a simple OFPR-800 positive photoresist process will be charaterized by generating a CD reponse surface space for the process. From that response, an optimum operating point for the resist process is obtained. Most importantly, after completing the statistically designed experiment(s), we know how the CD response varies over a much larger set of operating conditions than that unique set established as the baseline photoprocess.

Since a resist process has many different substeps, it is impractical to evaluate each variable individually. It is also unwise since the variables may interact. A statistical experimental approach, which investigates many variables simultaneously and can assign quantitative values to variable effects and interactions, is necessary.

The objective of this study was to develop and optimize a process for a photoresist (OFPR-800 manufactured by Dynachem) from both a critical dimension transfer and contrast points of view. Two of the statistical experiments--a 7-factor variable screen(62) and a 3-factor Box-Bhenken(61) response surface investigation--are described in this example. In addition, the track development process employed is characterized for completeness.

3.4.2 Background. The purpose of a variable screen experiment is to determine which of the many variables (independent variables) involved in any process step are significant, that is, which variables the engineer needs to control to optimize the overall process performance as determined by the process parameters (dependent variables). A variable screen design is a small part of a full 2^k factorial(61)(62). It is designed only to determine the significant independent variables in relatively few experimental trials or wafers, and is unable to identify any variable interactions. A full 2^k factorial can determine variable effects and interactions, but requires too many experimental runs to be practical for investigating more than 4 or 5 variables. Designs for variable screens are available in several references(61-63). It must be cautioned, to watch for main variable and two-factor interaction confounding when employing these fractional screening designs.

After identifying the significant variables for a process from a screen design, the final step is process optimization. This involves determining any independent variable interactions (non-additive responses) or non-linearity in the dependent variable response curves. Several statistical designs are available for this type of experiment, but unlike the variable screens are usually based on a full factorial experiment(61) or a higher resolution fractional factorial design. Since fewer variables are investigated, the process optimization experiment yields much more information than a variable screen design in approximately the same number of runs, because now the two factor and higher order interactions are no longer confounded in favor of screening a larger number of primary variables.

3.4.3 Experimental Designs. The resolution III screen design used in this example is given in Figure 32. The procedure for running a variable screen design is to choose two levels of interest for each variable (designated + and -, although they need not be quantitative values), and then run each sample, in random sequence, through the process determined by the screen design. Seven independent variables were examined: softbake time

SEVEN FACTOR SCREEN DESIGN

	PREBAKE TEMP. 70°C 90°C	PREBAKE TIME 60S 120S	POSTBAKE TEMP. 120° 140°	POSTBAKE TIME 60S 120S	U-1000 EXPOS. 0 +20%	SPIN CONV.SPEC	DEVELOPER METHOD MAN TRK
1	+	-	-	+	-	+	+
2	+	+	-	-	+	-	+
3	+	+	+	-	-	+	-
4	-	+	+	+	-	-	+
5	+	-	+	+	+	-	-
6	-	+	-	+	+	+	-
7	-	-	+	-	+	+	+
8	-	-	-	-	-	-	-

Figure 32. Seven factor screen design for searching experimental variables of a photoresist process for significance.

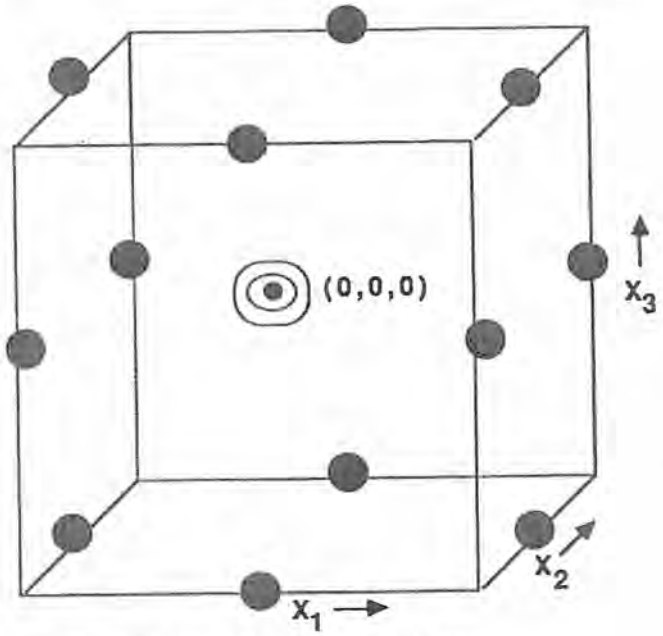
and temperature, postbake time and temperature, exposure, spin method, and development method. The results were quantitatively evaluated based on one dependent variable: resist image linewidth transfer to the wafer. The main variables screened are confounded with three two-factor interactions, therefore, this design will almost always be followed by a response surface design of higher resolution or by a higher order screening design.

The purpose of a process optimization experiment is to study in more detail a small number of variables that are known to be significant in their useful range without loss of precision. Based on the results of the variable screen design described earlier, softbake temperature and exposure were chosen for further investigation. Since this experiment was run with a Perkin-Elmer 544 projection aligner, exposure tool aperture was also chosen as a related process variable to make three total variables. The dependent variables measured were resist critical dimension transfer (sidewall angles: 70-80°) and resist contrast.

The 3-variable Box-Behnken cube design employed is shown in Figure 33. The cube is defined by 3 levels each of 3 variables; the experimental points are determined by the midpoints of the 12 edges of the cube to check for response surface curvature. The center point of the cube is replicated 3 times to provide an estimate of process variability (i.e., the precision of the experiment). The effect of this design is to run a complete 2 x 2 factorial, while holding the third variable at its center point. Since the Perkin Elmer 544 has the capability of exposing a single wafer with a number of different exposure levels, this design actually examined five different exposure levels for each run instead of only three. Other process information is given in Table XIV.

Critical dimension results were evaluated by line and pitch measurements made on the 2.0μ line of a 4.0μ pitch structure. Measurements were made on a Leitz MPV-CD system. The precision capability of this tool was determined to be +/- 0.09 micron (3-sigma), a value less than required for the process tolerance. Leitz measurements of the 1.5 and 2 micron resist dimensions showed a variation of only 5% or less across the 4 " wafer. Individual line measurements were calibrated vs. a sample measured by both the Leitz and a Cambridge SEM.

3.4.4 Developer Process Characteristics. The developer process employed was a NMD-3 metal-ion free spray/puddle process at the fab temperature (70°F) on a model GCA 1006 Wafertrac. The wafer was sprayed for 2 seconds at 100 rpm, followed by a 1 sec. static spray to ensure good puddle



BOX BEHNKEN DESIGN CUBE

X_1	X_2	X_3	
+1	+1	0	
+1	-1	0	
-1	+1	0	
-1	-1	0	
+1	0	+1	
+1	0	-1	
-1	0	+1	
-1	0	-1	
0	+1	+1	
0	+1	-1	
0	-1	+1	
0	-1	-1	
0	0	0	CENTER POINT
0	0	0	
0	0	0	

THREE-VARIABLE BOX-BEHNKEN DESIGN EXPERIMENTS

Figure 33. Three variable Box-Behnken experimental design for probing an experimental response surface.

TABLE XIV: Experimental Conditions

Coat: GCA Wafer Trac 1μm OFPR 800
Hotplate Bake, 45 sec. Temperature = variable

Expose: PE 544 Exposure time and aperture variable.

Develop: GCA Wafer Trac

Measurement: Leitz MPV-CD. CD measured was 2.0μm line on 4.0 pitch structure.

formation, followed by a static 45 sec. development and 30 sec. wafer rinse.

3.4.5 Variable Screen T-test. The data analysis of the experimental design of Figure 32 is performed for each independent variable by subtracting the average linewidth from those runs for which the variable was at its low level (-) from the average linewidth from those runs for which the variable was at its high level (+). This result is designated $Y_+ - Y_-$. Linewidth measurements were made at the center and edge of each wafer.

Theoretically, the result $Y_+ - Y_-$ measures the effect on linewidth of changing the independent variable from its lower level to its higher level. In the real world, however, each process has a certain amount of variability no matter how carefully the independent variables are controlled. One way to insure the results demonstrate a real effect or are significant beyond normal intrinsic process variability is to apply a t-test to the data.

The t-test is used to compare independent sample averages from two populations (in this case, (+) and (-) levels of the independent variable) to determine if the difference between them is statistically significant(64). It works by comparing the experimental result ($Y_+ - Y_-$) to that which should have occurred based upon variability results from either both populations of data or control wafers assuming a t-distribution, which is a small sample approximation of the normal (Gaussian) distribution. The greater the result is from the control wafer population variability, the more likely the result was caused by the independent variable instead of random process variation due to lack of experimental precision. If we choose a given "confidence level" (probability that our conclusion is correct) needed, we can calculate the t-statistic from our results and compare it to the t-table entry for the appropriate number of degrees of freedom and the level of confidence. If the test statistic is greater than the corresponding table entry, then we can conclude that the independent variable is significant (that is, it must be carefully monitored to assure process control) with a corresponding level of confidence.

The test statistic for the t-test is given by:

$$[5] \qquad T.S. = Y_+ - Y_- / Sp \left[\frac{1}{n_+} + \frac{1}{n_-}\right]^{\frac{1}{2}}$$

where, Y_+ and Y_- are as defined before, n_+ and n_- are the number of samples at each level, and Sp is the pooled variation calculated from:

[6] $$S_p = \left[\frac{\sum_i (n_i - 1)\ S_i^2}{\sum_i n_i - 1} \right]^{1/2}$$ where n_i is the

number of replicates at each experimental condition and S_i the cell variation between replicate observed dependent values.

3.4.6 Results and Analysis. The results from the variable screen are given in Table XV. Prebake temperature, develop method, postbake temperature and exposure are all clearly significant in the range studied. Spin method (conventional or special) is also significant. "Special" spin was a method developed to enable easier target detection by the Ultratech stepper alignment system by removing the spread cycle at low rpm and by shortening the final spin dry cycle at the final rpm. Unfortunately, it also resulted in large resist thickness variation across the wafer, which led to the large CD variations illustrated by the values in the table. "Special" spin resist coating has been discontinued for this reason and is not recommended.

Critical dimension vs. exposure results for the 3-factor Box-Behnken design at different softbake temperatures are graphed in Figure 34. Figure 34 shows two possible operating points for the process that will result in a critical dimension within specification: a 75°C softbake with approximately 75 millijoules/cm^2 exposure, or a 90°C softbake with approximately 96 millijoules /cm^2 exposure. The graph also suggests some variable interaction is occurring between 54-75 and 96-116 mJ/cm^2 since the three lines are less parallel over those regions. Aperture had a negligible effect on critical dimension within the range of interest (2.0 µm +/- 10%).

In order to evaluate the experimental results quantitatively, a Yates(65) analysis was performed on the data. The Yates algorithm is a method of taking advantage of the "hidden replication" found in factorial experiments: the average result (critical dimension) of the points at which a certain factor was at its low value is subtracted from the average result of the points at which the factor was at its high value. The result is a more accurate estimate of the actual effect of that factor than would be

TABLE XV: 7-FACTOR SCREEN DESIGN RESULTS

FACTOR	CENTER ISLAND IMAGE CD	EFFECTS (Y_+-Y_-) EDGE ISLAND IMAGE CD
SPIN METHOD	-0.29μ	+0.11μ
PREBAKE TEMP	-0.11	-0.18
PREBAKE TIME	+0.03	+0.09
DEVELOP METHOD	-0.30	-0.30
POSTBAKE TEMP	-0.53	-0.35
POSTBAKE TIME	+0.03	-0.05
EXPOSURE	+0.15	+0.21

CONFIDENCE LEVEL 0.11 A 90% (T-STATISTICS)

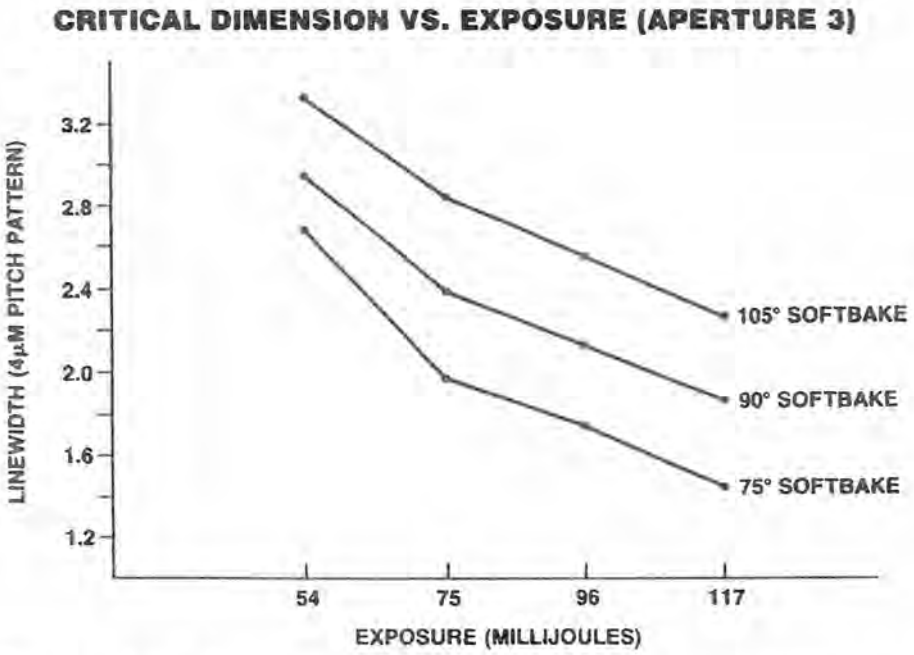


Figure 34. Critical dimension vs. exposure for OFPR-800 photoresist process.

available from only one measurement at the high and low value of each factor. The Yates algorithm is used to check for independent variable significance as well as variable interactions.

A Yates analysis can be performed for two levels of the variables only. Based on the graph shown in Figure 33, those levels closest to our expected working range were chosen. The results are shown in Table XV. The results confirm those inferred from the graph; exposure and softbake are clearly significant variables over the range studied, but aperture has a much smaller effect. All of the variable interactions are small enough to be safely ignored.

Iso-CD response surfaces have been drawn in three dimensions in Figure 35. Roughly speaking, an optimal working point would be near the center of the cube, a result that was not designed to occur intentionally. Note also, the exposure latitude for critical image control falls off rapidly at 75°C prebake, which would make operating at that prebake temperature risky; that is, if exposure unexpectedly changed a little the chance of CD failure would be great.

The second objective of this investigation was to optimize resist contrast where greatest resolution is possible. Since resist contrast also correlates with resist image sidewall angle, it is an important resist processing variable especially as linewidths decrease.

Contrast is determined by measuring remaining resist thickness as a function of exposure for underdeveloped wafers. Hence, exposure cannot be used as a variable in a contrast optimization experiment. Contrast was measured as a function of aperture and softbake, and the results are graphed in Figure 36. Aperture had little effect on contrast, but contrast was clearly greatest at a 75° softbake. Unfortunately, unexposed resist thickness loss was unacceptably high (i.e.,10%) with a 75° softbake. Some loss of process latitude (slope of line) also can be detected in the critical dimension vs. exposure graph at 75° softbake compared to 90° softbake in the exposure range needed for correct image size transfer. Therefore, it was decided to use a 90°C softbake despite an approximately 10% loss of contrast performance as an acceptable trade-off.

3.4.7 Conclusions. These general experimental designs enabled near optimum performance parameters to be chosen for the model photoresist process studied before Statistical Process Control (SPC) methods were implemented to monitor process performance. As a result of this careful process characterization, this process was successfully employed to fabricate CMOS test

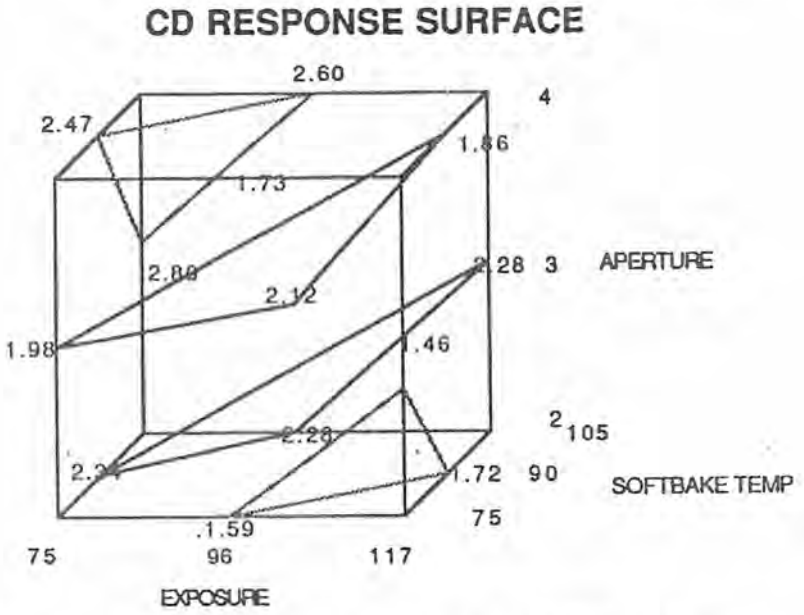


Figure 35. Iso-CD response surface for OFPR-800, generated using a Box-Behnken design.

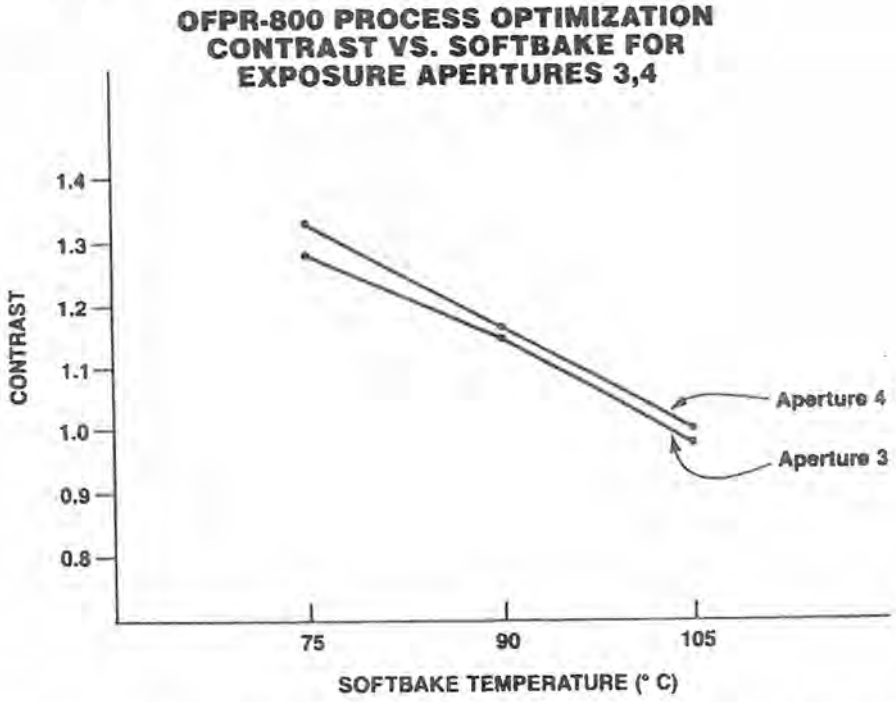


Figure 36. OFPR-800 process contrast vs. softbake temperature from Box-Behnken response surface design.

devices in SPC control over an extended period of time before process replacement with a higher contrast process. The variable screen and Box-Behnken response surface designs allowed a great deal of knowledge to be obtained in actually very few trials. The experimental designs employed were extremely efficient in terms of processing time, wafers used, measurement and analysis time, and with built-in design replication to provide experimental precision.

In the example above, the surface analysis was accomplished graphically, and no computer-aided analysis was employed. If computer facilities are available, regression programs are widely available and are useful in plotting the data graphically to achieve a compromise optimum set of process operating conditions. Other experimental designs, with their own advantages and disadvantages, could have been employed such as the central composite design(62)(66) (see also Chapter 4). All of the designs, however, are capable of providing the tools for successful and efficient process development to the process engineer on the fab line.

3.4.8 SPC Methods of Process Control. After the process optimization, whether it be a resist lithographic process, a coat process or any process, the process must be monitored to ensure it is operating within the specification limits usually dictated by the device design rules. These methods have been well documented(67). Two types of examples are provided in Figures 31, 37 and 38. Figure 31 is a wafer resist coat chart and the other two are CD control charts. In the figures, the spec limits are included for comparison. It must be realized: just employing SPC charting methods does not improve the baseline processes -- this comes through careful process optimization as shown above. The SPC charting methods just provide the data recording format for monitoring the process, and are not able in themselves to influence process quality/stability.

3.4.9 Resist Postbake and Removal. After the resist images have been developed, it is necessary to remove any residual developer solvents to help prevent image flow during post lithographic processing steps and to promote adhesion if wet etching steps follow. This thermal treatment is accomplished at preferably higher temperatures, as long as image flow is avoided. In fact, deep UV treatments (e.g., Fusion Systems)(68) and other plasma(69) and chemical treatments(70) have been reported for improving the post development process compatibility of the resist. For example, the higher the postbake temperature the more resistant the resist is to image flow and reticulation in RIE environments. Deep UV treatments and the other processes usually

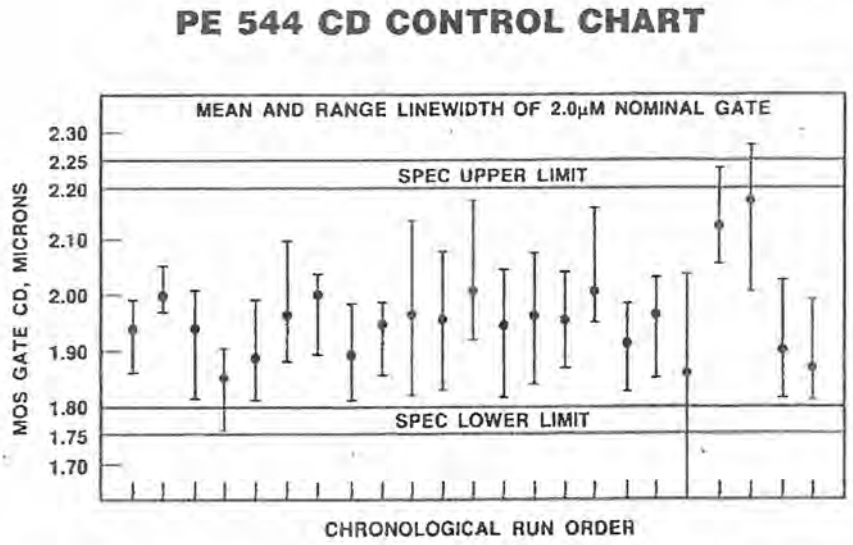


Figure 37. Two micron nominal CD control chart for OFPR-800 process using a Perkin-Elmer 544 projection printer (UV-4) as the lithographic tool.

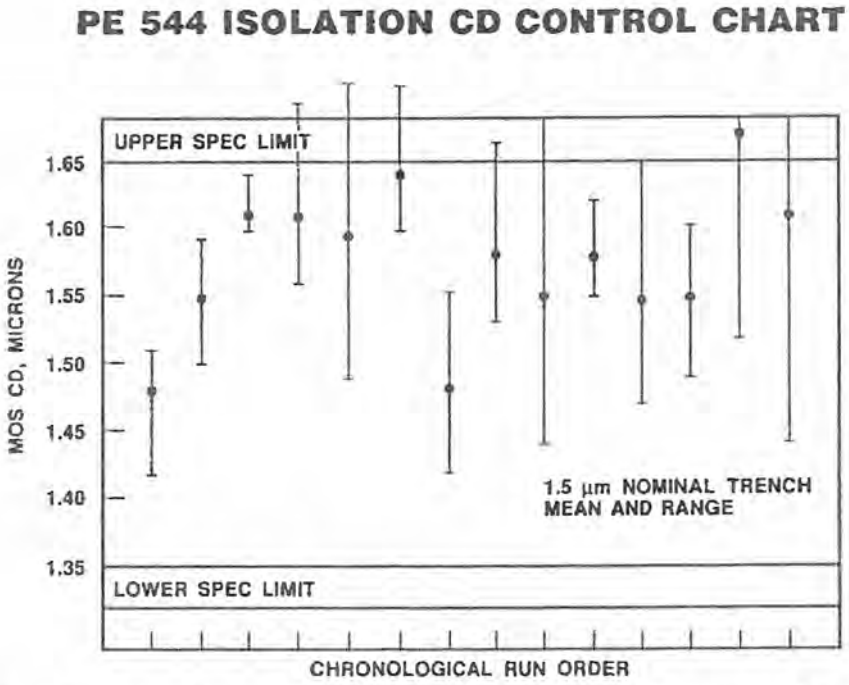


Figure 38. One and a half micron nominal CD control chart for OFPR-800 process using a Perkin-Elmer 544 projection printer (UV-4) as the lithographic tool.

allow higher postbake temperatures, hence, improved post development process compatibility.

Finally, the resist must be quantitatively removed from the substrate after each IC processing step -- it does not become an integral part of the vertically layered fabricated device as does patterned dielectric and metal layers. It functions only as the circuit specific patterning vehicle for layers which are not directly patternable themselves , and after that processing must be easily removed. This stripping can be accomplished by a variety of wet and dry oxidizing processes such as chromic-sulphuric acid mixtures, hydrogen peroxide mixtures, organic strippers, and oxygen rich plasma systems(71). (Also see Table XII.)

At first glance, this final process appears rather unimportant. But, recent results have been reported where plasma oxidizing removal techniques may deleteriously affect device performance(72) and many fab lines are discontinuing their use. One must be careful then to investigate the effects of these stripping processes upon device performance and /or surface contamination to further processing.

4.0 APPLICATIONS AND SPECIAL PROCESSES

4.1 Future Device Demands

Integrated circuit lithographic design rules have historically decreased over time, and will continue to do so -- at least to the 0.5-0.8 micron level over the next 2-5 years. The driving forces for these increased circuit packing density demands are cost per function decreases, faster switching speeds, and lower chip power consumption. These new design rules will necessitate either higher resist or lithographic tool resolution performance or both, as well as, anisotropic fine line etching technology. Since the etching technology exists and tool contrast is only improved by the purchase of expensive new equipment, the goal for some process engineers simplifies to one of improving resist process performance. The processes in this section address this issue. Quoting L.F. Thompson of AT&T Bell Labs, "it's all in the processing." Resist processing is really the only variable left to most lithographic engineers with which they can influence device production, because the photolithographic tool aerial image limit is basically fixed by the manufacturer.

Conventional single-level positive photoresist technology has recently progressed rapidly, especially in the mid-UV class,

but may be incapable of providing the necessary resist imaging required for the next generation of chips. Here, resist imaging thickness is the key issue to meet RIE etch masking requirements. Therefore, new resist processing technology may be needed. Furthermore, processes which extend the performance levels of existing projection exposure tools or provide depth of focus relief are very attractive due to the increasing cost of new higher performance exposure equipment and the return on net asset demands placed upon sales of new devices to pay for these tools.

While a great deal of resist process research has been occurring to extend phototool lifetime, advances in reduction lens design and reflective optical wavelength reductions have also been occurring. As a result, optical lithography is relegating direct-write e-beam lithography to a quick turn around Application Specific IC (ASIC) role, and extensive X-ray lithography usage has been delayed years. The advanced processes in this section will address both optical and e-beam future needs only; it is assumed the e-beam processes would also be extendable to X-ray, assuming high X-ray flux.

4.2 Applications

4.2.1 Dyed and Thinned Single Layer Resist (SLR) Processes. The first and most obvious thing to do to improve resist performance on the most difficult substrates (those requiring greatest resolution or those with reflective topography as for metal or some polysilicon levels) is to reduce the resist thickness or add dyes to it, respectively. The resulting dyed and usually thick (~2 microns) material is still a single level resist process, but without the added complexity of multi-level processes. Unfortunately, resist thinning is most feasible with multi-level processes and thinning accomplishes nothing towards reflective image notching relief, the main observed problem for reflective topographical situations. Furthermore, resist thinning presents a severe problem to step coverage and metal etching because of poor selectivity, and is in fact usually prohibitive. All of these negatives aside, resist thinning has been shown by IBM researchers(73) to improve linewidth control by 15% and focus control by 35%, when and if it is feasible to do it. The latter value further reinforces the restrictive applicability of resist thinning to multi-layer processes.

The more practical solution to reflective notching problems on reflective surfaces is provided by resist dyeing. Most device areas will select this option over multi-layer Portable Conformable Masks, PCM (3), processes (see Figure 39). Dyeing

Figure 39. Multilayer resist systems illustrating different multilayer processes and PCM techiques.

resists requires a price be paid in resist contrast(74) and exposure time(75), but dyeing does provide greater process latitude (see Table XVI) and reflective notching can be effectively eliminated(76) or at least minimized. Sandia workers(77) have provided a dye system for H and G line steppers which has a very small exposure penalty, just 15 mJ/cm^2. Bolson et al.(76) have demonstrated similar results and an approximately 60% gain in exposure latitude was achieved or a reduction in K from the Raleigh resolution equation from 1.1 to 0.6 was effectively obtained. On the negative side, adding dye to the resist formulation leads to a larger standing wave foot(78) and reduced image edge walls (see Figure 40) consistent with the observed bulk contrast reductions reported by Pampalone. Most dramatically, Brown and Arnold(78) have observed a 3-fold increase in CD exposure latitude, a result which explains the wide acceptance of this technique for metal layer lithography by development and production fab lines.

4.2.2 Image Reversal (IREV). Positive photoresist image reversal (i.e., negative toned imagery from a positive toned resist) is a new processing technology which addresses the deficiencies of dyed resists. Moreover, IREV can be accomplished on dyed material to achieve the best of both worlds, namely, relief from topographical or bulk effects and reflective notching minimization. Over the past five years, many papers have been published on this subject(79-87). The salient contents of those papers will be reviewed and compared. The main focus of this section is on single level thermal and base induced reversal processes for AZ 5214 and the Genesis Star image enhancement process for Shipley 1400 positive photoresists, respectively.

Image reversal is an alternative to conventional positive photoresist technology. Briefly, a single layer of positive photoresist is exposed using a projection aligner, reversed by either doing a post exposure thermal treatment on a hotplate or by adding a base to the resist, flood exposing and developing. The result is a negative toned image with a controllable edge wall angle, something dyed resists with conventional processing cannot deliver. The IREV processes are capable of printing images previously unattainable with the given exposure tool, thus, extending the resolution and focus latitude performance of the alignment tool, and the life of it as a capital asset.

4.2.3 Thermal Image Reversal. Marriott, Garza and Spak have written the definitive paper on thermal image reversal(86). Using both theoretical PROSIM simulation and empirical methods, the AZ 5214 IREV process has been

TABLE XVI: DYED PHOTORESIST RESULTS TABLE*

RESIST	OPTICAL CONTRAST	Q mJ/cm^2	RPL	DEVELOPER/MODE
OFPR 800 ON SILICON	1.3-1.6	104 (135)	1.0	NMD-3 (2.7%)/PUDDLE
OFPR 800 ON AL	"	20-88	1.6	NMD-3 (2.7%)/PUDDLE
OFPR 800 ON AL: TRILEVEL	"	123 (165)	1.1	NMD-3 (2.7%)/PUDDLE
OFPR (AR-15 DYED) ON AL	1.0	73	1.2	NMD-3 (2.7%)/PUDDLE
OFPR (MOTOROLA DYED) ON AL	1.1	166	0.9	NMD-3 (2.7%)/PUDDLE

* ULTRATECH 1000 STEPPER UTILIZED FOR TESTING

Figure 40. Edge wall profiles of heavily UV-3 dyed AZ-5214 to illustrate standing foot and poor edge wall angles consistent with low observed bulk contrast values.

optimized, and good agreement between theoretical images and real images obtained. The process was optimized for photospeed, resolution, focus and CD latitude, and vertical edge wall by adjusting the developer concentration to 0.21 N MF-312 (90 secs), setting the PEB temperature to 110 C, and by using a flood exposure after PEB. This data has been independently verified at Motorola (see Figure 41). An improvement of 1.25 micron in focus latitude, 150% improvement in CD control and a 8^{o} improvement in image edge wall were also reported(86). AZ researchers further reported a bulk contrast performance improvement of roughly 200% for IREV AZ 5214 over that for the positive performance mode. Consistent edge wall imagery improvement can be seen when comparing Figures 41 and 42, where Figure 42 portrays images with edge wall angles more typically observed from normal positive tone performance.

4.2.4 Base Reaction Process. Two types of base-induced positive photoresist image reversal processes have evolved, one where the basic chemical is added to the photoresist formulation prior to wafer spin(79-81,84), while the other involves a gas phase ammonia treatment of the wafer coated with the exposed resist film(82).

The mechanistic and theoretical treatments of image reversal photoprocesses are detailed in references 80 and 83. In summary, the chemistry of both processes involves a base catalyzed thermal decomposition of the indene carboxylic acid photoproduct. Following this reaction and a flood exposure of the wafer, subsequent aqueous base development with conventional developers leaves a negative tone image in the exposed area, where indene product is rendered insoluble. Development occurs in the unexposed area because the flood exposure converts the resist in that area to the normal photochemical intermediates which are base soluble (i.e., the resist functions conventionally in these areas). The two processes differ only in the process sequencing. With the chemical additive process, the thermolysis is carried out independently before flood exposure, while the vapor process carries them out simultaneously.

Two commercial microprocessor controlled vapor phase systems have evolved from this technology, the Yield Engineering (YES) Model 8 system and the Genesis ST-A-R 2001/2002 system. The YES 8 system delivers anhydrous ammonia gas to a heated stainless steel reaction chamber, while the 2001/2 system delivers a fresh controlled vapor fill to the temperature controlled and profiled reactor chamber every wafer load from a liquid amine decomposition subsystem.

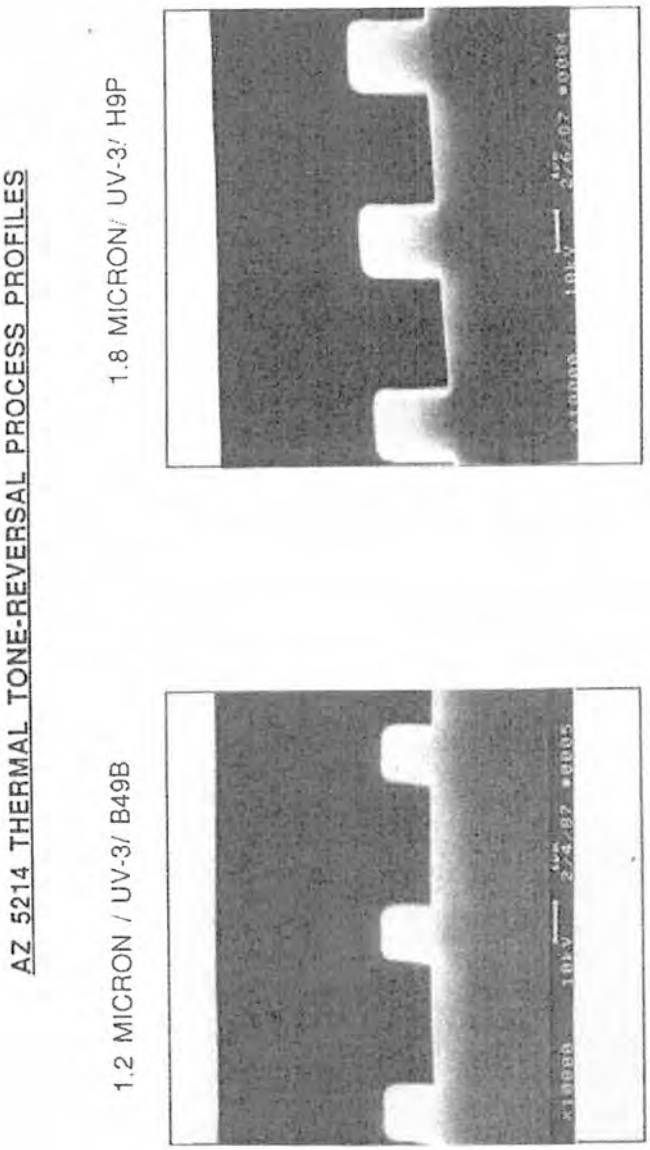


Figure 41. AZ-5214 thermal tone reversal process edge wall profiles illustrating vertical edge walls.

Figure 42. Edge wall profiles for conventionally developed positive photoresist images. Note, the edge walls are poorer than those for both IREV processes.

The systems vary in cost dramatically due to the base delivery technique, quality of materials and profiled temperature control systems. The ST-A-R system has sophisticated vapor delivery plumbing, combined with three zone balanced cascade temperature control and gas manifolding. YES 8, on the other hand, is a low cost system where the manufacturer claims the usage of 100% ammonia gas alleviates the control systems required for the liquid amine delivery system and the need for more exact temperature control. Although the systems differ considerably, both manufacturers claim good concentration and temperature control, low particulate contamination (YES; 5 1-micron particles/5" wafer), and good overall process performance.

4.2.5 Base Tone-Reversal Process Comparison. The solid phase base additive reversal systems reported in references 79-81 suffer from two basic problems. They generally suffer from low shelf-life(84-85) and poor resist image thickness and critical dimension uniformity across the wafer, wafer to wafer, and lot to lot. Inconsistent and sometimes incomplete reversal results were also reported in reference 81; these phenomena have been empirically verified. In addition, the base additive systems mix poorly, which probably contributes to the observed performance problems.

The vapor reversal systems are superior in these respects(82-85), and exhibit manufacturing compatibility if reduced throughput is acceptable; that is, two more processing steps are required with the commercial reversal systems vs. conventional processing. The two types of reversal processes differ mechanically only by the need to mix the additive formulation every 1-3 weeks due to shelf-life considerations, which raises concern about the overall manufacturability of that type of process, independent of irreproducibility effects(85).

4.2.6 Process Tuning. The vapor base IREV process discussed here in detail is basically the evolutionary culmination product of the efforts of references 79-82, but with further careful process and equipment optimizations carried out by Genesis researchers. The optimum time and temperature for the reversal reaction were determined to be between 30-90 minutes and 90-110°C, respectively(79-83). Of course, higher temperatures are precluded due to photoactive component thermal decomposition, and lower temperatures precluded by incomplete reversal reaction. Reference 83 clearly demonstrates the improved process contrast provided at 100°C reversal temperature. Since the remaining resist image thickness is basically invariant over these processsing ranges, other

development and exposure considerations dominate the reversal behavior over these time and temperature ranges (discussed later). The final process variable level selections were made on the basis of greatest observed process contrast/resolution.

4.2.7 Resist Image Edge Wall Angle. Initially, work at Motorola on image reversal was focused upon developing a process that yielded vertical resist edge walls for resolution and RIE etching requirements. A series of wafers was run varying prebake temperature, exposures, and development time, to establish a "ball park" process. From the results of these tests and the unpublished work of others, a lower prebake temperature (70°C), shorter hotplate prebake time (30 sec.), and higher flood exposure (470 mJ/cm^2)(83) were found to yield vertical resist image edge wall profiles and 1.25 micron line-space reproduction fidelity.

With this foundation, a study was completed to determine a first iteration on first exposure and development time process parameters. An array of wafers was processed varying both first exposure and development time. The GCA Wafertrac spray/puddle method of development was employed because of its ability to deliver a uniform, reproducible, and accurately time-controlled puddle. Plots of first exposure and development time on critical dimensions show the widest exposure and development latitude at 160 mJ/cm^2 and 45 seconds, respectively. It is important to note, image CD's change less with development time increases the greater the initial imaging exposure level. A SEM cross section of a sample with these process parameters exhibits the required 90^o edge wall angles (see Figures 16 and 43). As a result, these values were chosen as the optimum processing parameters for futher evaluation of processing effects upon process reproducibility. These values also represent a compromise between process latitude and throughput. The selection preference of an initial exposure level greater than 150 mJ/cm^2 was previously reported in references 81, 83, and 85. All three studies demonstrated the plateau behavior in remaining reversal image thickness at initial exposure levels greater than 150 mJ/cm^2. The dependence upon post reversal flood exposure level is discussed below.

4.2.8 Resist Contrast. A comparison of resist contrast was carried out between the standard S-1400 positive process and the image reversal process. The reversal process demonstrated a contrast of 2.2 (Figure 44), while the positive process only yielded a contrast of 1.6. These findings are very significant as resist contrast, resolution, and edge wall angle are related and

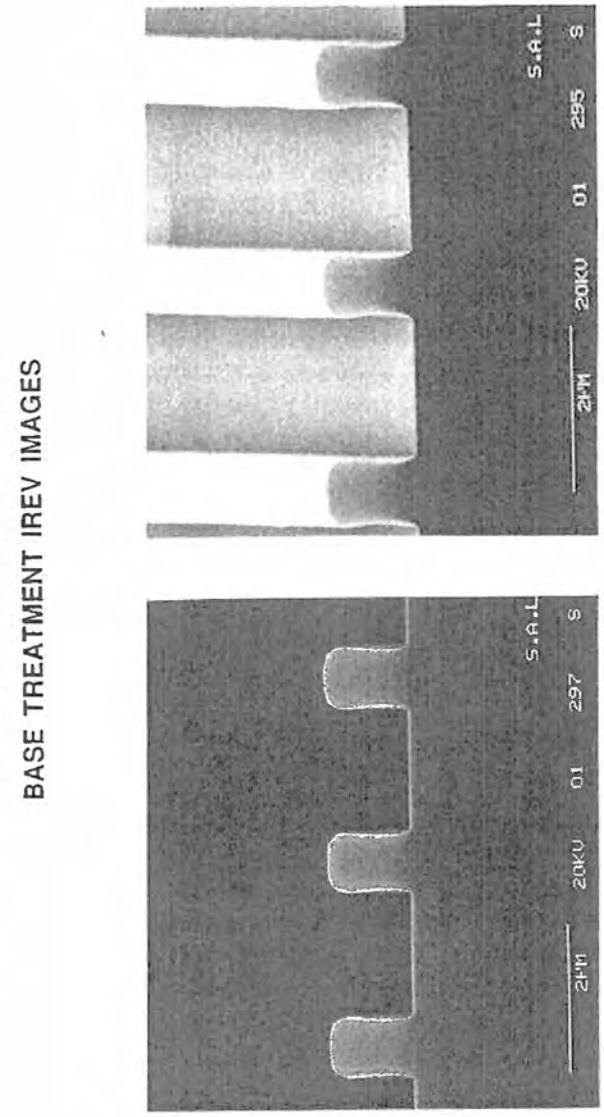


Figure 43. Base IREV process image edge wall profiles.

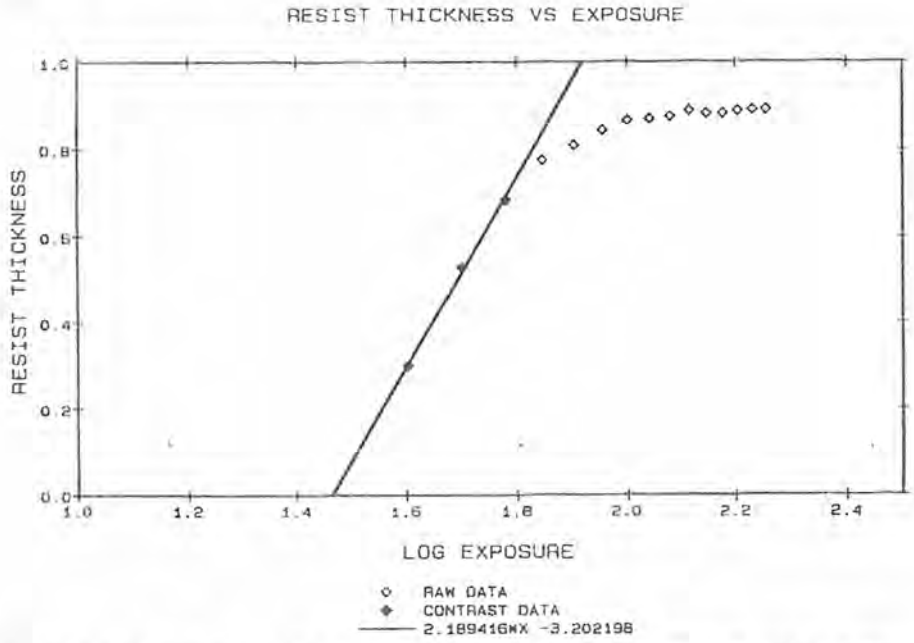


Figure 44. Contrast curve for base IREV Shipley 1400 resist process.

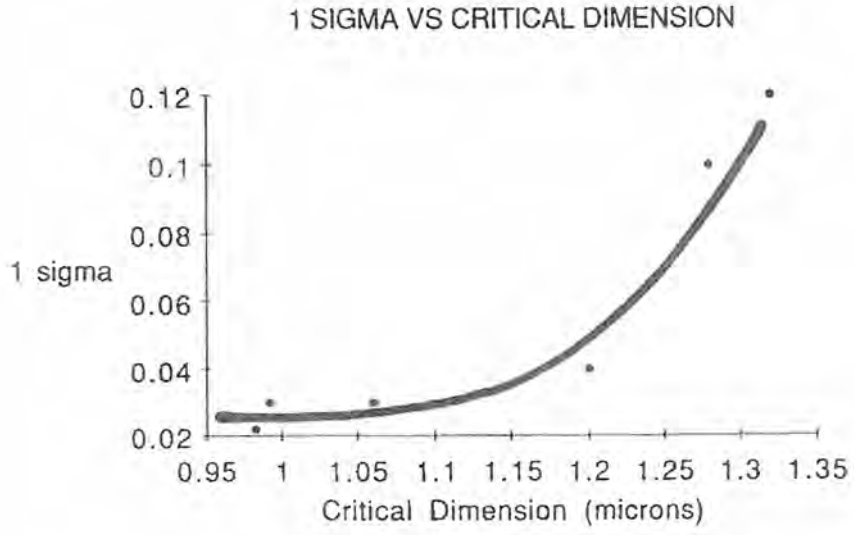


Figure 45. Base reversed process CD variation (1 sigma) vs. critical dimension for Shipley 1400.

well correlated(88). Contrast was previously compared for the IREV processes above in reference 82. There values of 2.38 and 1.18 were reported, respectively; it must be noted that different developers were employed. The effect, however, is still quite clear-- the image reversal process is the superior process in terms of contrast or resolution. No quantitative bulk contrast values were reported in reference 83, but the characteristic curves for the image reversed data are visually much steeper than those for the standard process, again, consistent with results cited and those of reference 83.

4.2.9 Process Latitude and CD Reproducibility. The development latitude for the image reversal process increases with increased first exposure level. At these exposure levels and greater, the reversal process becomes like that for conventional negative photoresist processes in that they can be overdeveloped with minimal impact upon CD. For normal positive resist processes this is not the case, and development times must be well-controlled for satisfactory CD performance. At lower first exposure levels, image CD's of the reversal process are more affected by development time than at greater exposure levels.

The exposure latitude (i.e., for 1st exposure) was measured for the reversal process, and the results compared to that for the normal photoprocess. Values ranging from 0.003 to 0.006 (160 mJ/cm^2) vs 0.015 micron-cm^2/mJ were observed, respectively. The resistance to CD change with exposure is 2.5-5X better for IREV. When first exposure values >160 mJ/cm^2 are employed, as in refs. 81 and 83, even better exposure latitude is observed. Thus, the base reaction reversal process possesses more than 2.5X greater exposure latitude, which translates to greater process control.

Within lot CD variation has been characterized for the base image reversal processes in references 82, 84, 85 and 89. In the earlier work(82,84), 3-sigma values of +/- 0.27 and 0.32 micron were reported for the early ST-A-R process and the Monazoline(79) additive and "Lift-off" process(84), respectively. With improved processes and equipment, came better CD control results: 0.08(85), 0.04(89), 0.08(90), and 0.06-0.09 micron for this work (see Figure 45). These latter values are far better than the typical values observed for conventional positive resist processes, which usually have values closer to those of the earlier image reversal numbers above. With the lower sub-0.1 micron 3-sigma reversal process CD variation values, the next-generation VLSI circuits should be manufacturable with reasonable yield.

A series of lots were processed according to the optimum process parameters to determine the reproducibility of generating vertical resist edge walls and critical dimension die to die, wafer to wafer, and lot to lot. Die to die uniformity for critical dimension consistently exhibited a 3-sigma value of less than 0.1 micron, and with vertical edge wall angle. Unfortunately, small to moderate deviations were sometimes found lot to lot. Figures 45 and 46 illustrate the correlation between critical dimension and both critical dimension deviation and edge wall angle.

Due to the significant deviations of critical dimension from lot to lot, two-level 7-variable resolution III screen designs were employed to determine the variables affecting linewidth variability. Of those variables screened, development method (Wafertrack vs manual puddle), mask orientation (0° vs. 90°), first expose to ST-A-R image reversal storage time (2.5 hrs. vs. 20 hrs.), and post-flood exposure storage temperature (20° vs. 30°) did not significantly affect critical dimension control. The two remaining variables, mask type (i.e., chrome reflectivity) and HMDS vapor treatment system did reproducibly cause significant linewidth differences.

4.2.10 Mask Effects. Differences in resist image CD transferred to the wafer, as a result of mask type, were quite substantial. Lines of 1.25 micron exposed using the bright chrome mask (BC mask) transferred to an average of 1.00 micron after image reversal. Those same lines exposed using an anti-reflective chrome mask (ARC mask) transferred to less than 0.6 micron after image reversal. This effect can be attributed to the additional exposure received by the resist due to reflections at the chrome space interface on the mask. This effect reinforces the fact that a greater first exposure increases line size, and suggests mask pattern size biasing must take chrome type into account at mask fabrication, but this is already done routinely, and should not be an additional burden of consequence(91).

The image reversal processes of this chapter are capable of 1) extending the effective resolution of the projection lithography tool utilized, 2) providing vertical edge walls for dry-etch considerations, and 3) providing superior resist image CD control vs. that of the resist when used in the conventional positive mode. Consistant with these observations, reference 83 further provides evidence of improved tool depth of focus with this process. The edge walls observed here and in references 83-85 have been theoretically accounted for in references 83 and 86 on the basis of image edge photoactive species concentration gradients, and the mechanism of the reversal processes beautifully delineated by MacDonald et al.(80).

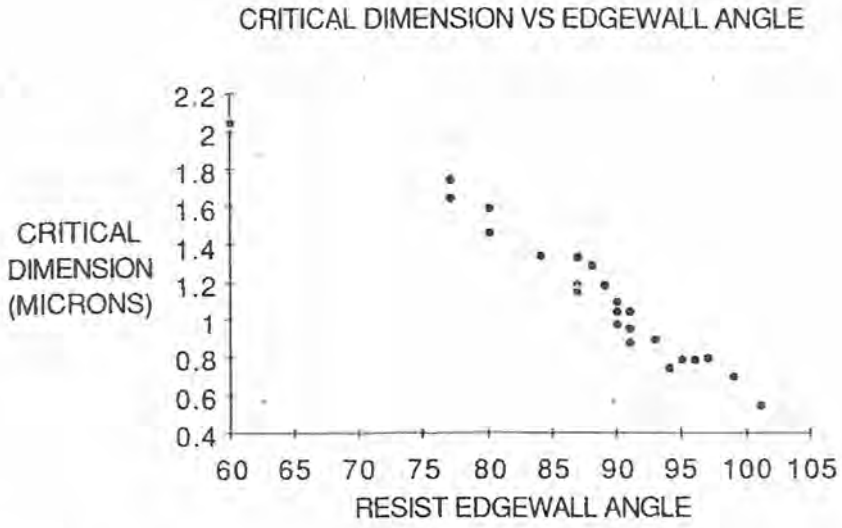


Figure 46. Critical dimension vs. edgewall angle for Shipley 1400 base IREV photoprocess.

As with any processing situation, image reversal processes have trade-off disadvantages to go along with the depth of focus, image contrast, CD control, and resist image edge wall advantages. Initial device level exposures must be equal to or greater than 2-3X normal levels. In addition, two other wafer throughput reducing processing steps must be added, namely, the vapor treatment and flood exposure steps. These disadvantages, coupled with the added one of greater sensitivity of IREV to optical proximity effects will most likely prevent widespread application of these processes to volume production.

All in all, it is felt the image reversal process advantages may overshadow the disadvantages for certain critical device fabrication levels, where standard resist processing technology simply cannot satisfy the future lithographic imaging requirements. Furthermore, recent work(90) has demonstrated image reversal behavior for dyed positive photoresist without degrading edge wall slope advantages, thus providing a process with relief from integrated standing wave and pattern scattering effects in addition to the relief from the bulk effect provided by the undyed reversal process.

4.3 Multi-layer Applications

4.3.1 Summary of Need. Multi-layer processing techniques, where layers of radiation sensitive (top), non-photosensitive organic, and/or inorganic materials sandwiched together to become the total patterning layer, have become common in semiconductor and computer manufacturing R & D labs. (See Figure 39)(3). Due to their complexity and problems that have appeared at bi-layer interfaces, these techniques have not been widely accepted in high volume production. Here, multi-layer resist processing techniques will be reviewed with emphasis upon problems associated with interfacial phenomena occurring between layers, especially for bi-layer systems.

Photolithography image edge and dimension quality is limited by two basic effects, bulk and substrate reflectivity (92,93). The bulk effect arises when lithography patterns are required at two different topographical layer levels of the vertically-fabricated monolithic circuit. Reflectivity effects occur when patterned areas of the circuit have different reflectivity coefficients, as well as topographical levels.

Lithographic exposure tool resolution performance can be influenced by resist processing. Stover et al.(94) have shown K from the resolution equation, $R = K\ wl/2NA$, is directly influenced by multi-layer processing: wl is the monochromatic

light wavelength and NA is the numerical aperture of the projection optics lens system; K is typically 0.8 in manufacturing with single layer resist processes but can be as low as 0.5 with multilayer processes(95). Linewidth control is also directly affected by resist processing, and greater resist image critical dimension control can be achieved through multi-layer processing(93) combined with anisotropic reactive-ion etching technology.

Lin(96) has done extensive research in bi-layer systems, multi-layer processes utilizing a UV sensitive material on top with a DUV absorbing or non-absorbing system underneath. This type of multi-layer system has seen limited circuit fabricaton application, because it is plagued by deleterious interfacial layers formed between layers at coat(93,97). These problems have been solved by various treatments both before and after image formation, but bi-layer technology has taken a backseat primarily to dyed thick single-layer photoresist processes(76). Some bi-layer processes are reported to be free of interfacial mixing problems(98), but the processes described later will all be free of this yield-killing potentiality.

Tri-layer systems(99) utilize an intermediate layer between the photosensitive top layer and the virtually developer-insoluble oxygen RIE patterned bottom layer. It is usually deposited by low temperature (<250°C) thin film deposition techniques, but can also be applied as a liquid spin-on-glass solution(100-2). The middle layer can also be a spun organic polymer (also water soluble) barrier layer coating for the lithographic tri-layer processes, as opposed to RIE tri-layer processes where the middle hard mask material must be RIE etched and cannot be developed by base developers or water. While the former technique is usually void of interfacial mixing layer problems, the latter technique can exhibit this problem intermittently.

All of the multi-level processes described are successful to some degree in relieving resolution and linewidth control limitations of current single-layer optical exposure equipment. Future device fabrication requirements and the application of high numerical aperture exposure equipment, however, will most likely create the need for multi-layer processes at one or two critical device levels, and the interfacial phenomena occurring in some of these systems will have to be well understood before these needs materialize in the 1990-92 timeframe.

4.3.2 Tri-layer Gate Processes (see Figure 39). Two tri-layer processes, one an RIE and the other lithographic, have seen a lot of activity in research fab areas over the last few

years(99-100) and at Motorola. The lithographic tri-layer process involves contast enhancement material, CEM(103-5), manufactured by General Electric(now Huls), which is a high extinction coefficient nitrone dyed bleaching layer, and I-line stepper patterning. The other process involves RIE image transfer to the substrate and e-beam lithography exposure. These processes will be used as illustrative examples and are described below.

The lithographic tri-layer is composed of a conventional resist bottom layer (e.g., Kodak 820, etc.), a water soluble poly(vinyl alcohol) barrier middle layer to prevent interlayer mixing as reported for bilayer systems, and the nitrone dyed CEM 388 top layer(106). The top CEM layer is applied at 0.5 micron for depth of focus latitude relief created by the poor depth of focus (DOF) dictated by the 0.42 NA I-line lens (DOF = +/-0.5 micron). The process provides vertical edge wall images in the bottom layer (see Figure 47) following CEM and barrier coat strip on a wafer track with CEM organic stripper and water, respectively, and a normal immersion development and rinse of the bottom resist layer. The only added process steps are the two added coat and strip processes, but the image edgewall gains and CD control are substantial.

The CEM process CD control at 3-sigma for a 0.6 (gate) and 0.5 micron (trench) CD's are 0.11 and 0.10, respectively. This control compares favorably to the single layer comparison numbers in the ≥0.25 micron region. When CD variations are small as for this process, they allow some total overlay tolerance to be given to registration, thus providing improved total overlay performance. This is visualized in Figure 48 where the overlay of vias and metal layers is shown; the total overlay of these two circuit layers depends upon the alignment accuracy between the levels as well as the metal and via CD's and their process CD variations. The CEM process also actually allows the employment of the I-line stepper at CD's about 0.15 micron below the single layer Raleigh limit of the tool; this occurs because the CEM process increases the contrast by a factor of 1.6 over the single layer contrast value for AZ 5214 and a factor of 2.9 over the Kodak 820 reference value. Stated another way, it allows tool operation at a reduced K factor.

RIE tri-level processes are used in e-beam lithography primarily to provide relief from proximity effects, which occur from cooperative exposure from nearby pattern backscattered electrons (see Figure 49), and for RIE etch selectivity advantages. A 0.5 micron tri-level gate processing sequence is shown in Figure 50. Greeneich(107) has demonstrated the dramatic reduction in backscattering coefficient and the improvement of

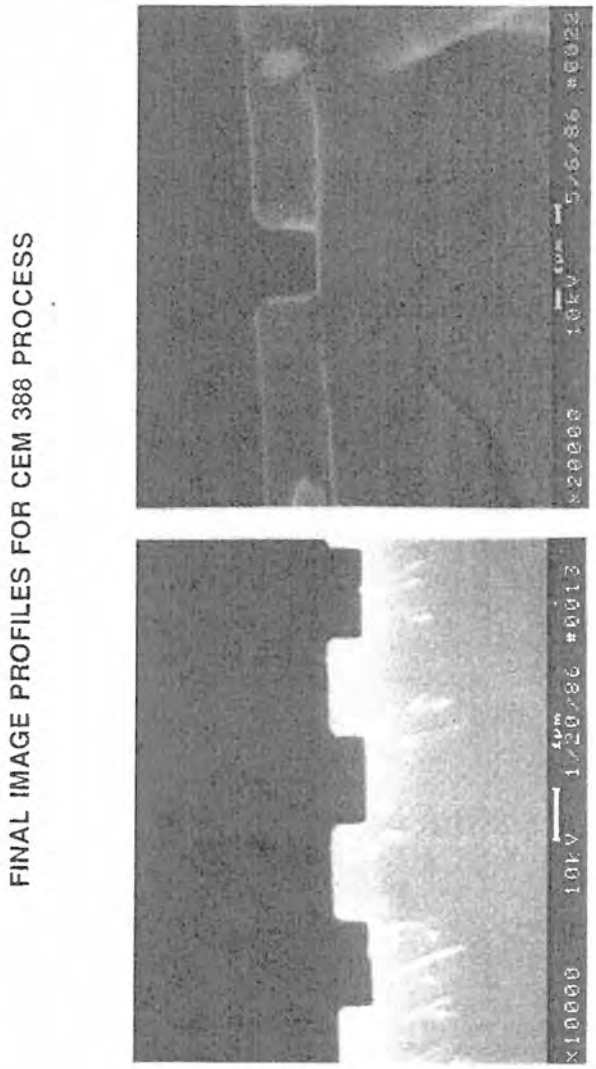


Figure 47. Edge wall profiles of the final resist image for the lithographic CEM tri-layer process. The bottom resist is Kodak 820.

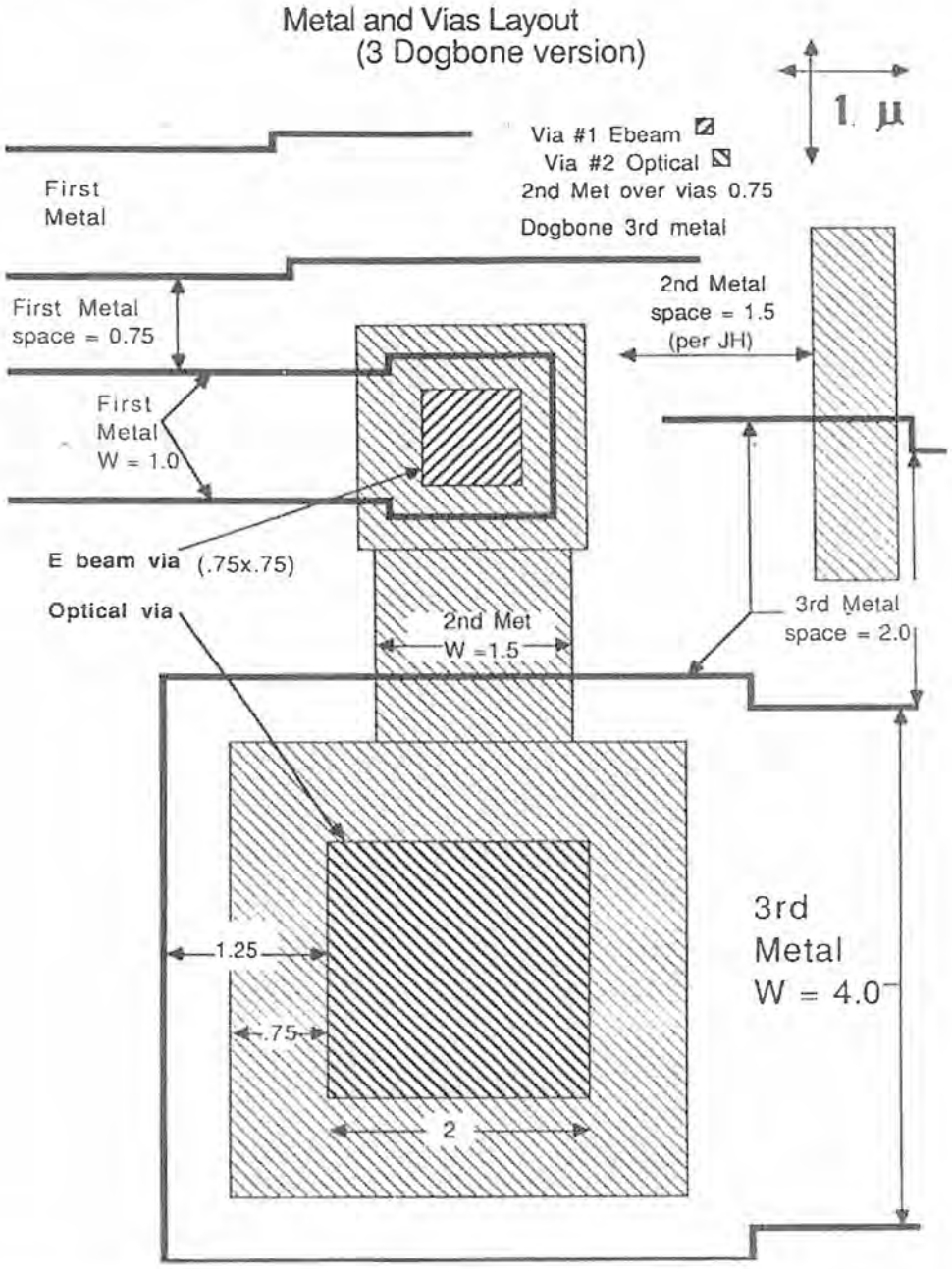


Figure 48. Metal and device level layout for hypothetical circuit. Note, the overlay tolerance would depend upon the level to level alignment and CD variation in an RMS fashion.

PROXIMITY/THICKNESS EFFECT

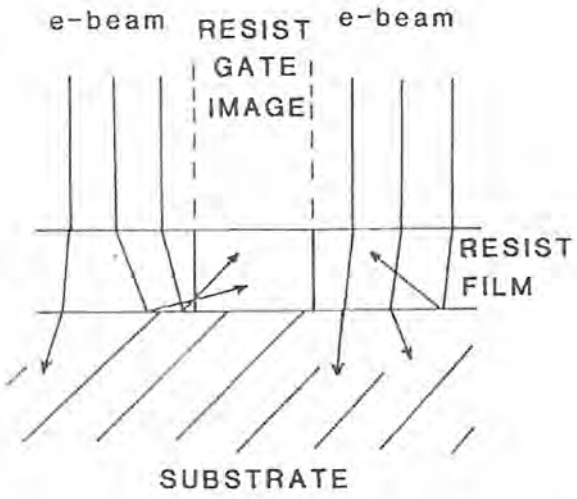


Figure 49. Proximity effect illustration for electron beam lithography cooperative exposure from adjacent written patterns.

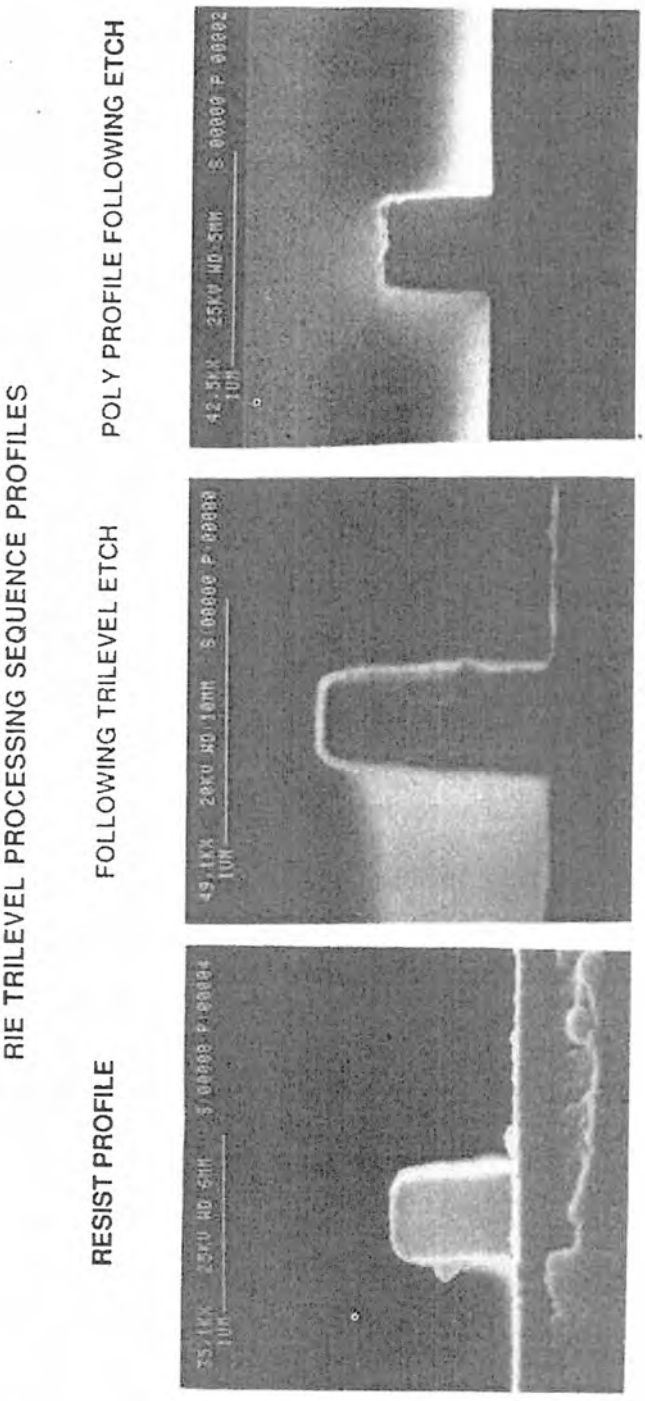


Figure 50. Edge wall profiles for gate lithography process.

image profile when a two micron thick planarizing layer is employed as the bottom layer. When employed as a photo process, this layer is usually a novolac or polyimide (PI) layer that can be dyed as seen for SLR processing for notching relief. For example, Bruce et al.(73) report a reduction of 30% in linewidth variation and increased depth of focus by employing a dyed PI which reduced substrate reflectivity to 4% from 33%. When the bottom layer is a conventional photoresist and is baked at high temperature, say 250°C, the bottom layer loses optical tranmission (e.g., for Hunt 204 T=0.25 at 405nm; Figure 51). Hence, even without dye the bottom layer benefits the optical lithography as well. This very process was used successully for CMOS gate and metal patterning processes employing an Ultratech 1000 1X stepper; the required 1.5 micron gate and 1.75 micron metal patterns could not be satisfactorily completed by a second generation SLR process at that time due to the reflective interference from the substrate.

When the middle layer of the tri-layer is a hard oxide layer, deposited by an ASM plasma-enhanced LPCVD unit , the process complexity is significant over SLR processing. Spin coatable intermediate layers are, however, available(100-2) thus allowing all layers to be applied by wafer track spinning. Unfortunately, some of these glasses do significantly undercut or etch during top layer development, so caution is advised with these systems. The top resists can be conventional photoresists or negative e-beam resists. When they are thin conventional resists, relief from lack of focus tolerance from high NA steppers and improved resolution is obtained.

Typical CD variation control for a tri-level gate process, using Alpha-methyl chloromethyl styrene (AMCMS-S) negative e-beam resist, is 0.05 (3-sigma) micron for the nominally written 0.5 micron gate, where the average gate dimension varies from 0.48 to 0.55 micron, lot to lot. When a positive resist, Hunt WX 214, is employed for delineating a device isolation pattern with the same RIE tri-level as above for the gate example, the CD control is typically worse at a mean = 0.57 +/-0.12 micron 3-sigma. Fortunately, the gate dimension is held tighter; this is essential to CMOS device performance because the gate length actually controls device performance.

4.4 Future Processes

With the advent of the extension of optical lithography to shorter wavelengths and higher numerical apertures to resolution values approaching 0.3 micron, the future processing needs will surely be in the multi-layer or in the surface sensitive

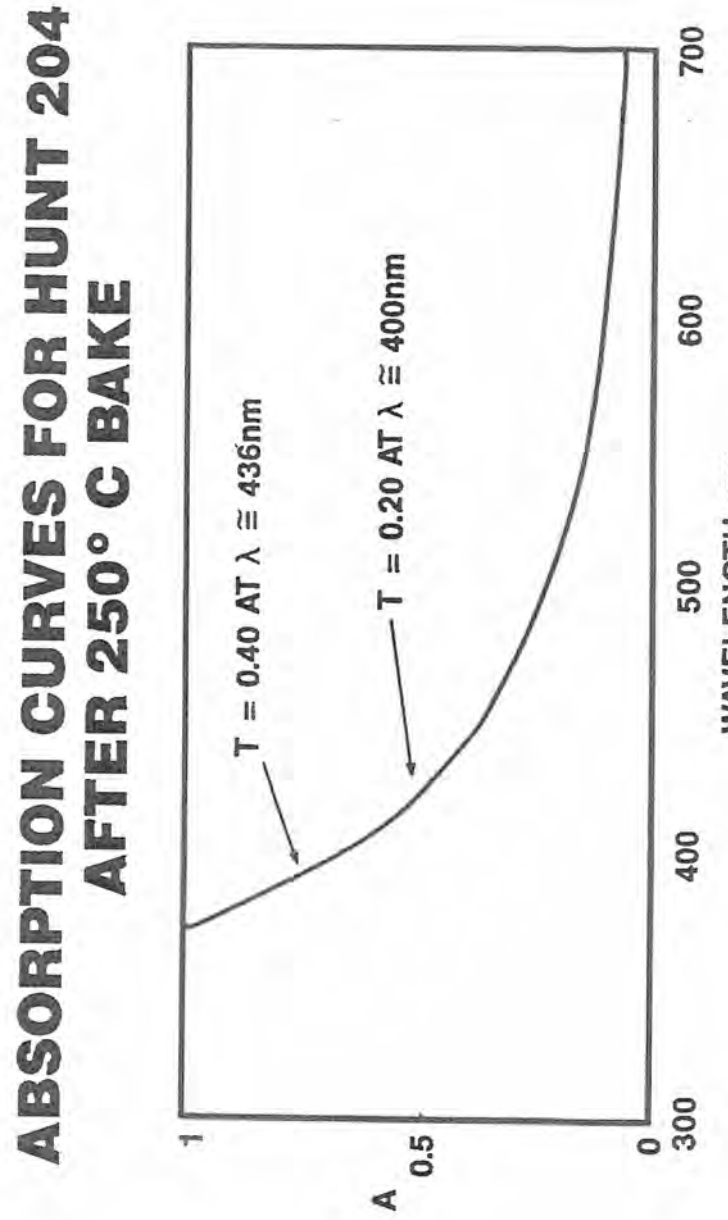


Figure 51. Opitcal transmission curve for bottom layer of RIE tri-level resist process.

processing area, termed Desire processes(108-9). This processing has considerable potential, because it would allow for relief of e-beam proximity effects and photolithographic bulk and focus tolerance effects.

The latter processing allows thick SLR systems to be employed as bi-layers for RIE selectivity and bulk effect relief, and with no interlayer mixing problems. Desire processing is accomplished by post HMDS treatment of the exposed photoresist to yield an in-situ silylated bi-layer, and renders the system as a RIE bi-layer system as opposed to the more typical lithographic bi-layer systems. The system requires oxygen RIE development, like tri-level systems, of the final image. It allows simplified processing over that for conventional bi-layer processes in that 1) the second resist spin and other top layer processing, 2) the top layer development, 3) the DUV flood exposure of the bottom layer, and 4) a subsequent separate development are eliminated and replaced by a high pressure HMDS treatment and RIE development. Obviously, Desire processes have an even greater advantage over trilayer processes due to greater overall process simplification.

Desire processing, like the other special processes of this section, possesses higher process contrast(109). This is achieved because the process images only the thin top part at the top of the thick resist layer. Furthermore, all feature sizes can be written at nearly the same exposure level, and dye can be incorporated to provide reflective notching effect relief. The process is not without problems, however, as swelling effects have been observed and reported at SPIE 1988. Although this processing is in the early stage of development, applications will probably emerge quickly, especially for pilot lines with advanced equipment.

5.0 SUMMARY AND FUTURE PREDICTIONS

Although many processing advances have been delineated in this last section, reduction of these advances to production of VLSIC's will occur with significant negative inertia. More advanced next-generation SLR systems will probably emerge first, especially at the lower wavelengths before multi-layer resist processes see extensive utilization. It should be noted that these new good SLR systems will also be needed as part of the multi-layer special processes. The high NA lithography tools may, however, accelerate the applications of these advanced processes out of forced necessity primarily for focus tolerance relief.

In the area of radiation resists, new sensitive SLR resists or surface sensitive thick resists for ASIC applications will evolve. Figure 52 illustrates clearly the need for resist speed in direct-write e-beam lithography. Furthermore, thick processes will be needed for RIE masking requirements, and multi-layer processes will be considered where SLR processes fail to provide adequate fabrication ability.

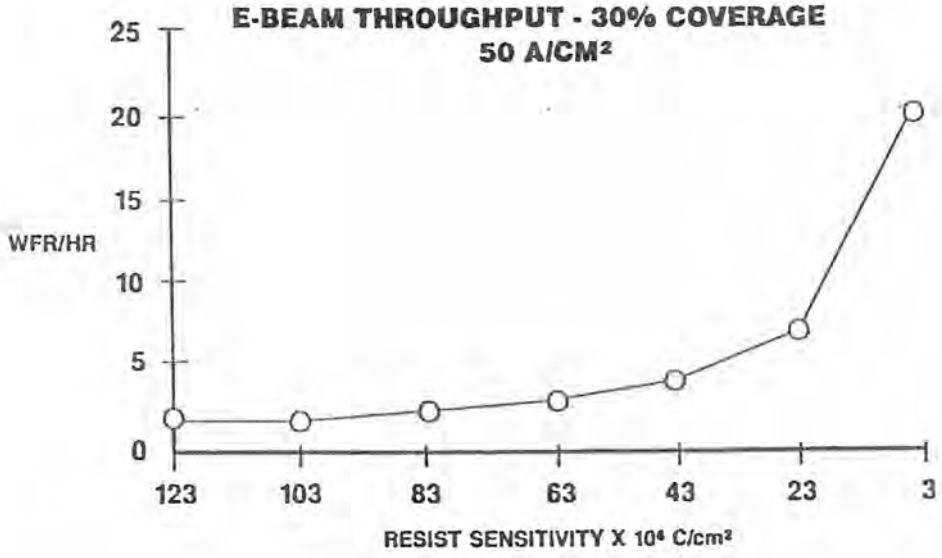


Figure 52. E-beam throughput vs. resist sensitivity for Perkin-Elmer AEBLE 150.

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