

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01376
Patent 6,197,696 B1

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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Rules

37 C.F.R. §42.2432

LIST OF EXHIBITS

- Exhibit 1001: U.S. Patent No. 6,197,696 to Aoi et al.
- Exhibit 1002: Expert Declaration of Dr. Bruce W. Smith, Ph.D.
- Exhibit 1003: U.S. Patent No. 3,617,824 to Shinoda et al.
- Exhibit 1004: U.S. Patent No. 3,838,442 to Humphreys.
- Exhibit 1005: U.S. Patent No. 6,140,226 to Grill et al.
- Exhibit 1006: U.S. Patent No. 5,635,423 to Huang et al.
- Exhibit 1007: U.S. Patent No. 5,741,626 to Jain et al.
- Exhibit 1008: C. Akrouf et al., "A 480-MHz Microprocessor in a $0.12\mu\text{m}$ L_{eff} CMOS Technology with Copper Interconnects," IEEE J. of Solid-State Circuits, Vol. 33, no. 11 (November 1998).
- Exhibit 1009: J.N. Burghartz et al., "Monolithic Spiral Inductors Fabricated Using a VLSI Cu-Damascene Interconnect Technology and Low-Loss Substrates," International Electron Devices Meeting (December 1996).
- Exhibit 1010: U.S. Patent No. 6,100,184 to Zhao et al.
- Exhibit 1011: U.S. Patent No. 6,103,616 to Yu et al.
- Exhibit 1012: File History of U.S. Patent No. 6,197,696 to Aoi et al.
- Exhibit 1013: Japanese Patent Application No. 10-079371 to Aoi.
- Exhibit 1014: Certified Translation of Japanese Patent Application No. 10-079371 to Aoi.
- Exhibit 1015: Japanese Patent Application No. 11-075519 to Aoi.
- Exhibit 1016: Certified Translation of Japanese Patent Application No. 11-075519 to Aoi.
- Exhibit 1017: U.S. Provisional Patent Application No. 60/071,628.

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- Exhibit 1018: U.S. Patent No. 5,592,024 to Aoyama et al.
- Exhibit 1019: Transcript of Teleconference with the Board, dated November 16, 2016.
- Exhibit 1020: <http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4251>.
- Exhibit 1021: IEEE, "Technical Digest of the International Electron Devices," 1996 International Electron Devices Meeting at San Francisco, CA, Table of Contents (December 8-11, 1996).
- Exhibit 1022: J.N. Burghartz et al., "Monolithic spiral inductors fabricated using a VLSI Cu-damascene interconnect technology and low-loss substrates," 1996 International Electron Devices Meeting at San Francisco, CA, pp. 99-102 (December 8-11, 1996).
- Exhibit 1023: <http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=15684>.
- Exhibit 1024: G. Gerosa, "Introduction to the Digital Section," IEEE Journal of Solid-State Circuits, vol. 33, no. 11, p. 1599 (Nov. 1998).
- Exhibit 1025: J. Dreibelbis, "Introduction to the Memory Section," IEEE Journal of Solid-State Circuits, vol. 33, no. 11, p. 1649 (Nov. 1998).
- Exhibit 1026: L.E. Thon, "Introduction to the Signal Processing Section," IEEE Journal of Solid-State Circuits, vol. 33, no. 11, pp. 176-643 (Nov. 1998).
- Exhibit 1027: http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=15684&filter%3DAND%28p_IS_Number%3A15684%29&pageNumber=2.
- Exhibit 1028: C. Akrouf et al., "A 480-MHz RISC Microprocessor in a 0.12- μm L_{eff} CMOS Technology with Copper Interconnects," IEEE Journal of Solid-State Circuits, vol. 33, no. 11, pp. 1609-16 (Nov. 1998).

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