



United States Patent [19]

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Boeck et al.

[45] **Date of Patent:** **Mar. 9, 1999**

[54] **METHOD FOR MANUFACTURING A LOW DIELECTRIC CONSTANT INTER-LEVEL INTEGRATED CIRCUIT STRUCTURE**

WO 87/04858 8/1987 WIPO H01L 21/90
WO 96/19830 6/1996 WIPO H01L 23/532

[75] Inventors: **Bruce Allen Boeck; Jeff Thomas Wetzel; Terry Grant Sparks**, all of Austin, Tex.

G. Minamihaba et al., "Double-Level Cu Inlaid Interconnects With Simultaneously Filled Via-Plugs", 2419A Int'l. Conf. on Solid State Devices & Materials, Aug. 21-24, 1995, pp. 97-99.

[73] Assignee: **Motorola Inc.**, Austin, Tex.

Yoshio Homma et al., Low Permittivity Organic Dielectrics for Multilevel Interconnection in High Speed ULSIs, Extended Abstracts of the 1995 Int'l. Conf. on Solid State Devices & Materials, pp. 154-156.

[21] Appl. No.: **727,159**

[22] Filed: **Oct. 7, 1996**

Yoshio Homma et al., "Low Permittivity Organic Dielectrics for Multilevel Interconnection in High Speed ULSIs", 2419A Int'l. Conf. on Solid State Devices and Materials, Aug. 21-24, 1995, pp. 154-156.

[51] **Int. Cl.⁶** **H01L 21/441**

[52] **U.S. Cl.** **438/619; 438/700; 438/633; 438/623**

[58] **Field of Search** **438/619, 622, 438/623, 627, 633, 700**

Partial European Search Report and Annex, EP 97 11 6851.

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Primary Examiner—Caridad Everhart

Attorney, Agent, or Firm—Keith E. Witek; Kent J. Cooper

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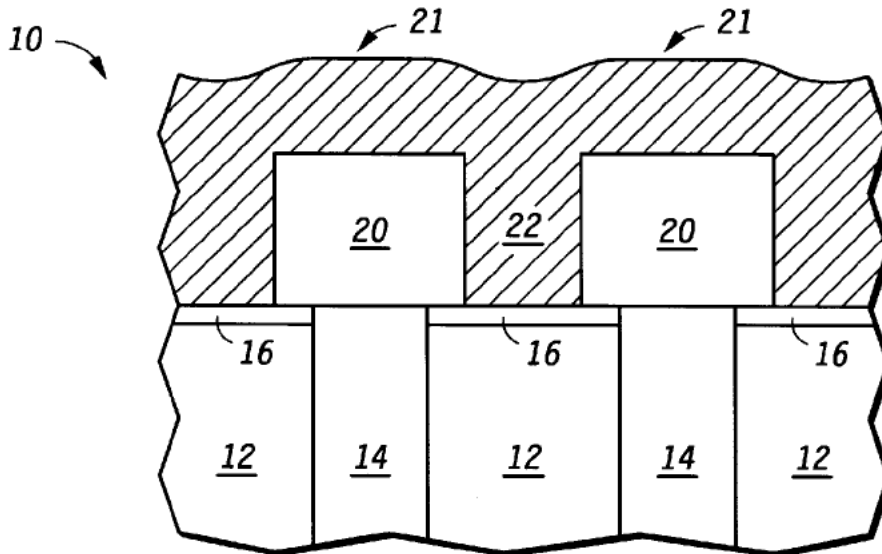
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[57] **ABSTRACT**

An interconnect structure having a dielectric layer with low dielectric constant is formed within an integrated circuit. In one embodiment of the invention, portions of a silicon dioxide layer (18) lying adjacent to a conductive interconnect (21) are removed to expose portions of a silicon nitride etch stop layer (16). A dielectric layer (22) having a low dielectric constant is then formed overlying the conductive interconnect (21) and the exposed portions of the silicon nitride etch stop layer (16). A portion of the dielectric layer (22) is then removed to expose the top surface of the conductive interconnect (21) to leave portions of the dielectric layer (22) between adjacent conductive interconnects (21). The resulting interconnect structure has reduced cross-talk between conductive interconnects (21) while avoiding prior art disadvantages of reduced thermal dissipation and increased mechanical stress.

50 Claims, 5 Drawing Sheets



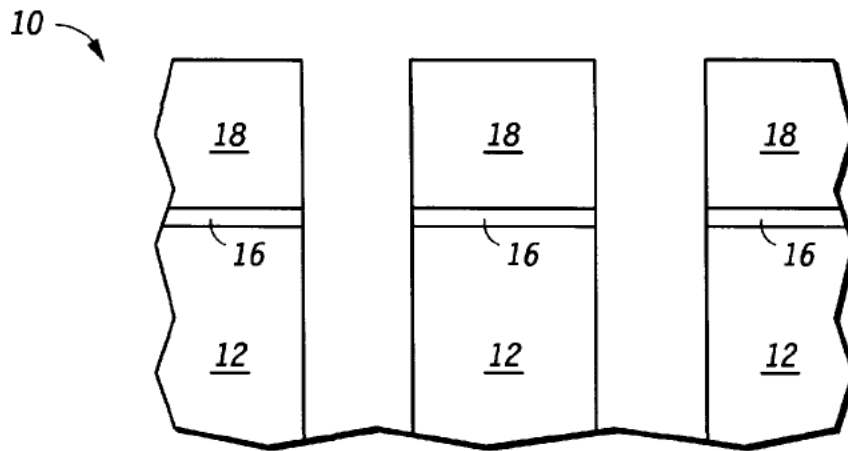


FIG. 1

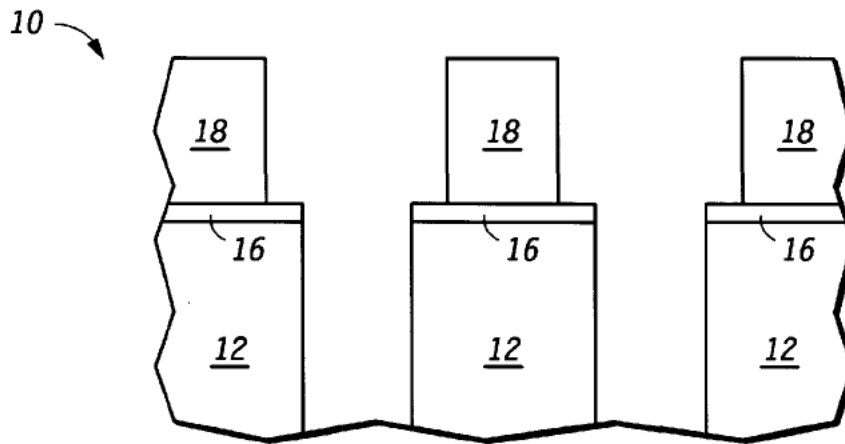


FIG. 2

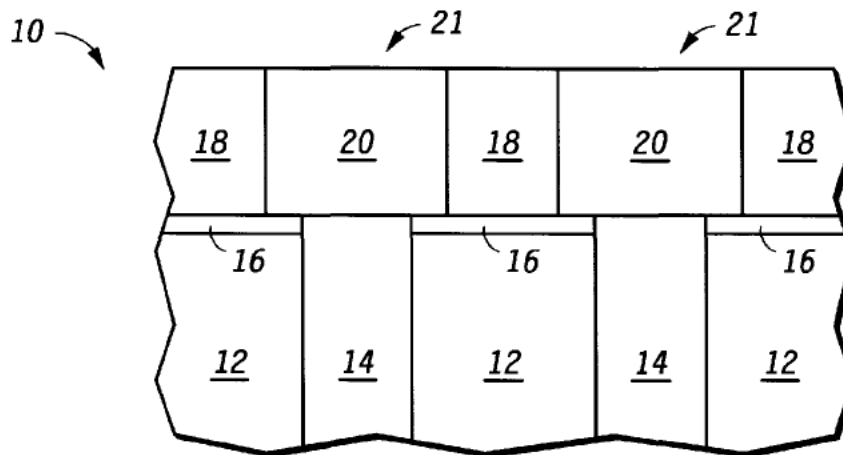


FIG. 3

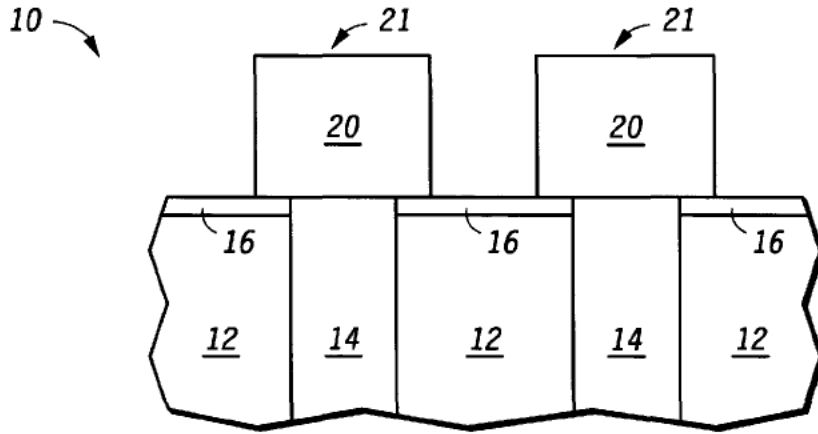


FIG. 4

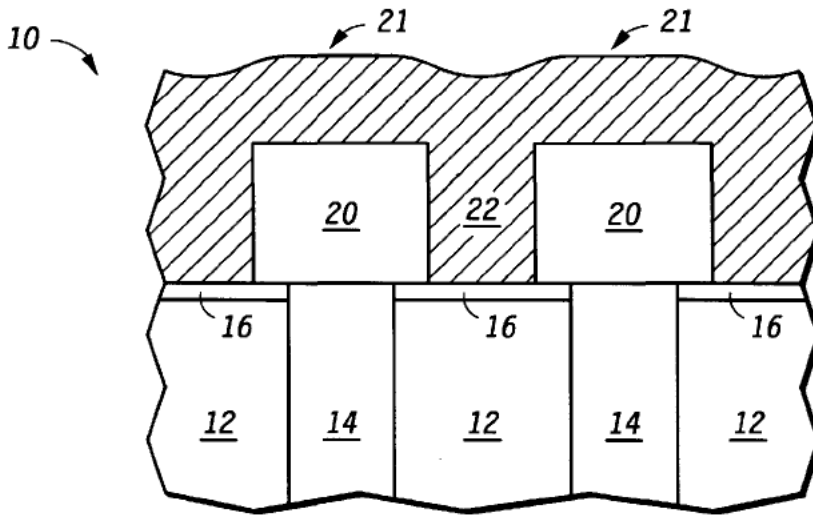


FIG. 5

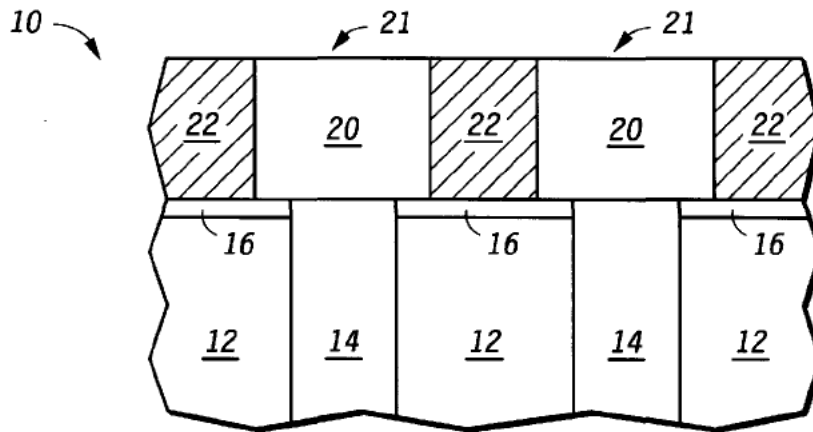


FIG. 6

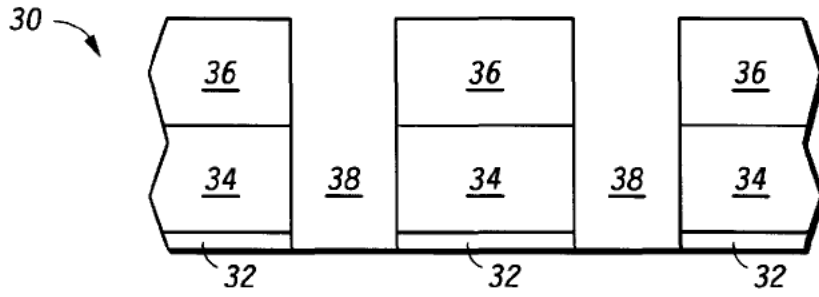


FIG. 7

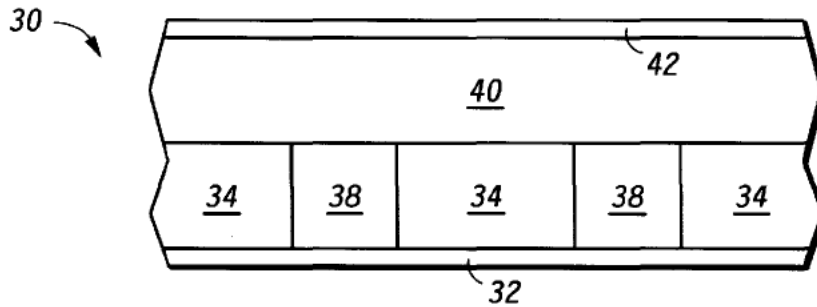


FIG. 8

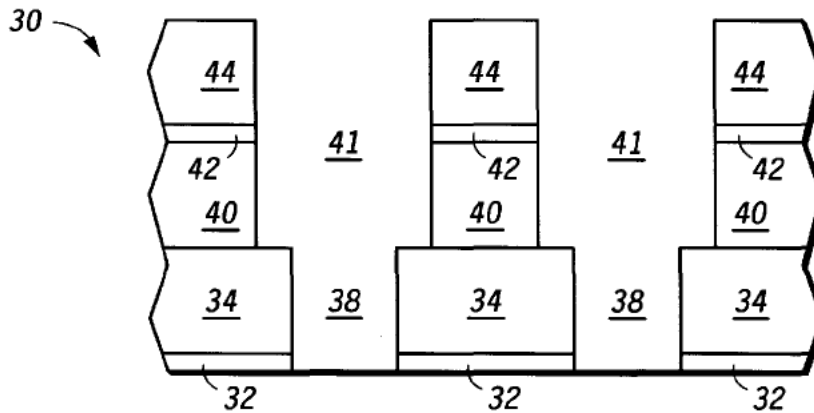


FIG. 9

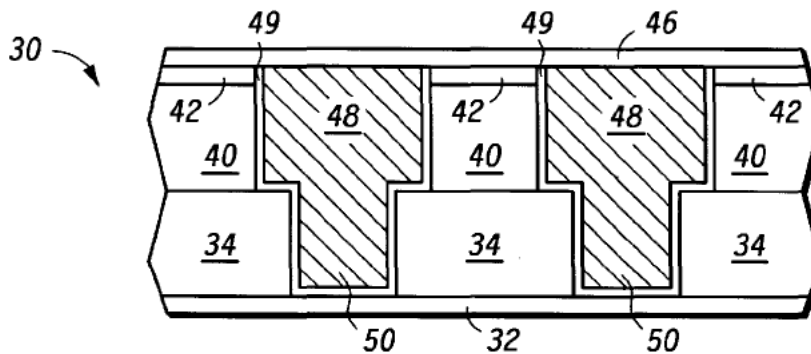


FIG. 10

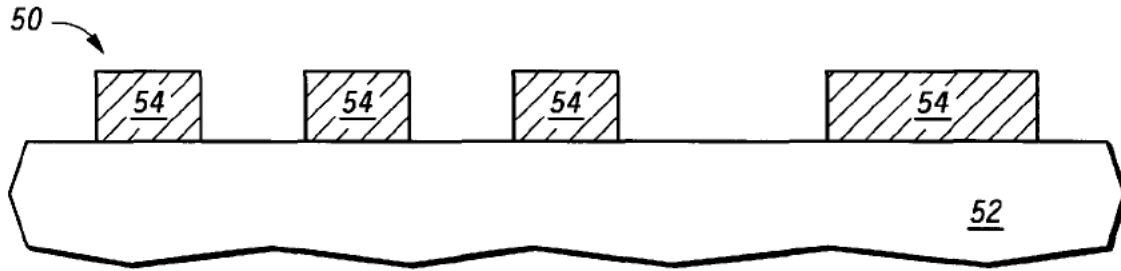


FIG. 11

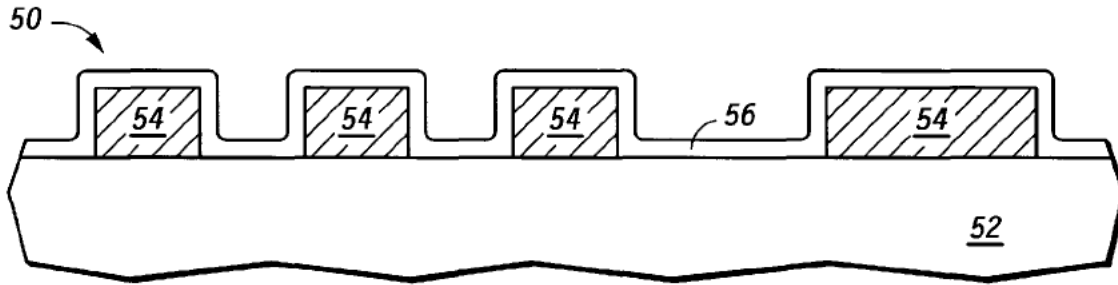


FIG. 12

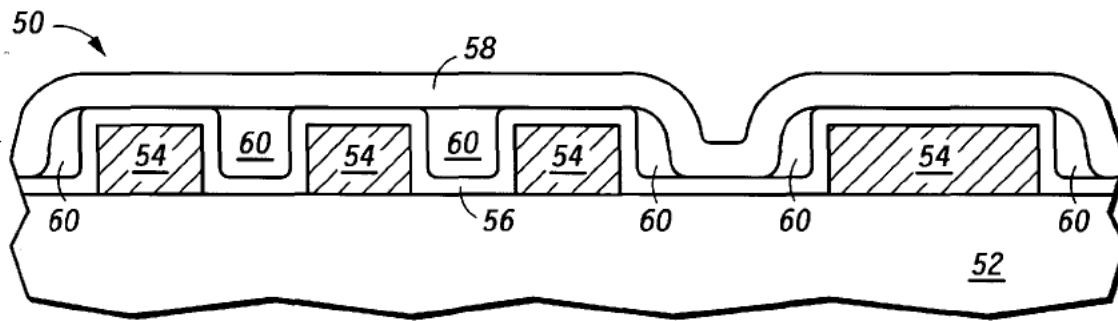


FIG. 13

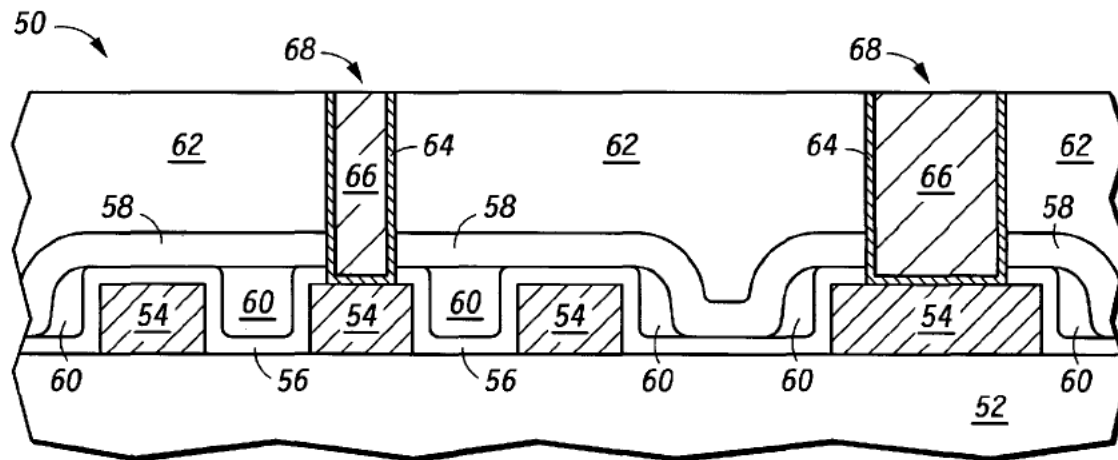


FIG. 14

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