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Filed on behalf of Qualcomm and GlobalFoundries

By: David L. McCombs, Reg. No. 32,271
David M. O'Dell, Reg. No. 42,044

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED, GLOBALFOUNDRIES INC.,
GLOBALFOUNDRIES U.S. INC., GLOBALFOUNDRIES DRESDEN
MODULE ONE LLC & CO. KG, GLOBALFOUNDRIES DRESDEN MODULE
TWO LLC & CO. KG
Petitioner

v.

DSS Technology Management, Inc.
Patent Owner

Case IPR2016-01314

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 6,784,552
CHALLENGING CLAIMS 8-12
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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4.	Claim 11: “The structure of claim 8, further comprising a second insulating layer on the etch stop layer and over the conductive layer”	46

U.S. Patent No. 6,784,552 Claims 8-12
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5. Claim 12: “The structure of claim 11, further comprising a second conductive material in the contact region” 47

B. Ground 2: Claims 8-12 Would Have Been Obvious Over Heath in View of Dennison48

1. Heath, in combination with Dennison, renders the claims obvious under an overly narrow construction of the “angle” limitation—*e.g.*, limiting it to a ***particular*** portion of the “side” of the insulative spacer—recited in claim 8 (element 8(g))..... 48

2. Even if Heath is found to not disclose an etch stop material over the insulating spacer, Heath, in combination with Dennison, renders the claims obvious..... 58

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Petitioner respectfully requests *Inter Partes* Review of claims 8-12 of U.S.

Patent No. 6,784,552 (the “’552 patent”) (Ex. 1101) pursuant to 35 U.S.C. §§ 311-19 and 37 C.F.R. § 42.1 *et seq.* The above-listed claims of the ’552 patent are presently the subject of a substantially identical petition for inter partes review styled *Intel Corporation v. DSS Technology Management, Inc.*, which was filed December 8, 2015 and assigned Case No. IPR2016-00288. Petitioner will seek joinder with that *inter partes* review under 35 U.S.C. § 315(c), 37 C.F.R. §§ 42.22 and 42.122(b).

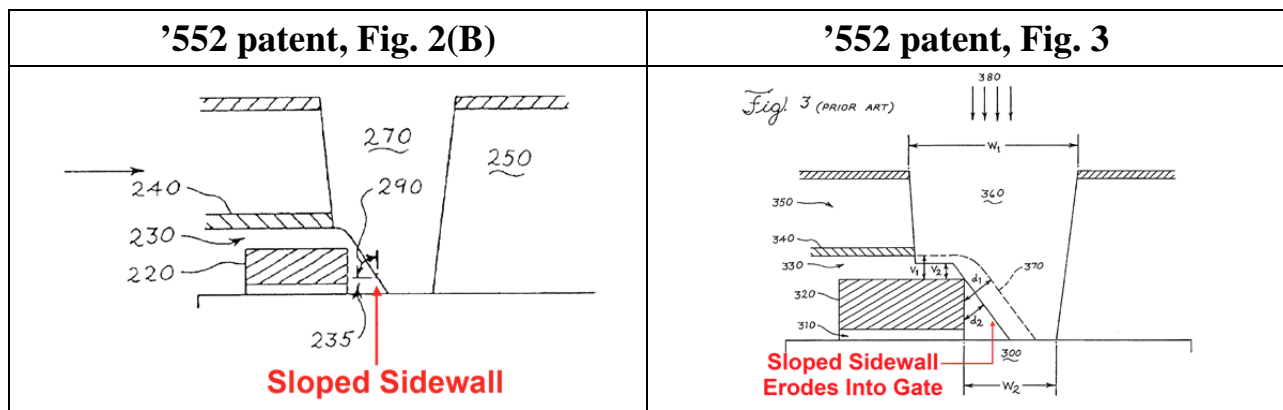
I. INTRODUCTION

The ’552 patent purports to provide a novel approach to semiconductor manufacturing but instead merely duplicates a well-known technique patented by inventor Barbara Heath nearly a decade before the alleged invention.

The ’552 patent is directed to the manufacture of transistors used in semiconductor products such as microprocessors and memory. Transistors are one of the basic building blocks of semiconductors—they are microscopic switches that turn on and off to allow semiconductors to process data. Transistors include various components and “contacts” that are used to connect a component of one transistor to a component of another transistor. The ’552 patent is directed to a particular technique for the formation of “contact openings”—openings created through the layers of a semiconductor device so that a contact can be formed

between components.

The patent asserts that prior art techniques for forming these contact openings resulted in an unacceptably high risk of creating unintentional connections (and thus a short-circuit) between the contacts and nearby components. Specifically, the patent explains that prior art techniques used non-conducting “sidewall spacers” between contact openings and nearby components to prevent unintentional connections. But the patent notes that during the process of creating the openings, these sidewall spacers could become sloped. According to the patent, a sloped sidewall spacer is particularly susceptible to erosion in subsequent fabrication steps such that it can be worn down to the point that the contact opening and a nearby component can make an unintentional connection:



In Fig. 2(B), described as “Prior Art,” the patent shows a contact opening 270, a sidewall spacer 235 that has become sloped as a result of the creation of the contact opening, and a nearby component 220. In Fig. 3, also described as “Prior Art,” the patent shows that in a subsequent step, the sloped sidewall spacer has

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