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APPLICATION FOR UNITED STATES PATENT

FOR

METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

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BACKGROUND OF THE INVENTION

Field of the Invention:

The invention relates to semiconductor device processes, and more particularly, to improved methods for etching openings in insulating layers and a semiconductor device with well defined contact openings.

Background of the Invention

In the fabrication of semiconductor devices, numerous conductive device regions and layers are formed in or on a semiconductor substrate. The conductive regions and layers of the device are isolated from one another by a dielectric. Examples of dielectrics include silicon dioxide, SiO_2, tetraethyl orthosilicate glass ("TEOS"), silicon nitrides, Si_xN_y, silicon oxynitrides, $SiO_xN_y(H_z)$, and silicon dioxide/silicon nitride/silicon dioxide ("ONO"). The dielectrics may be grown, or may be deposited by physical deposition (e.g., sputtering) or by a variety of chemical deposition methods and chemistries (e.g., chemical vapor deposition ("CVD")). Additionally, the dielectrics may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate glass ("BPTEOS").

At several stages of the fabrication of semiconductor devices, it is necessary to make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and the first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a "via". For purposes of the claimed invention, henceforth "contact opening" or "contact region" will be used to refer to contact openings and/or via. The opening may expose a device region within the silicon substrate, such as a source or drain, or may expose some other layer or structure, for example, an underlying metallization layer, local interconnect layer, or structure such as a gate. After the opening has been formed exposing a portion of the region or layer to be contacted, the opening is generally cleaned with a sputter etch, e.g., a Radio-Frequency ("RF") sputter etch, and then the opening is filled with a conductive material deposited in the opening and in electrical contact with the underlying region or layer.

To form the openings a patterning layer of photoresist is first formed over the dielectric layer having openings corresponding to the regions of the dielectric where the dielectric layer openings are to be formed. In most modern processes a dry etch is then performed wherein the wafer is exposed to a plasma, formed in a flow of one or more gases. Typically, one or more halocarbons and/or one or more other halogenated compounds are used as the etchant gas. For example, CF_4, CHF_3 (Freon 23), SF_6, NF_3, and other gases may be used as the etchant gas. Additionally, gases such as O_2, Ar, N_2, and others may be added to the gas flow. The particular gas mixture used will depend on, for example, the characteristics of the dielectric being etched, the stage of processing, the etch tool being used, and the desired etch characteristics, i.e., etch rate, sidewall slope, anisotropy, etc.

Many of the etch characteristics are generally believed to be affected by polymer residues that deposit during the etch. For this reason, the fluorine to carbon (F/C) ratio in the plasma is considered an important determinant in the etch. In general, a plasma with a high F/C ratio will have a faster etch rate than a plasma with a low F/C ratio. At very low rates, i.e., high carbon content, polymer deposition occurs and etching ceases. The etch rate as a function of the F/C ratio i typically different for different materials. The difference is used to create a selective etch, by using a gas mixture that puts the F/C ratio in the plasma at a value that leads to etching at a reasonable rate for one material, and that leads to no etching or polymer deposition for another. For example, an etchant that has an etch rate ratio or a selectivity ratio of two to one for silicon nitride compared to silicon dioxide is an effective stripper of silicon nitride from the semiconductor substrate, because it will selectively strip silicon nitride over silicon dioxide on a substrate surface. An etchant that has an etch rate ratio or a selectivity ratio of 0.85 to one for silicon nitride compared to silicon dioxide is not considered an effective stripper of silicon nitride from the semiconductor substrate because the etchant will not effectively strip silicon nitride to the exclusion of silicon dioxide.

The selectivity of the etch process is a useful parameter for monitoring the process based on the etch rate characteristic of the particular etchant. As noted above, particular etchants or etchant chemistries attack different materials at different etch rates. With respect to dielectrics, for example, particular etchants attack silicon dioxide, BPTEOS, TEOS, and silicon nitride dielectrics at different rates. To make openings in a substrate comprising a contact region surrounded by different dielectric layers, e.g., a dielectric layer of TEOS surrounded by a dielectric layer of silicon nitride, a process will utilize different etchants to make openings through the different dielectrics. Thus, the different etch rates of particular dielectric layers for an etchant may be used to monitor the creation of an opening through a dielectric layer.

Further, by adjusting the feed gases, the taper of the sidewall in the etched opening of the dielectric can be varied. If a low sidewall angle is desired, the chemistry is adjusted to try to cause some polymer buildup on the sidewall. Conversely, if a steep sidewall angle is desired, the chemistry is adjusted to try to prevent polymer buildup on the sidewall. Varying the etch gas pressure, for example, has a significant effect on the shape of the opening. This is because the etchant ions generally arrive in a direction perpendicular to the substrate surface, and hence strike the bottom surfaces of the unmasked substrate. The sidewalls of etched openings, meanwhile, are subjected to little or no bombardment. By increasing the pressure of the etch gas, the bombardment directed toward the sidewalls is increased; by decreasing the pressure of the etch gas, the bombardment directed toward the sidewalls is decreased. The changing of the etch chemistry is also directly related to selectivity. Etchants that provide a near 90° sidewall angle are generally not highly selective while highly selective etches typically produce a sloped sidewall.

Following the dielectric etch(es) and prior to any conductive material deposition in a contact region, native oxide on top of the conducting layers in the contact region is removed or cleaned through a non-chemical sputter etch, e.g., an RF sputter etch. In addition to alleviating the contact region of native oxide, the sputter etch can erode any insulating dielectric layer or layers. Thus, the parameters of the sputter etch must be carefully monitored so as not to excessively erode the insulating dielectric layer(s) and expose other underlying conductive material. Exposing insulated conductive material adjacent to the conductive material in the contact region results in poor quality contacts or a short circuit through the underlying conductive material. For a thorough discussion of oxide etching, see S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1, pp. 539-85 (1986).

The preceding discussion focused on the making of openings, e.g., contact openings, in dielectric material on a semiconductor substrate. The same principles are used in constructing device regions with a dielectric layer or layers. As geometries shrink, the forming of discreet devices on a semiconductor substrate

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