

DSS Infringement Contentions—Exhibit B
 '552 Patent

Infringement Contentions for US 6,784,552	
	<p>Plaintiff DSS Technology Management Inc. (“DSS”) serves its Infringement Contentions as to Defendants Intel, A Conn’s, and Wal-Mart (“Defendants”). DSS contends that Defendants are each individually liable for infringement asserts infringement of claims 1-7.</p> <p>Intel has and continues to make, use, sell, import, and/or offer to sale in the United States systems and methods used semiconductor structures made via Intel’s 22-nanometer (“nm”) FinFET process (the “Accused Products”). The re sell, import, and/or offer to sale the Accused Products. DSS has attached a list of processors, known to it at this time Intel’s 22-nm FinFET process. See Exhibit 1. These infringement contentions apply equally to any other Intel semiconductor structures made by an equivalent method with similar functionality, regardless of the specific product or process name.</p> <p>To date, the parties in this litigation have not engaged in any discovery, and no documents have been produced. All these disclosures is the result of publicly available information and independent examination and analysis of the Accused Products. In these circumstances, DSS presents these Infringement Contentions reflecting DSS’s current analysis of the facts presented. In the best of DSS’s knowledge, information, and belief, formed after an inquiry that is reasonable under the circumstances, DSS believes that the Accused Products are made in this disclosure is correct. Certain information about the Accused Products operation is not available without discovery. Accordingly, DSS reserves the right to seek leave to supplement and/or amend these disclosures as new information becomes available and as DSS has the opportunity to review relevant Defendant document productions. Infringement contentions DSS anticipates that additional facts and relevant documents will be uncovered and disclosed that could create good cause for supplementation and/or amendment of these contentions. DSS will continue to develop the evidence of infringement and DSS reserves the right to amend and supplement these Infringement Contentions.</p> <p>Furthermore, based on DSS’s view that certain Defendant systems, products, processes, and/or services could infringe the Accused Products in multiple ways, DSS’s Infringement Contentions may include alternative theories of infringement for the Accused Products that are mutually exclusive of other infringement theories or which may overlap with other infringement theories in certain circumstances.</p>
Claim 1	Infringement Evidence
<p>1.A structure, comprising:</p> <p>a) a conductive layer disposed over a substrate;</p>	<p>The Accused products contain semiconductor structures. Each of the 22 nanometer-process-based i3, i5, i7, Celeron, and Xeon processors contains the infringing semiconductor structure. Unless otherwise noted, TEM images of a Core i7 processor, Xeon processor and belief, all processors made on Intel’s 22-nanometer (“nm”) FinFET process—including the Atom, and Xeon processors—have the same gate-to-contact structures. Thus, those processors infringe as well.</p> <p>Infringing structures are found in the Accused products, including the Intel Core i7-4790 processor, which is made on a 22-nm FinFET process.</p>

INTEL 1106

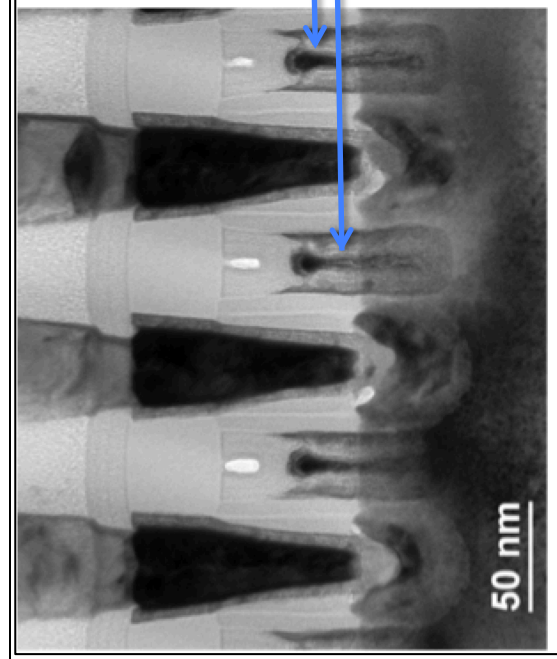
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Source: DSS2-0000755

The Accused Products have a conductive layer disposed over a substrate. The substrate, likely a silicon substrate, bottom of the below image. Conductive layers, the gates, are over the substrate. In the FinFET configuration where dimensional channel region, the gate is formed on top of the substrate, which includes the fin.

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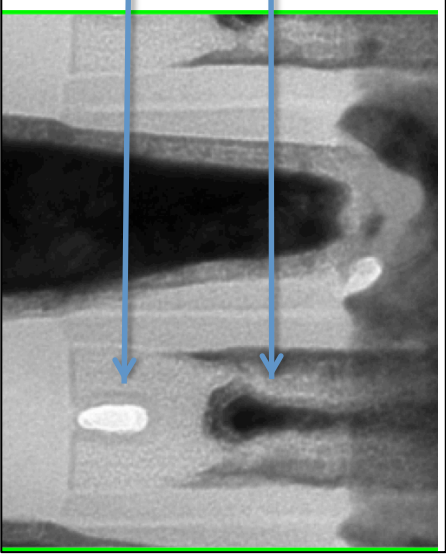


Source: DSS2-0000751

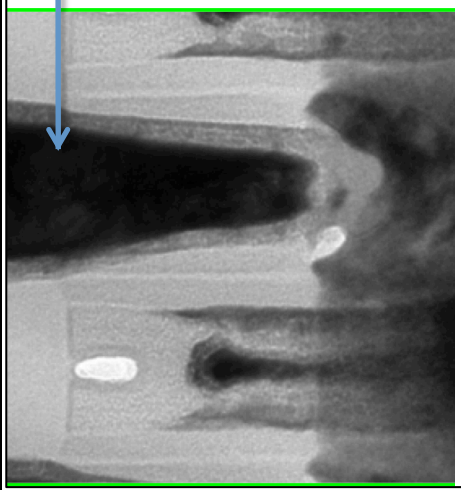
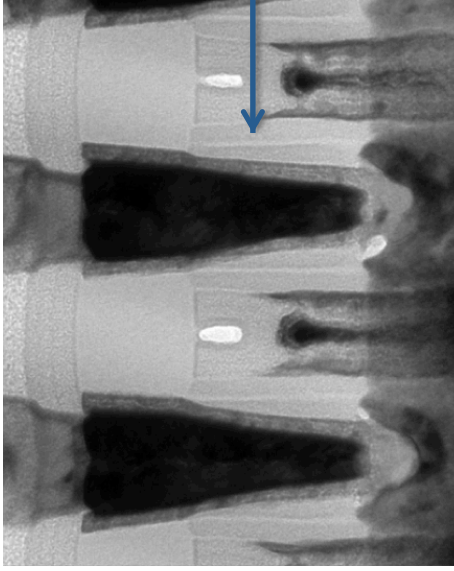
(b) a first insulating layer on the conductive layer:

The Accused Products have a first insulating layer on the conductive layer. The first insulating layer is the light gray conductive gate layer with a white “bead” in the center.

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	 <p>The micrograph shows a cross-section of a substrate with a contact region. A blue arrow labeled "First insulating layer" points to a light-colored, irregularly shaped region on the left. Another blue arrow labeled "Conductive layer" points to a dark, elongated region on the right. The background is a lighter, textured surface.</p>
<p>(c) a contact region in said first insulating layer;</p>	<p>Source: DSS2-0000751.</p> <p>The Accused Products have a contact region in the first insulating layer. The contact region is the opening through which the contact is made to the substrate. Both “contact openings”—an opening through a dielectric opening through a dielectric layer between polysilicon and a first metal layer—and “vias”—an opening in other opening through an intermetal dielectric layer—are “contact regions.” The contact region is shown as the dark region of the picture to the diffusion region.</p>

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	 <p style="text-align: center;">contact region</p> <p style="text-align: center;">Source: DSS2-0000751.</p>
<p>(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and</p>	<p>The Accused Products include at least one insulating spacer in the contact region. The insulating spacers are adjacent to the first insulating layer. The insulating spacers are the vertical, light grey materials on either side of the conductive layers.</p>  <p style="text-align: center;">insulating spacer</p> <p style="text-align: center;">Source: DSS2-0000751</p>

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