EXHIBIT 1002

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED, GLOBALFOUNDRIES INC., GLOBALFOUNDRIES U.S. INC., GLOBALFOUNDRIES DRESDEN MODULE ONE LLC & CO. KG, GLOBALFOUNDRIES DRESDEN MODULE TWO LLC & CO. KG
Petitioner

v.

DSS Technology Management, Inc.
Patent Owner

U.S. Patent No. 5,965,924
Claims 1-6, 13, 14 and 16

DECLARATION OF RICHARD BLANCHARD, PH.D. ON BEHALF OF PETITIONER

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    1. Independent Claim 1 33
    2. Claim 2: “A semiconductor structure according to claim 1, wherein said diffusion region is an N+ or a P+ region” 50
    3. Claim 3: “A semiconductor structure according to claim 1, wherein said insulator layer is formed of a material selected from the group consisting of silicon oxide and silicon nitride.” 51

4. Claim 14: "A semiconductor structure according to claim 1, wherein said polysilicon gate and said diffusion region being exposed in said via in the absence of said conducting plug." 52

5. Claim 16: "The structure according to claim 1, wherein said gate comprises polysilicon." 53

B. Ground II: Claims 4-6 and 13 are obvious in view of the combination of Sakamoto and Cederbaum 53

1. Claim 4: "a semiconductor structure according to claim 1, wherein said electrically conducting plug is a metal plug" / Claim 5: "a semiconductor structure according to claim 1, wherein said electrically conducting plug is a refractory metal plug." / Claim 6: "a semiconductor structure according to claim 1, wherein said electrically conducting plug is formed of a material selected from the group consisting of titanium, tantalum, molybdenum and tungsten" 54

2. Claim 13: A semiconductor structure according to claim 1, wherein said conducting plug comprises an outer glue layer and a plug material therein 60

IX. Availability for Cross-Examination 62

X. Right to Supplement 62

I, Richard Blanchard, declare as follows:

1. My name is Richard Blanchard.

2. My academic credentials include both a Bachelor of Science Degree in Electrical Engineering (BSEE) and a Master of Science Degree in Electrical Engineering (MSEE) from the Massachusetts Institute of Technology in 1968 and 1970, respectively. I subsequently obtained a Ph.D. in Electrical Engineering in 1982 from Stanford University

3. I have worked or consulted for more than 40 years as an Electrical Engineer. My primary focus has been on the development, manufacture, operation, and use of devices and integrated circuits, the assembly of these devices and integrated circuits, products that use them, and their failures. My employment history following my graduation from MIT began at Fairchild Semiconductor in 1970. At Fairchild, my responsibilities included circuit and device design, process development, and product engineering in the Linear Integrated Circuits Department.

4. In 1974, I joined Foothill College as an Associate Professor in the Engineering & Technology Division. My responsibilities included developing a program in Semiconductor Technology as well as teaching other courses in the division. While at Foothill College, I co-founded two

companies, Cognition and Supertex, and later joined Supertex as a Vice President in 1978. At Supertex, I designed and developed discrete DMOS (double-diffused metal oxide semiconductor) transistors, as well as integrated circuits that contained DMOS transistors. At Supertex, I also supervised the in-house assembly area, which included responsibility for the associated manufacturing processes. I left Suptertex to join Siliconix in 1982, where I soon became Vice President of Engineering, with the responsibility for directing all of the company's product design and development. At Siliconix, I directed and contributed to the development of both discrete transistors and integrated circuits, including aspects of their assembly.

5. In 1987, I joined IXYS Corporation as a Senior Vice President with the responsibility for organizing an integrated circuit department. At IXYS, I developed integrated circuits that contained DMOS devices or that interfaced to DMOS devices. My responsibilities included the design, assembly, and testing of these integrated circuits.

6. These duties continued until 1991, when I left IXYS to set up Blanchard Associates, a consulting firm specializing in semiconductor technology, including intellectual property. Soon thereafter, I was invited to

join Failure Analysis Associates, which I did in late 1991. At Failure Analysis Associates, I investigated failures in electrical and electronic systems in addition to performing design and development consulting.

7. I left Failure Analysis in 1998 to join IP Managers, which later merged with Silicon Valley Expert Witness Group, now known as Thomson Reuters Expert Witness Services ("Thomson Reuters"). At Thomson Reuters, I work with companies on patent and trade secret matters. I also consult for a number of semiconductor companies, working with them to develop products and intellectual property, or assisting them in other technical areas through Blanchard Associates. Design and development projects that I have worked on range from the design and evaluation of specific components, to the selection of the technology appropriate for the fabrication of different subsystems of a system.

8. I am a member of a number of professional societies, including the Institute of Electrical and Electronic Engineers, the International Microelectronics and Packaging Society, the American Vacuum Society, the Electronic Device Failure Analysis Society, and the Electrostatic Discharge Society. A copy of my curriculum vitae (including a list of all publications authored in the previous 10 years) is attached as Appendix A.

9. I have reviewed the specification, claims and file history of U.S. Patent No. 5,965,924, as well as the petition for inter partes review of this patent: IPR2016-00289, including the Declaration of Dr. John C. Bravman. I understand that the '924 patent was filed on July 24, 1997, issued from a "continued prosecution application" ("CPA") of U.S. App. No. 08/561,951 and claims priority to an application filed on November 22, 1995. I understand that, for purposes of determining whether a publication will qualify as prior art, the earliest date that the '924 patent could be entitled to is November 22, 1995. However, I further understand that the prior assignee claimed a conception date of May 17, 1995 during prosecution of the '924 application. Amendment and Rule 131 Declaration dated Jan. 5, 1998 (Ex. 1006). Even under that conception date, the cited references are prior art and invalidate the '924 patent.

10. I have reviewed the following patents in preparing this declaration:

- U.S. Patent No. 5,475,240 ("Sakamoto") (Ex. 1003).
- U.S. Patent No. 5,100,817 ("Cederbaum") (Ex. 1004).

11. I have reviewed the above patents and any other publication cited in this declaration.

12. I have considered certain issues from the perspective of a person of ordinary skill in the art as described below at the time the '924 patent application

was filed. In my opinion, a person of ordinary skill in the art for the ’924 patent would have found the ’924 patent invalid.

13. I have been retained by the Petitioner as an expert in the field of semiconductor device fabrication and design. I am working as an independent consultant in this matter and am being compensated at my normal consulting rate of $375 per hour for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration.

14. I have no financial interest in the Petitioner. I similarly have no financial interest in the ’924 patent, and have had no contact with the named inventor of the ’924 patent.

I. RELEVANT LAW

15. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as follows:

A. Claim Construction

16. I have been informed that claim construction is a matter of law and that the final claim construction will ultimately be determined by the Board. For the purposes of my analysis in this proceeding and with respect to the prior art, I have been informed that I should apply what is known as “the *Phillips* standard,” rather than the broadest reasonable interpretation standard.

17. Specifically, I have been informed and understand that since the '924 patent expired on November 22, 2015, the *Phillips* standard applies for the purposes of claim construction. I further understand that the *Phillips* standard means that claim terms are given their plain and ordinary meaning as understood by a person of ordinary skill in the art at the time of the invention in light of the claim language and the patent specification.

18. I have also been informed and understand that any claim term that lacks a definition in the specification is therefore given its plain and ordinary meaning as understood by one of ordinary skill in the art.

B. Anticipation

19. I have been informed and understand that a patent claim may be "anticipated" if each element of that claim is present either explicitly, implicitly, or inherently in a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

C. Obviousness

20. I have been informed and understand that a patent claim can be considered to have been obvious to a person of ordinary skill in the art at the time

the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.

21. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

22. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

23. I understand that one of ordinary skill in the art has ordinary creativity, and is not an automaton.

24. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

II. SUMMARY OF OPINIONS

25. It is my opinion that every limitation of the structures described in claims 1 through 6, 13, 14 and 16 of the ’924 patent are disclosed by the prior art, and are anticipated and/or rendered obvious by the prior art.

The following discussion and analysis is substantially the same as that of Dr. John C. Bravman in IPR2016-00289, supplemented with additional analysis and comments provided throughout this declaration.

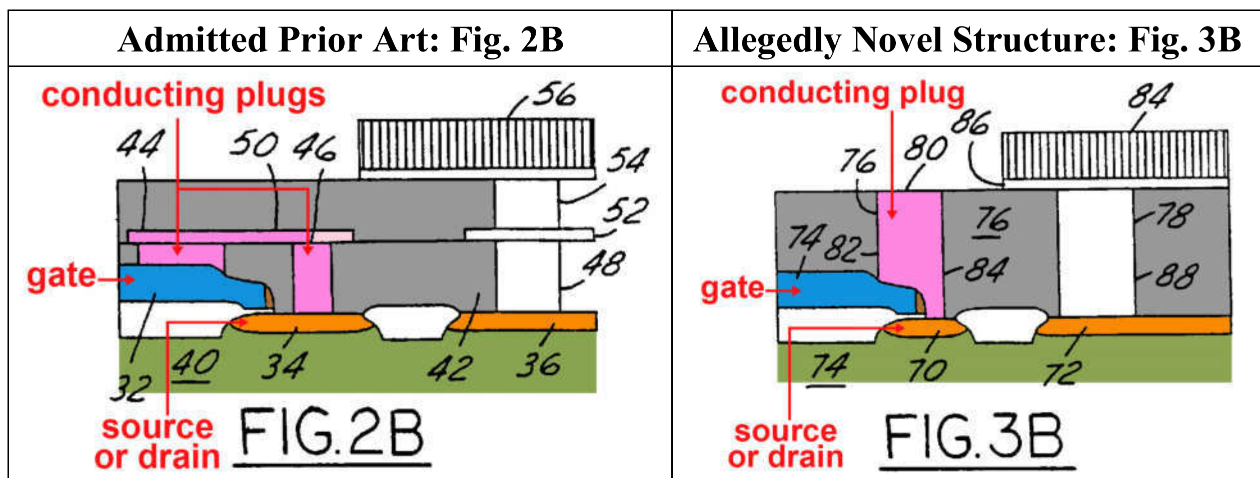
III. INTRODUCTION TO THE ’924 PATENT

26. The ’924 patent is directed to certain aspects of the structure and fabrication of transistors used in semiconductor and integrated circuit products such as microprocessors and memory. Transistors act as microscopic switches that turn on and off at extraordinarily high rates to enable aggregations of transistors (and other components) to process data. Transistors are made up of various structures including “contacts” that provide electrically conductive pathways into and out of certain structures within a transistor, and which thereby are used to connect transistors together.

27. The ’924 patent is concerned with electrically connecting different transistor parts to each other in a particular way. Transistors typically have three terminals through which electrical signals may pass: a “source,” a “drain,” and a

"gate." The '924 patent is concerned with connecting the gate of one transistor to, for example, the source or drain of a neighboring transistor.

28. According to the specification of the '924 patent, there were many well-known ways of making electrical connections between different transistor parts. As shown in Figure 2B (below), for instance, one of the prior art ways of connecting the components of two transistors was by using two electrical connections called "plugs"—one connected to the gate of one transistor, and the other connected to the source or drain of the other—and then connecting those plugs together. As shown in Figure 3B (below), the purported invention of the '924 patent was to replace the two plugs with one plug. [1]

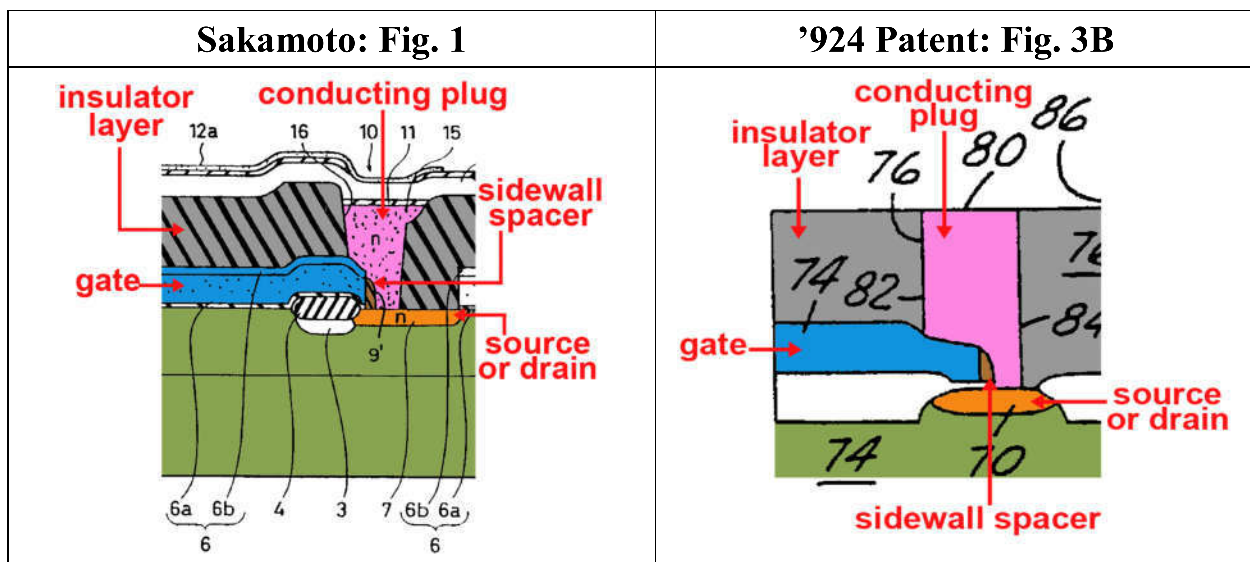


29. In both the prior art (Figure 2B) and the allegedly novel structure of the '924 patent (Figure 3B), the gate is connected to a diffusion region (*i.e.*, a

[1] All emphasis and annotations are added unless otherwise indicated.

source or drain) by either two connected plugs, or a single plug. The patent does not claim that the one-plug structure provides any performance benefits over the two-plug structure. Instead, the benefit was that the one-plug structure was easier to manufacture than the admitted prior art. ’924 patent at 1:57-2:63, 4:18-5:12 (Ex. 1001).

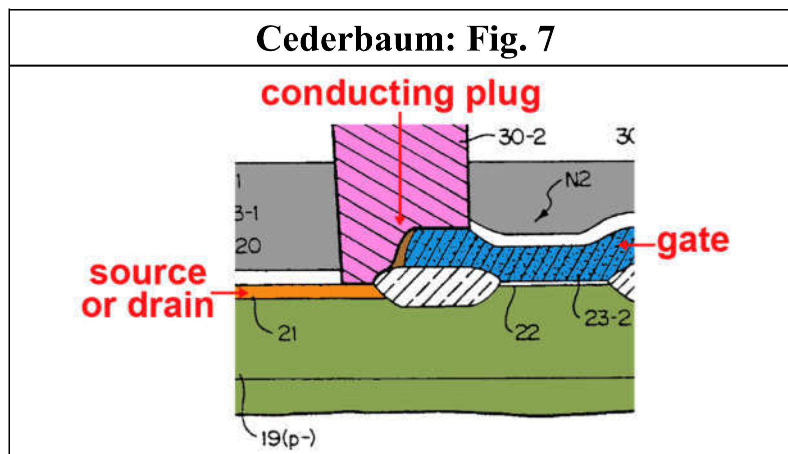
30. Long before the ’924 patent’s November 22, 1995 priority date, many others had already developed and used the exact same one-plug structure. U.S. Patent No. 5,475,240 (“Sakamoto”), for instance, which has an effective filing date of March 4, 1992, discloses the same one-plug structure that the ’924 patent contends is novel. Specifically, as shown in the patents’ respective figures, the one-plug structure of Sakamoto (Figure 1) is in all relevant aspects identical to the one-plug structure of the ’924 patent (Figure 3B).



31. As shown, both structures include a gate connected to a source or drain through a single plug.

32. U.S. Patent No. 5,100,817 ("Cederbaum") issued on March 31, 1992, and, just like the '924 one-plug structure, discloses a single conducting plug connecting a gate to a source or drain.

Cederbaum: Fig. 7



33. Sakamoto and Cederbaum were not at issue during prosecution of the '924 patent. These references anticipate and/or render obvious claims 1-6, 13, 14 and 16 the '924 patent.

IV. BRIEF DESCRIPTION OF THE TECHNOLOGY

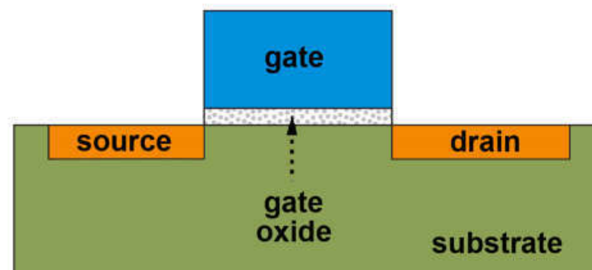
34. The '924 patent generally relates to the field of semiconductor integrated circuit manufacturing and claims particular structures for transistors in semiconductors, as well as a related method for manufacturing those structures.

A. Overview of Transistor Fabrication

1. Basic Structure of Transistors

35. Semiconductor integrated circuits, such as microprocessors and computer memory, are typically made up of hundreds of millions (and in some cases billions) of microscopic structures called transistors. Transistors act as microscopic switches that turn on and off at extraordinarily high rates to enable aggregations of transistors (and other components) to process data.

36. As shown in the figure below, transistors typically include three primary "electrodes" or "terminals"—a "gate," a "source," and a "drain":



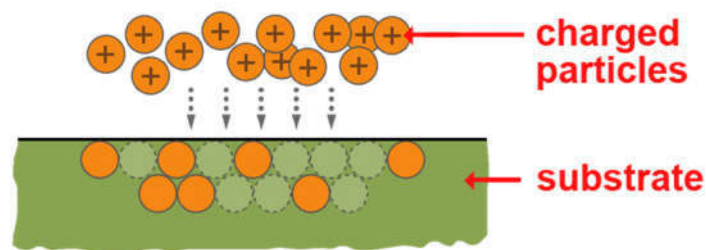
BASIC TRANSISTOR

37. The source and drain regions (also referred to as "diffusion regions") are transistor components that emit (source) and receive (drain) current/carriers when the transistor is "on." The gate typically sits between the source and drain and is a terminal that can have a voltage applied to it that in turn causes a current to flow between the source and drain. As of the time of the invention of the '924 patent, the source and drain of a transistor were typically formed in the surface of a

semiconductor "substrate," while the gate typically sat above the substrate and separated from it by a thin layer of insulator ("gate oxide").

2. Formation of Transistor Components

38. Transistor fabrication typically starts with a silicon substrate. In typical planar transistors, the source and drain regions ("diffusion regions") are created by implanting regions of the substrate with ions (charged atomic particles) of different materials—called "dopants" or "impurities." (Once implanted the ions become neutral atoms). This process—referred to as "doping" because it dopes the silicon substrate with atomic particles that have additional charge carriers—is shown below:

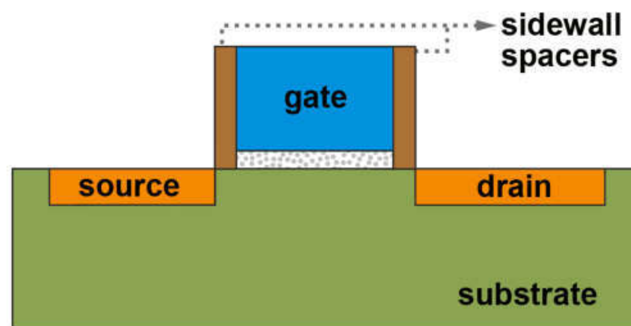


A mask can be used for directing the charged particles to specific locations in the substrate.

39. Structures can then be formed above the substrate by depositing layers of other materials onto the substrate. A gate electrode, for example, is formed by first growing or depositing a "gate oxide" (an insulator) on the substrate followed by depositing a conductive material (metal or polysilicon) on top of the gate oxide.

The conductive material acts as the gate, and the gate oxide creates a layer of isolation between the gate and the source/drain regions ("S/D regions" or "diffusion regions").

40. Insulating materials may then be deposited around and over the gate and the S/D regions to maintain electrical isolation where desired. Sidewall spacers, for instance, can be formed on each side of the gate electrode as shown below:



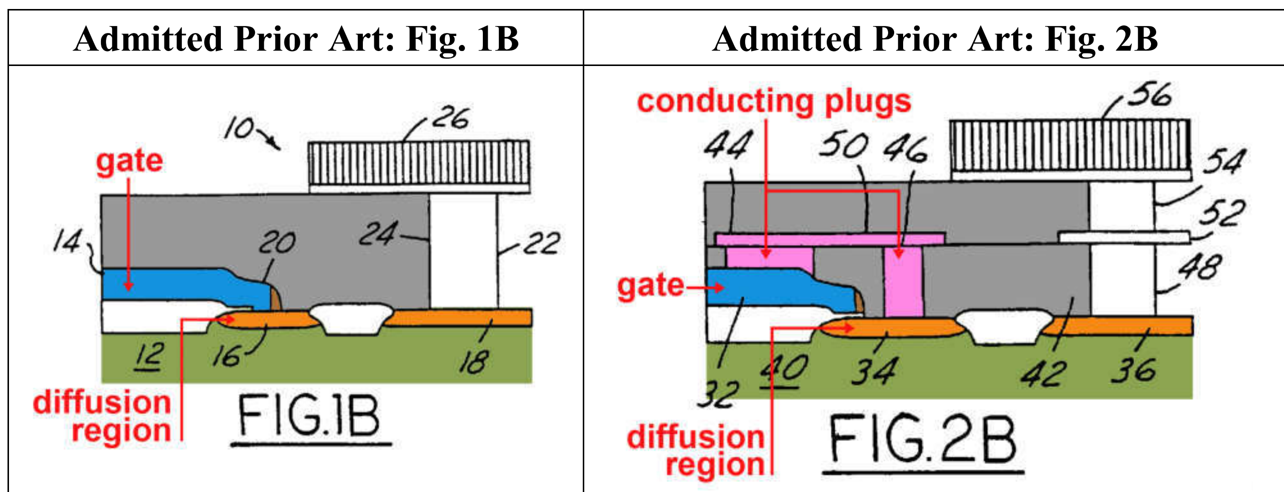
As was known as of the time of the '924 invention, such sidewall spacers help to prevent direct electrical contact between the gate electrode and nearby components and thus help to prevent short-circuits.

3. Local Interconnects

41. Many transistors can be connected together to form electronic circuits. For certain types of circuits, it is sometimes useful to connect the gate of one transistor to a diffusion region (the source or drain) of a nearby transistor. This

type of connection is called a "local interconnect," because connections are made locally between nearby transistors.

42. According to the specification of the '924 patent, a variety of different types of local interconnects were well-known prior to the purported invention. For example, as shown in Figure 1B of the '924 patent, one well-known way to form a local interconnect was to position the gate in a location where it physically touches the diffusion region on one side, creating an electrical connection. As shown in Figure 2B of the '924 patent, another well-known way to make a local interconnect was to place one electrically conductive "plug" above the gate and another "plug" above the diffusion (e.g., source or drain) region, and then electrically connect the two plugs together.



43. The '924 patent acknowledges that both examples were known prior art. *See* '924 patent at Figs. 1A, 1B, 2A, 2B, 1:25-2:45, 3:30-35 (Ex. 1001).

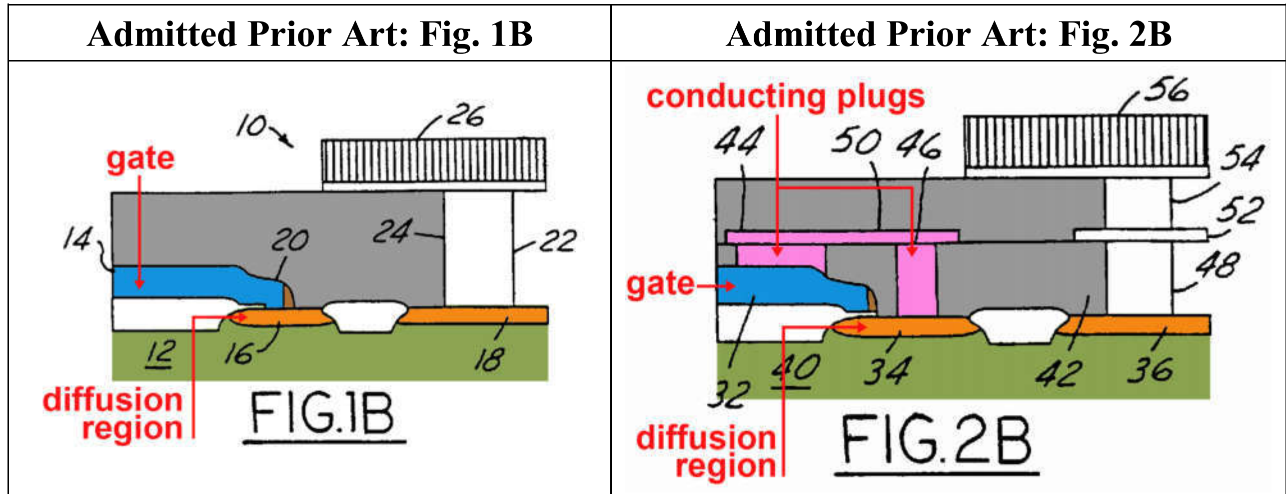
B. Overview of the ’924 Patent

44. The ’924 patent issued from U.S. App. No. 08/900,047, which was filed on July 24, 1997, and claims priority to an application filed on November 22, 1995. ’924 patent at cover page (Ex. 1001). The invention of the ’924 patent is a single plug to connect different transistor parts. ’924 patent at 2:32-67, 4:18-5:12 (Ex. 1001).

1. Problem Disclosed in the ’924 Patent

45. The ’924 patent addresses manufacturing inefficiencies in forming local interconnects. Figures 1 and 2 of the ’924 patent are prior art and show examples of two well-known types of local interconnects that (according to the ’924 patent) are inefficient to manufacture.

46. Figure 1B shows a “buried contact” local interconnect structure in which the gate directly touches—*i.e.*, is in direct electrical connection with—a diffusion region. According to the ’924 patent, the problem with this structure is that the gate has to be implanted with the same type of impurities as those implanted in the diffusion region. *See* ’924 patent at 1:57-2:11 (Ex. 1001). But most manufacturers use a variety of different types of impurities in different transistors. To use the “buried contact” approach, a manufacturer would have to ensure that any two transistors connected using this approach use the same impurities, which complicates the manufacturing process. *See id.*

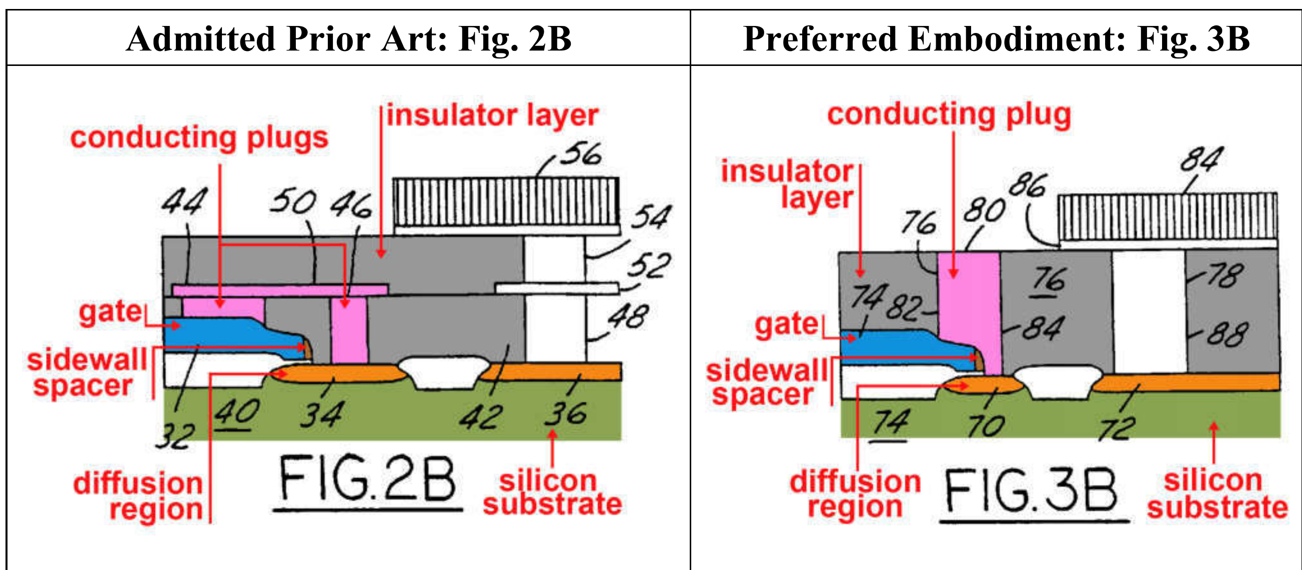


47. Figure 2B shows another prior art local interconnect structure, using what is called a "strapping" technique. To form this "strapping" local interconnect structure, a manufacturer creates two electrically conductive plugs (numbers 44 and 46)—one above the gate and one above a diffusion region. The manufacturer then places an electrically conductive "local strap" (number 50) on top of the plugs, electrically connecting the two plugs together. This local strap is also sometimes called a "shunt" or a "shunt layer." In combination, the two plugs and the local strap electrically connect the gate to a diffusion region. *See* '924 patent at 2:12-32 (Ex. 1001). According to the '924 patent, the problem with the strapping technique is that it requires a large number of manufacturing process steps, as well as significant space to accommodate the two plugs and the local strap. *See* '924 patent at 2:33-41 (Ex. 1001).

2. Summary of Invention of the ’924 Patent

48. The ’924 patent’s claimed structure includes nearly identical components as the prior art described in the specification. Specifically, both the claimed structure and the prior art include a substrate, a gate, a diffusion region, a sidewall spacer adjacent to the gate, and an insulating layer.

Admitted Prior Art: Fig. 2B | **Preferred Embodiment: Fig. 3B**



49. As shown in Figures 2B and 3B, in both the prior art of the ’924 patent and the structure of the disclosed embodiment, the gate is connected to the diffusion region (source or drain), by either two connected plugs, or a single plug. The diffusion region is located in a substrate and is not directly connected to the gate. The gate is substantially covered by an insulating layer.

50. The only feature that the patent describes as novel, which is shown in Figure 3B, is the use of a single metal plug to connect the gate and the diffusion region, rather than connecting the two components directly (as in the prior art

"buried contact" technique (Figure 1B)) or using two plugs (as in the prior art "strapping" technique (Figure 2B)). '924 patent at 2:64-67, 3:35-36 (describing Figure 3B as "a cross-sectional view of a preferred embodiment of the present invention."), 4:18-5:12, claims 1, 7 (Ex. 1001); *see also id.* at 2:42-63.

3. Prosecution History

51. The '924 patent issued from a "continued prosecution application" ("CPA") of U.S. App. No. 08/561,951. CPA Request dated Feb. 10, 1999 (Ex. 1005). During prosecution of the '924 patent, the Applicant tried to antedate a prior art reference, based on a lab notebook dated May 17, 1995. Amendment and Rule 131 Declaration dated Jan. 5, 1998 (Ex. 1006). For purposes of this Petition, I understand that the references relied upon by Petitioner all qualify as prior art even if the Patent Owner could ultimately prove a conception date as early as May 17, 1995.

52. According to this lab notebook, the novelty of the '924 invention arises from the use of a single plug—which is what allegedly leads to fewer processing steps as compared to known prior art techniques. *See* Rule 131 Declaration dated January 5, 1998, Exhibit A ("By ***placing a metallic plugged contact*** where poly is required to shunt to diffusion, contacts to [different types of] diffusion can be achieved …. [T]his will require no more layout area than the

traditional buried contact. This method has potential [manufacturing] process step savings of 8-11 steps over Trad. BC [traditional buried contact local interconnect (as shown in Figure 1B of the '924 patent)] and 6-8 steps over strapping [local interconnect (as shown in Figure 2B of the '924 patent)].") (Ex. 1006).

53. However, during prosecution, rather than relying on this "single plug" structure, the Applicant relied on other alleged differences to overcome the prior art applied by the Examiner. The present petition relies on prior art that was not before the Examiner. This prior art teaches not only the "single plug" aspect of the claims, but also all of the additional minor differences that the Applicant used to try to distinguish the Examiner's prior art.

a. The "sidewall spacer" limitations

54. The Examiner rejected the original claims under 35 U.S.C. § 102(e) based on U.S. Patent No. 5,451,434 to Nicholls ("Nicholls"). Office Action dated Nov. 7, 1996 at p. 3 (Ex. 1007). Nicholls taught a single metal plug that connects a diffusion region and a gate. In order to overcome the rejection, the Applicant added a limitation to the claims requiring a sidewall spacer adjacent to the gate. Amendment dated June 9, 1997 at pp. 2-3 (Ex. 1009). Nicholls expressly teaches the placement of a sidewall during manufacture, but also teaches that the sidewall can be completely or "partially removed" in a later manufacturing step. Nicholls at

4:25-32 (Ex. 1008). The Applicant overcame the rejection by arguing that the removal of the sidewall during manufacturing taught away from retaining a sidewall spacer adjacent to the gate. Amendment dated June 9, 1997 at pp. 3-4 (Ex. 1009). The prior art relied upon in this petition teaches the "sidewall spacer" limitation.

b. Direct electrical connection

55. The Examiner also rejected the claims under 35 U.S.C. § 102(e) based on U.S. Patent No. 5,541,427 to Chappell ("Chappell"). Office Action dated February 24, 1998 (Ex. 1010). Chappell taught a single metal plug that connects to both a diffusion region and a gate region. Chappell at 4:38-48 (Ex. 1011). The Applicant overcame the rejection by arguing that the metal plug of Chappell purportedly contacts a portion of the gate region that is not conductive, rather than the conductive portion of the gate itself. *See* Amendment dated April 23, 1998 at p. 4 ("'when the opening 42 is filled with an electrically conductive material, there is **no contact** to the electrically conductive portion of the gate stack'") (emphasis in original) (quoting Chappell at 4:38-48) (Ex. 1012). The prior art references relied upon in this petition teach a direct electrical connection between the diffusion region and the electrically conductive portion of the gate.

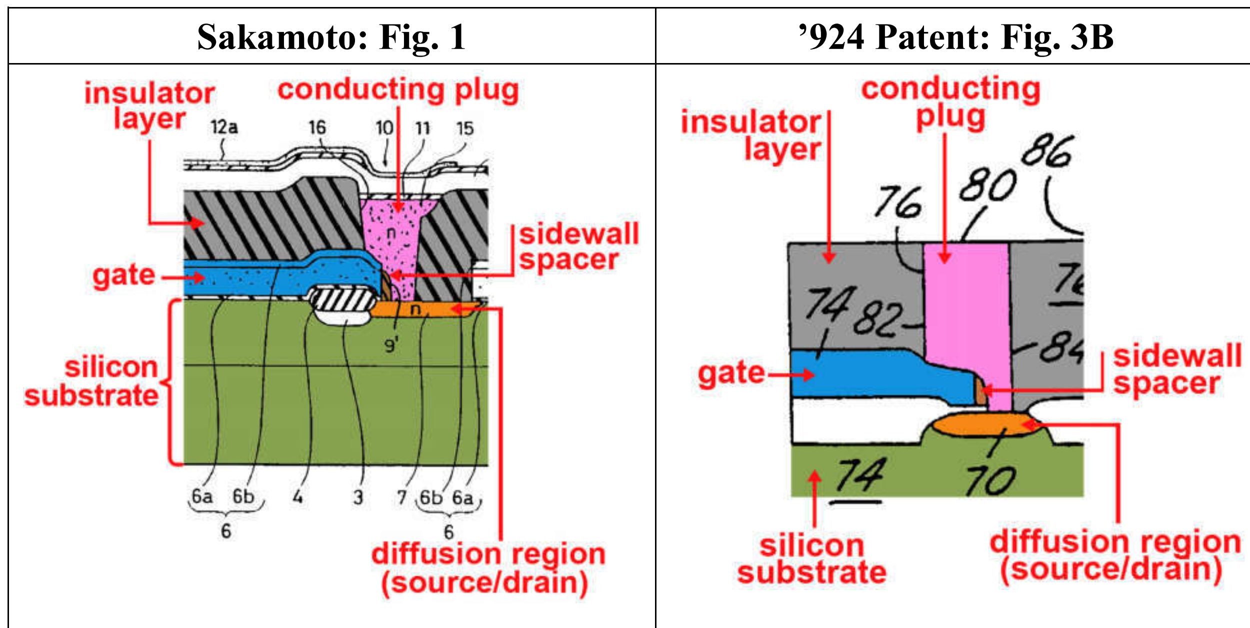
V. OVERVIEW OF THE PRIMARY PRIOR ART REFERENCES

56. The claimed invention of the ’924 patent—using a single plug to electrically connect the gate to the diffusion region—was well-known as of the May 17, 1995 purported conception date.

A. Overview of Sakamoto (Ex. 1003)

57. Sakamoto was filed on August 19, 1994, as a continuation of an earlier application filed on March 4, 1992, and issued on December 12, 1995. I understand that Sakamoto is prior art to the ’924 patent under 35 U.S.C. § 102(e).

58. Sakamoto is directed to precisely the same problem as the ’924 patent—how to effectively and efficiently connect different transistor portions together—and discloses precisely the same solution claimed in the ’924 patent—using a single plug. Sakamoto at 4:45-49 (“The first interconnection structure comprises a silicon plug layer embedded within an opening formed in the interlevel insulating layer and connected to both gate electrode of the first MOS drive transistor and source/drain region of the second MOS transfer transistor…”) (Ex. 1003); *see also id.* at 1:13-14. Figure 1 of Sakamoto shows a structure with the same components arranged in the same way as shown in Figure 3B of the ’924 patent. *Id.* at Fig. 1; ’924 patent at Fig. 3B (Ex. 1001).



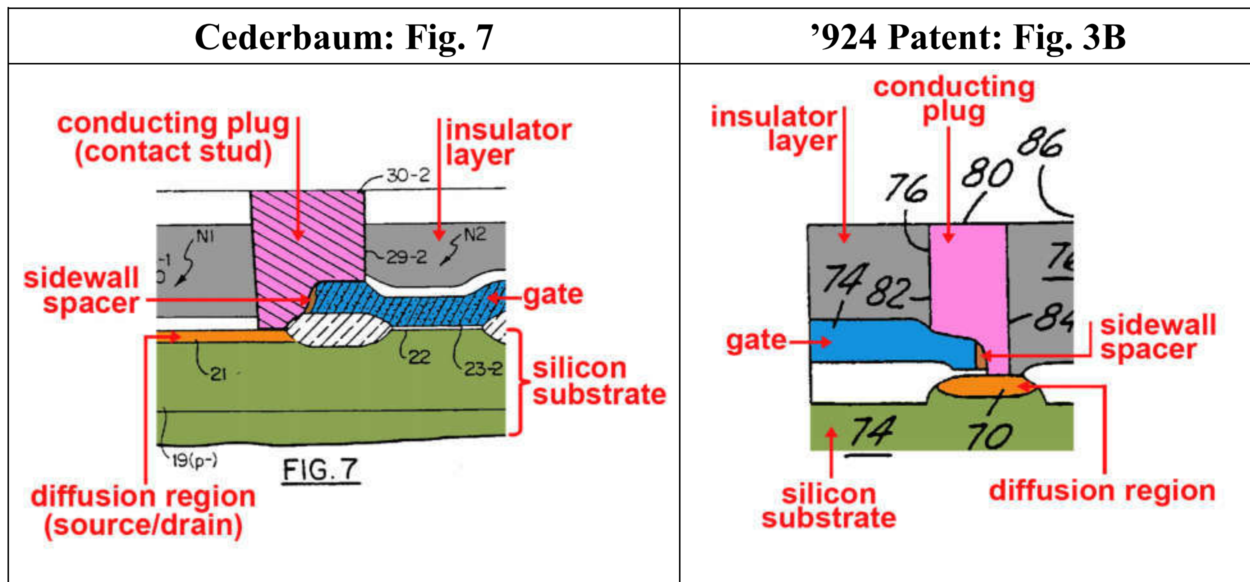
59. Both Figure 1 of Sakamoto and Figure 3B of the ’924 patent show a cross-sectional structure with a single plug. The plug fills an opening (labeled 16 in Sakamoto) containing a sidewall spacer and directly electrically connects a diffusion region to a gate. The diffusion region is located in a substrate and is not directly connected to the gate. The gate is also substantially covered by an insulating layer. *See* Sakamoto at 6:52-58 (“An opening 16 is formed in an interlevel insulating layer 9. An n+ source/drain region 7 of an n channel MOS transfer transistor 22b and a gate electrode 6 of an n channel MOS drive transistor 20a are exposed at the bottom of opening 16. A plug layer 15 of polycrystalline silicon directly connected to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16.”), 7:47-51 (“An opening 16 for direct contact is formed in interlevel insulating layer 9 … formation of the opening 16 leaving a

sidewall spacer 9' from the interlevel insulating layer 9 …”), 7:26-27 (“Oxide films 5 form gate oxide films 5,5 of MOS transistors 20a, 22b.”) (Ex. 1003); *see also* ’924 patent at 3:46-4:17 (Ex. 1001). Thus, Sakamoto and the ’924 patent both solve the same problem of connecting different transistor portions (e.g., source/drain to gate) by using a single plug interconnect. Sakamoto at 6:49-7:13 (Ex. 1003).

B. Overview of Cederbaum (Ex. 1004)

60. Cederbaum issued on March 31, 1992, and I understand that it is prior art under 35 U.S.C. § 102(b). Figure 7 of Cederbaum also discloses a structure that includes components arranged in a way that is identical in all relevant aspects as the structure in Figure 3B of the ’924 patent. Cederbaum at Fig. 7 (Ex. 1004); ’924 patent at Fig. 3B (Ex. 1001).

Cederbaum: Fig. 7	’924 Patent: Fig. 3B



61. Both Figure 7 of Cederbaum and Figure 3B of the '924 patent show a single plug (which Cederbaum calls a "contact stud"). The plug fills an opening (labeled 28-2 (Figure 6) in Cederbaum) containing a sidewall spacer and directly connects the source/drain region to the gate. *See* Cederbaum at Figs. 4-7, 7:33-49 (Figs. 4-7 show "active regions 21… to constitute the source and drain regions" and "[n]umeral[] … 23-2 designate[s] … the gate electrodes … ."), 7:49-57 ("Oxide sidewalls or spacers 24 have been formed on the lateral sides of the polysilicon gate electrodes for a better definition of the channel length of NFETs.") (Ex. 1004). The diffusion region is located in a substrate, and not directly connected to the gate, which is substantially covered by the insulating layer. Cederbaum at 7:33-40 ("The starting material consists of a conventional P^+ silicon substrate 18 having a P^- epitaxial layer 19…. N^+ implanted active regions 21 have been formed in the epitaxial layer 19 to constitute the source and drain regions…."), 8:26-50 (explaining the formation of the insulating phosphosilicate glass (PSG) layer 26 over the gate and substrate) (Ex. 1004). The contact stud is created by filling the opening with a "highly conductive material" that is "typically a metal." *Id.* at 9:32-34, 9:35-43 ("Prior to tungsten (W) filling, a titanium (Ti) layer is deposited" followed by "a thin titanium nitride (TiN).").

VI. CLAIM CONSTRUCTION

62. The ’924 patent expired on November 22, 2015. Accordingly, I as noted above, I understand that I should apply the claim construction based on the *Phillips* standard rather than the broadest reasonable interpretation standard applicable to non-expired patents.

63. The term “diffusion region formed in said substrate” is an element of all challenged claims. I conclude that the term should be construed to mean a “conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon substrate.” In a pending litigation, I understand that the Patent Owner has proposed to construe the term as a “conductive terminal region such as a source or drain formed in said substrate.” The Patent Owner thus agrees with me that the term requires a conductive terminal region, such as a source or drain, formed in the substrate. As a result, the only dispute between the Patent Owner and myself is whether the diffusion region “contains dopants implanted in the silicon substrate.” The patent makes clear that it does.

64. The plain language of the claims requires the diffusion region to be formed in the silicon substrate. Claim 1, for example, requires a “diffusion region formed in said [silicon] substrate.” ’924 patent at claim 1 (Ex. 1001). Similarly, claim 7 requires a “diffusion region in a silicon substrate.” *Id.* at claim 7. The

specification then explains, in a section describing “[t]he present invention,” that the diffusion region is formed in the substrate by implanting dopants in the substrate:

> The present invention provides a semiconductor structure that has a metal plug local interconnect (or shunt) for connecting a polysilicon gate to a diffusion region in a structure and a method of forming such a semiconductor structure.
>
> Referring initially to FIGS. 3A and 3B wherein an enlarged top view and a cross-sectional view of the ***present invention*** metal plug local interconnect is shown, respectively. Diffusion regions 70 and 72 of either ***N+ or P+ doping*** are first formed by an ***ion implantation*** process in the ***surface of the silicon substrate*** 74.

’924 patent at 3:40-51 (Ex. 1001); *see also id.* at 1:36-38 (explaining that the “ion implantation process … increase[s] the surface dopant concentration” in substrate), 1:21-22 (describing “region doped by impurity ions in a semiconductor substrate”). The ’924 patent does not describe any way of forming diffusion regions in a silicon substrate other than by implanting dopants in the substrate. Accordingly, the ’924 patent makes clear that the claimed diffusion regions contain dopants implanted in the substrate.

65. Moreover, at the time of the alleged invention of the '924 patent, one skilled in the art would have readily understood that a diffusion region is a conductive terminal region, such as a source or drain, that contains dopants implanted in the substrate. In order to form a diffusion region in a substrate, the dopants need to be inserted into the substrate. As the '924 patent explains, at the time of the alleged invention, this was done by implanting dopants into the substrate. This is confirmed by contemporaneous prior art references. Sakamoto and Nicholls, for example, teach the use of ion implantation to form a diffusion region. Sakamoto at 7:32-38 ("N type impurity ***ion*** … is ***implanted*** … by an ion implantation method…. Thus, ***n+ source/drain regions*** … are formed.") (Ex. 1003); Nicholls at 2:64-66 ("As shown in FIG. 1b, a ***dopant*** is then ***implanted*** into the silicon substrate so as to form active silicon implant regions 8, 10"), 3:55-4:13 (Ex. 1008).

66. Accordingly, the term "diffusion region formed in said substrate" should be construed to mean a "conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon substrate."[2]

VII. LEVEL OF ORDINARY SKILL IN THE ART

67. In my opinion, a person of ordinary skill in the art at the time of the alleged invention would have had at least a B.S. degree in electrical engineering or materials science (or equivalent experience), and would have at least two or three years of experience with semiconductor device fabrication and design. I met and/or exceeded these requirements for one of ordinary skill in the art at the time of the filing of the '924 patent.

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[2] I am informed and understand that in pending litigation between the Patent Owner and a Petitioner, the parties have proposed competing constructions for one additional limitation. I have reviewed these competing constructions and determined that the prior art meets these limitations under either party's construction, so I have not attempted to construe them for the purposes of this petition. The prior art also discloses the required "diffusion region formed in said substrate" limitation under either party's construction.

VIII. SPECIFIC GROUNDS FOR PETITION

68. The sections below demonstrate in detail how the prior art discloses the limitations of the challenged claims of the '924 patent, and how those claims are anticipated and/or rendered obvious by the prior art.

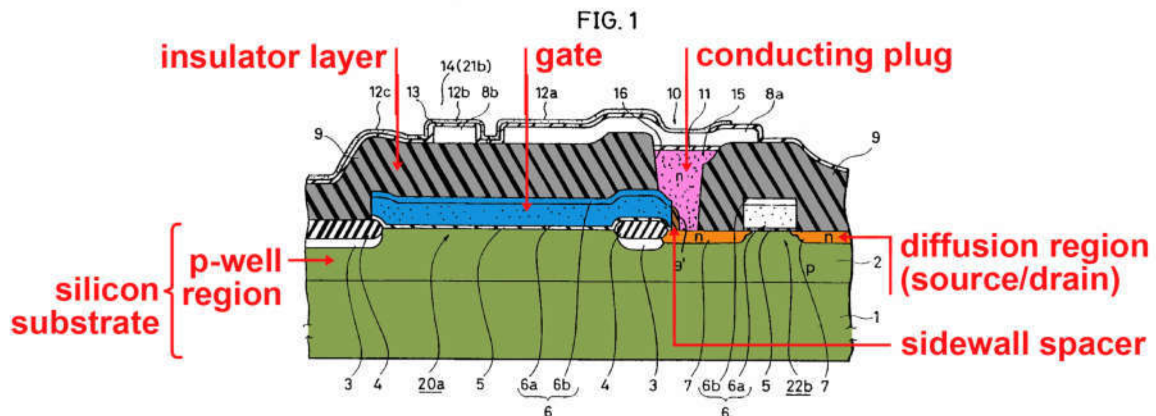
A. Ground I: Claims 1-3, 14 and 16 are anticipated by Sakamoto

1. Independent Claim 1

69. Sakamoto discloses each and every element of claim 1 and thus, anticipates the claim under 35 U.S.C. § 102(e).

a. "A semiconductor structure comprising:"

70. Figure 1 of Sakamoto (shown below) discloses "a semiconductor structure." One skilled in the art would understand that the SRAM memory cell of Sakamoto discloses "a semiconductor structure."



Sakamoto at Fig. 1, 6:39-8:52 (describing Figure 1), Title ("Contact structure of an interconnection layer for a ***semiconductor device*** and a multilayer interconnection

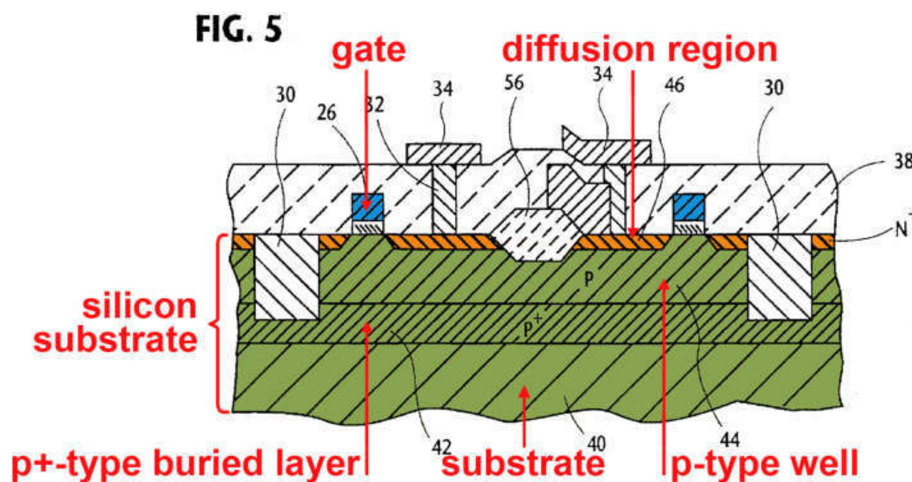
SRAM"), 1:13-16 ("The present invention relates to improvement of a contact structure of an interconnection in a region having steps in ***a semiconductor device*** having a multilayer interconnection structure.") (Ex. 1003); *see also id.* at claims 1-9, Abstract, Title, 1:18-3:35, 3:60-4:2, 5:1-18, 5:33-50, 13:13-25.

b. [a]: "a silicon substrate having a top surface"

71. One skilled in the art would understand that the semiconductor structure of Figure 1 of Sakamoto discloses a silicon substrate having a top surface—namely, silicon substrate 1, containing p-well region 2—for several reasons. Sakamoto at Fig. 1 (Ex. 1003).

72. First, although Figure 1 shows a line delineating the p-well region 2, the text of Sakamoto makes clear to one skilled in the art that the p-well region 2 is a part of the silicon substrate 1 because the "p well 2" is formed in the "surface of substrate 1." *Id.* at 7:17-21 ("p type impurity ***is implanted in a main surface of a silicon substrate 1***... Subsequently, implanted p type impurity is ***diffused to the depth*** of about 2-3 μm ***from the main surface*** of substrate 1 by heat treatment to ***form a p well 2***."), 2:22-26; *see also id.* at 1:19-24, 4:14-19, 4:20-67, 6:39-48 (explaining the similarity between Figure 1 and background Figure 28), 7:40-43, 8:13-17, and claims 1, 4 and 7.

73. Second, during prosecution of the parent application for the ’924 patent, the Examiner similarly considered a p-type well formed in a silicon substrate to be part of the substrate, even though the relevant prior art figure shows them delineated with different labels. Specifically, as shown below in Figure 5 of U.S. Patent No. 5,453,640 (“Kinoshita”) (Ex. 1013), the prior art disclosed a diffusion region 46 that is formed within the p-type well 44 and shows the gate electrode 26 formed on a top surface of the p-type well 44:



Kinoshita at Fig. 5 (Ex. 1013); *id.* at 4:20-35 (identifying gate electrode 26, substrate 40, buried layer 42, p-type well 44, and diffusion region 46 in Figure 5), 3:34-35. Confirming that the Examiner considered the p-type well to be part of the substrate, the Examiner concluded that Figure 5 discloses “a semiconductor device comprising: a silicon substrate (40), a diffusion region (46) ***formed within*** said substrate, [and] a polysilicon gate electrode (26) ***formed on a top surface of*** said

substrate ….” April 17, 1996 Office Action at 3 (Ex. 1017). In my opinion this is consistent with what a person of ordinary skill in the art would understand.

74. In responding to the Examiner's rejection, the Applicant did not dispute the Examiner's assertion that the p-type well 44 was part of the substrate 40. In fact, the Applicant expressly acknowledged that another separately delineated layer in Figure 5—the buried layer 42—is also part of the substrate 40. *See* Amendment dated August 14, 1996 at 4 ("Kinoshita further teaches a block of static memory cells using CMOS transistors, wherein metal interconnections, e.g., ground lines for the CMOS transistors, are simplified by ***using buried layers in the substrate***… .") (Ex. 1014).

75. Third, the line delineating the p-well region 2 part of silicon substrate 1 is not present in all figures of Sakamoto, and Sakamoto elsewhere explicitly shows that regions, such as well regions, are formed in silicon substrate 1 (making clear that p-well region 2 is a part of the silicon substrate). *See* Sakamoto at Fig. 25, 12:57-58 ("On a surface of a silicon substrate 1, for example, an n type impurity region 30 is formed."), claim 1 ("…said first MOS transfer transistor and said second MOS transfer transistor being formed ***on the main surface of the silicon substrate*** … a source/drain region of said second MOS transfer transistor… a source/drain region of said first MOS transfer transistor…") (Ex. 1003). Thus,

one skilled in the art would understand that the p-well region 2 is part of silicon substrate 1 in the semiconductor structure disclosed in Sakamoto.

c. [b] "a diffusion region formed in said substrate adjacent to said top surface [of said substrate]"

76. As discussed above in the Claim Construction section, the term "diffusion region formed in said substrate" should be construed as a "conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon substrate." Sakamoto discloses the claimed diffusion region.[3]

77. Figure 1 of Sakamoto discloses a diffusion region (n+ source/drain region 7) formed in the substrate (silicon substrate 1 with p-well region 2) adjacent to the top surface of the substrate.

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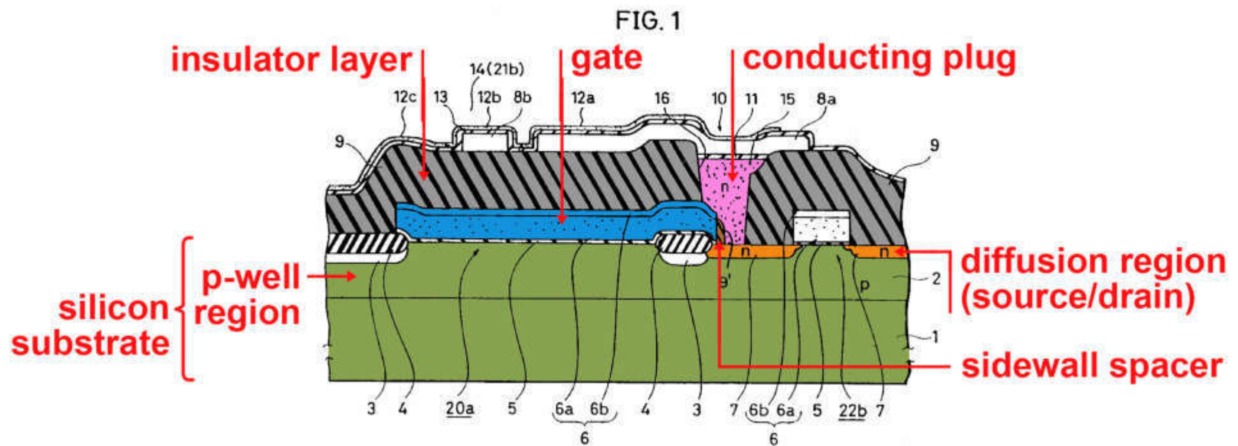
[3] Even the '924 patent notes that a diffusion region formed in a substrate adjacent to the top surface of the substrate was known to a person of ordinary skill in the art at the time of the '924 patent. *See* '924 patent at prior art Fig. 2B, 2:15-20 ("a polysilicon gate 32 is first formed without direct contact with the diffusion region 34 and 36 in a silicon substrate 40.") (Ex. 1001).



Sakamoto at Fig. 1 (Ex. 1003).

78. As shown in Figure 1 above, the p-well region 2 is formed below the top surface of the silicon substrate 1, and the source/drain region 7 is formed below the top surface of the p-well region 2 (and thus below the top surface of the substrate). *See* Sakamoto at Fig. 1 (Ex. 1003); *see also id.* at 2:23-29 ("[a]n n channel MOS drive transistor 20a and an n channel MOS transfer transistor 22b each comprises n+ source/drain regions 7, 7, a gate oxide film 5 and gate electrode 6."), claim 1 ("…said first MOS transfer transistor and said second MOS transfer transistor being formed ***on the main surface of the silicon substrate*** … ***a source/drain region*** of said second MOS transfer transistor… ***a source/drain region*** of said first MOS transfer transistor…"), Title, Abstract, 1:13–16, 2:23-29, 3:60-4:2, 4:20-67, 5:1-18, 5:33-50, 6:39-61, 7:14-39, 12:57-58, 13:13-25.

79. Sakamoto further teaches that the diffusion region contains dopants implanted in the silicon substrate. Sakamoto at 7:17-21 ("p type impurity ***is implanted in a main surface of a silicon substrate 1***... Subsequently, implanted p type impurity is ***diffused to the depth*** of about 2-3 µm ***from the main surface of substrate 1*** by heat treatment to ***form a p well 2***."), 7:32-38 ("N type impurity ion … ***is implanted into p well 2*** by an ion implantation method… Thus, n+ source/drain regions 7 … are formed.") (Ex. 1003).

80. Finally, Sakamoto teaches that the diffusion region is a "conductive terminal region, such as a source or drain," because it constitutes a source/drain region 7 of a transistor and electrically connects the transistor to other components in the semiconductor structure. Sakamoto at 6:51-61 ("An n+ source/drain region 7 of an n channel MOS transfer transistor 22b and a gate electrode 6 of an n channel MOS drive transistor 20a are exposed at the bottom of opening 16. A plug layer 15 of polycrystalline silicon directly connected to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16. N type impurity… is introduced into polycrystalline silicon plug layer 15 in order to provide conductivity."), claim 1 ("…said first MOS transfer transistor and said second MOS transfer transistor being formed ***on the main surface of the silicon substrate***

… ***a source/drain region*** of said second MOS transfer transistor… ***a source/drain region*** of said first MOS transfer transistor…”) (Ex. 1003).[4]

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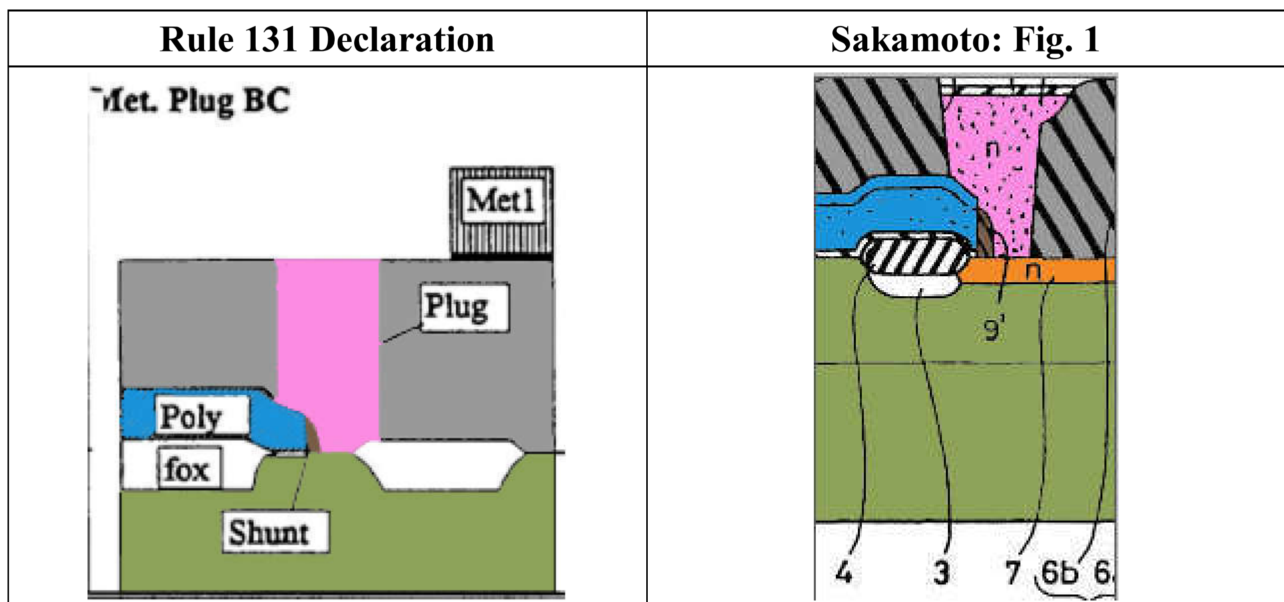
[4] I am informed and understand that in pending litigation between the Patent Owner and a Petitioner, the Patent Owner has proposed to construe “diffusion region formed in said substrate” as “conductive terminal region such as a source or drain formed in said substrate.” Sakamoto teaches the Patent Owner’s construction as well because, as I explained above, it teaches a diffusion region that is a conductive terminal region such as a source or drain (Sakamoto at 6:51-61 (Ex. 1003)) and that is formed in the substrate (*id.* at Fig. 1, 7:17-38). Accordingly, even under the Patent Owner’s construction, Sakamoto discloses this claim limitation.

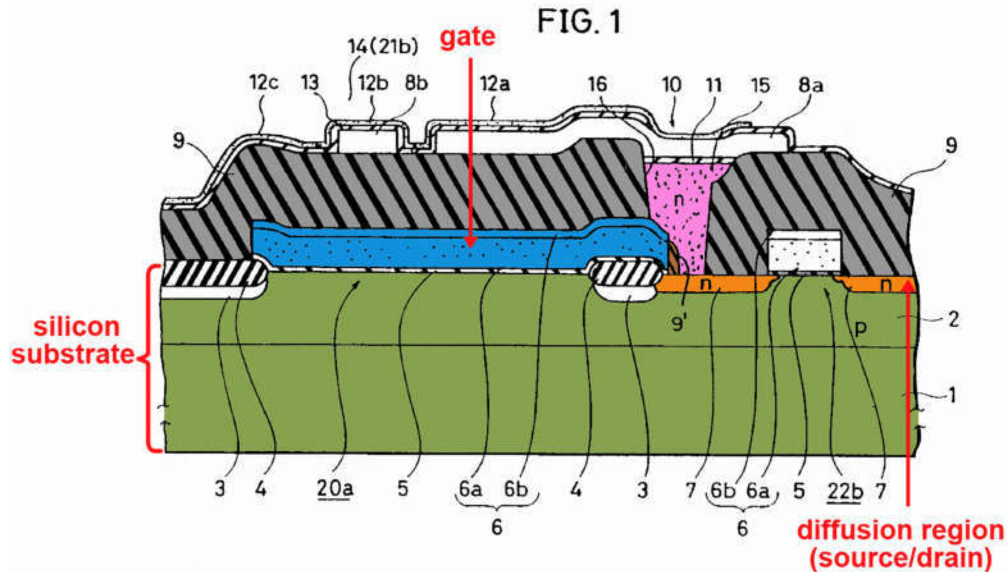
d. [c]: "a gate formed on the top surface of said substrate juxtaposed to but not contacting said diffusion region"

81. Sakamoto discloses a gate (gate electrode 6) formed on the top surface of the substrate (silicon substrate 1 with p-well region 2):[5]

[5] Sakamoto shows the gate on top of a "field oxide film 4." Sakamoto at 7:17-29 (Ex. 1003). Applicant's purported conception documents also show the gate over the same field oxide (labeled "fox"). Accordingly, Sakamoto's gate is formed on the top surface of the substrate, just like the '924 patent's gate is formed on the top surface of the substrate.



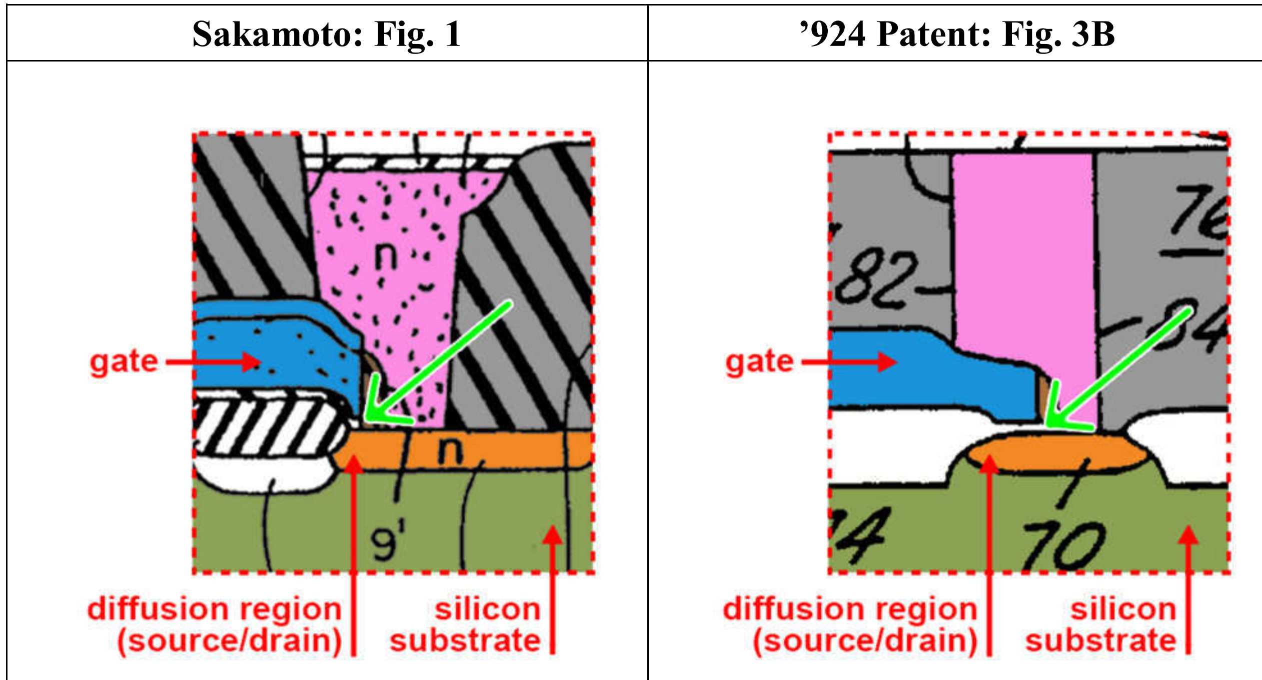
Rule 131 Declaration, Exhibit A (Ex. 1006); Sakamoto at Fig. 1 (Ex. 1003).



Sakamoto at Fig. 1, 6:52-58 ("A plug layer 15 of polycrystalline silicon directly connected to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16."), 7:17-32 ("a silicon substrate 1 … form gate electrodes 6, 6 of MOS transistors 20a, 22b…") (Ex. 1003); *see also id.* at claim 1, 2:23-32, 4:20-67, 6:39-7:7, 7:17-52, 12:57-58.

82. As shown in Figure 1, Sakamoto also discloses that the gate is juxtaposed to but not contacting the diffusion region (n+ source/drain region 7), as shown by the white space identified by the green arrow separating the gate from the diffusion region:

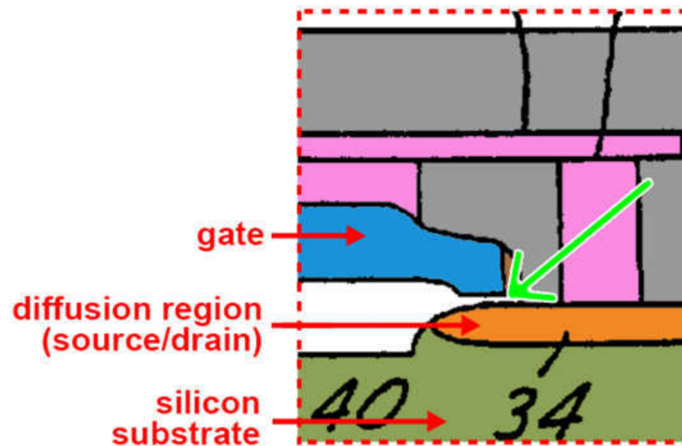
Sakamoto: Fig. 1	’924 Patent: Fig. 3B



83. The white region is an oxide film 5 that separates the gate from the diffusion region. Sakamoto at Fig. 1, 7:24-27 (“Oxide films 5 of 12 nm-15 nm thickness are formed on the surface of the p well 2…. Oxide films 5 form gate oxide films 5,5 of MOS transistors 20a, 20b.”) (Ex. 1003); *see also id.* at 2:23-31, 6:42-45, 6:52-58, 6:66-7:7, 7:17-52, 12:57-58. This is identical to the structure shown above in Figure 3B of the ’924 patent. ’924 patent at Fig. 3B (Ex. 1001). Indeed, there would be no need for a plug to connect the gate and diffusion region if they were directly connected. *See, e.g.*, *id.* at Figs. 1A, 1B, 1:24-2:10

(describing the prior art buried contact approach where gate and diffusion region are directly connected and there is no plug).[6]

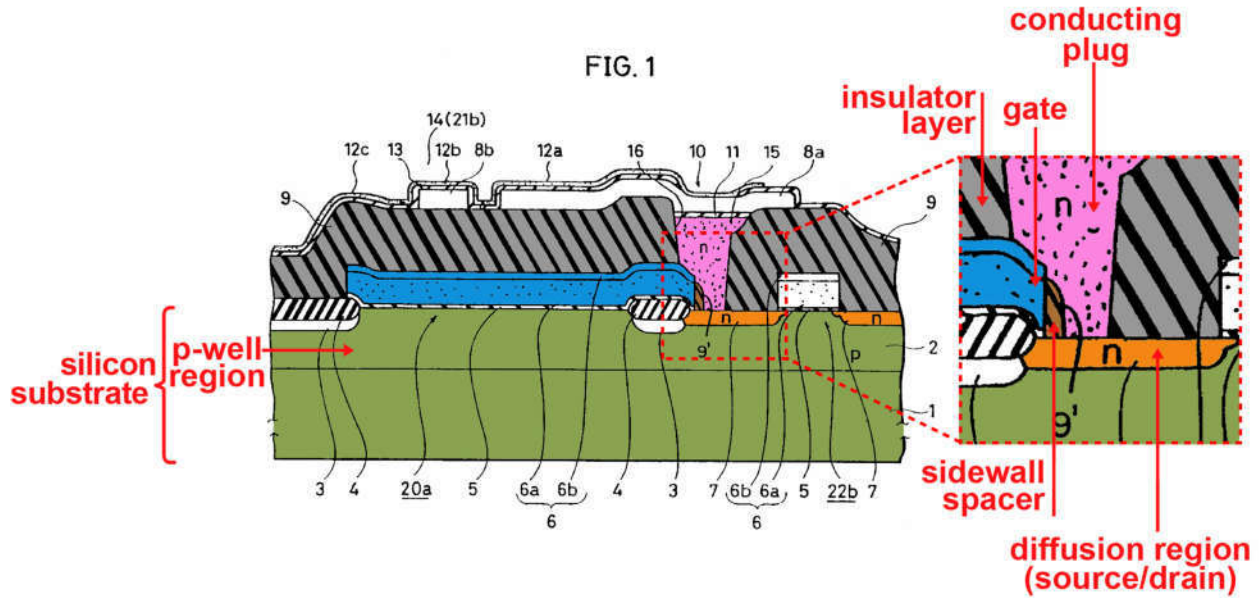
[6] As is shown in Figure 2B of the prior art, even the '924 patent notes that a gate formed on a top surface of a substrate, juxtaposed to but not contacting a diffusion region, was known to a person of ordinary skill in the art at the time of the '924 patent:



'924 patent at prior art Fig. 2B, 2:15-20 ("a polysilicon gate 32 is first formed without direct contact with the diffusion regions 34 and 36 in a silicon substrate 40.") (Ex. 1001).

e. [d]: "a sidewall spacer adjacent to said gate and disposed above said diffusion region"

84. Figure 1 of Sakamoto discloses a sidewall spacer (sidewall spacer 9') adjacent to the gate electrode 6 and disposed above the diffusion region 7:



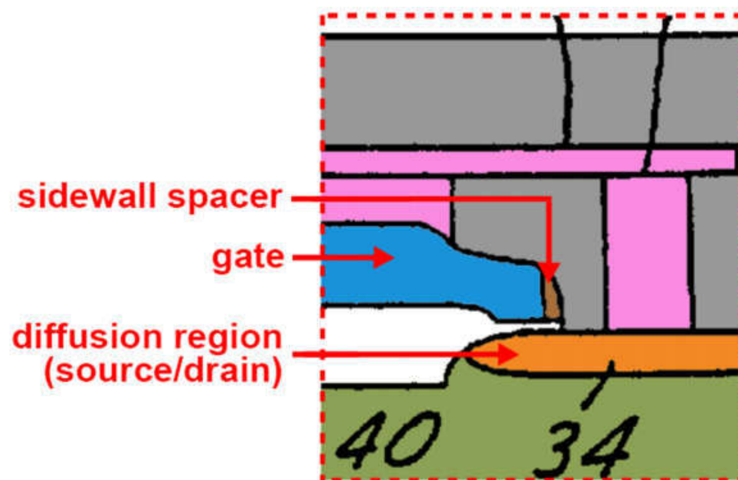
Sakamoto at Fig. 1, 7:44-52 ("a sidewall spacer 9'" is located in the "opening 16"), claims 6 and 9 (Ex. 1003).[7]

f. [e]: "an insulator layer substantially covering said gate and said diffusion region"

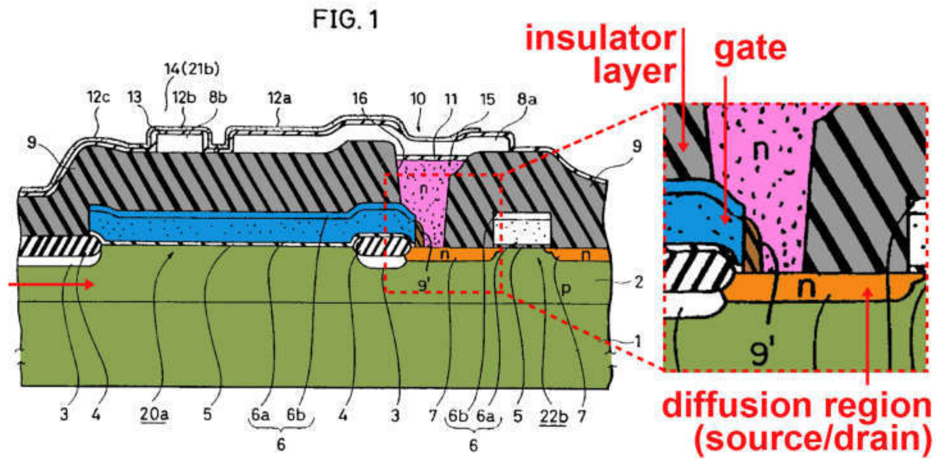
85. Figure 1 of Sakamoto discloses an insulator layer (insulating layer 9) substantially covering the gate electrode 6 and the diffusion region 7.

---

[7] As is shown in Figure 2B of the prior art, even the '924 patent notes that a sidewall spacer adjacent to the gate and disposed above the diffusion region was known to a person of ordinary skill in the art at the time of the '924 patent:



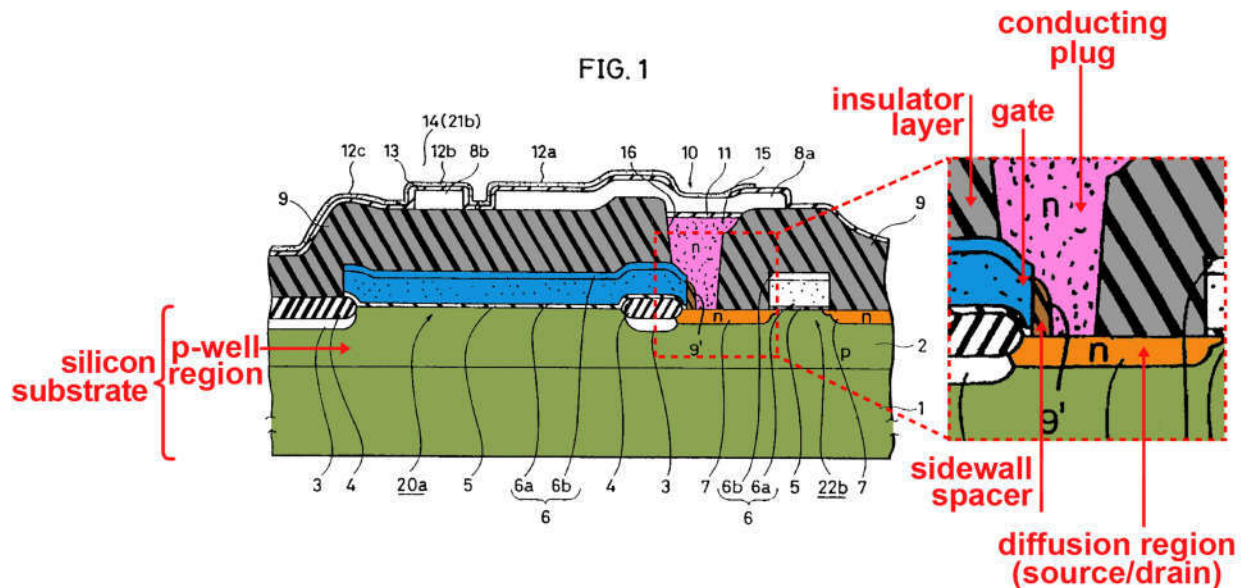
'924 patent at prior art Fig. 2B (Ex. 1001).



Sakamoto at Fig. 1, 7:40-47 ("Subsequently, a BPSG (BoroPhospho Silicate Glass) film is deposited on the whole surface of silicon substrate 1 …. In this step, an interlevel insulating layer 9 having a planarized surface is formed."), 2:47-53 ("[a]n opening 16 is formed in interlevel insulating layer 9. Inside opening 16, gate electrode 6 of n channel MOS drive transistor 20a and one of n+ source/drain regions 7 of n channel MOS transfer transistor 22b is exposed.") (Ex. 1003); *see also id.* at Fig. 2, Abstract, claims 1, 4, and 7, 2:33-34, 3:60-63, 4:20-67, 5:3-6, 5:20-23, 5:35-38, 6:39-7:14, 7:47-52.

g. *[f]: "a conducting plug at least partially filling a via in said insulation layer that exposes said sidewall spacer in the absence of said conducting plug, said conducting plug providing direct electrical communication between said gate and said diffusion region."*

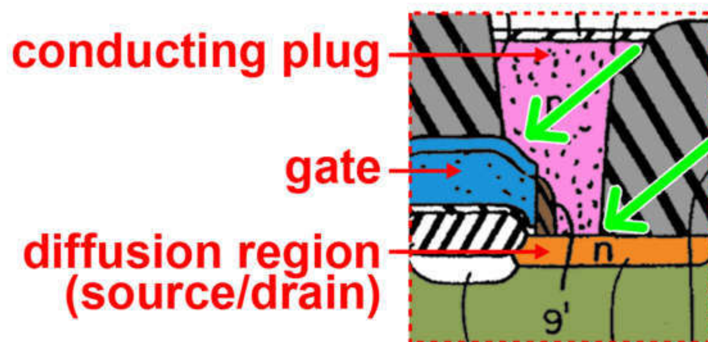
86. Sakamoto discloses the claimed conducting plug. Figure 1 of Sakamoto shows (and Sakamoto explains) a conducting plug (plug layer 15) at least partially filling a via (opening 16) in the insulating layer (insulating layer 9):



Sakamoto at Fig. 1 (Ex. 1003); *see also id.* at Figs. 2-5, claims 1, 4, and 7, 6:49-7:14 ("An opening 16 is formed in an interlevel insulating layer 9 …. A plug layer 15… directly connected to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16."), 7:15-8:12 (plug layer 15 is formed when "[p]olycrystalline silicon layer 15a is deposited … to fill opening 16 [and] is etched, leaving a portion of the … layer only within opening 16….").

87. As shown in the figure above, absent the plug 15, the sidewall spacer 9' would be exposed by the via. *Compare* Sakamoto at Fig. 2 (showing sidewall spacer 9' exposed in opening 16 during manufacturing process before plug 15 is formed) *with* Fig. 4 (showing plug 15 covering sidewall spacer 9' later in the process) (Ex. 1003). *See also id.* at Fig. 1, 6:52-55 ("[a]n n+ source/drain region 7 … and a gate electrode 6 … are ***exposed*** at the bottom of opening 16"), 7:46-50 ("a sidewall spacer 9'" is located in the opening 16), 2:49-52, claims 4, 6, 7 and 9. Because Sakamoto teaches the source/drain 7 region and gate electrode 6 are "exposed" by opening 16, the sidewall spacer 9' is also exposed by the opening 16.

88. Figure 1 also shows (and Sakamoto explains) that the conducting plug provides direct electrical communication between the gate and the diffusion region:



Sakamoto at Fig. 1, 6:49-7:14 ("An opening 16 is formed…. A plug layer 15 of polycrystalline silicon ***directly connected*** to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16. N type impurity … is introduced into

polycrystalline silicon plug layer 15 ***in order to provide conductivity***."), 1:45-57 (Ex. 1003). As Figure 1 shows, the plug layer 15 directly touches both of those elements and is a "conducting" plug. *Id.* at Fig. 1, 6:56-61; *see also id.* at 6:66-7:13, 7:47-50, 7:53-61, claims 1-4, 6, 7 and 9.

2. Claim 2: "A semiconductor structure according to claim 1, wherein said diffusion region is an N+ or a P+ region"

89. Sakamoto discloses that the diffusion region (n+ source/drain region 7) is "an N+ or a P+ region" (*i.e.*, an n+ region).[8] Specifically, Sakamoto discloses that the diffusion region is an "N+ … region," because it expressly refers to the diffusion region as an "***n+*** source/drain region 7." Sakamoto at 6:52-58 ("An ***n+*** source/drain region 7 [is] exposed at the bottom of opening 16."), 7:32-38 ("Thus, ***n+*** source/drain regions 7 of four MOS transistors 20a, 20b, 22a, 22b are formed.") (Ex. 1003); *see also id.* at 2:22-29.

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[8] Even the '924 patent notes that N+ and P+ diffusion regions were known to a person of ordinary skill in the art at the time of the '924 patent. *See* '924 patent at 1:15-2:11 ("In the semiconductor fabrication process, it is frequently required to make local interconnect between a gate polysilicon layer to N+ and P+ diffusion regions.") (Ex. 1001).

3. Claim 3: "A semiconductor structure according to claim 1, wherein said insulator layer is formed of a material selected from the group consisting of silicon oxide and silicon nitride."

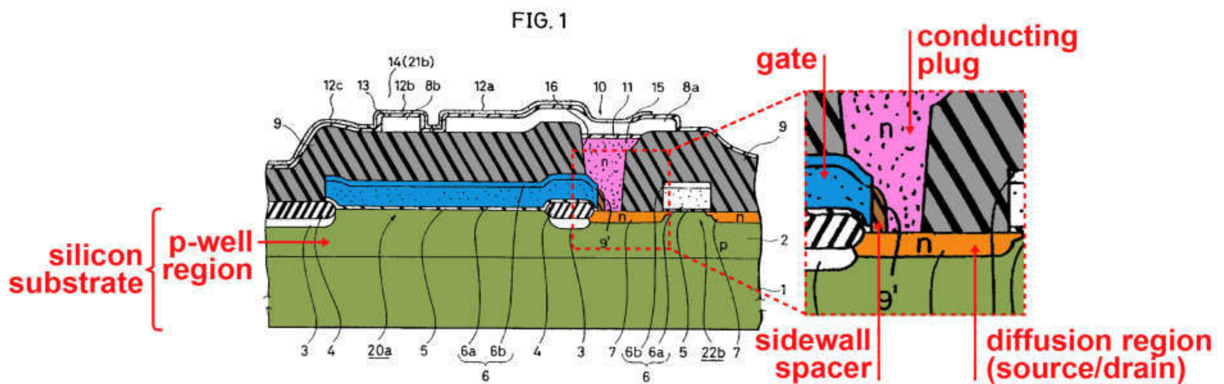
90. Sakamoto discloses forming the insulating layer 9 from a BPSG (BoroPhospho Silicate Glass) film. Sakamoto at 7:39-47 ("a BPSG (BoroPhospho Silicate Glass) film … is softened and reflowed by heat treatment, so that a surface of the BPSG film is planarized. In this step, an interlevel insulating layer 9 … is formed.") (Ex. 1003). A person of skill in the art would readily recognize that BPSG is a type of silicon oxide. *See* Hiatt (1994) at p. 185 ("Doped silicon oxides such as phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG)…") (Ex. 1015); '924 patent at 3:61-63 ("an insulating layer 76 of ***silicon oxide***"), 4:39 ("#13-Nit/***BPSG***"), 4:52 ("#13-Nit/***BPSG***") (Ex. 1001).

91. A person of ordinary skill would further recognize that silicon oxide and silicon nitride are commonly used interchangeably in semiconductor structures. For example, even the '924 patent itself, in discussing the "prior art interconnect" structures at column 1:15-2:45, discloses the interchangeability of the silicon oxide ("BPSG") with silicon nitride ("Nit"). '924 patent at 4:39 ("#13-***Nit/BPSG***"), 4:52 ("#13-***Nit/BPSG***") (Ex. 1001).

92. Thus, one skilled in the art would understand that Sakamoto discloses an insulator layer formed of a material selected from a group consisting of silicon oxide and silicon nitride, *i.e.*, formed of either silicon oxide or silicon nitride.

4. Claim 14: "A semiconductor structure according to claim 1, wherein said polysilicon gate and said diffusion region being exposed in said via in the absence of said conducting plug."

93. Sakamoto discloses that the polysilicon gate 6 and the diffusion region 7 would be exposed in the via (opening 16) in the absence of the conducting plug 15.



Sakamoto at Fig. 1, 6:52-55 ("[a]n n+ source/drain region 7 … and a gate electrode 6 … are exposed at the bottom of opening 16."), Fig. 2 (showing gate 6 and source/drain region 7 exposed in via (opening 16) before plug 15 is formed) (Ex. 1003); *see also id.* at 2:28-32, 2:49-52, 7:27-32, claims 4, 6, 7 and 9.

5. Claim 16: "The structure according to claim 1, wherein said gate comprises polysilicon."

94. Sakamoto discloses that the gate electrode 6 comprises polysilicon.[9] Polysilicon is also known as "polycrystalline silicon." Cederbaum at 1:17 ("polycrystalline silicon (polysilicon)") (Ex. 1004); Seto (1975) at Introduction (Ex. 1016) ("polycrystalline silicon (polysilicon)"). Sakamoto discloses that the gate electrode 6 is "formed of polycrystalline silicon" (*i.e.* polysilicon). Sakamoto at 2:28-32, 2:49-52, 7:27-32 ("A polycide film formed of polycrystalline silicon 6a and refractory metal silicide 6b … is patterned … to form gate electrodes 6, 6 ….") (Ex. 1003).

B. Ground II: Claims 4-6 and 13 are obvious in view of the combination of Sakamoto and Cederbaum

95. Dependent claims 4-6 and 13 add limitations specifying particular (and obvious design) choices for the material used in the conducting plug.

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[9] Even the '924 patent notes that a polysilicon gate was known to a person of ordinary skill in the art at the time of the '924 patent. *See* '924 patent at 2:11-32 ("a polysilicon gate 32 is first formed without direct contact with the diffusion regions 34 and 36 in a silicon substrate."), 1:15-1:24 ("In the semiconductor fabrication process, it is frequently required to make local interconnect between a gate polysilicon layer to N+ and P+ diffusion regions."), 1:25-2:11 (Ex. 1001).

Sakamoto, when combined with Cederbaum, renders obvious these claims under 35 U.S.C. § 103(a). Each of these claims depends from claim 1. Therefore the analysis with respect to claim 1 as set forth above in Ground I is incorporated by reference.

1. Claim 4: "a semiconductor structure according to claim 1, wherein said electrically conducting plug is a metal plug" / Claim 5: "a semiconductor structure according to claim 1, wherein said electrically conducting plug is a refractory metal plug." / Claim 6: "a semiconductor structure according to claim 1, wherein said electrically conducting plug is formed of a material selected from the group consisting of titanium, tantalum, molybdenum and tungsten"

96. Sakamoto discloses an electrically conducting plug made of polycrystalline silicon. Sakamoto at 6:56-58 ("plug layer 15 of ***polycrystalline silicon*** directly connected to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16.") (Ex. 1003); *see also id.* at 6:66-7:13, 7:53-62, 8:7-21, 9:67-10:23.

97. Claim 4: Cederbaum discloses an electrically conducting plug (contact stud 30-2) which is a metal plug formed of tungsten, thereby disclosing the limitations of claim 4. Cederbaum at 9:31-65 ("[Prior to ***tungsten (W) filling***, a titanium (Ti) layer is deposited [in] the first stud openings 28-1, 28-2 and 28-3…. Next, a thin titanium nitride (TiN) layer is formed over the titanium layer…. A ***tungsten layer*** is then deposited … to entirely fill the first stud openings.…

Planarization of the Ti-TiN and ***W [i.e., tungsten]*** composite layer produces first contact pads 29 and ***first contact studs 30*** in first stud openings 28."), claim 14 (Ex. 1004).

98. Claim 5: Cederbaum's tungsten metal plug (contact stud 30-2) is also a refractory metal plug, which meets the requirement of claim 5. *See, e.g.*, Cederbaum at 9:31-65, claim 14 (Ex. 1004); '924 patent at 1:53-54 ("A ***refractory metal plug such as a tungsten plug*** is then deposited…") (Ex. 1001); Nicholls at 6:41-60 ("refractory metal such as tungsten" and "[e]xamples of such selectively depositable refractory metals are tungsten, copper, molybdenum and tantalum.") (Ex. 1008).

99. Claim 6: Finally, as already stated above, Cederbaum discloses an electrically conducting plug (contact stud 30) formed of tungsten, which is a material selected from the group consisting of titanium, tantalum, molybdenum and tungsten, as required by claim 6. Cederbaum at 9:31-65, claim 14 (Ex. 1004).

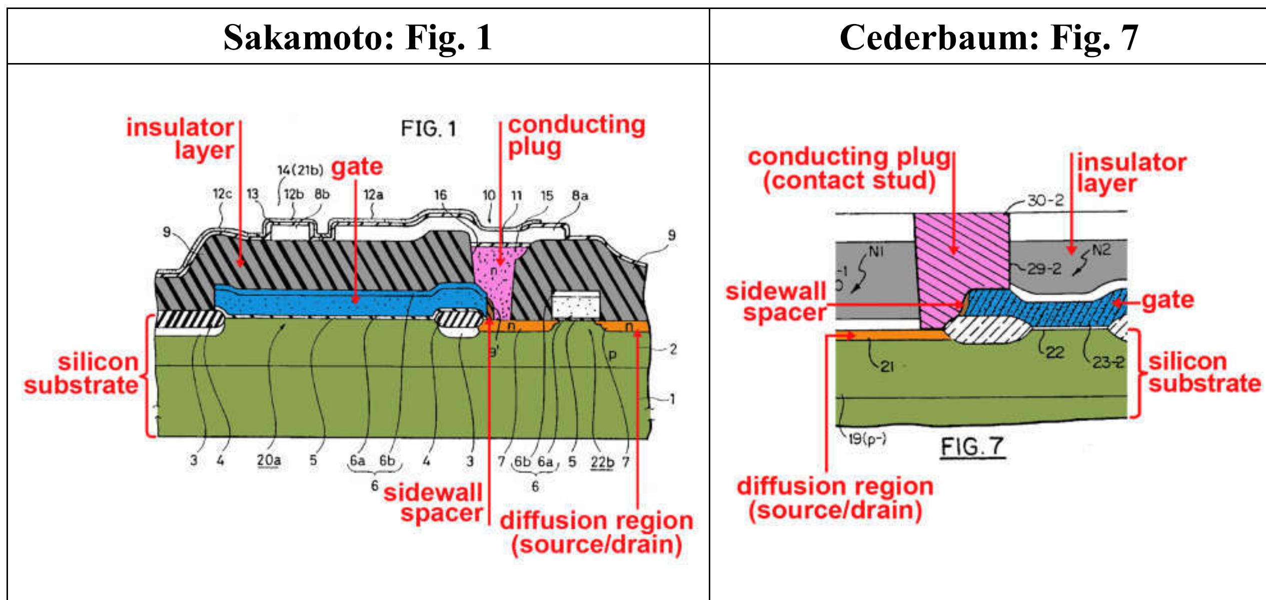
100. It would have been obvious for one skilled in the art to replace the polycrystalline plug 15 of Sakamoto with the refractory metal tungsten plug (contact stud 30) of Cederbaum for multiple reasons. [10]

101. First, both Sakamoto and Cederbaum describe the same type of devices directed to the same problem: improving the structure of transistors used in semiconductor devices—in particular, the problem of stacking transistors in a particular type of memory circuit called a Static Random Access Memory ("SRAM") cell. *See* Sakamoto at 1:29-32 ("a semiconductor device having a structure in which semiconductor elements are ***stacked*** on a substrate, a structure of an ***SRAM (Static Random Access Memory)*** will be described."), 1:13-16 (Ex. 1003); Cederbaum at 1:7-14 ("The present invention relates to … a method of forming ***stacked***, self-aligned polysilicon gate PFET devices…. In particular, the method has applicability in the forming of ***stacked*** self-aligned polysilicon gate

[10] Even the '924 patent notes that a tungsten refractory metal conducting plug was known to a person of ordinary skill in the art at the time of the '924 patent. *See* '924 patent at 1:50-56 ("A refractory metal plug such as a tungsten plug is then deposited into hole 24."), 2:23-32 ("After the deposition of a glue layer (not shown), metal plugs 44, 46 and 48 are deposited into the vias. After a tungsten plug etch back and a local interconnect masking/etching process…") (Ex. 1001).

PFETs … in six device (6D) ***SRAM cells***.") (Ex. 1004); *see also* '924 patent at 2:32-63, 4:10-15 (Ex. 1001).

102. In fact, Sakamoto and Cederbaum (and the '924 patent) disclose nearly identical structures with nearly identical components.



103. Like Figure 1 of Sakamoto, Figure 7 of Cederbaum shows an electrically conducting plug (contact stud 30-2) within an opening 28-2 (Figure 6) which contains a sidewall spacer 24 (Figure 4). The contact stud 30-2 directly connects a diffusion region (source/drain 21) to a gate (gate electrode 23-2). The source/drain 21 is formed in a substrate and is not directly connected to the gate electrode 23-2, which is substantially covered by an insulating layer 26. Cederbaum at Figs. 4- 7, 7:31-40, 7:37-52 ("N+ implanted active regions 21… constitute the source and drain regions of the NFETs," "[n]umeral[]…23-2

designate[s]…the gate electrode[] of NFETs…," and "[o]xide sidewalls or spacers 24 have been formed on the lateral sides of the polysilicon gate electrodes"), 8:26-39, 9:28-68, 13:31-37 (Ex. 1004).

104. Second, the particular material to be used for electrical conductivity would have been a simple design choice to one of ordinary skill in the art. It was known that there were multiple materials that could be used to make an electrical connection between different parts of a transistor. *See, e.g.*, Nicholls at 6:41-54 (explaining "an advantage of using a refractory metal such as tungsten over aluminium" as a plug), 6:55-60 ("The present invention is not limited to the use of tungsten [as a plug] but can be carried out utilising any refractory metal ... which preferably can be selectively deposited into a contact hole. Examples of such selectively depositable refractory metals are tungsten, copper, molybdenum and tantalum.") (Ex. 1008). The use of a refractory metal is thus a mere implementation detail which one skilled in the art would have known about and been motivated to use.

105. Third, as both Sakamoto and Cederbaum explain, there are advantages to using an electrically conducting plug formed of a refractory metal, such as tungsten (as in Cederbaum) instead of a polycide film formed from polycrystalline silicon and a metal (as in Sakamoto). Sakamoto describes the benefits of increased

conductivity of the plug and increased conductivity and ohmic contact between the plug and other components, such as the source/drain region 7. *See* Sakamoto at 8:5-12 ("Impurity ion is ion-implanted into polycrystalline silicon plug layer 15 … in order to provide conductivity."), 2:28-32, 2:62-64, 6:58-63, 7:3-7 ("ohmic contact of interconnection layer 8a, polycrystalline silicon plug layer 15, and source/drain region 7 can be obtained by having titanium silicide layer 11 interposed between interconnection layer 8a and polycrystalline silicon plug layer 15."), 7:26-28, 10:5-8 ("Fine ohmic contact can be also provided between the silicon plug layer and the upper interconnection layer of p type conductivity by interposing a refractory metal silicide layer etc.") (Ex. 1003). Cederbaum then describes a tungsten conducting plug (contact stud 30-2) that has the better conductivity and lower resistivity as compared to a polycide/polycrystalline silicon plug (like Sakamoto's plug). Cederbaum at 4:39-41 ("[p]olycide is a quite good conductive material, however it is known to exhibit higher resistivities than metal."), 9:32-34 ("filling the first stud openings with a highly conductive material (typically a metal, such as tungsten)"), 6:47-48 ("[t]he [conventional] N+/P+ diode contact structure is replaced by a tungsten contact stud forming an ohmic contact.") (Ex. 1004).

2. Claim 13: A semiconductor structure according to claim 1, wherein said conducting plug comprises an outer glue layer and a plug material therein

106. Cederbaum discloses that the conducting plug (contact stud 30-2) comprises an outer glue (titanium nitride (TiN)) layer and an inner plug material (tungsten (W)).[11] Specifically, Cederbaum discloses first depositing a titanium layer, then a titanium nitride (TiN) layer, and finally the tungsten (W) conducting plug in the via (stud opening 28). Cederbaum at 9:31-47 ("Prior to ***tungsten (W) filling***, a titanium (Ti) layer is deposited [in] the first stud openings 28-1, 28-2 and 28-3…. Next, a thin ***titanium nitride (TiN)*** layer is formed over the titanium layer…. A ***tungsten layer*** is then deposited … to entirely fill the first stud openings."), 9:63-65 ("Planarization of the Ti-***TiN*** and ***W [i.e., tungsten]***

[11] Even the '924 patent notes that a conducting plug comprising an outer glue layer and a plug material therein was known to a person of ordinary skill in the art at the time of the '924 patent. *See* '924 patent at 2:23-25 ("After the deposition of a glue layer (not shown), metal plugs 44, 46 and 48 are deposited into the vias."), 1:50-54 ("After the formation of the contact holes 24, a thin layer of titanium tungsten or titanium nitride is normally deposited into the contact hole to improve adhesion. A refractory metal plug such as a tungsten plug is then deposited into hole 24.") (Ex. 1001).

composite layer produces ***first contact pads 29*** and ***first contact studs 30*** in first stud openings 28.") (Ex. 1004).

107. One skilled in the art would understand that because a titanium nitride (TiN) layer is deposited in the opening 28 before the tungsten (W) layer is deposited, the titanium nitride (TiN) layer is an outer glue layer and the tungsten (W) layer is the inner plug material of the resulting conducting plug. Namely, since the titanium nitride (TiN) layer is thin and is deposited before the tungsten (W) layer, the titanium nitride (TiN) layer thinly covers the bottom and sides of the opening 28, leaving an interior hole into which the tungsten (W) layer can be subsequently filled. Cederbaum at 9:31-47 ("***Prior to tungsten (W) filling***, a titanium (Ti) layer is deposited with a thickness of about 40 nm to ***plate the bottom and side-walls of the first stud openings 28-1, 28-2 and 28-3***…. Next, a ***thin titanium nitride (TiN)*** layer is formed over the titanium layer.") (Ex. 1004).

108. Cederbaum teaches that the titanium nitride (TiN) layer acts as an outer glue layer because it improves adhesion of the inner tungsten layer, just as the '924 patent itself teaches. Cederbaum at 9:36-43 ("TiN layer is utilized ***to improve adhesion of the tungsten layer***.") (Ex. 1004); '924 patent at 1:50-56 ("a thin layer of … titanium nitride is normally deposited into the contact hole ***to improve adhesion***."), 2:23-27 (Ex. 1001).

109. One skilled in the art would have been motivated to combine Cederbaum and Sakamoto by using the tungsten plug of Cederbaum instead of the polycide plug of Sakamoto for the reasons I stated above in Section VIII.B.1. One skilled in the art would have been further motivated to use a titanium nitride (TiN) layer as an outer glue layer as disclosed in Cederbaum because, as Cederbaum describes, the glue layer provides improved adhesion for the tungsten plug, thereby improving the electrical and/or physical connection of the tungsten plug. Cederbaum at 9:36-43.

IX. AVAILABILITY FOR CROSS-EXAMINATION

110. In signing this declaration, I recognize that the declaration will be filed as evidence in a case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will appear for cross examination within the United States during the time allotted for cross examination.

X. RIGHT TO SUPPLEMENT

111. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to take into account new information as it becomes available to me.

Jurat

112. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Dated: June 11, 2016

Dr. Richard Blanchard

APPENDIX A

Richard A. Blanchard, Ph.D.

Professional Profile

Dr. Blanchard has over 40 years of combined industry, research, academic, and consulting experience. His research covers semiconductor device and electronics design, semiconductor device physics, semiconductor manufacturing processes and equipment, failure analysis, and reverse engineering of semiconductor devices and electronic circuits. Dr. Blanchard is a named inventor on more than 200 issued U.S. patents. As a result, he has been involved in numerous patent and trade secret litigation matters including a number of ITC proceedings. He has also authored or co-authored books and articles dealing with semiconductor design, process development, and failure analysis.

Dr. Blanchard has worked at Blanchard Associates, Los Altos, Silicon Valley Expert Witness Group, Mountain View, Exponent Failure Analysis Associates, Inc., Menlo Park, CA, IXYS Corporation, San Jose, Siliconix, Inc. Santa Clara, Supertex, Inc. Sunnyvale, Cognition, Inc. Mountain View, Foothill College, Los Altos Hills, and at Fairchild Semiconductor, Mountain View, CA.

Credentials and Professional Affiliations

1982	Stanford University	Ph.D., Electrical Engineering
1970	M.I.T.	MSEE
1968	M.I.T.	BSEE

- Senior Member, Institute of Electrical and Electronics Engineers
- Member, Electronic Device Failure Analysis Society
- Member, International Microelectronics & Packaging Society
- Member, American Vacuum Society
- Member, National Fire Protection Association
- Court Appointed Special Master

Patents

Patent Number	Date Issued	Title
9,362,348	6/7/2016	Method of manufacturing a light emitting, power generating, Or other electronic apparatus
9,356,595	5/31/2016	Bidirectional two-base bipolar junction transistor devices, operation, circuits, and systems with collector-side base driven, diode-mode turn-on, double base short at initial turn-off, and two base junctions clamped by default
9,355,853	5/31/2016	Systems and methods for bidirectional device fabrication
9,349,928	5/24/2016	Method of manufacturing a printable composition of a liquid or gel suspension of diodes
9,343,593	5/17/2016	Printable composition of a liquid or gel suspension of diodes
9,337,262	5/10/2016	Structures and methods with reduced sensitivity to surface charge
9,316,362	4/19/2016	LED lighting apparatus formed by a printable composition of a liquid or gel suspension of diodes and methods of using same
9,306,048	4/05/2016	Dual depth trench-gated MOS controlled thyristor with well-defined turn-on characteristics
9,263,573	2/16/2016	Power semiconductor devices, structures and related methods
9,236,528	1/12/2016	Light emitting, photovoltaic or other electronic apparatus and system
9,236,527	1/5/2016	Light emitting, photovoltaic or other electronic apparatus and system
9,231,582	12/8/2015	Bidirectional two-phase bipolar junction transistor devices, operation, circuits and systems with diode-mode-turn-on and collector-side base driven
9,209,798	12/8/2015	Bidirectional two-phase bipolar junction transistor operation, circuit and systems with two base junctions clamped by default
9,209,713	12/1/2015	Bidirectional two-phase bipolar junction transistor operation, circuit and systems with two base junctions clamped by default
9,203,401	12/1/2015	Bidirectional two-phase bipolar junction transistor operation, circuit and systems with base short at initial turn-off
9,203,400	12/1/2015	Bidirectional two-phase bipolar junction transistor operation, circuit and systems with diode-mode turn-on
9,200,758	11/17/2015	LED lighting apparatus formed by a printable composition of a liquid of gel suspension of diodes and methods of using same
9,190,894	11/3/2015	Bidirectional two-phase bipolar junction by a printable composition of a liquid or gel suspension of diodes and method of using same
9,130,124	9/08/2015	Diode for a Printable Composition
9,123,705	9/01/2015	Conductive Ink for Filling Vias
9,105,812	8/11/2015	Diode for a Printable Composition
9,099,568	8/04/2015	Three-Terminal Printed Devices. Interconnected as Circuits
9,082,648	7/14/2015	Vertical Insulated-gate turn-off device having a planar gate
9,076,861	7/07/2015	Schottky and MOSFET and Schottky structures, devices and methods
9,059,710	6/16/2015	Systems, circuits, devices, and methods with bidirectional bipolar

9,054,707	6/09/2015	transistors
9,054,706	6/09/2015	Systems, circuits, devices, and methods with bidirectional bipolar transistors
9,048,118	6/02/2015	Systems, circuits, devices, and methods with bidirectional bipolar transistors
9,035,350	5/19/2015	Lateral transistors with low-voltage drop shunt to body diode
9,029,909	5/12/2015	Systems, circuits, devices, and methods with bidirectional bipolar transistors
		Systems, circuits, devices, and methods with bidirectional bipolar transistors
9,024,379	5/5/2015	Trench transistors and methods with low-voltage-drop shunt to body diode
9,018,833	4/28/2015	Apparatus with Light Emitting or Absorbing Diodes
8,940,627	1/27/2015	Conductive Iink for Filling Vias
8,937,502	1/20/2015	Lateral Insulated Gate Turn-off Devices
8,890,238	11/18/2014	Power Semiconductor Devices, structures and related methods
8,878,238	11/4/2014	MCT device with base-width-determined latching and non-latching states
8,878,237	11/4/2014	Active edge structures providing uniform current flow in insulated gate turn-off thyristors
8,877,101	11/4/2014	Method of manufacturing a light emitting, power generating or other electronic apparatus
8,852,467	10/7/2014	Method of Manufacturing a printable composition of a liquid or gel suspension of diodes
8,847,307	9/30/2014	Power semiconductor devices, methods, and structures with embedded dielectric layers containing permanent charges
8,846,457	9/30/2014	Printable composition of a liquid or gel suspension of diodes
8,809,126	8/19/2014	Printable composition of a liquid or gel suspension of diodes
8,803,191	8/12/2014	Systems, Devices, and Methods with Integrable FET-Controlled Lateral Thyristors
8,753,947	6/17/2014	Method of Manufacturing a Light Emitting. Photovoltaic or other Electronic Apparatus and Systems
8,753,946	6/17/2014	Method of Manufacturing a Light Emitting. Photovoltaic or other Electronic Apparatus and Systems
8,742,912	06/03/2014	Self-powered sensor system for monitoring tire pressure
8,742,456	06/03/2014	Integrating a Trench-gated Thyristor with a Trench-gated Rectifier
8,723,408	05/13/2014	Diode for Printable Composition
8,704,301	04/22/2014	Devices, Methods, and systems with MOS-gated Trench-to-trench Lateral Current Flows
8,704,295	04/22/2014	Schottky and MOSFET+Schottky Structures, Devices and Methods
8,679,903	03/25/2014	Vertical quadruple conduction channel insulated gate transistor
8,674,593	03/18/2014	Diode for a printable composition
8,669,612 B2	03/11/2014	Technique for Forming the Deep Doped Columns in Superjunction
8,643,055 B2	02/14/2014	Series Current Limiter Device
8,581,341 B2	11/12/2013	Power MOSFET with Embedded Recessed Field Plate and Methods

of Fabrication

8,580,644 B2	11/12/2013	Multi-Level Lateral floating Coupled Capacitor Transistor Structures
8,575,688 B2	11/5/2013	Trench Device Structure and Fabrication
8,569,117 B2	10/29/2013	Systems and Methods Integrating Trench-Gated Thyristor with Trench-Gated Rectifier
8,513,732 B2	08/20/2013	High Voltage Power MOSFET having low on-resistance
8,456,393	06/04/2013	Method of Manufacturing a Light Emitting, Photovoltaic or other Electronic Apparatus and System
8,456,392	06/04/2013	Method of Manufacturing a Light Emitting, Photovoltaic or other Electronic Apparatus and System
8,450,795	05/28/2013	Technique for Forming the Deep Doped Columns in Superjunction
8,415,879	04/09/2013	Diode for Printable Composition
8,395,568	03/12/2013	Light Emitting, Photovoltaic or other Electronic Apparatus and System
8,390,060	03/05/2013	Power Semiconductor Devices, Structures, and Related Methods
8,384,630	02/26/2013	Light Emitting Photovoltaic or other Electronic Apparatus and System
8,354,711	01/15/2013	Power MOSFET and its Edge Termination
8,330,217	12/11/2012	Devices, Methods, and Systems with MOS-Gated Trench-to-Trench Lateral, Current Flow
8,330,213	12/11/2012	Power Semiconductor Devices, Methods, and Structures with Embedded Dielectric Layers Containing Permanent Charges
8,319,278	11/27/2012	Power Device Structures and Methods Using Empty Space Zones
8,310,006	11/13/2012	Devices, Structures, and Methods using Self-aligned Resistive Source Extensions
8,193,565	06/05/2012	Multi-level Lateral Floating Coupled Capacitor Transistor Structures
8,133,768	03/13/2012	Method of Manufacturing a Light Emitting Photovoltaic or Other Electronic Apparatus and System
8,049,271	11/01/2011	Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Formation of Floating Islands
7,989,293	08/02/2011	Trench Device Structure and Fabrication
7,825,492	11/02/2010	Isolated Vertical Power Device Structure with Both N-Doped and P-Doped Trenches
7,745,885	06/29/2010	High Voltage Power MOSFET Having Low On-Resistance
7,736,976	06/15/2010	Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands
7,705,397	04/27/2010	Devices, Methods, and Systems with MOS-Gated Trench-to-Trench Lateral Current Flow
7,704,842	04/27/2010	Lateral High-Voltage Transistor with Vertically-Extended Voltage-Equalized Drift Region
7,586,165	09/08/2009	Microelectromechanical Systems (MEMS) Device Including a Superlattice

7,586,148	09/08/2009	Power Semiconductor Device Having a Voltage Sustaining Region that Includes Doped Columns Formed by Terraced Trenches
7,557,394	07/07/2009	High-Voltage Transistor Fabrication with Trench Etching Technique
7,544,544	06/09/2009	Low Capacitance Two-Terminal Barrier Controlled TVS Diodes
7,535,041	05/19/2009	Method for Making a Semiconductor Device Including Regions of Band-Engineered Semiconductor Superlattice to Reduce Device-On Resistance
7,531,850	05/12/2009	Semiconductor Device Including a Memory Cell with a Negative Differential Resistance (NDR) Device
7,531,829	05/12/2009	Semiconductor Device Including Regions of Band-Engineered Semiconductor Superlattice to Reduce Device-On Resistance
7,504,305	03/17/2009	Technique for Forming the Deep Doped Regions in Superjunction Devices
7,473,966	01/06/2009	Oxide-Bypassed Lateral High Voltage Structures and Methods
7,442,584	10/28/2008	Isolated Vertical Power Device Structure with Both N-Doped and P-Doped Trenches
7,411,249	08/12/2008	Lateral High-Voltage Transistor with Vertically-Extended Voltage-Equalized Drift Region
7,397,097	07/08/2008	Integrated Released Beam Layer Structure Fabricated in Trenches and Manufacturing Method Thereof
7,339,252	03/04/2008	Semiconductor Having Thick Dielectric Regions
7,304,347	12/04/2007	Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands
7,244,970	07/17/2007	Low Capacitance Two-Terminal Barrier Controlled TVS Diodes
7,224,027	05/29/2007	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Diffusion from Regions of Oppositely Doped Polysilicon
7,202,494	04/10/2007	FinFET Including a Superlattice
7,199,427	04/03/2007	DMOS Device with a Programmable Threshold Voltage
7,138,289	11/21/2006	Technique for Fabricating Multilayer Color Sensing Photodetectors
7,094,621	08/22/2006	Fabrication on Diaphragms and "Floating" Regions of Single Crystal Semiconductor for MEMS Devices
7,091,552	08/15/2006	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Ion Implantation
7,084,455	08/01/2006	Power Semiconductor Device Having a Voltage Sustaining Region that Includes Terraced Trench with Continuous Doped Columns Formed in an Epitaxial Layer
7,067,376	06/27/2006	High Voltage power MOSFET Having Low On-Resistance
7,061,072	06/13/2006	Integrated Circuit Inductors Using Driven Shields
7,023,069	04/04/2006	Method for Forming Thick Dielectric Regions Using Etched Trenches
7,019,360	03/28/2006	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching Using an Etchant Gas that is also a Doping Source

7,015,104	03/21/2006	Technique for Forming the Deep Doped Columns in Superjunction
6,992,350	01/31/2006	High Voltage Power MOSFET Having Low On-Resistance
6,949,432	09/27/2005	Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface
6,921,938	07/26/2005	Double Diffused Field Effect Transistor Having Reduced On-Resistance
6,906,529	06/14/2005	Capacitive Sensor Device With Electrically Configurable Pixels
6,882,573	04/19/2005	DMOS Device with a Programmable Threshold Voltage
6,861,337	03/01/2005	Method for Using a Surface Geometry for a MOS-Gated Device in the Manufacture of Dice Having Different Sizes
6,812,526	11/02/2004	Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface
6,812,056	11/02/2004	Technique for Fabricating MEMS Devices Having Diaphragms of "Floating" Regions of Single Crystal Material
6,794,251	09/21/2004	Method of Making a Power Semiconductor Device
6,790,745	09/14/2004	Fabrication of Dielectrically Isolated Regions of Silicon in a Substrate
6,777,745	08/17/2004	Symmetric Trench MOSFET Device and Method of Making Same
6,750,523	06/15/2004	Photodiode Stacks for Photovoltaic Relays and the Method of Manufacturing the Same
6,750,104	06/15/2004	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching Using an Etchant Gas that is also a Doping Source
6,734,495	05/11/2004	Two Terminal Programmable MOS-Gated Current Source
6,730,963	05/04/2004	Minimum Sized Cellular MOS-Gated Device Geometry
6,724,044	04/20/2004	MOSFET Device Having Geometry that Permits Frequent Body Contact
6,724,039	04/20/2004	Semiconductor Device Having a Schottky Diode
6,713,351	03/30/2004	Double Diffused Field Effect Transistor Having Reduced On-Resistance
6,710,414	03/23/2004	Surface Geometry for a MOS-Gated Device that Allows the Manufacture of Dice Having Different Sizes
6,710,400	03/23/2004	Method for Fabricating a High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Rapid Diffusion
6,689,662	02/10/2004	Method of Forming a High Voltage Power MOSFET Having Low On-Resistance
6,686,244	02/03/2004	Power Semiconductor Device Having a Voltage Sustaining Region that Includes Doped Columns Formed with a Single Ion Implantation Step
6,660,571	12/09/2003	High Voltage Power MOSFET Having Low On-Resistance
6,656,797	12/02/2003	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Ion Implantation
6,649,477	11/18/2003	Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands

6,627,949	09/30/2003	High Voltage Power MOSFET Having Low On-Resistance
6,624,494	09/23/2003	Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer
6,621,107	09/16/2003	Trench DMOS Transistor with Embedded Trench Schottky Rectifier
6,593,619	07/15/2003	High Voltage Power MOSFET Having Low On-Resistance
6,593,174	07/15/2003	Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same
6,576,516	06/10/2003	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Diffusion from Regions of Oppositely Doped Polysilicon
6,566,201	05/20/2003	Method for Fabricating a High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Rapid Diffusion
6,538,279	03/25/2003	High-Side Switch with Depletion-Mode Device
6,492,663	12/10/2002	Universal Source Geometry for MOS-Gated Power Devices
6,479,352	11/12/2002	Method of Fabricating High Voltage Power MOSFET Having Low On-Resistance
6,472,709	10/29/2002	Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface
6,468,866	10/22/2002	Single Feature Size MOS Technology Power Device
6,465,304	10/15/2002	Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer
6,432,775	08/13/2002	Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface
6,420,764	07/16/2002	Field Effect Transitor (sic. Transistor) Having Dielectrically Isolated Sources and Drains and Methods for Making Same
6,403,427	06/11/2002	Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same
6,399,961	06/04/2002	Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same
6,369,426	04/09/2002	Transistor with Integrated Photodetector for Conductivity Modulation
6,368,918	04/09/2002	Method of Fabricating Nan (sic. an) Embedded Flash EEPROM with a Tunnel Oxide Grown on a Textured Substrate
6,331,794	12/18/2001	Phase Leg with Depletion-Mode Device
6,316,336	11/13/2001	Method for Forming Buried Layers with Top-Side Contacts and the Resulting Structure
6,291,845	09/18/2001	Fully-Dielectric-Isolated FET Technology
6,272,050	08/07/2001	Method and Apparatus for Providing an Embedded Flash-EEPROM Technology
6,239,752	05/29/2001	Semiconductor Chip Package that is also an Antenna
6,225,662	05/01/2001	Semiconductor Structure with Heavily Doped Buried Breakdown Region
6,215,170	04/10/2001	Structure for Single Conductor Acting as Ground and Capacitor Plate Electrode Using Reduced Area
6,198,114	03/06/2001	Field Effect Transistor Having Dielectrically Isolated Sources and

		Drains and Method for Making Same
6,069,385	05/30/2000	Trench MOS-Gated Device
6,064,109	05/16/2000	Ballast Resistance for Producing Varied Emitter Current Flow Along the Emitter's Injecting Edge
6,046,473	04/04/2000	Structure and Process for Reducing the On-Resistance of MOS-Gated Power Devices
6,011,298	01/04/2000	High Voltage Termination with Buried Field-Shaping Region
5,985,721	11/16/1999	Single Feature Size MOS Technology Power Device
5,981,998	11/09/1999	Single Feature Size MOS Technology Power Device
5,981,318	11/09/1999	Fully-Dielectric-Isolated FET Technology
5,960,277	09/28/1999	Method of Making a Merged Device with Aligned Trench FET and Buried Emitter Patterns
5,897,355	05/27/1999	Method of Manufacturing Insulated Gate Semiconductor Device to Improve Ruggedness
5,869,371	02/09/1999	Structure and Process for Reducing the On-Resistance of MOS-gated Power Devices
5,856,696	01/05/1999	Field Effect Transistor Having Dielectrically Isolated Sources and Drains
5,821,136	10/13/1998	Inverted Field-Effect Device with Polycrystalline Silicon/Germanium Channel
5,801,396	09/01/1998	Inverted Field-Effect Device with Polycrystalline Silicon/Germanium Channel
5,798,549	08/25/1998	Conductive Layer Overlaid Self-Aligned MOS-Gated Semiconductor Devices
5,773,328	06/30/1998	Method Of Making A Fully-Dielectric-Isolated FET
5,756,386	05/26/1998	Method of Making Trench MOS-Gated Device with A Minimum Number of Masks
5,710,443	01/20/1998	Merged Device with Aligned Trench FET and Buried Emitter Patterns
5,708,289	01/13/1998	Pad Protection Diode Structure
5,701,023	12/23/1997	Insulated Gate Semiconductor Device Typically Having Subsurface-Peaked Portion of Body Region for Improved Ruggedness
5,691,555	11/25/1997	Integrated Structure Current Sensing Resistor For Power Devices Particularly For Overload Self-Protected Power MOS Devices
5,668,025	09/16/1997	Method of Making a FET with Dielectrically Isolated Sources and Drains
5,663,079	09/02/1997	Method of Making Increased Density MOS-Gated Semiconductor Devices
5,648,670	07/15/1997	Trench MOS-Gated Device with a Minimum Number of Masks
5,640,037	06/17/1997	Cell with Self-Aligned Contacts
5,637,889	06/10/1997	Composite Power Transistor Structures Using Semiconductor Materials With Different Bandgaps
5,591,655	01/07/1997	Process for Manufacturing a Vertical Switched-Emitter Structure with Improved Lateral Isolation
5,589,415	12/31/1996	Method for Forming a Semiconductor Structure with Self-Aligned Contacts

5,576,245	11/19/1996	Method of Making Vertical Current Flow Field Effect Transistor
5,574,301	11/12/1996	Vertical Switched-Emitter Structure with Improved Lateral Isolation
5,528,063	06/18/1996	Conductive-Overlaid Self-Aligned MOS-Gated Semiconductor Devices
5,485,027	01/16/1996	Isolated DMOS IC Technology
5,298,781	03/29/1994	Vertical Current Flow Field Effect Transistor with Thick Insulator Over Non-Channel Areas
5,237,481	08/17/1993	Temperature Sensing Device for Use in a Power Transistor
5,218,228	06/08/1993	High Voltage MOS Transistors with Reduced Parasitic Current Gain
5,164,325	11/17/1992	Method of Making a Vertical Current Flow Field Effect Transistor
5,156,989	10/20/1992	Complementary, (sic) Isolated DMOS IC Technology
5,132,235	07/21/1992	Method for Fabricating a High Voltage MOS Transistor
5,034,785	07/23/1991	Planar Vertical Channel DMOS Structure
4,983,535	01/08/1991	Vertical DMOS Transistor Fabrication Process
4,978,631	12/18/1990	Current Source with a Process Selectable Temperature Coefficient
4,958,204	09/18/1990	Junction Field-Effect Transistor with a Novel Gate
4,956,700	09/11/1990	Integrated Circuit with High Power, Vertical Output Transistor Capability
4,952,992	08/28/1990	Method and Apparatus for Improving the On-Voltage Characteristics of a Semiconductor Device
4,929,991	05/29/1990	Rugged Lateral DMOS Transistor Structure
4,920,388	04/24/1990	Power Transistor with Integrated Gate Resistor
4,916,509	04/10/1990	Method for Obtaining Low Interconnect Resistance on a Grooved Surface and the Resulting Structure
4,914,058	04/03/1990	Grooved DMOS Process with Varying Gate Dielectric Thickness
4,896,196	01/23/1990	Vertical DMOS Power Transistor with an Integral Operating Condition Sensor
4,893,160	01/09/1990	Method for Increasing the Performance of Trenched Devices and the Resulting Structure
4,868,537	09/19/1989	Doped SiO_2 Resistor and Method of Forming Same
4,851,366	07/25/1989	Method for Providing Dielectrically Isolated Circuit
4,845,051	07/04/1989	Buried Gate JFET
4,835,586	05/30/1989	Dual-Gate High Density FET
4,827,324	05/02/1989	Implantation of Ions into an Insulating Layer to Increase Planar PN Junction Breakdown Voltage
4,824,795	04/25/1989	Method for Obtaining Regions of Dielectrically Isolated Single Crystal Silicon
4,816,882	03/28/1989	Power MOS Transistor with Equipotential Ring
4,799,100	01/17/1989	Method and Apparatus for Increasing Breakdown of a Planar Junction
4,798,810	01/17/1989	Method for Manufacturing a Power MOS Transistor
4,794,436	12/27/1988	High Voltage Drifted-Drain MOS Transistor
4,791,462	12/13/1988	Dense Vertical J-MOS Transistor
4,774,196	09/27/1988	Method of Bonding Semiconductor Wafers

4,767,722	08/30/1988	Method for Making Planar Vertical Channel DMOS Structures
4,759,836	07/26/1988	Ion Implantation of Thin Film $CrSi_2$ and SiC Resistors
4,707,909	11/24/1987	Manufacture of Trimmable High Value Polycrystalline Silicon Resistors
4,682,405	07/28/1987	Methods for Forming Lateral and Vertical DMOS Transistors
4,402,003	08/30/1983	Composite MOS/Bipolar Power Device
4,398,339	08/16/1983	Fabrication Method for High Power MOS Device
4,393,391	07/12/1983	Power MOS Transistor With a Plurality of Longitudinal Grooves to Increase Channel Conducting Area
4,345,265	08/17/1982	MOS Power Transistor with Improved High-Voltage Capability
4,344,081	08/10/1982	Combined DMOS and a Vertical Bipolar Transistor Device and Fabrication Method Therefor (sic)
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