IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Ting P. Yen
Serial No.:	08/900,047
Title:	METAL PLUG LOCAL INTERCONNECT
Filed:	July 24, 1997
Attorney Docket No.:	0325.00124
Examiner:	V. Wallace
Art Unit:	2503
In Response To:	Office Action mailed February 24, 1998

CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to BOX AF, Assistant Commissioner for Patents, Washington, D.C. 20231, on April 23, 1998.

By: Victoria T. Gorgon
Victoria T. Gorgon

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed February 24, 1998, please consider the following amendment and remarks regarding the above-captioned patent application to place the patent application in condition for allowance.

IN THE CLAIMS

Please amend the claims as follows:

~~13.~~ (TWICE AMENDED) A semiconductor structure comprising:

a silicon substrate having a top surface,

a diffusion region formed in said substrate adjacent to said top surface,

a [polysilicon] gate formed on the top surface of said substrate juxtaposed to but not contacting said diffusion region,

a sidewall spacer adjacent to said [polysilicon] gate and disposed above said diffusion region,

an insulator layer substantially covering said [polysilicon] gate and said diffusion region, and

a conducting plug at least partially filling a via in said insulation layer that exposes said sidewall spacer in the absence of said conducting plug, said conducting plug providing direct electrical communication between said [polysilicon] gate and said diffusion region.

~~14.~~ (AMENDED) A method of forming a local interconnect in a semiconductor structure, comprising the step of:

depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region, said semiconductor structure comprising said diffusion region in a silicon

substrate, said gate being on said substrate juxtaposed to but not contacting said diffusion region, said sidewall spacer being disposed above said diffusion region, said via being in an insulating material on said gate.

Please add the following new claims:

16 ~~18~~. (ADDED) The structure according to claim 1 ~~13~~, wherein said gate comprises polysilicon.

17 ~~19~~. (ADDED) The method according to claim 7 ~~14~~, wherein said gate comprises polysilicon.

R E M A R K S

Applicant appreciates Examiner Wallace's indication that the declaration filed on January 9, 1998 overcomes the Sugiyama reference.

Rejection Under 35 U.S.C. § 102(e)

The rejection of claims 3-6, 9-14 and 16-17 under 35 U.S.C. § 102(e) as being anticipated by Chappell ('427) is respectfully traversed and should be withdrawn.

Chappell discloses a silicon substrate 10, a diffusion region 43, a gate stack 18, a sidewall spacer 28, a diffusion region 43 and a contact/metallization layer 44A-D (see column 3, line 58-61, column 5, lines 11-14, column 6, lines 1-17, FIGS 5-8 and 10).

Chappell does not, however, disclose a conducting plug providing direct electrical communication between the gate and diffusion

region. Specifically, FIG. 5 shows the diffusion region 43 at a position in the silicon 10 that is adjacent to the gate stack 18. It is noted that in FIG. 2, the top portion of the gate stack 18 is labeled 26 in FIG. 2 and is labeled 24 in FIG. 5. Apparently, the reference numeral 24 in FIG. 5 should be a 26. This is particularly true in view of column 4, lines 38-48 which states that the "nitride cap 26 etches at a much lower rate so that the tungsten silicide or tungsten layer 24 is not reached and thus, when the opening 42 is filled with an electrically conductive material, there is **no contact** to the electrically conductive portion of the gate stack 18." This is in contrast with the present invention that provides a conducting plug providing direct electrical communication between the gate and diffusion region. As such, Chappell does not anticipate the presently pending claims and the rejection should be withdrawn.

REJECTIONS UNDER 35 U.S.C. 103

The rejection of Claims 2, 8 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Chappell in view of Jones ('089) is respectfully traversed.

Jones discloses a semiconductive device including a conductive plug region 32. Glue layers are generically identified as being used in conductive plug technology.

Jones is silent with regard to a conducting plug providing electrical communication between a gate and a diffusion region. Therefore, Jones fails to cure the deficiencies of Chappell with regard to the presently claimed invention. Neither Chappell nor Jones

disclose or suggest a conducting plug providing direct electrical communication between a gate and a diffusion region. Therefore, the pending claims are fully patentable and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our Deposit Account No. 02-____.

Respectfully submitted,

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