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# United States Patent [19]

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Cederbaum et al.

[45] Date of Patent: **Mar. 31, 1992**

[54] **METHOD OF FORMING STACKED SELF-ALIGNED POLYSILICON PFET DEVICES AND STRUCTURES RESULTING THEREFROM**

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[73] Assignee: **International Business Machines Corporation, Armonk, N.Y.**

[21] Appl. No.: **729,250**

[22] Filed: **Jul. 12, 1991**

[30] **Foreign Application Priority Data**

Jul. 31, 1990 [EP] European Pat. Off. .... 90480112.3

[51] Int. Cl.<sup>5</sup> ..... **H01L 21/265**

[52] U.S. Cl. .... **437/41; 437/56; 437/57; 437/200; 437/915; 437/245; 437/913; 437/52**

[58] Field of Search ..... **437/41, 195, 52, 56, 437/915, 245, 200, 59, 913, 57, 58**

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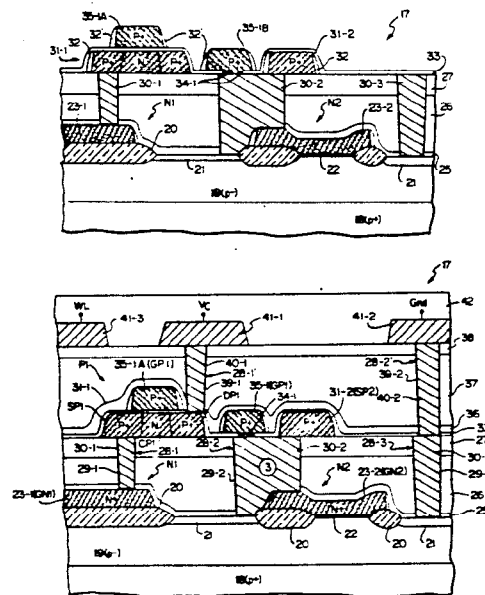
Primary Examiner—Brian E. Hearn

Assistant Examiner—Michael Trinh  
Attorney, Agent, or Firm—Richard A. Romanchik

[57] **ABSTRACT**

A stacked semiconductor structure including a base structure (18/19) is comprised of a semiconductor substrate having active regions (21) of devices (N1, . . . ) formed therein and/or a plurality of polysilicon lines (23-1, . . . ) formed thereupon; a first thick passivating layer (26/27) having a set of first metal contact studs (30-1, . . . ) therein contacting at least one of said active regions (21) and/or said polysilicon lines (23-1, . . . ), the surface of said first metal contact studs being coplanar with the surface of said first thick passivating layer; a plurality of first polysilicon lands (31-1, . . . ) formed on the said thick passivating layer, certain portions of said first polysilicon lands defining the source, drain and channel regions forming the body of a PFET device with at least one region (SP1) contacting one of said first metal contact studs; a thin insulating layer (33) forming the gate dielectric layer of said PFET device; a plurality of highly doped second polysilicon lands (35-1A, . . . ) formed over by said thin insulating layer (33); a certain portion of said second polysilicon lands (35-1A, . . . ) forming the gate electrode (GP1) of said PFET device (SP1) which is self-aligned with said source (SP1) and drain (DPI) regions; a second thick passivating layer (37/38) having a set of second metal contact studs (40-1, . . . ) therein contacting at least one of said first or second polysilicon lands (31-1, . . . ; 35-1, . . . ) and/or said first contact studs (30-1, . . . ); the surface of said second metal contact studs is coplanar with the surface of said second thick passivating layer; a first metal interconnection configuration having metal lands (41-1, . . . ) electrically contacting at least one of said second metal contact studs (40-1, . . . ); and, a final insulating film (42).

14 Claims, 7 Drawing Sheets



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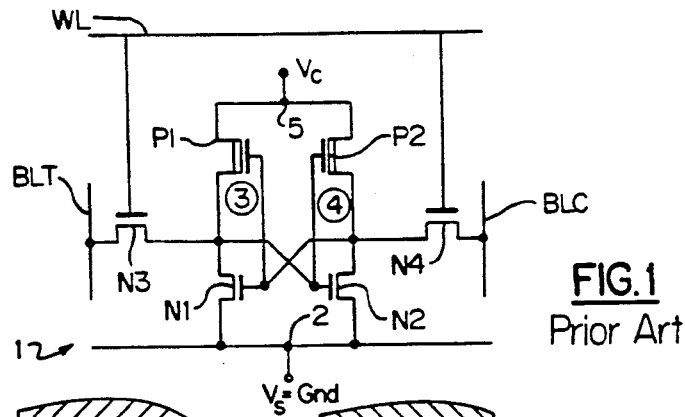


FIG. 1  
Prior Art

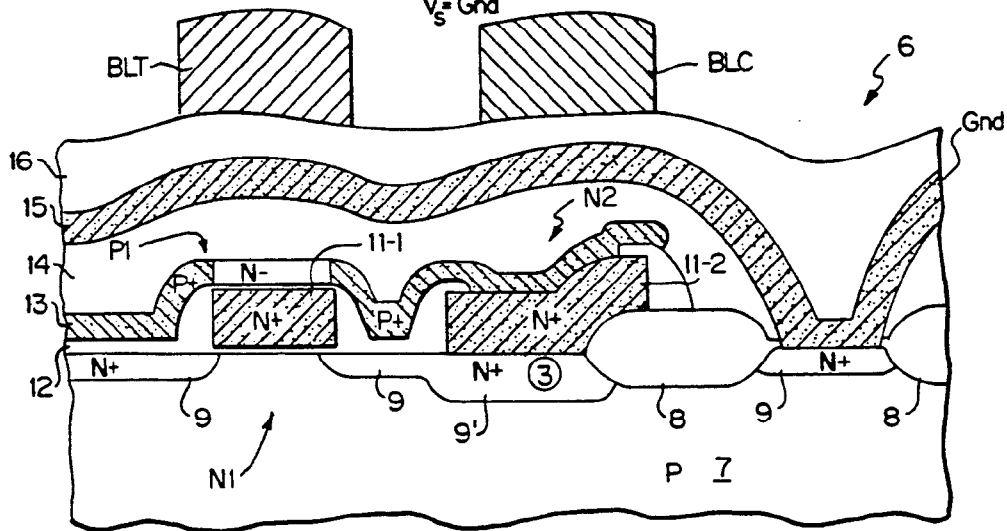


FIG. 2  
Prior Art

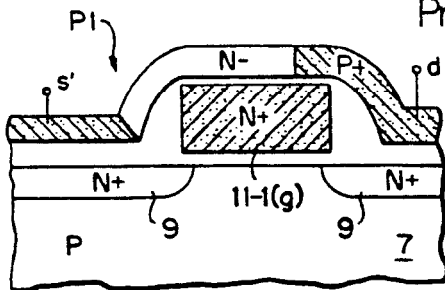


FIG. 3A  
Prior Art

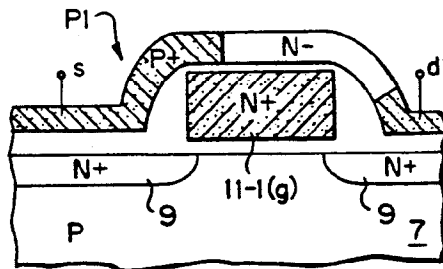
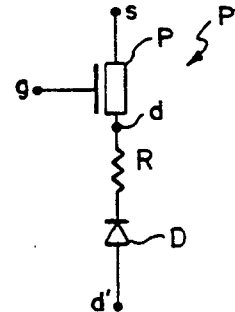
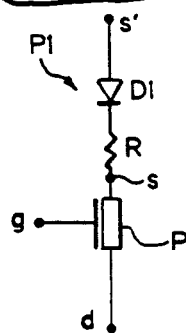
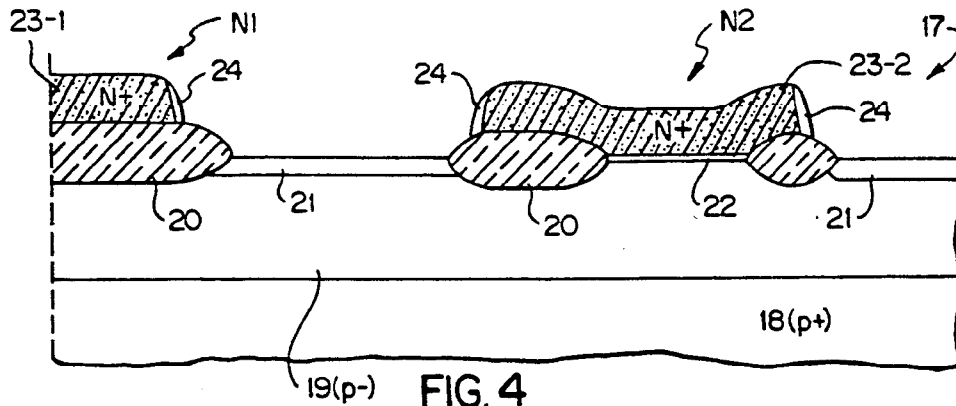
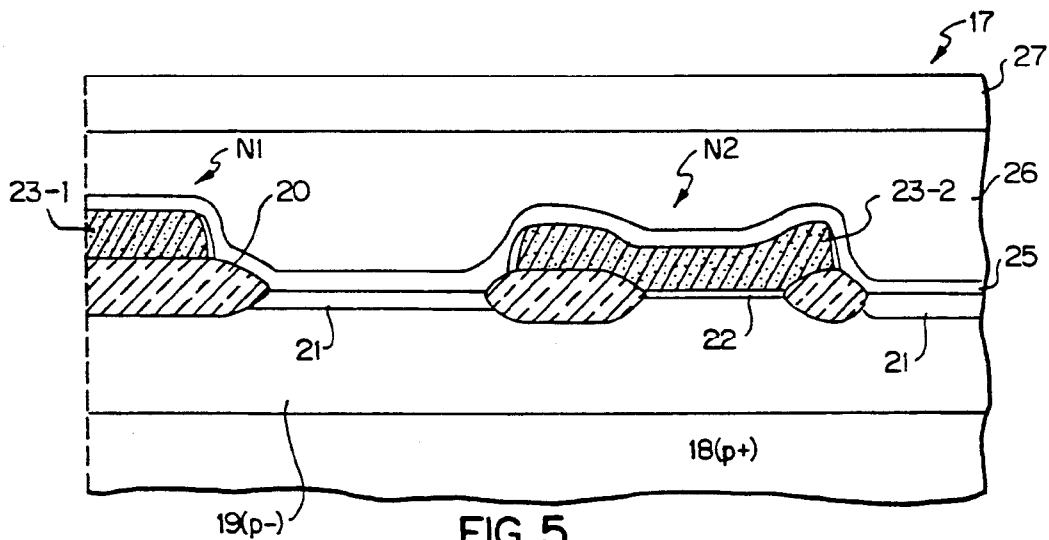


FIG. 3B  
Prior Art

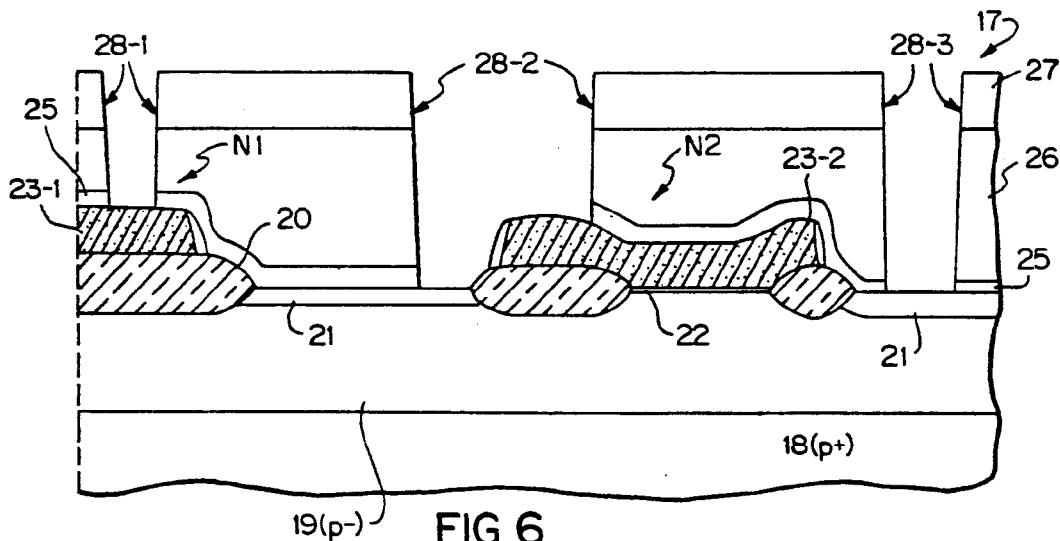




**FIG. 4**  
Prior Art



**FIG. 5**



**FIG. 6**

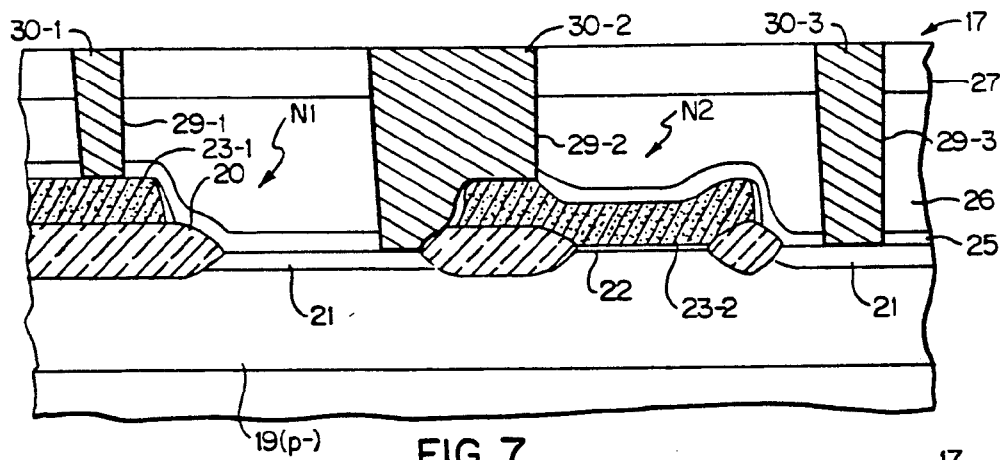


FIG. 7

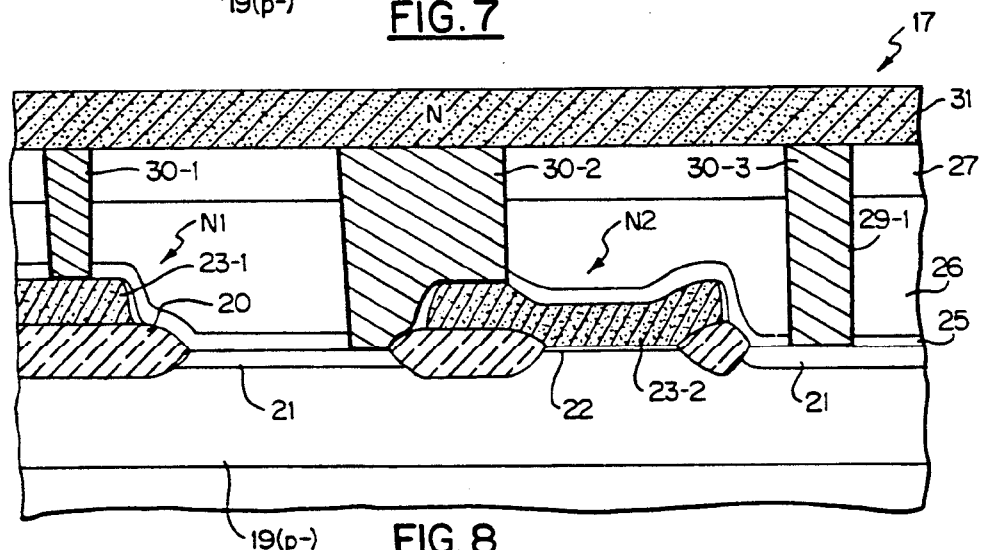


FIG. 8

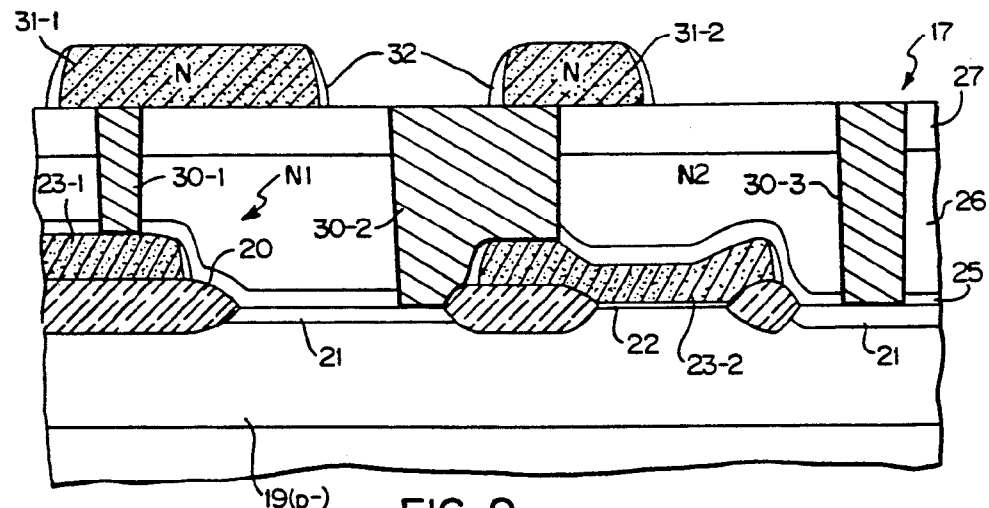


FIG. 9

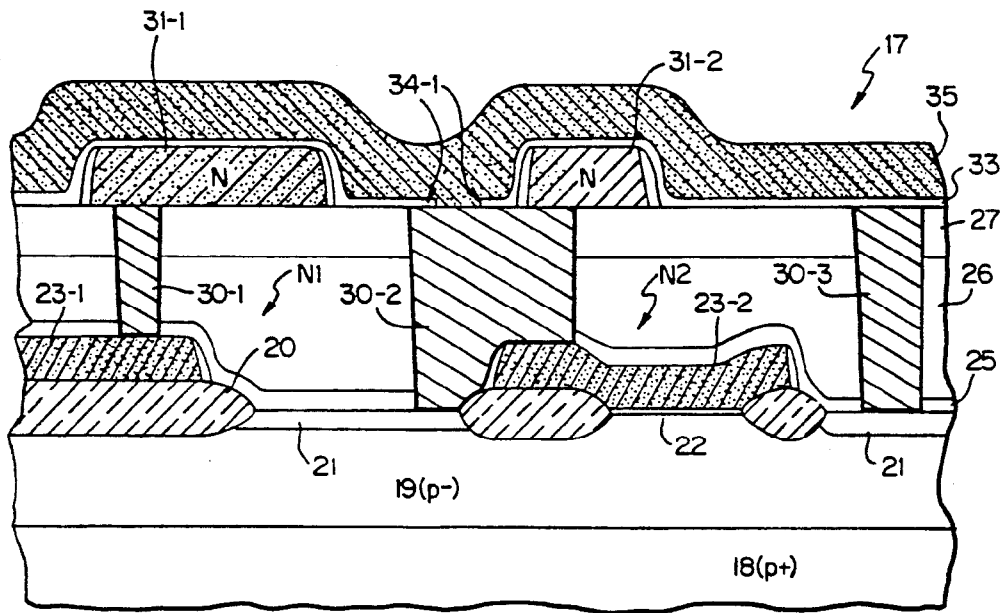


FIG. 10

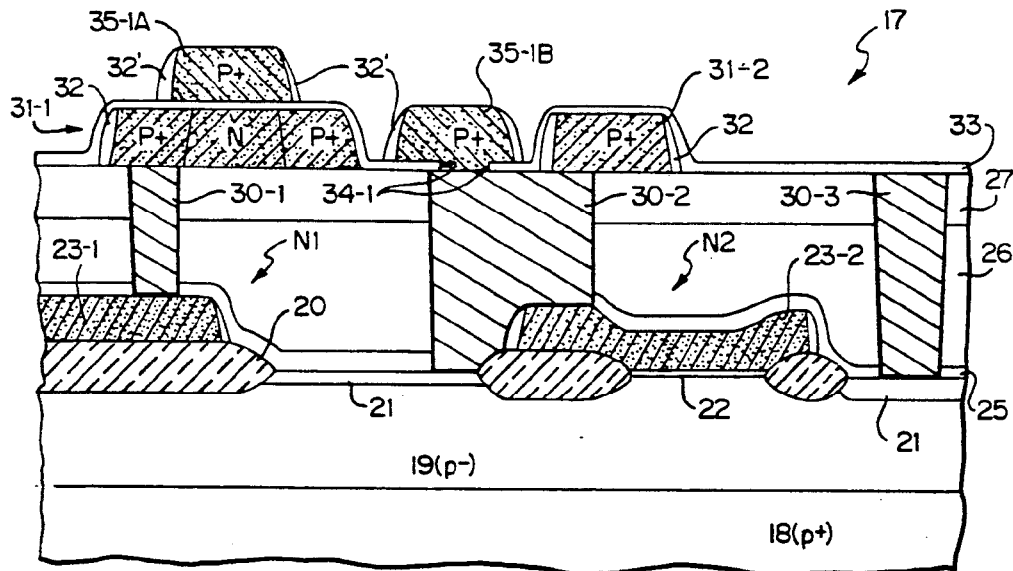


FIG. 11

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