

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED, GLOBALFOUNDRIES INC.,
GLOBALFOUNDRIES U.S. INC., GLOBALFOUNDRIES DRESDEN
MODULE ONE LLC & CO. KG, GLOBALFOUNDRIES DRESDEN
MODULE TWO LLC & CO. KG,
Petitioner,

v.

DSS TECHNOLOGY MANAGEMENT, INC.,
Patent Owner.

Case IPR2016-01311
Patent 6,784,552 B2

Before BRYAN F. MOORE, BRIAN J. McNAMARA, and
MINN CHUNG, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, and Globalfoundries Dresden Module Two LLC & Co. KG (collectively, “Petitioner”) filed a Petition (Paper 3, “Pet.”), requesting an *inter partes* review of claims 1–7 (the “challenged claims”) of U.S. Patent No. 6,784,552 B2 (Ex. 1001, “the ’552 patent”) owned by DSS Technology Management, Inc. (“Patent Owner”). 35 U.S.C. § 311. Petitioner also timely filed a Motion for Joinder (Paper 4, “Mot. for Joinder”) of this proceeding with *Intel Corporation v. DSS Technology Management, Inc.*, IPR2016-00287 (“Intel IPR2016-00287”), which is the subject of a Decision to Institute entered on June 8, 2016. Petitioner represents that the instant Petition “is identical to the petition in [Intel IPR2016-00287].”¹ Mot. for Joinder 6. We have jurisdiction under 37 C.F.R. § 42.4(a) and 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Having considered the arguments and the associated evidence presented in the Petition, for the reasons described below, we institute *inter partes* review of claims 1–7.

¹ We understand Petitioner to mean identical in all substantive matters, as the identity of the parties is different. Petitioner also acknowledges that it relies on the testimony of a different expert than the expert witness in Intel IPR2016-00287, but states that the testimony is essentially the same. Mot. for Joinder 4, 6.

A. Real Parties In Interest

Petitioner Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, Globalfoundries Dresden Module Two LLC & Co. KG identifies itself as real parties-in-interest. Pet. 7.

B. Related Proceedings

Petitioner states that Patent Owner has asserted the '552 patent in the following patent infringement cases: *DSS Tech. Mgmt., Inc. v. Intel Corp.*, Case No. 6:15-cv-130-JRG (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. Samsung Elec. Co., Ltd.*, Case No. 6:15-cv-690 (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. SK Hynix, Inc.*, Case No. 6:15-cv-691 (E.D. Tex.); and *DSS Tech. Mgmt., Inc. v. Qualcomm, Inc.*, Case No. 6:15-cv-692 (E.D. Tex.). Pet. 7.

Petitioner notes that it has filed a separate petition for *inter partes* review of claims 8–12 of the '552 patent. *Id.* at 8. That proceeding has been designated IPR2016-01314. The '552 patent is also the subject of *Samsung Elec. Co., Ltd. v. DSS Tech. Mgmt., Inc.*, Case IPR2016-00782, as well as the following instituted trial proceedings: *Intel Corp. v. DSS Tech. Mgmt., Inc.*, Cases IPR2016-00287 and IPR2016-00288; *SK Hynix, Inc. v. DSS Tech. Mgmt., Inc.*, Case IPR2016-00192. *Id.* at 7–8.

C. The '552 Patent

The '552 patent describes a process of semiconductor device fabrication and a structure of a semiconductor device having “substantially rectangular” lateral insulating spacers adjacent to gate electrodes. Ex. 1001, Abstract. The '552 patent defines the term “substantially rectangular” to

mean that “a side of the spacer has an angle relative to the substrate surface of more than 85°.” *Id.* at col. 8, ll. 40–42. Figure 4(D) of the ’552 patent is reproduced below.

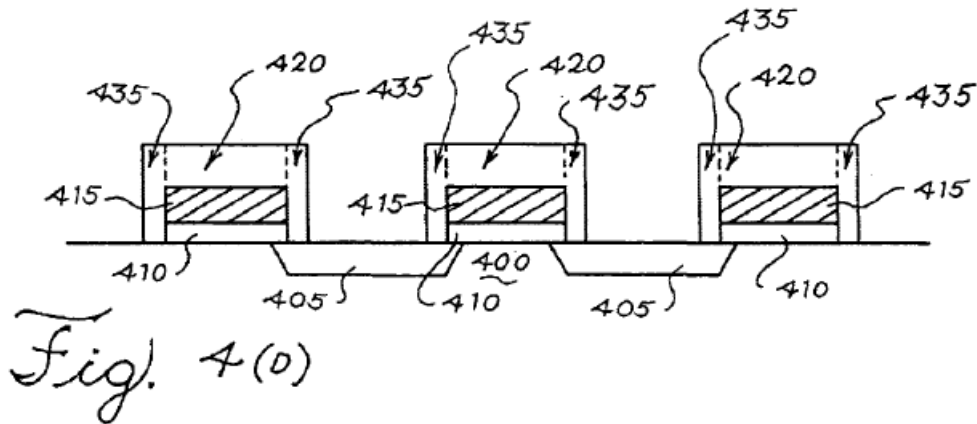


Figure 4(D) illustrates a cross-sectional view of a series of gates 415 (also called conducting layers or polysilicon layers) completely encapsulated in insulating material 420, e.g., TEOS (tetraethyl orthosilicate glass), where spacers 435 of the insulating material adjacent to the gates have substantially rectangular profiles. *Id.* at col. 9, ll. 9–13; col. 11, ll. 40–46. As shown in Figure 4(D), gates 415 are insulated from sources or drains 405 by insulating dielectric layers 410. *See id.* at col. 10, ll. 49–50. The ’552 patent describes a process of making high quality contacts to the sources or drains, such as “self-aligned” contacts, by etching structures over substrate 400 and sources or drains 405. *Id.* at col. 7, ll. 19–22; col. 8, ll. 4–6.

Figure 4(I) of the '552 patent is reproduced below.

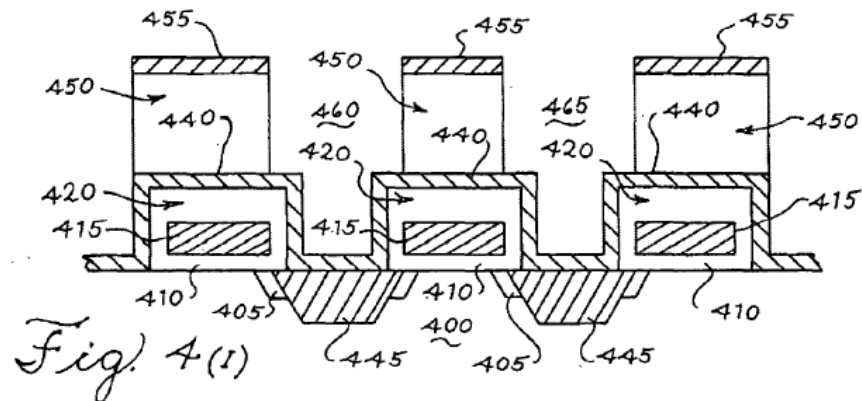


Figure 4(I) illustrates additional structures deposited and etched over the structure described in Figure 4(D), such as second dielectric layer 440 (called etch stop layer), blanket layer 450, and photoresist mask layer 455. *Id.* at col. 9, ll. 33–39; col. 11, ll. 63–65; col. 12, ll. 34–42. According to the '552 patent, etch stop layer 440, e.g., silicon nitride layer 440, depicted in Figure 4(I) is distinct or different from the underlying TEOS insulating layer. *Id.* at col. 12, ll. 10–11. The etch stop layer protects the underlying TEOS layer when blanket layer 450 made of BPTEOS² is etched away to create contact openings 460 and 465 above source or drain 445. *See id.* at col. 12, ll. 36–42; col. 4, ll. 41–59.

A second etch is then performed to remove etch stop layer 440 covering source or drain 445 in contact openings 460 and 465. *Id.* at col. 12, ll. 48–52; col. 7, ll. 43–45. The '552 patent describes that the second etch is “almost completely anisotropic,” which means that the etchant etches in the

² BPTEOS is an acronym for borophosphosilicate tetraethyl orthosilicate glass. *See Ex. 1001, col. 11, ll. 6–7.*

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