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# United States Patent [19]

[11] Patent Number: 5,374,836

Vinal et al.

[45] Date of Patent: \* Dec. 20, 1994

## [54] HIGH CURRENT FERMI THRESHOLD FIELD EFFECT TRANSISTOR

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5,192,990	3/1993	Stevens	257/336
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[75] Inventors: Albert W. Vinal, Cary; Michael W. Dennen, Raleigh, both of N.C.

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[73] Assignee: Thunderbird Technologies, Inc., Research Triangle Park, N.C.

0070744 1/1983 European Pat. Off.

[\*] Notice: The portion of the term of this patent subsequent to Mar. 16, 1993 has been disclaimed.

(List continued on next page.)

[21] Appl. No.: 37,636

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[22] Filed: Feb. 23, 1993

*Characteristics of P-Channel MOS Field Effect Transistors with Ion-Implanted Channels*, Hswe, M. et al., Solid-State Electronics, vol. 15, pp. 1237-1243, 1972.

(List continued on next page.)

### Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 977,689, Nov. 18, 1992, which is a continuation of Ser. No. 826,939, Jan. 28, 1992, Pat. No. 5,194,923.

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[51] Int. Cl.<sup>3</sup> ..... H01L 29/10

### [57] ABSTRACT

[52] U.S. Cl. .... 257/344; 257/386; 257/403; 257/408; 257/900

A high current Fermi-FET includes an injector region of the same conductivity type as the Fermi-Tub region and the source and drain regions, located adjacent the source region and facing the drain region. The injector region is preferably doped at a doping level which is intermediate the relatively low doping concentration of the Fermi-Tub and the relatively high doping concentration of the source region. The injector region controls the depth of the carriers injected into the channel and maximizes injection of carriers into the channel at a predetermined depth below the gate. The injector region may also extend to the Fermi-tub depth to decrease bottom leakage current. Alternatively, a bottom leakage current control region may be used to decrease bottom leakage current. Lower pinch-off voltage and increased saturation current are obtained by providing a gate sidewall spacer which extends from adjacent the source injector region to adjacent the sidewall of the polysilicon gate electrode of the Fermi-FET. The gate sidewall spacer preferably comprises an insulator having permittivity which is greater than the permittivity of the gate insulating layer.

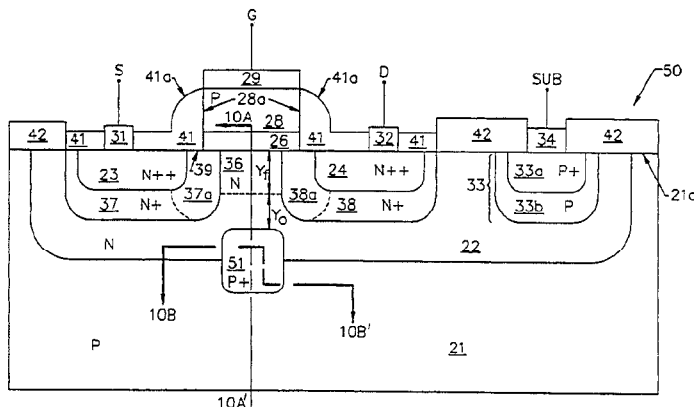
[58] Field of Search ..... 257/327, 336, 340, 344, 257/345, 403, 408, 386, 900, 404

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146 Claims, 28 Drawing Sheets



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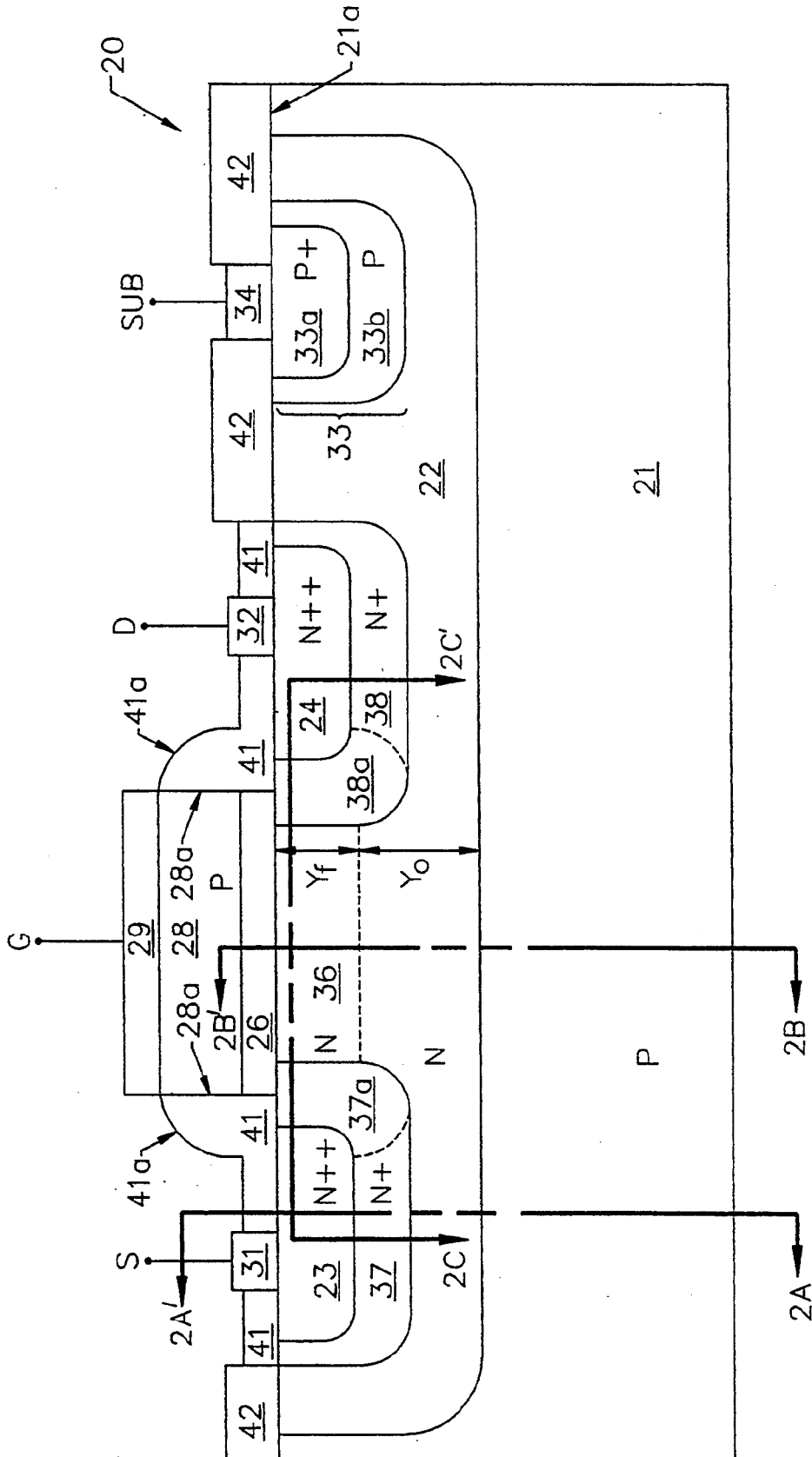


FIG. 1.

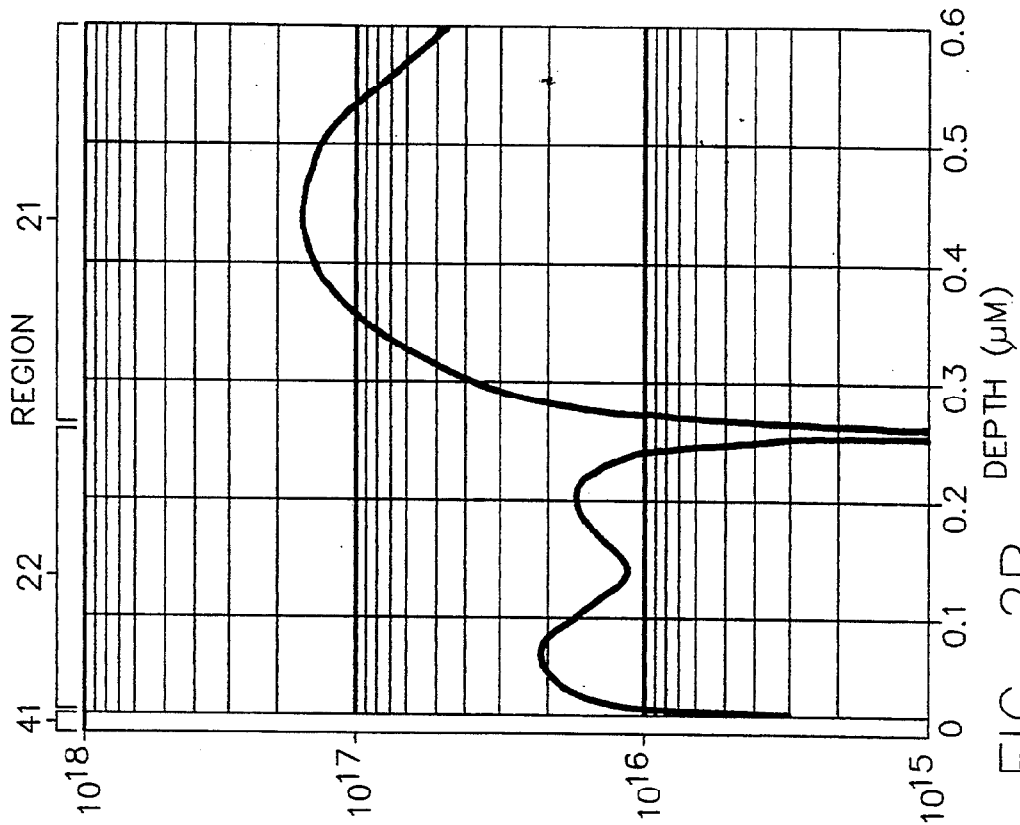


FIG. 2B.

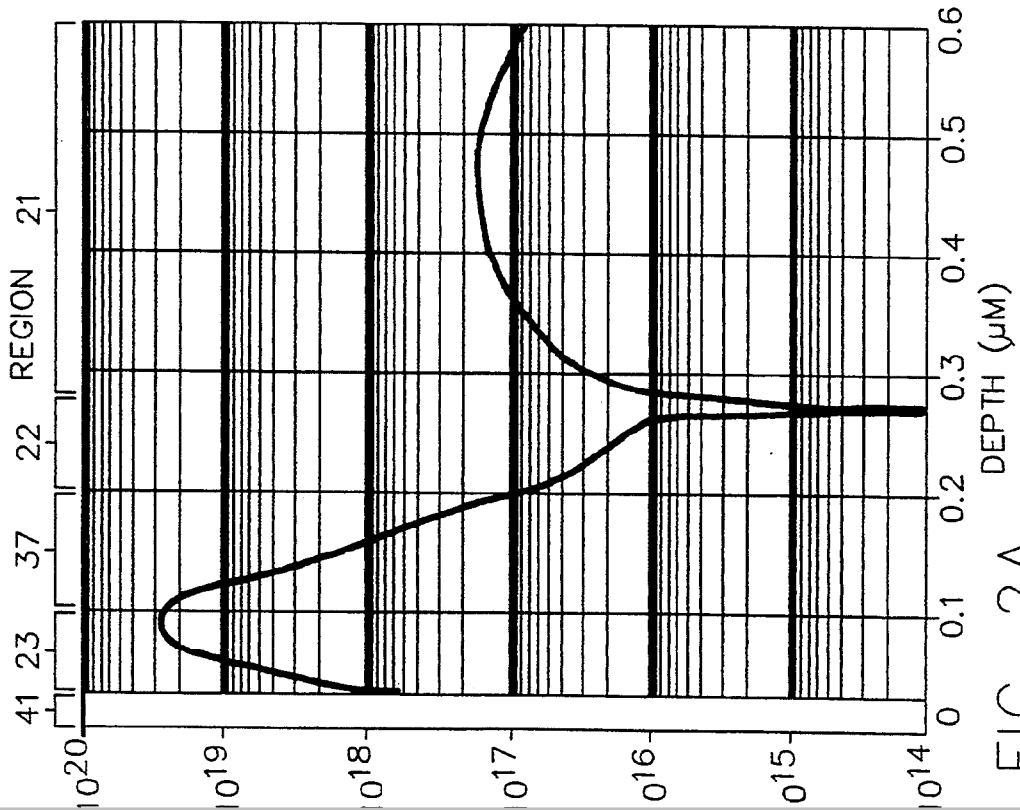


FIG. 2A.

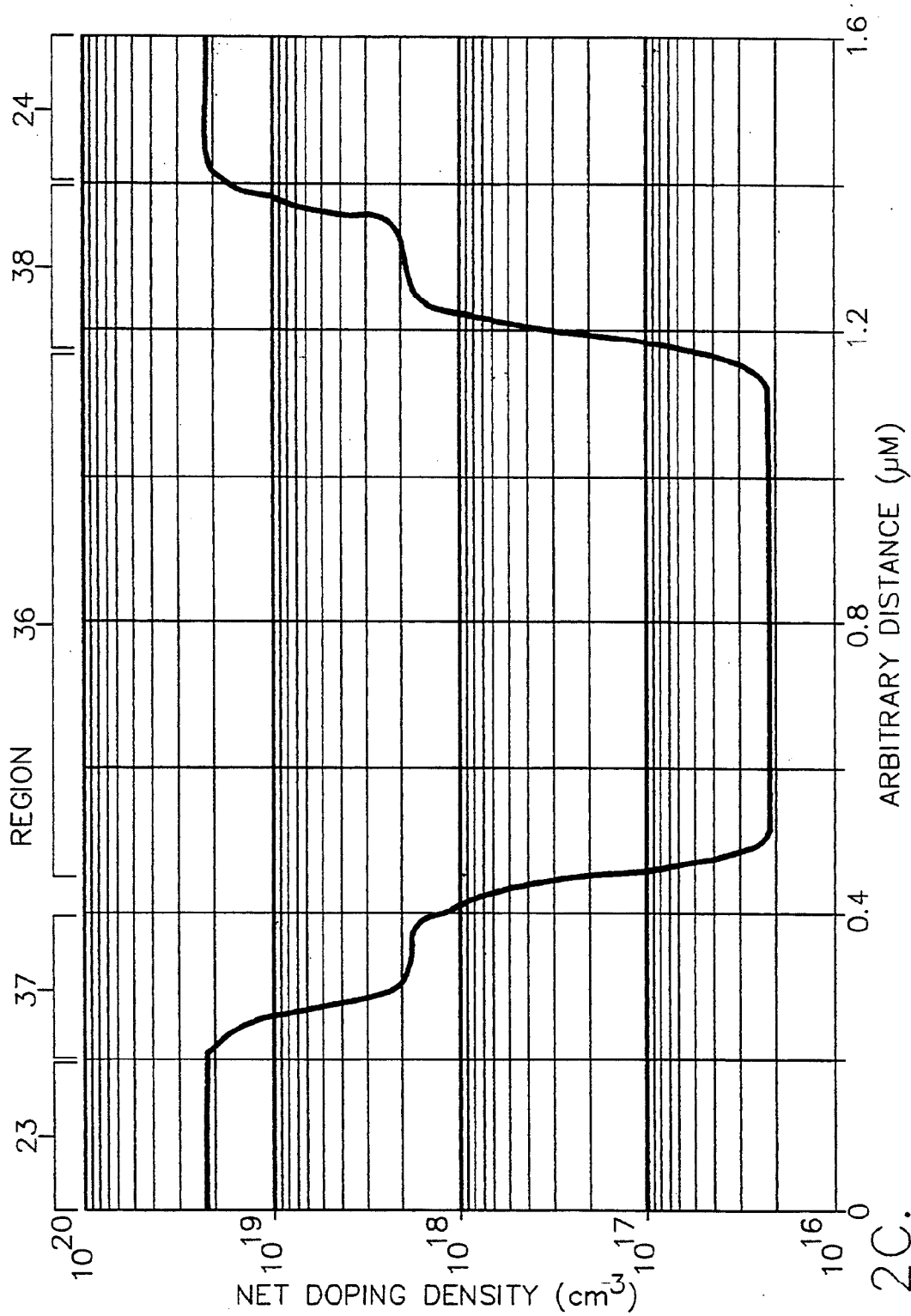


FIG. 2C.

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