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United States Patent [19]

Nulty et al.

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[45] Date of Patent: *May 23, 2000

[54] **METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING**

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[73] Assignee: **Cypress Semiconductor Corporation**, San Jose, Calif.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/577,751**

[22] Filed: **Dec. 22, 1995**

[51] **Int. Cl.**[7] **H01L 21/4763**

[52] **U.S. Cl.** **438/634**; 438/637; 438/639; 438/738; 438/740

[58] **Field of Search** 437/195, 190; 438/595, 634, 639, 637, 738, 740

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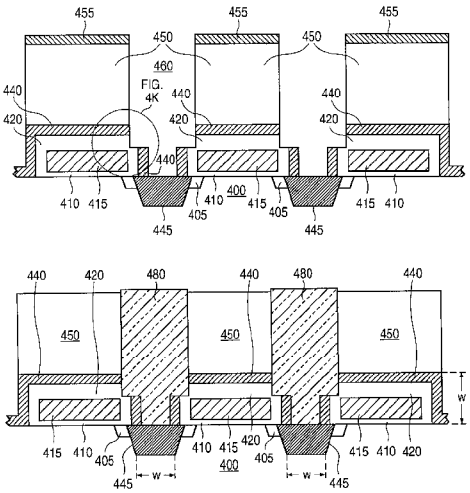
Primary Examiner—John F. Niebling
Assistant Examiner—Lynne A. Gurley

[57] **ABSTRACT**

A process for minimizing lateral spacer erosion of an insulating layer adjacent to a contact region and an apparatus whereby there is provided a contact opening with a small alignment tolerance relative to a gate electrode or other structure are disclosed. The process includes the steps of forming a conductive layer on a semiconductor body, then depositing an insulating layer adjacent to the conductive layer. Next, substantially rectangular insulating spacers are formed adjacent to the gate electrode. An etch stop layer is deposited adjacent the insulating layer, followed by an etch to remove the etch stop layer material from the contact region. This etch is conducted under conditions wherein the etch removes the etch stop layer, but retains the substantially rectangular lateral spacer profile of the first insulating layer. The apparatus is capable of maintaining high quality contacts between the conductive material in the contact region and an device region, such as a source or drain, or some other layer or structure, and is an effective structure for small feature size structures, particularly self-aligned contact structures.

28 Claims, 8 Drawing Sheets



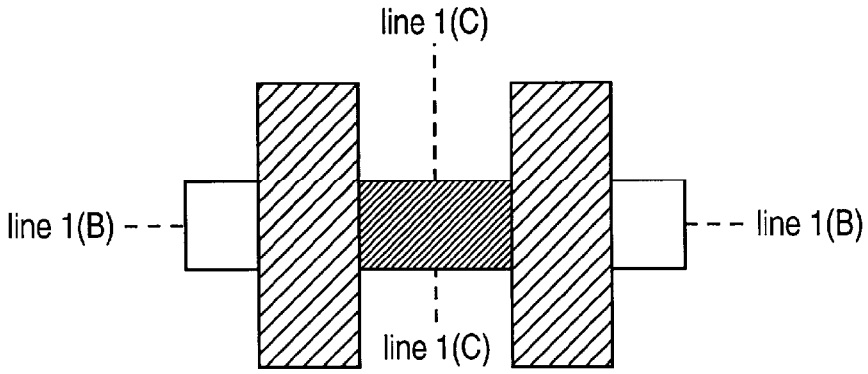


Figure 1A
(PRIOR ART)

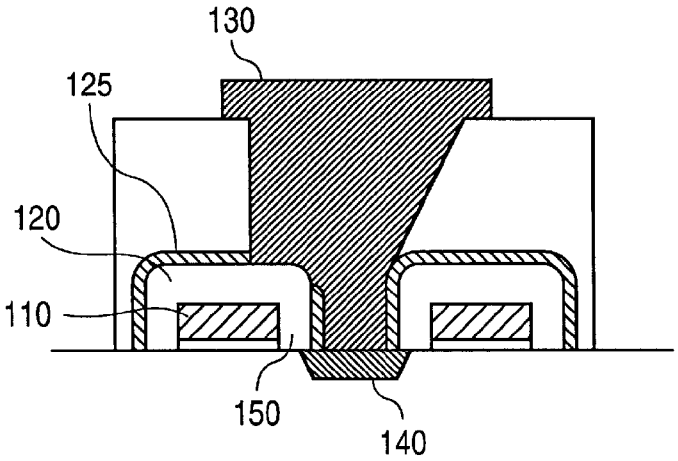


Figure 1B
(PRIOR ART)

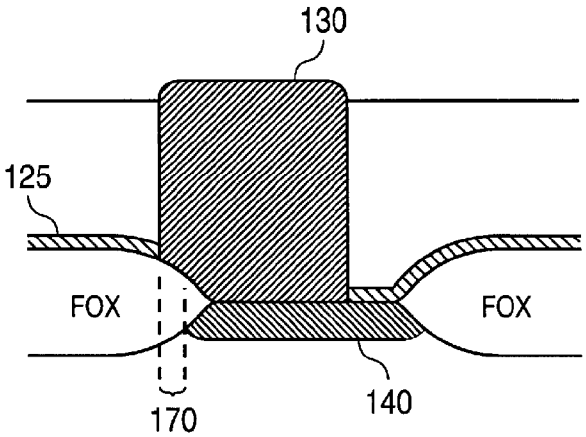


Figure 1C
(PRIOR ART)

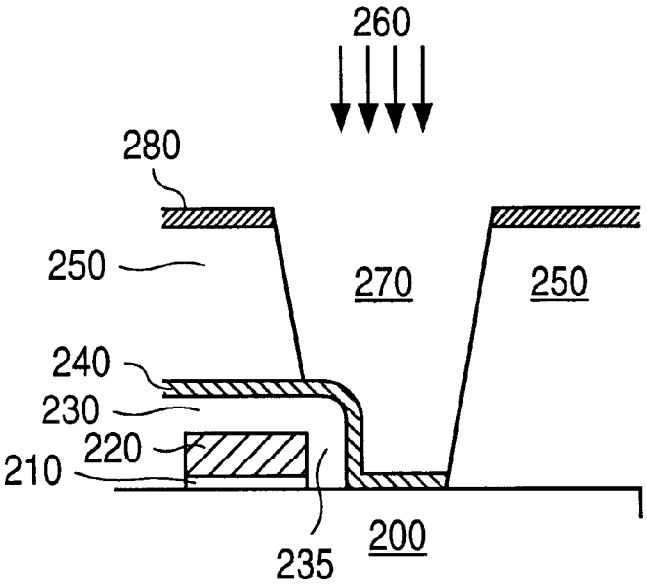


Figure 2A
(PRIOR ART)

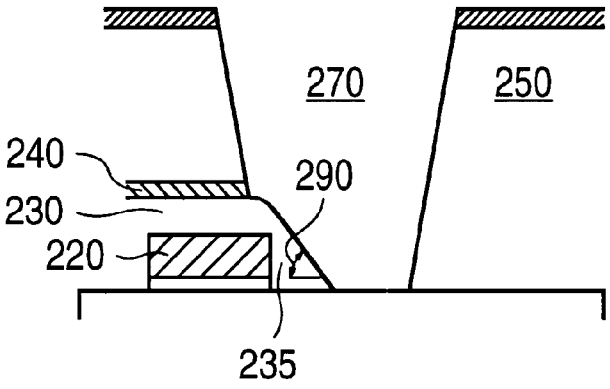


Figure 2B
(PRIOR ART)

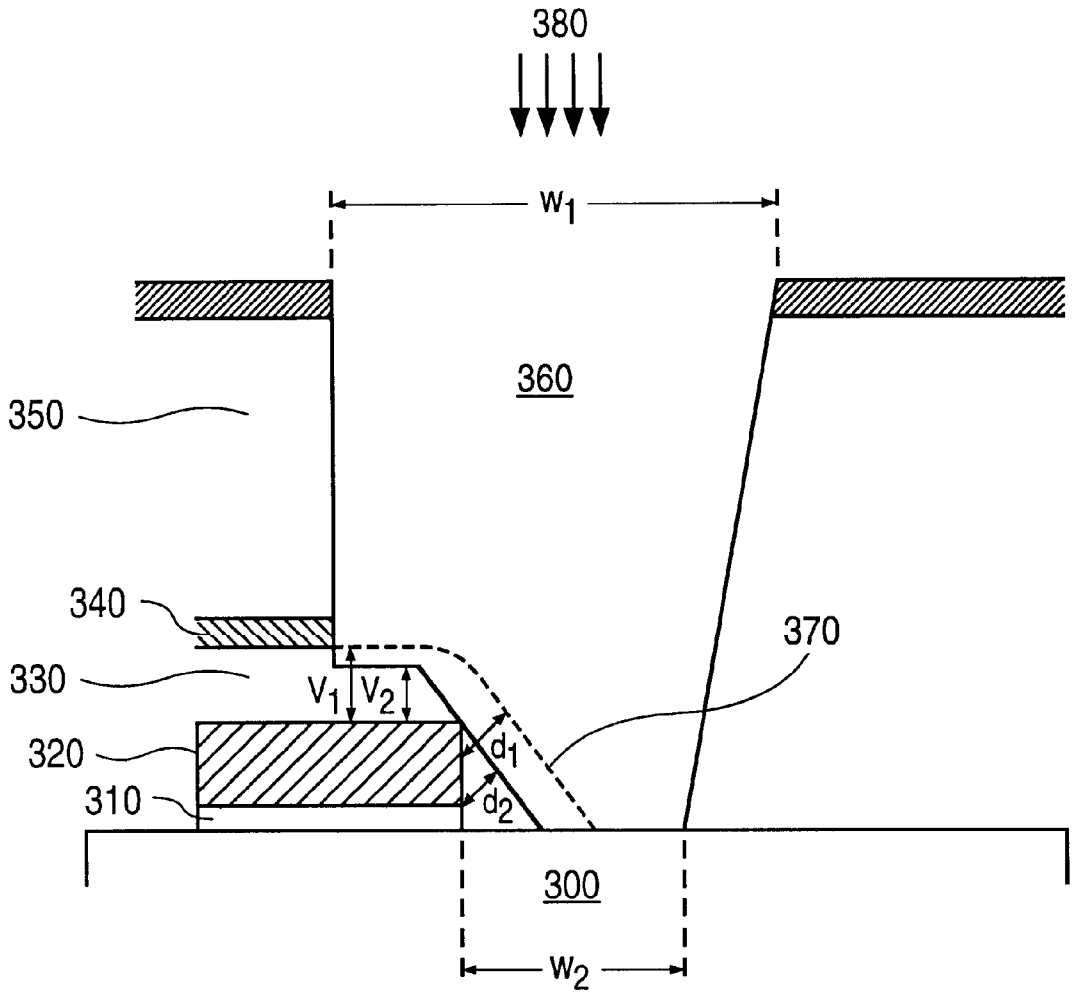


Figure 3
(PRIOR ART)

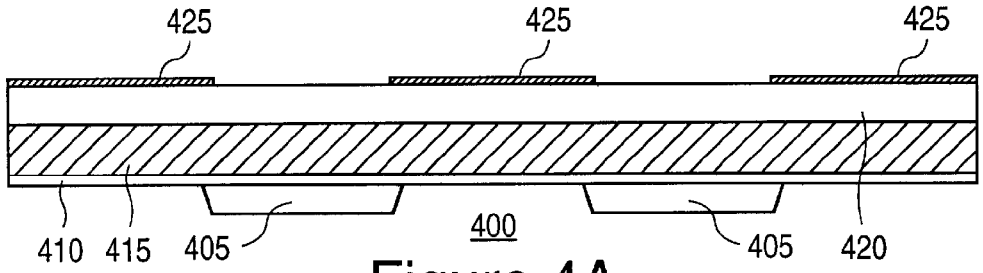


Figure 4A

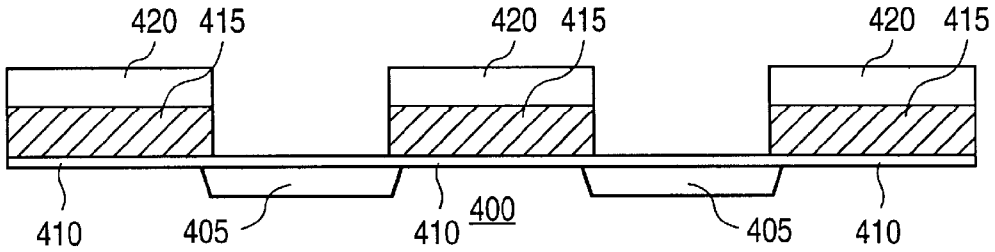


Figure 4B

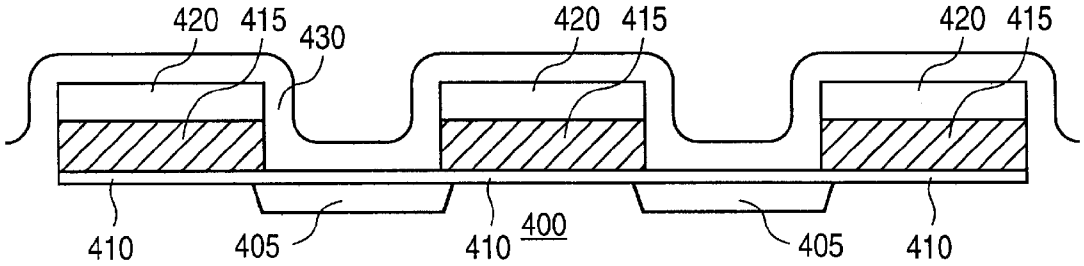


Figure 4C

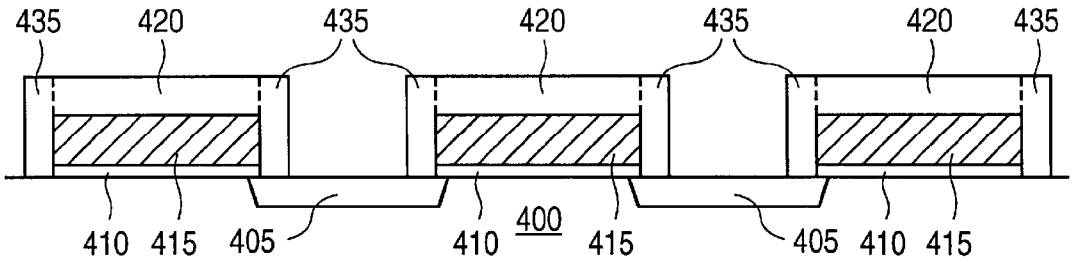


Figure 4D

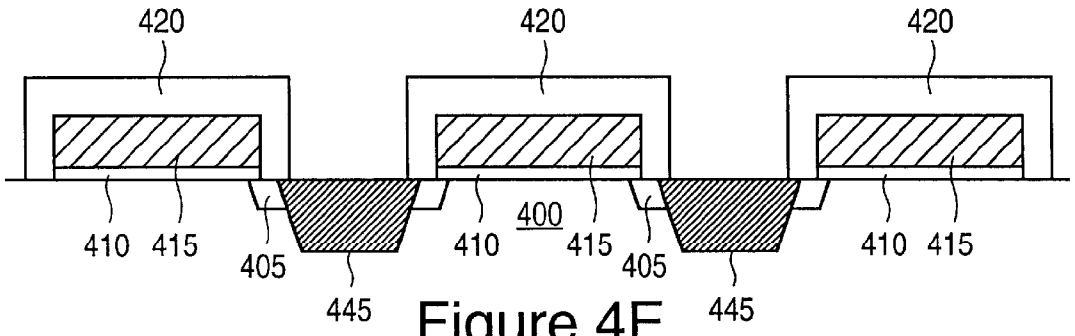


Figure 4E

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