UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED, GLOBALFOUNDRIES INC., GLOBALFOUNDRIES U.S. INC., GLOBALFOUNDRIES DRESDEN MODULE ONE LLC & CO. KG, GLOBALFOUNDRIES DRESDEN MODULE TWO LLC & CO. KG
Petitioner

v.

DSS Technology Management, Inc.
Patent Owner

U.S. Patent No. 6,784,552
Claims 1-7

DECLARATION OF RICHARD BLANCHARD, PH.D. ON BEHALF OF PETITIONER

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I, Richard Blanchard, declare as follows:

1. My name is Richard Blanchard.

2. My academic credentials include both a Bachelor of Science Degree in Electrical Engineering (BSEE) and a Master of Science Degree in Electrical Engineering (MSEE) from the Massachusetts Institute of Technology in 1968 and 1970, respectively. I subsequently obtained a Ph.D. in Electrical Engineering in 1982 from Stanford University

3. I have worked or consulted for more than 40 years as an Electrical Engineer. My primary focus has been on the development, manufacture, operation, and use of devices and integrated circuits, the assembly of these devices and integrated circuits, products that use them, and their failures. My employment history following my graduation from MIT began at Fairchild Semiconductor in 1970. At Fairchild, my responsibilities included circuit and device design, process development, and product engineering in the Linear Integrated Circuits Department.

4. In 1974, I joined Foothill College as an Associate Professor in the Engineering & Technology Division. My responsibilities included developing a program in Semiconductor Technology as well as teaching other courses in the division. While at Foothill College, I co-founded two companies, Cognition and Supertex, and later joined Supertex as a Vice

President in 1978. At Supertex, I designed and developed discrete DMOS (double-diffused metal oxide semiconductor) transistors, as well as integrated circuits that contained DMOS transistors. At Supertex, I also supervised the in-house assembly area, which included responsibility for the associated manufacturing processes. I left Suptertex to join Siliconix in 1982, where I soon became Vice President of Engineering, with the responsibility for directing all of the company's product design and development. At Siliconix, I directed and contributed to the development of both discrete transistors and integrated circuits, including aspects of their assembly.

5. In 1987, I joined IXYS Corporation as a Senior Vice President with the responsibility for organizing an integrated circuit department. At IXYS, I developed integrated circuits that contained DMOS devices or that interfaced to DMOS devices. My responsibilities included the design, assembly, and testing of these integrated circuits.

6. These duties continued until 1991, when I left IXYS to set up Blanchard Associates, a consulting firm specializing in semiconductor technology, including intellectual property. Soon thereafter, I was invited to join Failure Analysis Associates, which I did in late 1991. At Failure

Analysis Associates, I investigated failures in electrical and electronic systems in addition to performing design and development consulting.

7. I left Failure Analysis in 1998 to join IP Managers, which later merged with Silicon Valley Expert Witness Group, now known as Thomson Reuters Expert Witness Services ("Thomson Reuters"). At Thomson Reuters, I work with companies on patent and trade secret matters. I also consult for a number of semiconductor companies, working with them to develop products and intellectual property, or assisting them in other technical areas through Blanchard Associates. Design and development projects that I have worked on range from the design and evaluation of specific components, to the selection of the technology appropriate for the fabrication of different subsystems of a system.

8. I am a member of a number of professional societies, including the Institute of Electrical and Electronic Engineers, the International Microelectronics and Packaging Society, the American Vacuum Society, the Electronic Device Failure Analysis Society, and the Electrostatic Discharge Society.

9. A copy of my curriculum vitae (including a list of all publications authored in the previous 10 years) is attached as Appendix A.

10. I have reviewed the specification, claims and file history of U.S. Patent No. 6,784,552, as well as the petition for inter partes review of this patent: IPR2016-00287, including the Declaration of Dr. John C. Bravman. I understand that the ’552 patent was filed on March 31, 2000 and claims priority to U.S. Patent Appl. No. 08/577,751 (now U.S. Patent No. 6,066,555) filed on December 22, 1995. I understand that, for purposes of determining whether a publication will qualify as prior art, the earliest date that the ’552 patent could be entitled to is December 22, 1995. However, I further understand that the prior assignee claimed a priority date prior to April 21, 1995 during prosecution of the ’555 parent application. ’555 Declaration Under 37 C.F.R. 1.131, Feb. 25, 1999 (Ex. 1011) at 3. In any case, the cited references are prior art and invalidate the ’552 patent.

11. I have reviewed the following patents and publications in preparing this declaration:

- U.S. Patent No. 4,686,000 (“Heath”) (Ex. 1003).
- European Patent Publ. No. 0592078 (“Hawley”) (Ex. 1004).
- U.S. Patent No. 5,541,427 (“Chappell”) (Ex. 1005).
- U.S. Patent No. 5,338,700 (“Dennison”) (Ex. 1006).
- U.S. Patent No. 5,374,836 (“Vinal”) (Ex. 1009).
- U.S. Patent No. 5,053,351 (“Fazan”) (Ex. 1012).

- J. Dulak et al., *Etch mechanism in the reactive ion etching of silicon nitride*, Journal of Vacuum Science & Technology A 9, 775 (1991) ("Dulak") (Ex. 1010).

12. I have reviewed the above patents and publications and any other publication cited in this declaration.

13. I have considered certain issues from the perspective of a person of ordinary skill in the art as described below at the time the '552 patent application was filed. In my opinion, a person of ordinary skill in the art for the '552 patent would have found the '552 patent invalid.

14. I have been retained by the Petitioner as an expert in the field of semiconductor device fabrication and design. I am working as an independent consultant in this matter and am being compensated at my normal consulting rate of $375 per hour for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration.

15. I have no financial interest in the Petitioner. I similarly have no financial interest in the '552 patent, and have had no contact with the named inventor of the '552 patent.

I. RELEVANT LAW

16. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as follows:

A. Claim Construction

17. I have been informed that claim construction is a matter of law and that the final claim construction will ultimately be determined by the Board. For the purposes of my analysis in this proceeding and with respect to the prior art, I have been informed that I should apply what is known as "the *Phillips* standard," rather than the broadest reasonable interpretation standard.

18. Specifically, I have been informed and understand that the '552 patent has expired, and the *Phillips* standard applies for the purposes of claim construction. I further understand that the *Phillips* standard means that claim terms are given their plain and ordinary meaning as understood by a person of ordinary skill in the art at the time of the invention in light of the claim language and the patent specification.

19. I have also been informed and understand that any claim term that lacks a definition in the specification is therefore given its plain and ordinary meaning as understood by one of ordinary skill in the art.

B. Anticipation

20. I have been informed and understand that a patent claim may be "anticipated" if each element of that claim is present either explicitly, implicitly, or inherently in a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

C. Obviousness

21. I have been informed and understand that a patent claim can be considered to have been obvious to a person of ordinary skill in the art at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.

22. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

23. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;

- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

24. I understand that one of ordinary skill in the art has ordinary creativity, and is not an automaton.

25. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

II. SUMMARY OF OPINIONS

26. It is my opinion that every limitation of the structures described in claims 1 through 7 of the '552 patent are disclosed by the prior art, and are anticipated and/or rendered obvious by the prior art.

The following discussion and analysis is substantially the same as that of Dr. John C. Bravman in IPR2016-00287, supplemented with additional analysis and comments provided throughout this declaration.

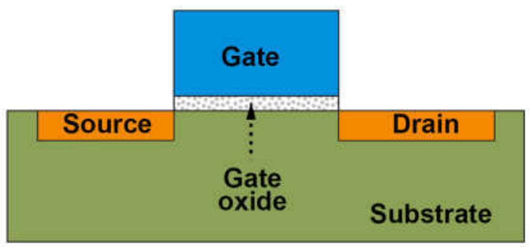
III. BRIEF DESCRIPTION OF THE TECHNOLOGY

A. Basic Structure of Transistors

27. The '552 patent relates to the field of semiconductor integrated circuit manufacturing. Semiconductor integrated circuits, such as microprocessors and

computer memory, are typically made up of hundreds of millions (and in some cases billions) of microscopic structures called transistors. Transistors act as microscopic switches that turn on and off at extraordinarily high rates to enable aggregations of transistors (and other components) to process data.

28. As shown in the figure below, transistors typically include three primary "electrodes" or "terminals"—a gate, a source, and a drain—embedded in or on a substrate and surrounded by dielectrics and other materials:



BASIC TRANSISTOR

29. The source and drain regions (also referred to as "diffusion regions") are transistor components that emit (source) and receive (drain) current/carriers when the transistor is "on." The gate typically sits between the source and drain and is a terminal that can have a voltage applied to it that in turn causes a current to flow between the source and drain.

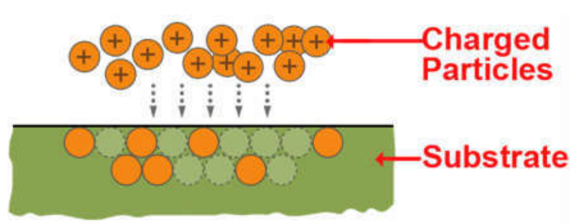
30. The gate, source and drain of a transistor typically need to be connected to other components to form an electrical circuit. The '552 patent refers to the structures used to make these connections as "contacts." Contacts consist of one or more conducting materials (*e.g.*, a metal) that allow current to flow between

transistor components. In many cases, it is important to maintain electrical isolation between contacts and other nearby components (such as a gate electrode) so that current that is supposed to flow to other parts of the circuit does not instead flow to these nearby components (*e.g.*, the gate). As described in more detail below, structures called sidewall spacers can be formed between the contact and the nearby components to maintain this electrical isolation.

B. Overview of Transistor Fabrication

1. Formation of Transistor Components

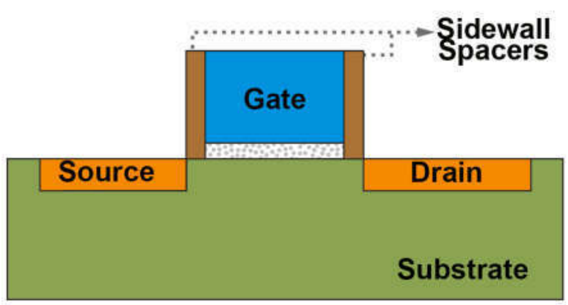
31. Transistor fabrication typically starts with a silicon substrate. In typical planar transistors, source and drain regions ("diffusion regions") are created by implanting regions of the substrate with ions (charged atomic particles) of different materials—called "dopants" or "impurities". (Once implanted the ions become neutral atoms.) This process—referred to as "doping" because it dopes the silicon substrate with atomic particles that have additional charge carriers—is shown below:



A mask can be used for directing the charged particles to specific locations in the substrate.

32. Structures can then be formed above the substrate by depositing layers of other materials onto the substrate. A gate electrode, for example, is formed by first growing or depositing a "gate oxide" (an insulator) on the substrate followed by depositing a conductive material (metal or polysilicon) on top of the gate oxide. The conductive material acts as the gate and the gate oxide creates a layer of isolation between the gate and the source/drain and substrate regions ("S/D regions" or "diffusion regions").

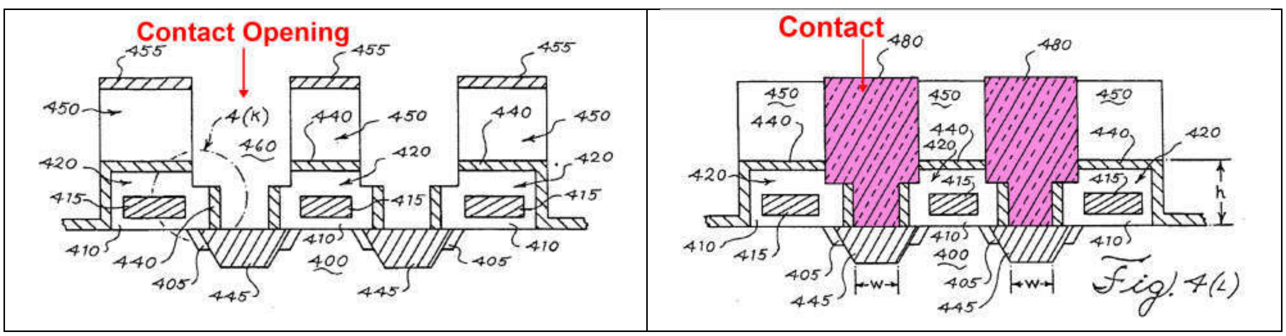
33. Insulating materials may then be deposited around and over the gate and the S/D regions to maintain electrical isolation where desired. Sidewall spacers, for instance, can be formed on each side of the gate electrode as shown below:



As was known as of the time of the alleged '552 invention, such sidewall spacers help to prevent direct electrical contact between the gate electrode and nearby components and thus help to prevent short-circuits.

2. Etching to Create Contact Openings

34. Gate electrodes and S/D regions of transistors must typically be connected to other components in the semiconductor device. These connections are made using "contacts"—connections between components that allow electrical signals to pass between the components. Contacts are formed by creating openings through the layers of a semiconductor device (*i.e.* "contact openings") and then performing a process that fills the openings with a conductive material. Fig. 4(J) of the '552 patent shows a fully-formed contact opening 460, while Fig. 4(L) shows the contact opening after it has been filled with a conductive material 480 (pink) to form the contact[1]:



The process of removing material to create contact openings is known as "etching." To perform etching, semiconductor manufacturers use "etchants." As was known at the time of the alleged '552 invention, etchants have various known properties that can be chosen depending on the type of etching desired.

[1] All emphasis and annotations added unless otherwise indicated.

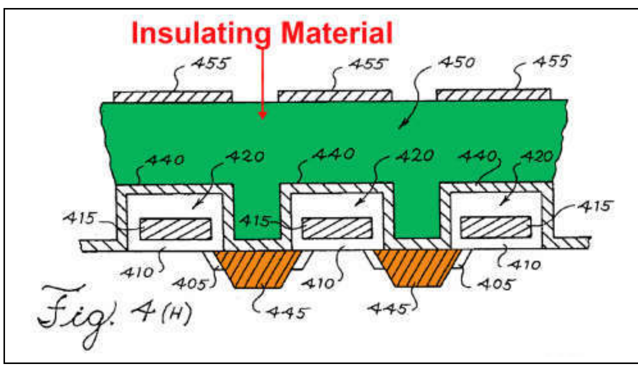
35. Etching can be performed "isotropically" or "anisotropically." An isotropic etch will etch material in all directions (*e.g.*, both vertically and horizontally with respect to the substrate surface). An anisotropic etch will etch material more effectively in a particular direction (*e.g.*, vertically but not horizontally relative to the substrate surface).

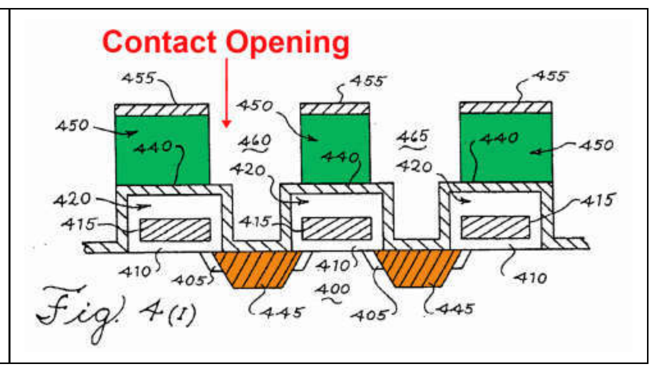
36. Etching can also be "wet" or "dry." Wet etching refers to etching in which the etchant is a liquid, which will dissolve through a particular material to create a contact opening. Dry etching—sometimes based on the physical process known as "sputtering"—is etching away material by using a gas or plasma to bombard the material to be etched with ions. Generally, wet etching is used to perform isotropic etching (*i.e.*, all directions) and dry etching is used to perform anisotropic etching (*i.e.*, one direction).

37. Etchants can also be "selective" or "non-selective." The "selectivity" of an etchant refers to its effectiveness at etching away one type of material versus another type of material. A highly-selective etchant relative to a particular material will etch away that material at a much faster rate than a different type of material. A non-selective etchant will etch away both types of materials at approximately the same rate. *See, e.g.*, '552 at 2:12-21; *see also id*. at 4:66-5:2. The same etchant can behave as either a selective or non-selective etchant depending on the material being etched, the processing conditions, and other parameters of the etching

process. For example, an etchant that is selective as to one material can be non-selective as to another.

38. As was well-known at the time of the ’552 patent, contact openings of various shapes and sizes can be created depending on the etching method chosen. As shown in Figs. 4(H) and 4(I) of the ’552 patent, the etchant removes material to create an “opening” in the layers of a semiconductor device. Fig. 4(H) shows a transistor structure with insulating material 450 (green) covering the diffusion regions 445 (orange). Fig. 4(I) shows the same structure after the insulating material has been etched to create contact openings 460 and 465 which extend down towards the diffusion regions:

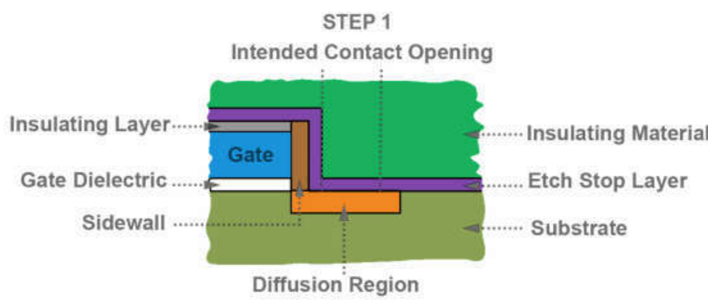




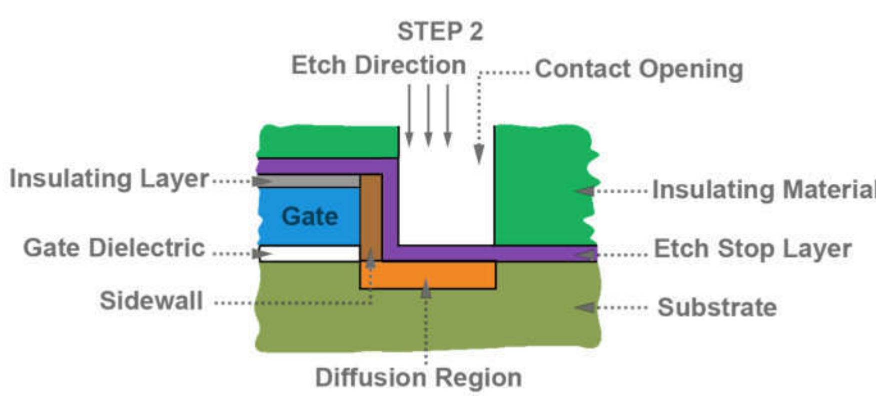
39. As was also well known, “etch stop layers” (material 440 in Figs. 4(H) and 4(I)) can be used to avoid etching areas not intended to be removed. An etch stop layer, as its name suggests, effectively stops an etchant from further eroding or removing material once the etching process reaches the etch stop layer.

Etch stop layers are thus used to protect components (*e.g.*, a gate electrode or S/D region) by stopping the etchant before it reaches the protected component.

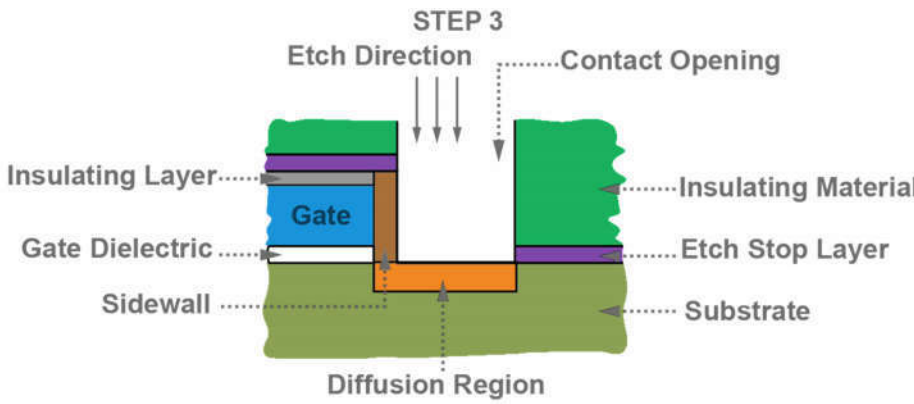
40. The following figures illustrate the process. The figure below (step 1) shows a diffusion region with an etch stop layer above it and further covered by an insulating material:



41. As shown in the figure below (step 2), to make a contact opening down to the diffusion region, an etchant is applied to the insulating material. (Masking layer not shown.) The etchant effectively etches away the insulating material but not the etch stop layer. As a result, when the etchant reaches the etch stop layer, etching is stopped. In this way, the etch stop layer prevents the etchant from etching into and damaging the diffusion region:



42. As shown in the figure below (step 3), the etch stop layer can then be removed by using a different (and usually more precise) etching process to complete the contact opening down to the diffusion region (masking layer not shown):

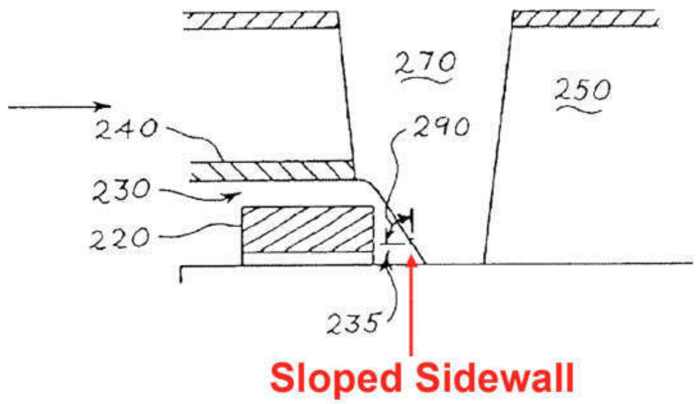


IV. OVERVIEW OF THE ’552 PATENT

A. The Alleged Problem in the Art

43. The ’552 patent purports to describe an improved technique for forming contact openings in transistors. The patent asserts that prior art techniques for forming contact openings resulted in an unacceptably high risk of creating unintentional connections (and thus a short-circuit) between the contacts and nearby components. Specifically, according to the patent, the use of highly selective etchants to create contact openings caused the sidewall spacers between a contact opening and a nearby component (such as a gate electrode) to become

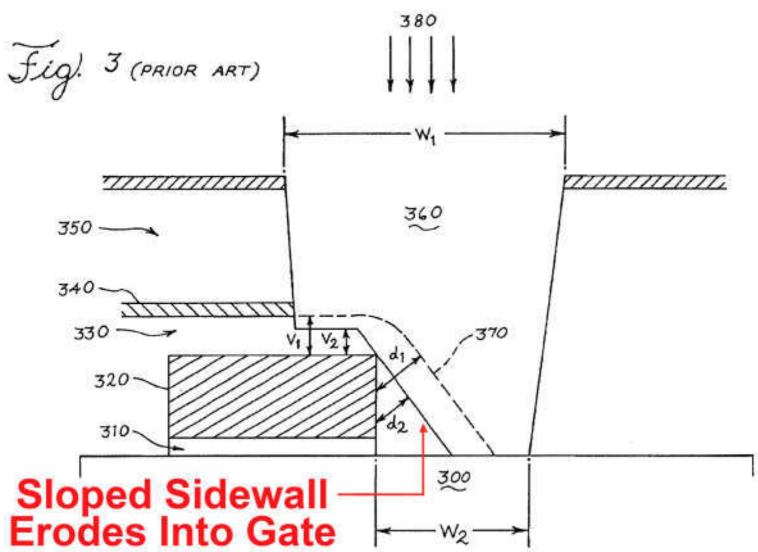
sloped. ’552 at 5:6-14 (“The properties of the highly selective etch of the overlying etch stop layer 240 will ***transform a substantially rectangular spacer into a sloped spacer***.”); *id.* at 2:4-6, 2:39-41. This is shown in Fig. 2(B):



The figure, described as “Prior Art,” shows a contact opening 270, a sidewall spacer 235, and a gate electrode 220 that needs to remain isolated from the contact opening. As shown, the sidewall spacer has become “sloped.” ’552 at 5:6-14; *see also id.* at 5:51-55.

44. The patent then explains that, in subsequent fabrication steps, a sloped sidewall is particularly susceptible to erosion such that it can be worn down to the point that the contact opening and a nearby component (*e.g.*, the gate electrode) can come into unintentional contact. Specifically, the patent explains that, after the contact opening is formed, an additional etching step is usually performed to clean the contact opening. ’552 at 5:55-56 (explaining that “RF sputter etch” is performed). This final etching step—which is a dry etch performed using vertical

bombardment—can erode the remaining insulating material separating the gate electrode from the contact opening. The patent explains that because the sidewall spacer has become sloped, it is more directly exposed to the vertical bombardment and thus more susceptible to erosion. ’552 at 5:59-6:1 (“The dynamics of the sputter etch 380 are that it proceeds vertically, directing high-energy particles at the contact region. . . . ***Because the spacer portion 370 is sloping or diagonal, a significant surface area portion of the spacer portion 370 is directly exposed to the high-energy particles from the RF sputter etch 380.***”). This is shown in Fig. 3:



As shown, as a result of this process, the sloped sidewall spacer has become further eroded from the dotted line (370) to the solid line such that the gate electrode 320 is now exposed to the contact opening. ’552 at 6:14-19 (“[T]he result of the sputter etch 380 is that the sputter etch 380 laterally erodes the diagonal portion of the TEOS spacer portion 370 adjacent to the contact region to a point where the polysilicon layer 320 [*i.e.*, the gate electrode] is no longer isolated from the contact region 360 by an insulating layer."). According to the patent, such contact results in a short-circuit and thus a non-functioning transistor. '552 at 6:19-21.

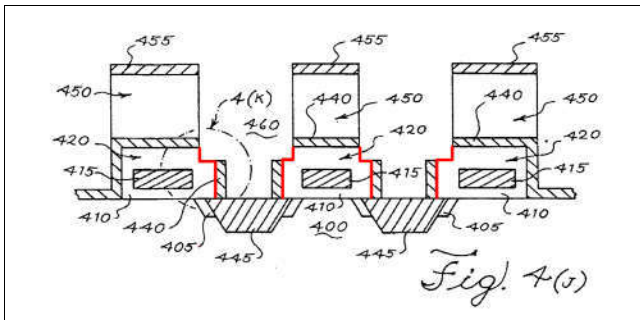
B. The Alleged '552 Patent Invention

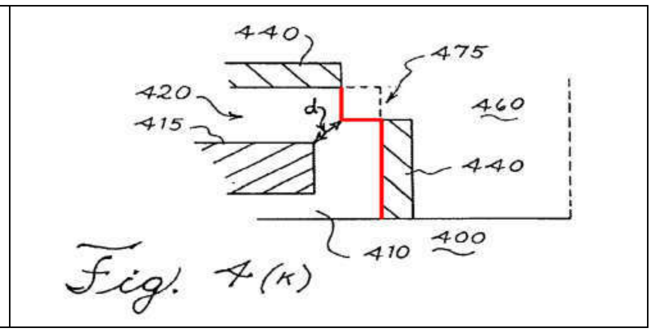
45. The patent purports to solve this problem by using a process that prevents the formation of a sloped spacer and instead retains the "substantially rectangular" shape of the lateral spacer. '552 at 11:48-49 ("[C]are is taken to etch the spacers 435 such that the spacers 435 have a substantially rectangular profile."), 13:9-16 ("Of primary significance, the spacer portion 435 of the TEOS layer retains its substantially rectangular profile. . . . ***The invention relates to these process conditions as well as others that result in the retention of a boxy spacer***." (TEOS is a common type of insulator used in integrated circuits)).

46. The patent does not purport to have invented the use of sidewall spacers, the use of anisotropic etchants to etch in a vertical direction, or the use of such etchants to form contact openings. All of this was indisputably well-known. '552 at 1:10-7:13 (Background). Instead, the patent claims as its novel concept the use of a known etchant in such a way that retains the "substantially rectangular" shape of the sidewall spacer. Specifically, the patent describes using an anisotropic etchant that etches only vertically relative to the substrate surface to

form a contact opening. According to the patent, the use of such an etchant avoids the problem of creating a sloped spacer and instead "retains the substantially rectangular lateral spacer portion" of the lateral spacer. '552 at 7:45-51 ("The etch-stop is also almost completely anisotropic, meaning that the etchant etches in one direction-in this case, vertically (or perpendicular relative to the substrate surface) rather than horizontally. The etch removes the etch stop insulating layer and ***retains the substantially rectangular lateral spacer portion*** of the first insulating layer.").

47. Figs. 4(J) and 4(K) (which is a blow up of 4(J)) show the contact opening after etching is complete:





'552 at 12:54-13:10. As shown by the red lines in the figures, after the contact opening 460 has been etched, the sidewalls (420) have vertical sides thus retaining their "substantially rectangular" shape.

48. As a result, according to the patent, the lateral spacer is less susceptible to erosion in the subsequent sputter etch step—which involves the vertical bombardment of the contact region with high energy particles—and thus

the risk of unintentional contact (and short-circuit) with nearby components is reduced. ’552 at 7:62-8:3 (“Unlike prior art processes whereby the sputter etch erodes the underlying sloping lateral spacer portion of the first insulating layer adjacent to the conducting layer, the sputter etch does not significantly erode the substantially rectangular lateral spacer of the first insulating layer, thus allowing the conductive layer of the device structure to remain completely isolated. . . .”). Claim 1 is the sole challenged independent claim. The dependent claims add only implementation details such as: the specific materials for certain components (claims 2-3); additional specificity regarding the materials around the insulating spacer (claims 4-5); additional insulating layers on the structure (claim 6); and conductive material in the contact region (claim 7).

C. Prosecution History

49. The ’552 patent was filed on March 31, 2000. The ’552 patent is a divisional of, and claims priority to, U.S. Patent No. 6,066,555 (the “’555 patent”), which was filed on December 22, 1995.

50. The original claims of the ’552 patent were directed to forming a transistor structure with a “substantially rectangular” spacer portion adjacent to a contact opening. Application, Mar. 31, 2000 (Ex. 1013) at 28-32. On the day they were filed, twenty-four of the twenty-six original claims were canceled by the applicants and new claims were added by preliminary amendment. Prelim.

Amendment, Mar. 31, 2000 (Ex. 1014) at 1-3. The new independent claims recited the common components of prior art transistor structures, including a substrate, gate electrode ("a conductive layer"), etch stop material, and sidewall spacers ("insulating spacers"). The dependent claims added the further requirement that the spacers be "substantially rectangular." *Id*. at 2-3.

51. The claims were rejected by the Examiner on various grounds, including under 35 U.S.C. § 102(b) as anticipated by a prior art patent to Dennison (Ex. 1006). Office Action, June 1, 2001 (Ex. 1015) at 6-9. The Examiner determined, among other things, that Dennison disclosed all of the components of the claimed transistor structure, including an insulating spacer with "a substantially rectangular profile in the contact region. . . ." *Id*. at 6.

52. The applicants responded to the rejections by attempting to distinguish Dennison on the basis that it did not disclose an "etch stop layer" as claimed in the '552 application. Amendment, Oct. 1, 2001 (Ex. 1016) at 20. The Examiner disagreed and concluded that Dennison disclosed a layer that is "well known in the art to use as an etch stop material. . . ." Office Action, Jan. 9, 2002 (Ex. 1017) at 4.

53. The applicants then responded by amending the independent claims to expressly require the etch stop material to be "different" from the insulating spacer. Amendment, Apr. 29, 2002 (Ex. 1018) at 2. The applicants further argued that

prior art methods of transistor fabrication "use[d] etchants with high selectivity" that could "transform a substantially rectangular spacer adjacent to the contact region into a sloped spacer." *Id.* at 3. The applicants explained that the alleged invention "avoids this problem by retaining the substantially rectangular profile of the insulating spacers." *Id.*

54. The Examiner maintained the rejections for all of the claims. The Examiner found that even though Dennison did not disclose an etch stop material that was different from the insulating spacer, such an etch stop layer would have been obvious. Office Action, Sept. 11, 2002 (Ex. 1019) at 3. The Examiner also found that the insulating spacer disclosed in Dennison, like the insulating spacer claimed in the '552 application, had a "substantially rectangular profile in the contact region." *Id.* The applicants filed a request for reconsideration but the Examiner maintained his rejection of all pending claims. *See* Request for Reconsideration, Mar. 4, 2003 (Ex. 1020); Office Action, May 20, 2003 (Ex. 1021).

55. The applicants then amended the independent claims to expressly require "wherein the insulating spacer has a substantially rectangular profile in the contact region." Amendment, Feb. 6, 2004 (Ex. 1022) at 2-3; *see also id.* at 4 ("As illustrated in Figure 4K of the present specification, the spacer retains a

substantially rectangular or 'boxy' profile, *i.e.*, the sides of the spacer are not sloping.").

56. After a discussion with the Examiner on February 19, 2004, the applicants amended the specification to define "substantially rectangular" as follows: "The phrase 'substantially rectangular' means that a side of the spacer has an angle relative to the substrate surface of more than 85°." Corrected Amendment, Mar. 31, 2004 (Ex. 1023) at 2, 6. The applicants also amended the independent claims again to require "wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°." *Id.* at 3-4. Following this amendment, the Examiner allowed the claims. Allowance, Apr. 20, 2004 (Ex. 1024).

57. As this Petition will demonstrate, the use of substantially vertical sidewall spacers was well known. As described below, the Heath prior art patent—which was not disclosed during prosecution of the '552 patent—discloses the use of such vertical sidewall spacers. Accordingly, even the applicants' minor claimed distinction over the prior art was in fact no distinction at all.

V. OVERVIEW OF THE PRIMARY PRIOR ART REFERENCES

A. Summary of the Prior Art

58. After reviewing the '552 patent and the prior art discussed herein, my conclusion is that there is nothing novel in the challenged claims. The alleged

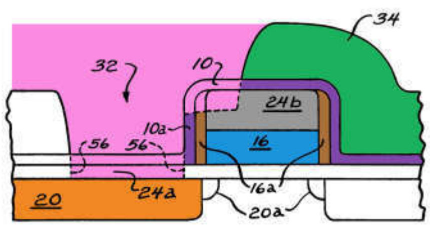
invention of the ’552 patent consists of using known techniques (non-highly selective, anisotropic etching) to etch a contact opening with a known (substantially rectangular) profile and to create a transistor comprising known components (gate electrodes, diffusion regions, insulating materials, sidewall spacers and etch stop material). These techniques and structures were well-known by persons of ordinary skill in the art over a decade before the ’552 patent was filed and almost eight years before the earliest alleged priority date.

B. Overview of Heath (Ex. 1003)

59. U.S. Patent No. 4,686,000 to Heath was filed on February 19, 1986 and issued on August 11, 1987. I understand that Heath is therefore prior art under 35 U.S.C. § 102(b).

60. Heath is directed to the same alleged problem—avoiding a short-circuit between the contact and the gate electrode—as the ’552 patent and discloses solving it in precisely the same way: through the use of a non-conductive sidewall spacer with vertical sides. Heath at Abstract (“An improved process for self-aligned contact window formation in an integrated circuit leaves a ‘Stick’ of etch stop on ***vertical sidewall*** surfaces to be protected.”).

61. Specifically, Heath discloses a transistor structure consisting of the same components arranged in the same way as the alleged invention of the ’552 patent. As shown below in Fig. 8C (color coded), just like the structure described in the ’552 patent, Heath’s transistor structure includes a **source/drain diffusion region 20** (orange) in a substrate, a **gate electrode 16** (blue) with **sidewall spacers 16a** (brown), an **etch stop material 10a** (purple), a **contact opening 32** (pink), and additional **insulating layers 24b** and **34** (gray and green):



62. Critically, as shown above in the figure, Heath discloses maintaining a sidewall spacer with “vertical sides”—*i.e.*, 90° with respect to the horizontal substrate surface—resulting in a substantially rectangular profile. Heath at Abstract (“An improved process for self-aligned contact window formation in an integrated circuit leaves a “Stick” of etch stop ***on vertical sidewall*** surfaces to be protected.”); Heath at 5:26-30, 10:12-13. Specifically, Heath describes etching “anisotropic[ally]” in a vertical direction to maintain the vertical sidewalls of the lateral spacer. *Id.* at Abstract, 10:2-11 (“[T]he part of layer 10 between dashed lines 56 is removed leaving a ***vertical stick 10a*** of layer 10. . . . Some oxide 24 will remain on the top of gate electrode 16 even after the etch exposes the source/drain

region 20 within the contact window, and ***because the nitride removal is anisotropic*** [*i.e.*, it can etch vertically], ***the 'stick' 10a will remain on the side, so no short to electrode 16 can occur***.").

63. Heath specifically explains that the purpose of this design is to avoid creating a short-circuit between the contact that will be placed in the opening and nearby components. Heath at 10:7-11 ("[B]ecause the nitride removal is anisotropic, the 'stick' 10a will remain on the side, so ***no short to electrode 16 can occur***."); *id*. at 11:11-15. Heath thus solved the same problem in the same way as the '552 patent nearly ten years before the application for the '552 patent was filed.

C. Overview of Supporting References

64. The supporting references relied on in this Petition show that any implementation details not specifically disclosed in Heath (*e.g.*, the types of materials used for layers of the transistor structure) were also well known.

1. Hawley (Ex. 1004)

65. European Patent Application No. 0 592 078 to Hawley was published April 13, 1994. I understand that Hawley is therefore prior art under 35 U.S.C. § 102(b).

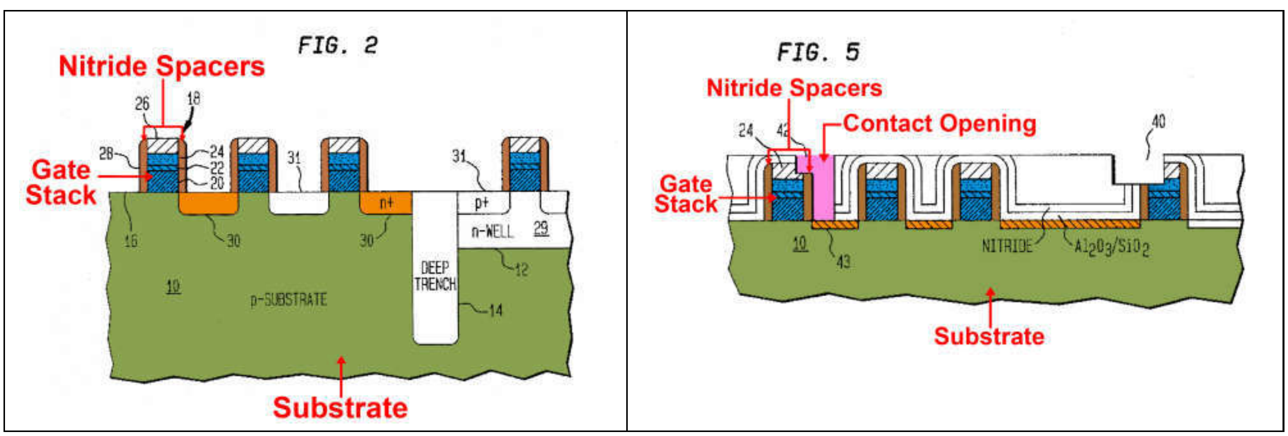
66. Like Heath and the '552 patent, Hawley is generally directed to the formation of openings in semiconductor devices. Hawley discloses, among other

things, forming a contact opening using multiple etch stop layers made of different materials—including silicon nitride and silicon dioxide as claimed in the '552 patent. Hawley at 2:39-44 (explaining that first and second etch stop layers can be made of silicon nitride and silicon dioxide respectively); Abstract (explaining that etch stop layers can be made of different materials).

2. Overview of Chappell (Ex. 1005)

67. U.S. Patent No. 5,541,427 to Chappell et al. was filed on December 3, 1993 and issued on July 30, 1996. I understand that Chappell is therefore prior art under 35 U.S.C. § 102(e).

68. Like Heath, Hawley, and the '552 patent, Chappell is directed to the fabrication of contact openings in semiconductor devices. Chappell discloses a **contact opening 42** (pink) formed next to a **gate stack 22-24** (mislabeled in Fig. 5) (blue) with adjacent **spacers 28** (brown):



Chappell at Figs. 2, 5; *id*. at 3:58-4:49. As in Heath, the contact opening of Chappell is formed such that it does not contact the gate electrode. *Id*. at 4:41-49

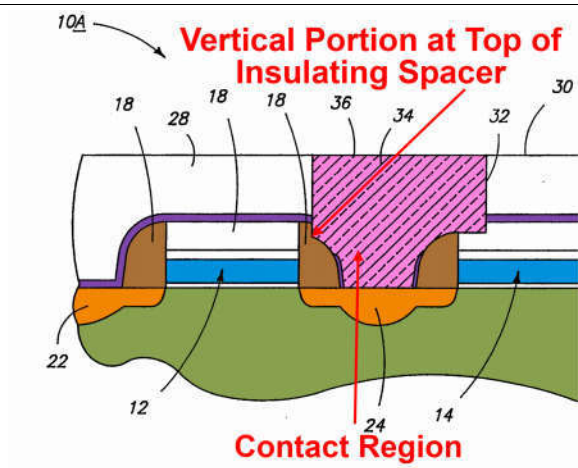
("This opening is placed so that it is borderless to the gate stack. . . . [W]hen opening 42 is filled with an electrically conductive material, there is no contact to the electrically conduc[t]ive portions of gate stack 18."). Chappell discloses that the spacers 28 are nitride. *Id*. at 4:7-8 ("Nitride spacers 28 are formed along the gate edges.").

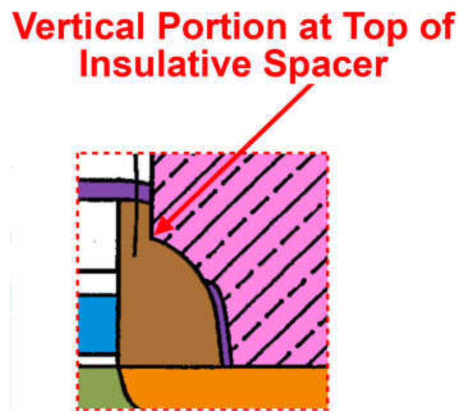
3. Overview of Dennison (Ex. 1006)

69. U.S. Patent No. 5,338,700 to Dennison et al. was filed on April 14, 1993 and issued on August 16, 1994. I understand that Dennison is therefore prior art under 35 U.S.C. § 102(b). Dennison was made of record during prosecution of the '552 patent but was not considered in combination with Heath.

70. Dennison is directed to the formation of contact openings in transistor structures. Dennison at 1:11-32. Specifically, Dennison describes a structure in which silicon nitride (Si_3N_4) insulating spacers (brown) line the contact opening. Dennison at Fig. 1; *see also id.* 3:29-34, 4:6-10.

71. Dennison explains that, as shown in Fig. 2A below, etching to remove the etch stop material from over the diffusion region and otherwise clean the contact opening can also result in partial etching of the insulating spacer 18 such that a ***substantially vertical portion at the top of the insulating spacer*** remains (as shown by the red arrow below):





(zoomed in)

VI. CLAIM CONSTRUCTION

72. The following discussion proposes constructions for certain terms of the challenged claims and support for those constructions.

73. The ’552 patent has expired. Accordingly, as noted above, I understand that I should apply the claim construction based on the *Phillips* standard rather than the broadest reasonable interpretation standard applicable to non-expired patents.

74. I propose to construe one term that appears in claim 1 of the ’552 patent as follows:

Term	Proposed Construction
“a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°” (claim 1)	“a side of the insulating spacer has an angle relative to the horizontal substrate surface that is greater than 85° and less than or equal to 90°”

75. I conclude that the plain language of the claims, the specification, and the Patent Owner's statements in co-pending litigation confirm that the term "a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°" should be construed as "a side of the insulating spacer has an angle relative to the horizontal substrate surface that is greater than 85° and less than or equal to 90°." Specifically, I conclude that the claimed "side" should not be limited to a ***particular*** side (or particular portion of a side) of the insulating spacer, but instead should be construed to be any side of the spacer that is at an angle relative to the horizontal substrate surface that is greater than 85° and less than or equal to 90°. My conclusion is based on at least the following reasons.

76. First, the plain language of the claims confirms that the term should be construed to require the spacer to have a side with a particular angle relative to the substrate surface. The claims state that "***a side***"—*i.e.*, any side—of the insulating spacer can be the side with the required angle. '552 at claims 1, 8. The claims do not limit the "side" to a particular side (or a particular portion of a side) of the insulating spacer but instead allow the angle to be measured relative to "a side" of the spacer. The claims then specify that the required angle is either a "right angle or an acute angle of more than 85°" (*i.e.,* it must be an angle greater

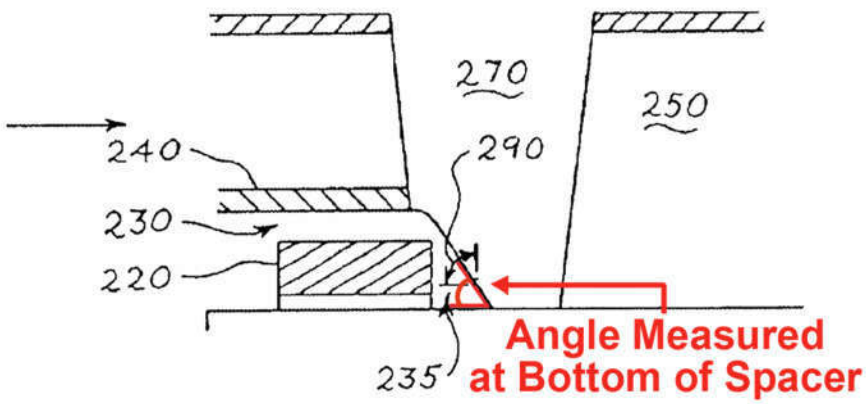
than 85 degrees but less than or equal to 90 degrees).[2] *Id*. Finally, the claims state that the required angle is one that is relative to the substrate surface, meaning that it is relative to a horizontal surface. *Id.*; *see also id.* at 7:45-48 (explaining that substrate surface is horizontal). Accordingly, the plain language of the claims confirms that the term should be construed as: "a side of the insulating spacer has an angle relative to the horizontal substrate surface that is greater than 85° and less than or equal to 90°."

77. Second, consistent with the claims, the specification confirms that the term requires "a side" of the spacer—*i.e.*, any side of the spacer, not a particular side or portion of a side—to have the required angle relative to the horizontal substrate surface. The specification explains that the substrate surface is horizontal. '552 at 7:45-48 ("The etch-stop is also almost completely anisotropic, meaning that the etchant etches in one direction-in this case, ***vertically (or perpendicular relative to the substrate surface) rather than horizontally***."); Figs. 2(B), 4(K) (showing the substrate surface as horizontal). The specification then explains that the required angle is between the horizontal substrate surface and any side of the sidewall spacer. '552 at Fig. 2(B) (showing angle of interest); *id.* at 5:13-17 ("FIG. 2(B) presents a polysilicon layer 220 encapsulated in a TEOS layer

[2] An acute angle is an angle that is less than 90 degrees.

230 with a spacer portion 235 adjacent to the contact opening 270, the spacer portion 235 having an angle 290 that is less than 85°."), Fig. 4(K) (showing angle of interest), 13:9-10 ("Of primary significance, the spacer portion 435 of the TEOS layer 420 retains its substantially rectangular profile.").

78. In Fig. 2(B) below, for instance, which shows the "prior art" sloped spacer, the angle (angle 290) is measured as between the bottom right side of the insulating spacer and the horizontal substrate surface:



'552 at 5:13-17 ("FIG. 2(B) presents a polysilicon layer 220 encapsulated in a TEOS layer 230 with a spacer portion 235 adjacent to the contact opening 270, the spacer portion 235 having an angle 290 that is less than 85°.").

79. In Fig. 4(K) below, which shows the purportedly improved spacer, the angle (near item 475) is measured at the top right side of the insulating spacer (shown in red below):

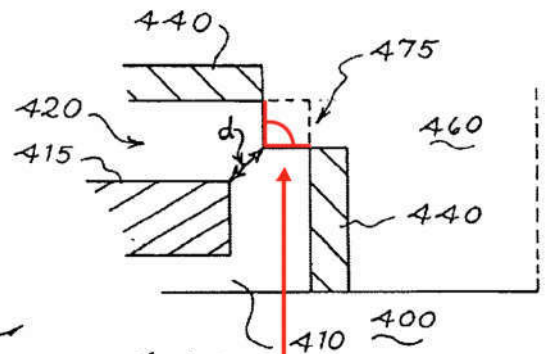


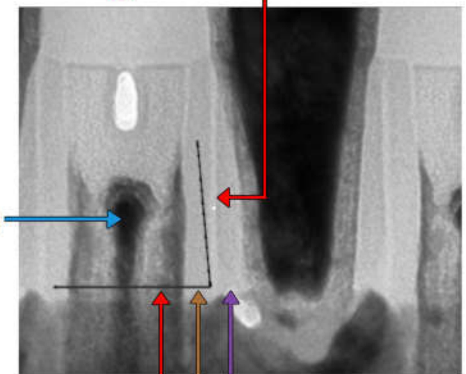
Fig. 4(k)

’552 at 13:9-10 (“Of primary significance, the spacer portion 435 of the TEOS layer 420 retains its substantially rectangular profile.”); *see also id.* at 8:41-43 (“The phrase ‘substantially rectangular’ means that ***a side*** ***of the spacer has an angle relative to the substrate surface*** of more than 85°.”). Thus, the angle can be measured as between any side of the insulating spacer and the substrate surface.

80. I have been told that the Patent Owner has taken the position that the angle of interest can be measured as between the bottom right side of the alleged insulating spacer—which has a stick of the alleged etch stop material adjacent to it[3]—relative to the horizontal substrate surface (as shown by the black line the Patent Owner drew in the image below):

---

[3] The specification makes clear that the claimed “side” may have a stick of etch stop material remaining adjacent to it. *See* ’552 at 12:58-65 (“The etchant removes material primarily from the base of the contact opening 460, and ***does not remove all of the etch stop material*** adjacent to the spacer portion 435 of the TEOS layer



81. Accordingly, the claim term should be construed such that the angle of interest should be measured between a side of the insulating spacer and the horizontal substrate surface. The term should therefore be construed to mean "a side of the insulating spacer has an angle relative to the horizontal substrate surface that is greater than 85° and less than or equal to 90°."[4]

---

420. Thus, the ***remaining etch stop material*** adjacent to the spacer portion 435 of the TEOS layer 420 serves as additional spacer material to ***insulate the polysilicon layer 415*** from a conductive contact that will subsequently be added to the contact opening.").

[4] I am informed and understand that in pending litigation between the Patent Owner and a Petitioner, the parties have proposed competing constructions for two additional limitations. I have reviewed these competing constructions and

VII. LEVEL OF ORDINARY SKILL IN THE ART

82. In my opinion, a person of ordinary skill in the art at the time of the alleged invention would have had at least a B.S. degree in electrical engineering or materials science (or equivalent experience), and would have at least two or three years of experience with semiconductor device fabrication and design. I met and/or exceeded these requirements for one of ordinary skill in the art at the time of the filing of the ’552 patent.

VIII. SPECIFIC GROUNDS FOR PETITION

83. The below sections demonstrate in detail how the prior art discloses each and every limitation of the claims of the ’552 patent, and how those claims are anticipated and/or rendered obvious by the prior art.

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determined that the prior art meets these limitations under either party’s construction, so I have not attempted to construe them for the purposes of this petition. (The prior art also discloses the required “angle” limitation under either party’s construction.) Furthermore, I am informed and understand that the parties agree that the term “contact region” should be construed to mean “contact opening or vias.” ’552 patent at 1:38-41 (“For purposes of the claimed invention, henceforth ‘contact opening’ or contact region’ will be used to refer to contact openings and/or vias.”).

A. Ground 1: Claims 1-2, 4-7 are Anticipated by Heath

1. Independent Claim 1

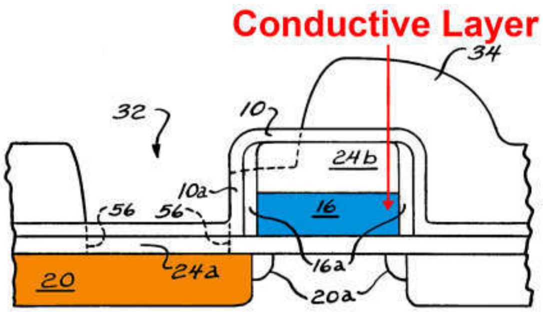
84. Fig. 8C of Heath shows a cross-section of a transistor structure that discloses each element of claim 1 of the ’552 patent. I will use Fig. 8C of Heath as a reference, identifying where each element is found in Heath along with additional supporting disclosure from the Heath specification.

a. “A structure, comprising”

85. Heath discloses a transistor structure containing all of the limitations of claim 1 of the ’552 patent, as will be described below with reference to Fig. 8C. Heath, Fig. 8C; *id*. at 10:33-35 (“Many methods may be used to produce a ***transistor structure*** which has source/drain implants like those shown in FIG. 8C.”), Figs. 2-7.

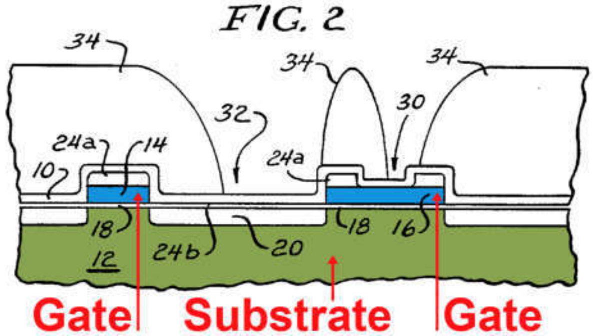
b. “(a) a conductive layer disposed over a substrate”

86. Heath discloses a **gate electrode 16**, which is a “conductive layer disposed over a substrate”:



Heath, Fig. 8C; *id*. at 9:44-47 ("FIGS. 8A, 8B and 8C relate to establishing a contact window to a source/drain region next to a ***gate electrode*** or field-shield electrode 16. . . ."), 9:50-52 ("FIGS. 8A and 8B show a gate electrode 16 and an active area 20 in the substrate to the left of gate electrode 16."), Figs. 2-7. The gate electrode is made of polysilicon, which persons of ordinary skill in the art would readily understand to be electrically conductive in a transistor structure. Heath at 8:8-11 ("[T]he next step is to mask contacts to polysilicon gate electrode 16. . . ."). Fig. 2 of Heath shows that the **gate electrodes 14 and 16** are formed over the **substrate 12** as part of the same process:

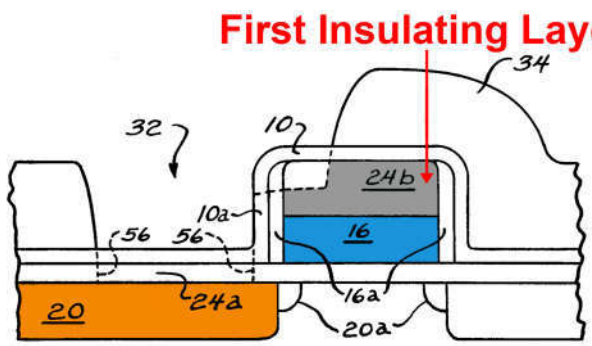
FIG. 2



Heath at 7:36-38 ("FIG. 2 illustrates a layer 10 operable as an etch stop and a ***substrate 12*** having poly ***gate electrodes 14 and 16*** over a relatively thin gate oxide 18.”).[5]

c. *“(b) a first insulating layer on the conductive layer”*

87. The transistor structure shown in Fig. 8C includes a “first insulating layer”—**oxide layer 24b**—“on the conductive layer”—**gate electrode 16**—as required by the claim:



Heath, Fig. 8C; *id*. at 9:52-55 (“Oxide layer 24 covers the active area 20 and the top of gate electrode 16. It is relatively thin over the source/drain 20 as shown at 24a, but is relatively thick on the top of gate electrode 16, as shown at 24b.”). Oxide is a common insulating material that would be readily known by persons of ordinary skill in the art to be an insulating layer in the transistor structure of Heath.

d. *“(c) a contact region in said first insulating layer”*

88. Heath discloses a contact region that has been created through the insulating oxide layer to the source/drain diffusion region. As shown in Fig. 8C,

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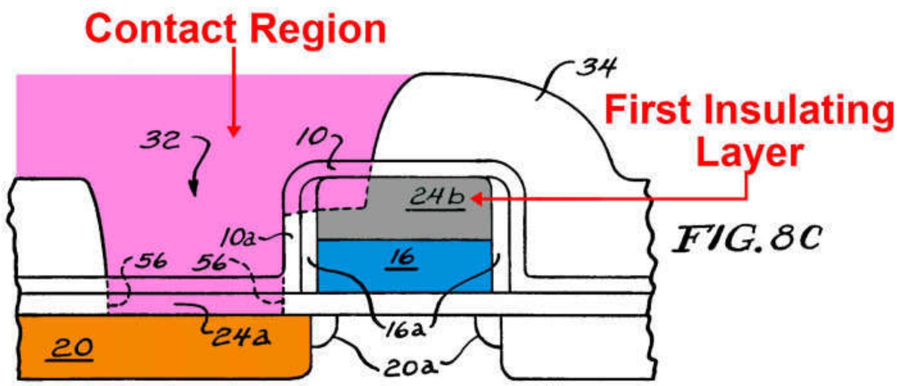
[5] Diffusion region 20 is a region of the substrate 12 that has been implanted with dopants to change its conductivity.

Heath discloses **contact window 32**—the claimed "contact region"—in the **oxide layer 24b** (the claimed "first insulating layer") that extends down to the **source/drain 20**:



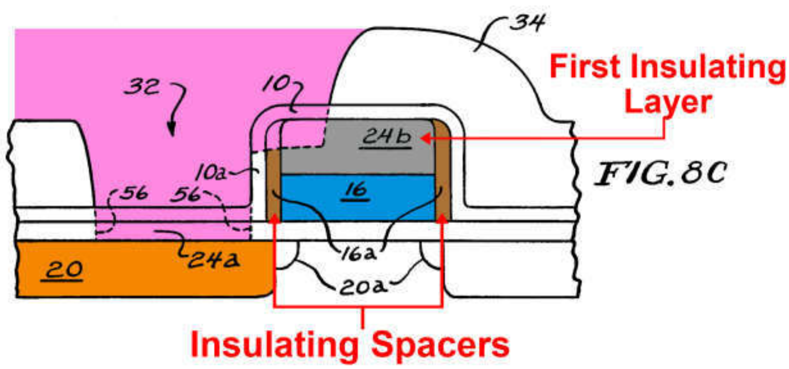
Heath, Fig. 8C; *id*. at 10:57-61 ("[A] ***contact window 32*** to source/drain 20"). The area in which material has been ***removed*** to create the contact region (including portions of etch stop layer 10, spacer 16a, and insulating layers 24a and 24b) has been colored in pink above.[6]

> ***e. "(d) at least one insulating spacer in the contact region adjacent to the first insulating layer"***

---

[6] The '552 patent similarly describes the process of forming a contact region "in" the insulating layer above the gate as etching an opening through the insulating layer. *See, e.g.*, '552 patent at 11:14-17 ("Referring to FIG. 4(B), a series of photolithographic etches are performed to remove the TEOS layer 420 material and the polysilicon layer 415 from the diffusion regions 405 to form contact openings."), Fig. 4(B).

89. Heath discloses a sidewall spacer in the contact region that is adjacent to the oxide insulating layer. As shown in Fig. 8C below, Heath discloses the claimed "insulating spacer"—**sidewall spacer 16a**—in the "contact region" (**contact window 32**) and adjacent to the "first insulating layer" (**oxide layer 24**):



Heath, Fig. 8C; *id*. at 10:12-27 ("The invented process can be used to protect a gate electrode when there is a ***sidewall spacer***. . . . This structure results from implantation techniques combined with the addition of a ***sidewall spacer 16a***. . . . In this case, spacer 16a is formed illustratively of ***oxide***. . . ."). Sidewall spacer 16a is an insulating oxide. Heath at 10:23-25.

f. "(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer"

90. As shown in Fig. 8C, Heath discloses a silicon nitride **etch stop layer 10** over the "first insulating layer" (**oxide layer 24**) and adjacent to the insulating spacers (**sidewall spacers 16a**):

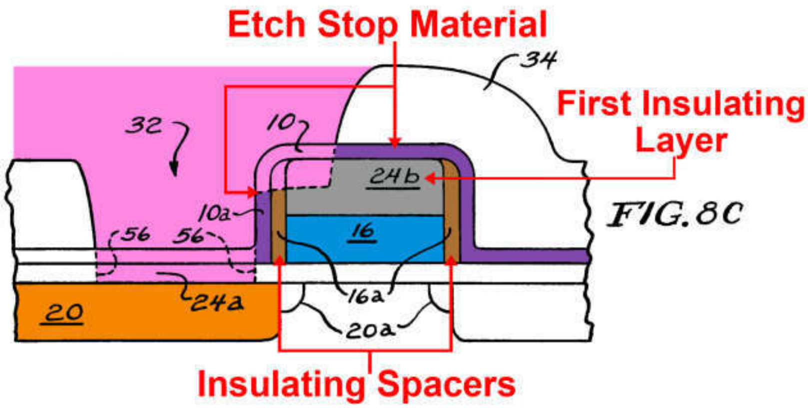


FIG. 8C

Heath, Fig. 8C. The **etch stop layer 10** is a "different material"—specifically, silicon nitride—from the **sidewall spacer**—an oxide. Heath at 5:38-39 ("The ***etch stop*** preferably is ***silicon nitride***."), Abstract, 9:2-4, 9:66-67, 10:12-27 ("***spacer 16a*** is formed illustratively of ***oxide***").

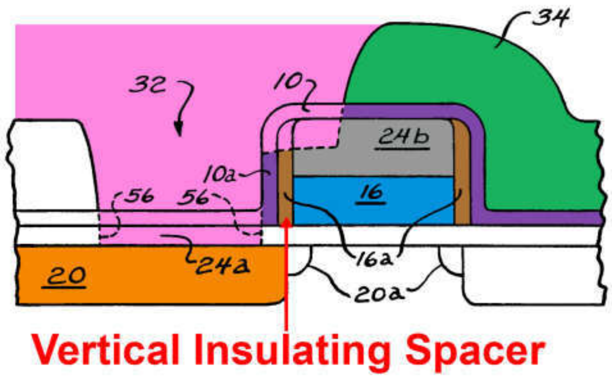
91. In both the '552 patent and Heath, a vertical "stick" of etch stop material remains adjacent to the sidewall spacer in the contact opening after the etching process forms the contact opening. *Compare* '552 at 12:58-65 ("The etchant removes material primarily from the base of the contact opening 460, and ***does not remove all of the etch stop material*** adjacent to the spacer portion 435 of the TEOS layer 420. Thus, the ***remaining etch stop material*** adjacent to the spacer portion 435 of the TEOS layer 420 serves as additional spacer material to ***insulate the polysilicon layer 415*** from a conductive contact that will subsequently be added to the contact opening.") *with* Heath at 10:1-11 ("Next, the etchant is changed … and the part of layer 10 between dashed lines 56 is removed, ***leaving the vertical 'stick' 10a of layer 10***. . . . Some oxide 24b will remain on the top of

gate electrode 16 even after the etch exposes the source/drain region 20 within the contact window, and because the nitride removal is anisotropic, ***the 'stick' 10a will remain on the side, so no short to electrode 16 can occur***.").

g. "[(f)] wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°"

92. As I explained above, the term "a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle of more than 85°" should be construed to mean "a side of the insulating spacer has an angle relative to the horizontal substrate surface that is greater than 85° and less than or equal to 90°." But Heath discloses this limitation under any plausible construction of this term.

93. Heath discloses a sidewall spacer 16a with a side that is at a right angle relative to the substrate surface. In fact, Heath specifically refers to the sidewall spacer as "***vertical***" (in other words, at a 90° angle) with respect to the substrate. Heath at Abstract ("An improved process for self-aligned contact window formation in an integrated circuit leaves a 'Stick' of etch stop on ***vertical sidewall surfaces*** to be protected."). This is shown in Fig. 8C:



Heath at Fig. 8C, Abstract; *see also id.* at 11:1-10.

94. Because the sidewall spacer 16a is described as "vertical," the entire side of the sidewall spacer is at a 90° angle relative to the horizontal substrate surface. Thus, the sidewall spacer of Heath meets this limitation regardless of where along the side of the sidewall spacer the angle is measured relative to the substrate surface, as shown in the two examples below[7]:

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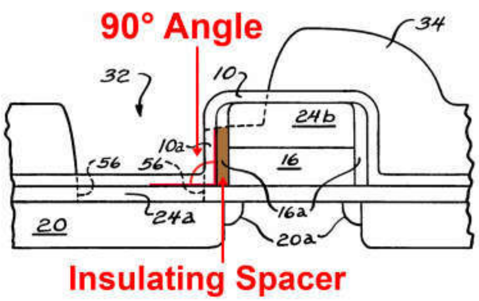
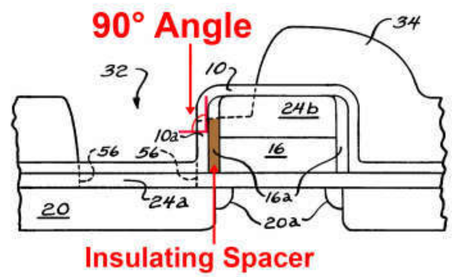
[7] Claim 1 requires "at least one insulating spacer in the contact region. . . ." Claim 1 further requires that "a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°." The specification makes clear that the claimed "side" of the spacer may have a stick of etch stop material remaining adjacent to it. *See* '552 at 12:58-65 ("The etchant removes material primarily from the base of the contact opening 460, and ***does not remove all of the etch stop material*** adjacent to the spacer portion 435 of the TEOS layer 420. Thus, the ***remaining etch stop material*** adjacent to the

Angle measured near bottom of spacer:	**Angle measured near top of spacer:**
 FIG.8C	 FIG.8C

2. <u>Claim 2: "The semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon nitride"</u>

95. Claim 2 requires that the "etch stop material" of claim 1 be comprised of a specific material—silicon nitride. Heath discloses using a silicon nitride etch stop material. Heath at 5:38-39 ("The etch stop preferably is ***silicon nitride***."); *see also id.* at Abstract; 9:66-67. Silicon nitride is a common material in integrated circuits and is often used as an etch stop layer and, indeed, the '552 patent teaches that silicon nitride etch stop layers were well-known in the prior art. '552 at 4:42-

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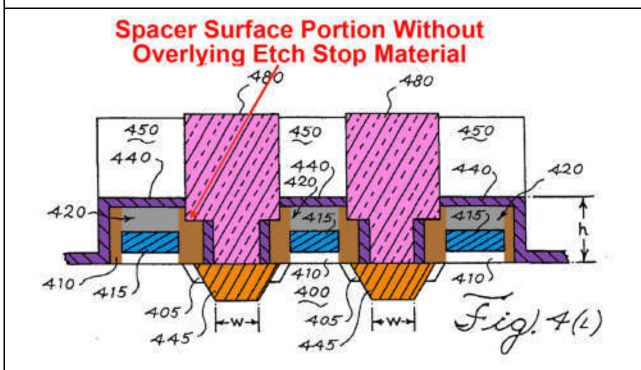
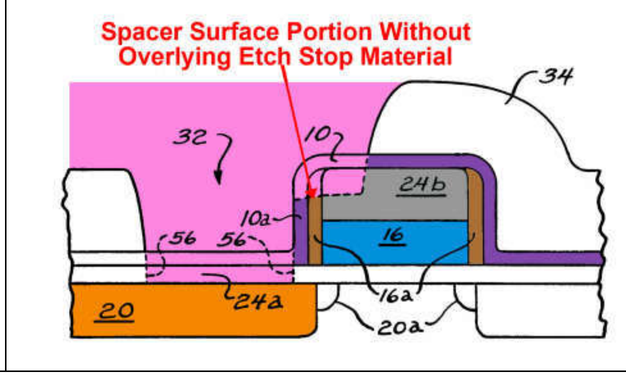
spacer portion 435 of the TEOS layer 420 serves as additional spacer material to ***insulate the polysilicon layer 415*** from a conductive contact that will subsequently be added to the contact opening."). *Compare with* Heath at 10:1-11 ("Next, the etchant is changed … and the part of layer 10 between dashed lines 56 is removed, leaving the vertical 'stick' 10a of layer 10. . . . [B]ecause the nitride removal is anisotropic, the 'stick' 10a will remain on the side. . . .").

44 ("A separate insulating or etch stop layer, for example a silicon nitride layer 240, overlies the TEOS layer 230 and the contact region 270."); *id*. at Fig. 2.

3. <u>Claim 4: "The structure of claim 1, wherein the insulating spacer has a surface portion in the contact region without overlaying etch stop material"</u>

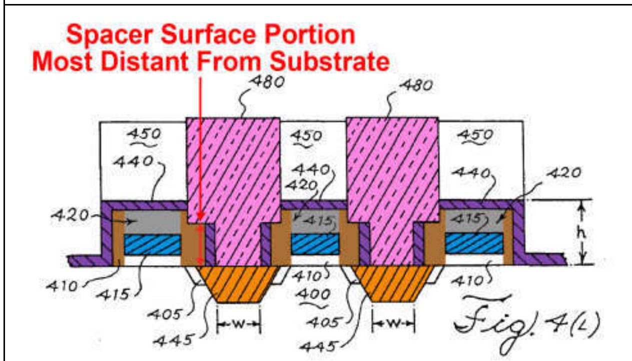
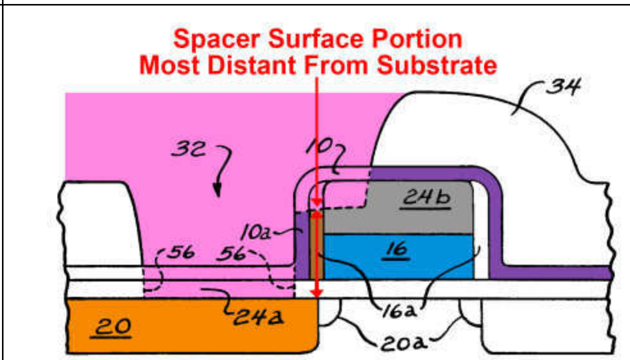
96. Claim 4 requires that the "insulating spacer"—*i.e.*, **sidewall spacer 16a** in Heath—have a surface portion in the contact region that is not covered by etch stop material, as shown in Fig. 4(L) of the '552 patent below. As shown in Fig. 8C, Heath discloses that the "insulating spacer"—**sidewall spacer 16a**—has a surface portion (indicated by the red arrow) in the contact region— **contact window 32**—without overlaying etch stop material—**etch stop layer 10**:

<table>
<tr><th>'552 patent, Fig. 4(L)</th><th>Heath, Fig. 8C</th></tr>
<tr><td>
</td><td>
</td></tr>
</table>

The portion of the **sidewall spacer 16a** indicated by the red arrow does not have etch stop material overlaying it because that portion of the **etch stop layer 10** has been removed via the etching process in order to create the **contact window 32**. *See* Heath at 10:1-3 ("Next, the etchant is changed as described supra, and the part of layer 10 between dashed lines 56 is ***removed***, leaving the vertical 'stick' 10a of layer 10.”).

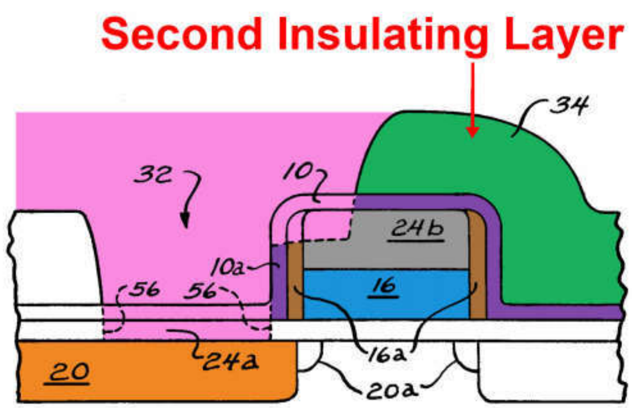
4. Claim 5: “The structure of claim 4, wherein the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate”

97. Claim 5 requires that the portion of the “insulating spacer”—*i.e.*, **sidewall spacer 16a** in Heath—identified above in connection with claim 4 (without overlaying etch stop material) be the portion of the “insulating spacer” that is farthest away from the substrate surface, as shown in Fig. 4(L) of the ’552 patent below (red arrow showing distance between substrate surface and portion of insulating spacer without overlying etch stop material). As shown by the red arrow in Fig. 8C below, the portion of the **sidewall spacer 16a** in **contact window 32** without overlaying **etch stop layer 10** (identified above in connection with claim 4) is the portion of that **sidewall spacer 16a** that is farthest away (*i.e.*, “most distant”) from the substrate surface:

<table>
<tr><th>’552, Fig. 4(L)</th><th>Heath, Fig. 8C</th></tr>
<tr><td>
</td><td>
</td></tr>
</table>

5. Claim 6: “The structure of claim 1, further comprising a second insulating layer on the etch stop layer and over the conductive layer”

98. Claim 6 requires an additional insulating layer to be placed over the etch stop layer and conductive layer. As shown in Fig. 8C, Heath discloses a second insulating layer—**dielectric layer 34**—on the **etch stop layer 10** and over the conductive layer (**gate electrode 16**). **Dielectric layer 34** is made of borophosphosilicate glass ("BPSG"), an insulator, and is deposited on the **etch stop layer 10** and over conductive **gate electrode 16**, as required by the claims:



Heath, Fig. 8C; *id*. at 7:48-50 ("A very thick BPSG (borophosphosilicate glass) ***dielectric 34*** covers the layer 10 except in contact windows 30 and 32.").

6. <u>Claim 7: "The structure of claim 6, further comprising a second conductive material in the contact region"</u>

99. While claims 1and 6 require "a conductive layer disposed over a substrate"— **gate electrode 16**—claim 7 further requires a "second conductive material in the contact region." This second conductive material in the contact region refers to the electrically conductive material that is placed into the contact region, thus forming the contact. '552 patent at 13:43-45 ("FIG. 4(L) presents a

cross-sectional planar side view of the structure of the invention wherein ***conductive contacts 480*** have been deposited in the contact openings 460."). Heath discloses that contact window 32 can be filled with metal to form a contact. Heath at 11:50-51 ("add metal or other conductive material for interconnects."); *id.* at 12:8-9, 12:42-43.

B. Ground 2: Claim 3 Would Have Been Obvious Over Heath in View of Hawley and Chappell

1. Claim 3: "The semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon dioxide"

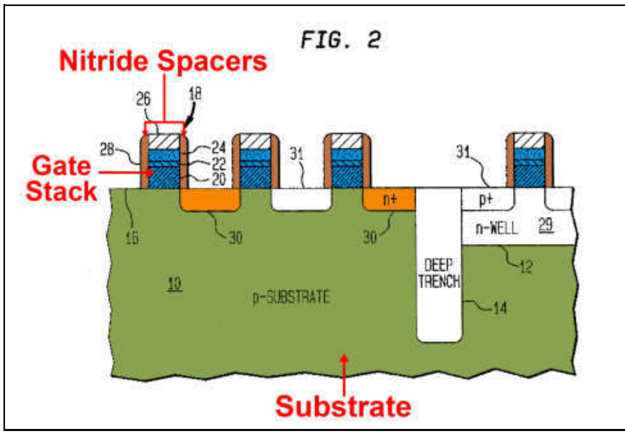
100. Claim 3 depends from claim 1, therefore the analysis with respect to claim 1 as set forth in Ground 1 is incorporated by reference as if recited herein. Claim 3 requires that the etch stop material of claim 1 comprises silicon dioxide.

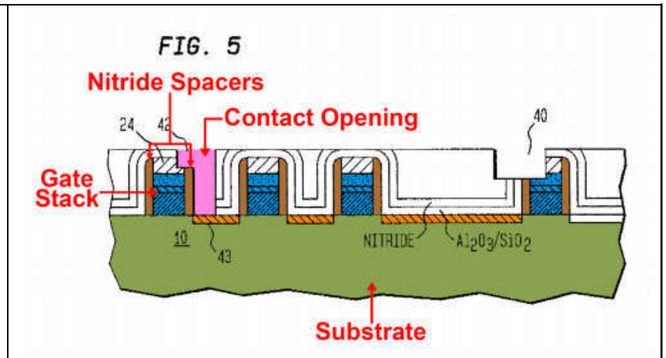
101. Heath expressly teaches that materials other than silicon nitride can be used as etch stop materials. Heath at 6:18-20 (while "[s]ilicon nitride is preferred … ***one could use another material***" as the etch stop material); *id.* at 6:21-25 ("Other substances may be useful for the process, as long as they can be used as an etch stop for the interlevel dielectric, are insulators, and can be removed in subsequent processing steps."). Moreover, during prosecution of the '552 patent, after the applicants had amended the claims to require the etch stop material to be a "different material" from the insulating spacer, the Examiner recognized that "***it would have been obvious to one of ordinary skill in the art*** at the time

when the invention was made" to use different materials for the etch stop and insulating spacer. Office Action, Sept. 11, 2002 (Ex. 1019) at 3.

102. European Patent Publ. No. 0592078 ("Hawley") (Ex. 1004), which, like Heath and the '552 patent is directed to the use of etch stop layers in the fabrication of layered structures in semiconductors, specifically teaches using ***silicon dioxide*** as an etch stop layer. Hawley at 2:43-44 ("***The second etch-stop dielectric layer***, if used, ***may comprise a thin layer of silicon dioxide***."). Thus, one of ordinary skill in the art would have known that he/she could replace the silicon nitride etch stop layer in Heath with silicon dioxide as taught by Hawley.

Because claim 3 depends from claim 1—which requires the etch stop material to be "different material" than the insulating spacer—the insulating spacer must also be a different material than silicon dioxide to meet this claim. While Heath discloses using an oxide spacer, using different materials for the sidewall spacer (*e.g.*, a nitride) was also well-known in the art at the time of the alleged invention of the '552 patent. U.S. Patent No. 5,541,427 ("Chappell") (Ex. 1005), which, like Heath and the '552 patent is directed to the fabrication of contact openings to diffusion regions, expressly discloses **nitride spacers** (brown) formed next to a **gate stack** (blue) and **contact opening** (pink) over a **substrate** (green):





Chappell at Figs. 2, 5; *id.* at 4:7-8 ("***Nitride spacers 28 are formed along the gate edges***."); *see also* U.S. Patent No. 5,374,836 ("Vinal") (Ex. 1009) at 3:5-8 ("For example, in typical field effect transistor devices, where the gate insulator is silicon dioxide, ***the gate sidewall spacer is preferably silicon nitride***."); U.S. Patent No. 5,053,351 ("Fazan") (Ex. 1012) at 3:50-54 ("dielectric ***spacers 26 (also either oxide or nitride)***"). Thus, a combination of Heath, Hawley, and Chappell discloses all elements of claim 3.

103. A person of ordinary skill in the art would have been motivated to combine Heath, Hawley, and Chappell to obtain the structure described in claim 3.

104. ***First***, all three references relate to the same techniques (the formation of contact openings in transistor structures) in the same field (transistor fabrication and design). Heath at Abstract ("An improved process for self-aligned ***contact window formation*** in an integrated circuit. . . ."); Hawley at Abstract ("A process for forming a via. . . ."), 4:16-18 ("An antifuse via 18 is etched through interlayer dielectric layer 18 to expose the upper surface of barrier layer 14."); Chappell at

2:16-18 ("The invention is further directed to a ***process for separately forming contacts*** to diffusion regions and gate stacks on a semiconductor substrate.").

105. ***Second,*** the choice of materials for spacers and etch stop layers was a simple design choice for one of ordinary skill in the art. Indeed, the '552 patent itself recognizes that it would "be ***appreciated by those of ordinary skill in the art*** that this silicon nitride layer 440 [*i.e.*, the claimed etch stop material] could instead be an insulating layer of, for example, ***silicon dioxide,*** SiO_2, ONO, or $SiO_xN_y(H_z)$." '552 at 11:66-12:2.

106. ***Third,*** as the Examiner recognized during prosecution of the '552 patent, a person of ordinary skill in the art would have been motivated to use different materials for the etch stop layer and insulating spacers because it would "minimiz[e] current leakage and short circuits." Office Action, Sept. 11, 2002 (Ex. 1019) at 3.

107. Accordingly, it would have been obvious to a person of ordinary skill in the art to use a variety of material combinations for forming the sidewall spacer and etch stop layer of the transistor structure taught by Heath.

C. Ground 3: Claims 1-2, 4-7 Would Have Been Obvious Over Heath in View of Dennison

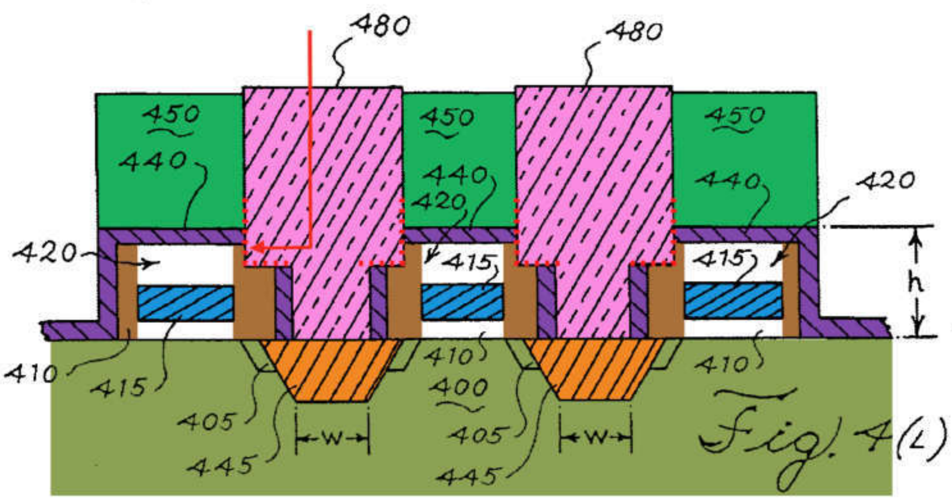
108. As set forth above in connection with Grounds 1 and 2, Heath anticipates claims 1-2 and 4-7, and renders obvious claim 3. Heath, in

combination with Dennison, also renders each of the claims obvious under two alternative scenarios as set forth below.

1. Heath, in combination with Dennison, renders the claims obvious under an overly narrow construction of the "angle" limitation—*e.g.*, limiting it to a ***particular*** portion of the "side" of the insulating spacer—recited in claim 1 (element 1(f))

109. Claim element 1(f) provides as follows: "[(f)] wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°". For the reasons I stated above in the Claim Construction section, the proper construction of the term "a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°" is "a side of the insulating spacer has an angle relative to the horizontal substrate surface that is greater than 85° and less than or equal to 90°".

110. I am informed and understand that the Patent Owner may argue that claim 1 should be construed such that the claimed "angle" with respect to the substrate surface (recited in element 1(f)) can be measured only: (i) from the upper portion of the sidewall spacer; and/or (ii) from a side of the spacer created as a result of a partial etch into the sidewall spacer. This particular "side" of the spacer is shown by the arrow and dotted red lines representing a 90° angle in the figure below:

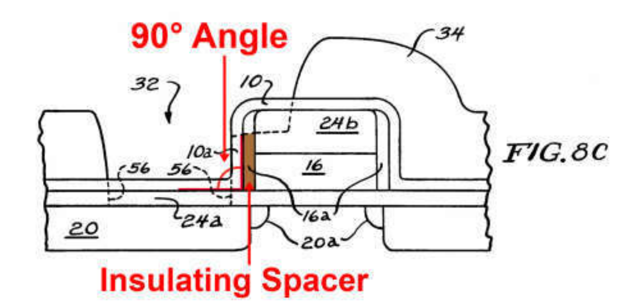
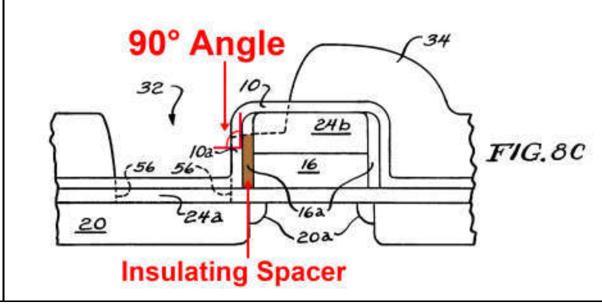


111. As I explained in the Claim Construction section, a construction limiting the "side" from where the claimed "angle" is measured solely to the particular portion of the side indicated by the red arrow above would be inconsistent with the claim language (which does not specify any particular portion of a "side"), the specification (which shows an example of the angle being measured from the lower portion of one side of the spacer), and the Patent Owner's own statements in the co-pending litigation (where the Patent Owner measures the angle at a side in the lower portion of the sidewall spacer that has not been etched). Section VI *above*. But even if such a narrow construction were adopted, the claims would still be obvious in view of Heath in combination with Dennison.[8]

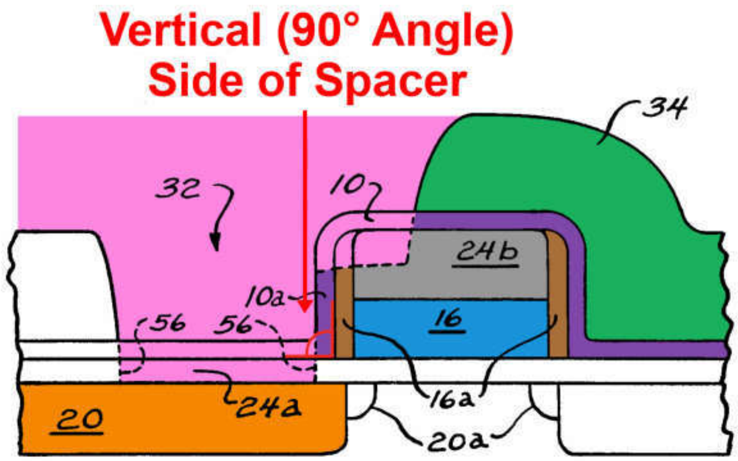
[8] The only element affected by such a narrow construction of the claimed "angle" is element 1(f). The analysis for claim 1 and its dependent claims is otherwise the same as set forth in Ground 1. That analysis is incorporated herein by reference.

a. *Heath discloses a vertical sidewall spacer whether it is measured at the bottom or the top portions of the spacer.*

112. Heath discloses a vertical sidewall spacer whether it is measured at the bottom or the top portions of the spacer as shown in red below (and thus discloses the required "angle" even if limited to alternative construction (i) above):

Angle measured near bottom of spacer:	**Angle measured near top of spacer:**
	

113. As explained above in Ground 1, Heath discloses several sides of sidewall spacer 16a that are at a right angle to the substrate surface. *See, e.g.*, Heath at Fig. 8C. Specifically, as shown in Fig. 8C and described in the specification, Heath teaches a transistor structure with a "vertical" **sidewall spacer 16a** in the **contact window 32** that forms a 90° angle (shown in red) relative to the horizontal substrate surface:



Heath at Fig. 8C, Abstract ("An improved process for self-aligned contact window formation in an integrated circuit leaves a "Stick" of etch stop on ***vertical sidewall*** surfaces to be protected.").

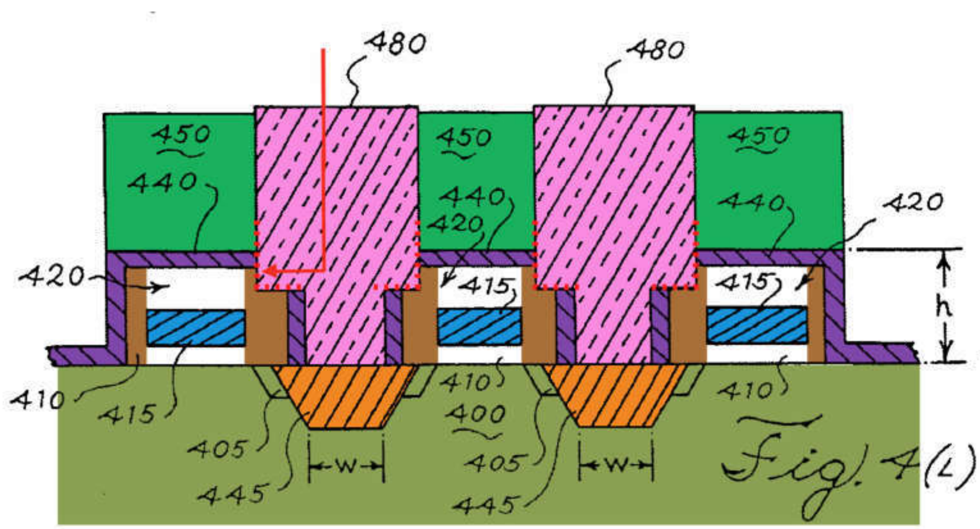
114. Because the sidewall spacer 16a is described as "vertical," the entire side of the sidewall spacer is at a 90° angle relative to the horizontal substrate surface. As a result, the sidewall spacer meets these limitations regardless of where along the side of the sidewall spacer the angle is measured relative to the substrate surface (*i.e.*, it is vertical at the bottom and top portions) as shown above.

b. It would have been obvious to perform slightly less etching in Heath such that a vertical side remains in a partially etched portion at the top of the spacer, thus meeting the "angle" limitation of claim 1 under the overly narrow construction described above

115. I am informed and understand that the Patent Owner may also argue that the angle may only be measured from a side of the spacer created as a result of a partial etch into the sidewall spacer. As discussed above, that would be incorrect.

But even if such a construction were adopted, Heath in combination with Dennison discloses such an angle.

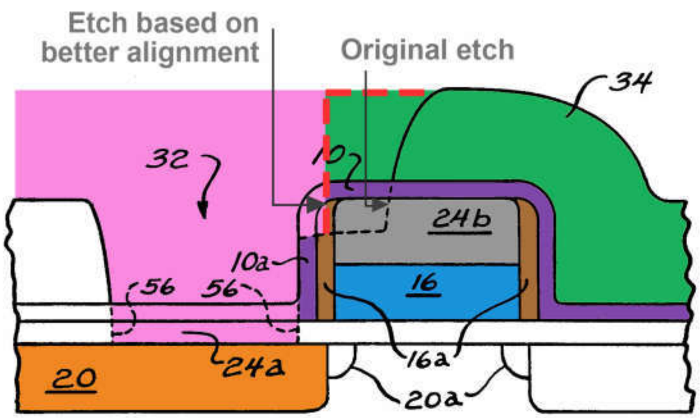
116. Fig. 4(L) of the ’552 patent shows a side of the insulating spacer that is vertical with respect to the substrate surface at a portion of the spacer that has been partially etched into, as shown by the red arrow below:



It is noted that the width of the sidewall spacers changed greatly between Fig. 4(I) and Figs. 4(J)-(L).

117. It would have been obvious to perform slightly less etching in Heath such that a vertical side remains in a partially etched portion at the top of the spacer (as required if the “angle” is limited per the alternative constructions (i) and (ii) above). Specifically, as shown in the figure below, it would have been obvious to a person of ordinary skill in the art to align the etching used to create the contact opening (in pink) in Fig. 8C more closely with the diffusion region (in orange) at

the bottom of the contact opening (and thus further to the left as shown by the red dotted line), such that a vertical side remains in a partially etched portion at the top of sidewall spacer 16a:



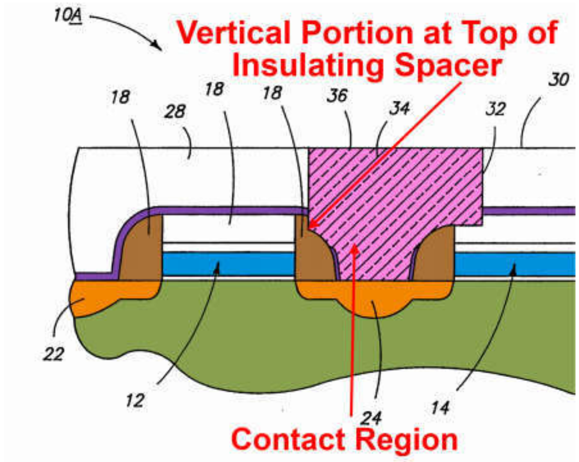
The process/results described in Heath are consistent with the process/results described in the '552 patent.

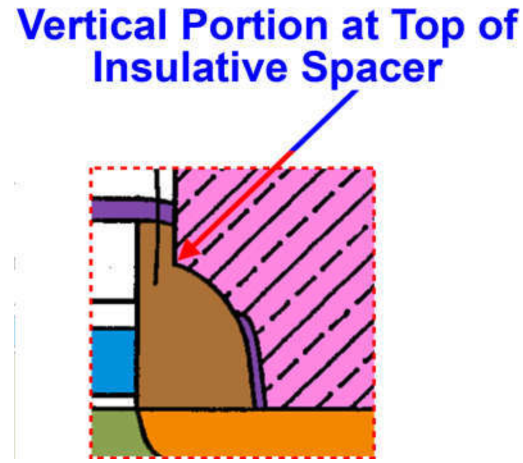
118. As shown in the figure, such an etch (shown by the red dotted line) would remove only part of the top portion of the spacer thus leaving a vertical upper portion of the spacer that has been only partially etched away. It would have been obvious to a person of ordinary skill in the art to perform such an etch for several reasons.

119. First, as I explained in the background of the invention section of the '552 patent itself, it was known that the etching performed can be precisely controlled using well-understood techniques, and it would have been obvious to adjust the parameters of the etching recipe, such as pressure and feed gas, to achieve the etch shown in the figure above. '552 at 2:37-39 ("[B]y adjusting the

feed gases, the taper of the sidewall in the etched opening of the dielectric can be varied."); *see also id.* at 2:36-43 ("If a low sidewall angle is desired, the chemistry is adjusted to try to cause some polymer buildup on the sidewall. Conversely, if a steep sidewall angle is desired, the chemistry is adjusted to try to prevent polymer buildup on the sidewall."), 2:54-56 ("Etchants that provide a near 90° sidewall angle are generally not highly selective while highly selective etches typically produce a sloped sidewall."). Therefore, as the '552 patent itself concedes in the background section, a person of ordinary skill in the art would have known how to use a non-highly selective etch to achieve a vertical upper portion of the spacer that has been only partially etched away (as shown in the figure).

120. Second, the prior art specifically discloses performing etching in such a way that a vertical side remains in a partially etched portion at the top of the spacer. Dennison, which is also directed to the formation of contact openings in a transistor structure, provides one example. As shown by the arrow below, Dennison discloses etching only ***partially*** through the sidewall (brown), leaving a vertical side of the partially etched sidewall relative to the substrate surface:



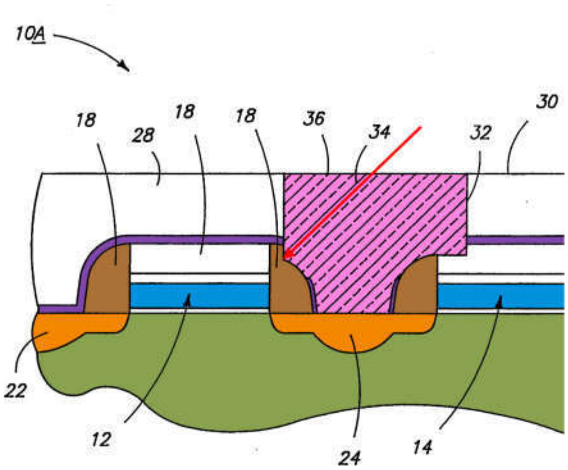


(zoomed in)

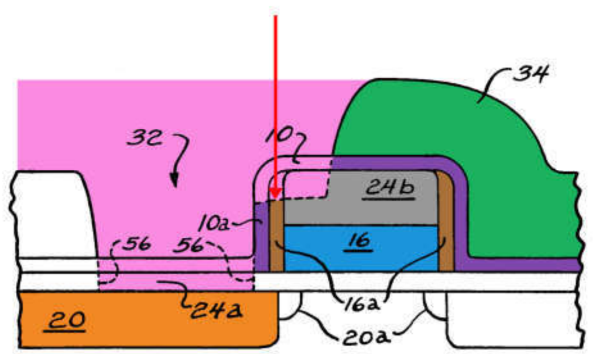
Dennison, Fig. 2A; *see also id*., Figs. 2A-11B.

121. The only difference between the amount that the sidewall spacer is etched in Heath—which etches all the way through the sidewall spacer (as shown by the red arrow in the figure below)—and Dennison—which etches only partially through the sidewall spacer (as shown by the red arrow below)—is the degree to which the etching proceeds laterally (to the left in Dennison and to the right in Heath):

Dennison, Fig. 2A

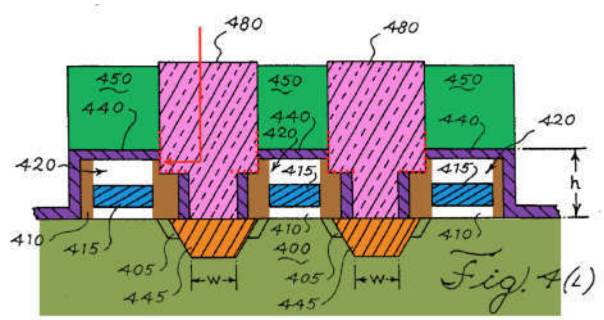
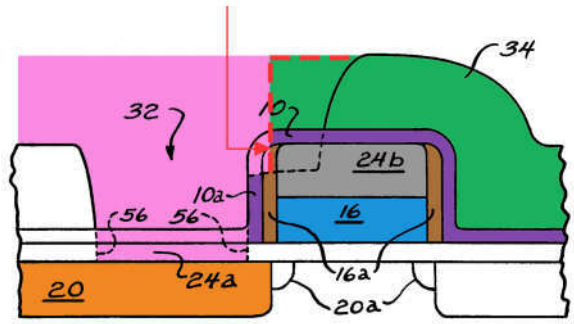


Heath, Fig. 8C



122. As shown in the figures above, the etch to create the contact openings (pink) proceeds further to the right in Heath than it does to the left in Dennison. The result is that the entire top of the spacer is etched away in Heath while some of the top of the spacer remains in Dennison. This difference in etching is a result of a difference in alignment of the contact openings with the diffusion regions (orange) below. Specifically, in Dennison, the left side of the contact opening (pink) is nearly aligned with the underlying diffusion region 24 (orange); in Heath, the upper right portion of the contact opening (pink) is significantly misaligned with the underlying diffusion region 20 (orange). Because of this misalignment in Heath, the etching proceeds farther to the right and the entire top of the spacer is etched away. But this is a matter of nanometers—even a better alignment of ***only a few nanometers*** in the opposite direction would result in less lateral etching in Heath such that the sidewall spacer is only partially etched (as in the left side of the contact opening shown in pink in Dennison).

123. Moreover, the specific etchants used to form the contact opening disclosed in Heath would, if used in the manner discussed above, result in the partially etched portion of the sidewall spacer 16a having a vertical side as shown in Fig. 8C of Heath, similar to Fig. 4(L) of the ’552 patent:

'552 patent, Fig. 4(L)	**Heath, Fig. 8C**
	

124. Furthermore, Heath discloses etching using CHF_3 and O_2. Heath at 9:10-12 ("The second dry etch can occur in, for example, an Applied Materials model 8110 etcher using O_2 and CHF_3."). It was well-known to persons of ordinary skill in the art that CHF_3 and O_2 etch the materials used in Heath's etch stop and spacer layers —Si_3N_4 (silicon nitride) and SiO_2 (silicon dioxide)—at nearly identical rates.[9] This means that the etchant used to etch the sidewall in

[9] *See also* J. Dulak et al., *Etch mechanism in the reactive ion etching of silicon nitride*, Journal of Vacuum Science & Technology A 9, 775 (1991) ("Dulak") (Ex. 1010)—prior art under at least 35 U.S.C. § 102(b)—which discloses that an etching device made by the same manufacturer as the device used by Heath (Applied Materials model 8130), using the ***same*** etchants (CHF_3 - 10% O_2) to etch the ***same*** materials (Si_3N_4 (silicon nitride) and SiO_2 (silicon dioxide)) as in Heath would lead to a 90° sidewall angle between sidewall spacer 16a and the surface of the substrate 20, as both would be etched at nearly the same rate because the

Heath will result in a substantially vertical side of the spacer—*i.e.*, the etchant used in Heath to etch only partially through the sidewall spacer (as shown above) would retain a substantially vertical sidewall (*i.e.*, near 90° sidewall angle as between sidewall spacer 16a and the surface of the substrate 20). As discussed above, Heath specifically discloses etching that results in vertical structures. Heath at Abstract ("An improved process for self-aligned contact window formation in an integrated circuit leaves a "Stick" of etch stop on ***vertical sidewall surfaces*** to be protected."); *id.* at 10:1-3.

125. Finally, a person of ordinary skill in the art would have been motivated to combine the teachings of Dennison with the structure disclosed by Heath in order to create a sidewall spacer with a vertical side formed in a partially etched portion at the top of the spacer. Dennison and Heath are directed to the formation of the same types of structures (*e.g.*, contact openings and sidewalls) in the same way (*e.g.*, using particular etchants) in the same field (the field of transistor fabrication). Sections V(B)-(C) *above*. As Heath recognizes, better alignment is a common goal in the formation of contact openings. Heath at 3:8-12

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etchant is not highly selective. Dulak at 776-77; *see also* '552 at 2:54-56 ("Etchants that provide a near 90° sidewall angle are generally not highly selective while highly selective etches typically produce a sloped sidewall.").

("One commonly desires to align the contact window to some known edge, typically one edge of a gate electrode or an isolation edge. . . ."). Better alignment, for instance, helps protect against the contact region accidentally encroaching on the gate electrode and creating a short circuit, which is precisely what Heath is directed to. Heath at 10:7-11; *id*. at 11:11-15. Dennison discloses that better alignment can leave a vertical side of a partially etched sidewall relative to the substrate surface. *See* Dennison at Fig. 2A. Even better alignment in Heath of only a few nanometers in the opposite direction (*i.e.* to the left in Fig. 8C above) would result in Heath's contact opening being etched only partially through the sidewall spacer thus leaving a vertical side of the partially etched sidewall relative to the substrate surface. A person of ordinary skill in the art would therefore have been motivated to apply the teachings of Dennison to Heath and perform etching in such a way that a vertical side remains in a partially etched portion at the top of the spacer (as required if the "angle" is incorrectly limited per the alternative constructions (i) and (ii) above).

* * *

126. Accordingly, even if the claims were incorrectly construed such that the "angle" with respect to the substrate surface (recited in element 1(f)) can be measured only: (i) from the upper portion of the sidewall spacer; and/or (ii) from a

side of the spacer created as a result of a partial etch into the sidewall spacer, the claims would still be obvious in view of Heath in combination with Dennison.

D. Ground 4: Claim 3 Would Have Been Obvious Over Heath in View of Dennison, Hawley and Chappell

127. Claim 3 depends from claim 1. Claim 3 is therefore obvious for the same reasons stated with respect to Ground 2—which describes the combination of Heath with Hawley and Chappell—and Ground 3—which describes the combination of Heath with Dennison under the alternative claim interpretations.

IX. AVAILABILITY FOR CROSS-EXAMINATION

128. In signing this declaration, I recognize that the declaration will be filed as evidence in a case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will appear for cross examination within the United States during the time allotted for cross examination.

X. RIGHT TO SUPPLEMENT

129. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to take into account new information as it becomes available to me.

Jurat

130. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Dated: June 11, 2016

Richard Blanchard

Dr. Richard Blanchard

APPENDIX A

Richard A. Blanchard, Ph.D.

Professional Profile

Dr. Blanchard has over 40 years of combined industry, research, academic, and consulting experience. His research covers semiconductor device and electronics design, semiconductor device physics, semiconductor manufacturing processes and equipment, failure analysis, and reverse engineering of semiconductor devices and electronic circuits. Dr. Blanchard is a named inventor on more than 200 issued U.S. patents. As a result, he has been involved in numerous patent and trade secret litigation matters including a number of ITC proceedings. He has also authored or co-authored books and articles dealing with semiconductor design, process development, and failure analysis.

Dr. Blanchard has worked at Blanchard Associates, Los Altos, Silicon Valley Expert Witness Group, Mountain View, Exponent Failure Analysis Associates, Inc., Menlo Park, CA, IXYS Corporation, San Jose, Siliconix, Inc. Santa Clara, Supertex, Inc. Sunnyvale, Cognition, Inc. Mountain View, Foothill College, Los Altos Hills, and at Fairchild Semiconductor, Mountain View, CA.

Credentials and Professional Affiliations

1982	Stanford University	Ph.D., Electrical Engineering
1970	M.I.T.	MSEE
1968	M.I.T.	BSEE

- Senior Member, Institute of Electrical and Electronics Engineers
- Member, Electronic Device Failure Analysis Society
- Member, International Microelectronics & Packaging Society
- Member, American Vacuum Society
- Member, National Fire Protection Association
- Court Appointed Special Master

Patents

Patent Number	Date Issued	Title
9,362,348	6/7/2016	Method of manufacturing a light emitting, power generating, Or other electronic apparatus
9,356,595	5/31/2016	Bidirectional two-base bipolar junction transistor devices, operation, circuits, and systems with collector-side base driven, diode-mode turn-on, double base short at initial turn-off, and two base junctions clamped by default
9,355,853	5/31/2016	Systems and methods for bidirectional device fabrication
9,349,928	5/24/2016	Method of manufacturing a printable composition of a liquid or gel suspension of diodes
9,343,593	5/17/2016	Printable composition of a liquid or gel suspension of diodes
9,337,262	5/10/2016	Structures and methods with reduced sensitivity to surface charge
9,316,362	4/19/2016	LED lighting apparatus formed by a printable composition of a liquid or gel suspension of diodes and methods of using same
9,306,048	4/05/2016	Dual depth trench-gated MOS controlled thyristor with well-defined turn-on characteristics
9,263,573	2/16/2016	Power semiconductor devices, structures and related methods
9,236,528	1/12/2016	Light emitting, photovoltaic or other electronic apparatus and system
9,236,527	1/5/2016	Light emitting, photovoltaic or other electronic apparatus and system
9,231,582	12/8/2015	Bidirectional two-phase bipolar junction transistor devices, operation, circuits and systems with diode-mode-turn-on and collector-side base driven
9,209,798	12/8/2015	Bidirectional two-phase bipolar junction transistor operation, circuit and systems with two base junctions clamped by default
9,209,713	12/1/2015	Bidirectional two-phase bipolar junction transistor operation, circuit and systems with two base junctions clamped by default
9,203,401	12/1/2015	Bidirectional two-phase bipolar junction transistor operation, circuit and systems with base short at initial turn-off
9,203,400	12/1/2015	Bidirectional two-phase bipolar junction transistor operation, circuit and systems with diode-mode turn-on
9,200,758	11/17/2015	LED lighting apparatus formed by a printable composition of a liquid of gel suspension of diodes and methods of using same
9,190,894	11/3/2015	Bidirectional two-phase bipolar junction by a printable composition of a liquid or gel suspension of diodes and method of using same
9,130,124	9/08/2015	Diode for a Printable Composition
9,123,705	9/01/2015	Conductive Ink for Filling Vias
9,105,812	8/11/2015	Diode for a Printable Composition
9,099,568	8/04/2015	Three-Terminal Printed Devices. Interconnected as Circuits
9,082,648	7/14/2015	Vertical Insulated-gate turn-off device having a planar gate
9,076,861	7/07/2015	Schottky and MOSFET and Schottky structures, devices and methods
9,059,710	6/16/2015	Systems, circuits, devices, and methods with bidirectional bipolar

9,054,707	6/09/2015	transistors
9,054,706	6/09/2015	Systems, circuits, devices, and methods with bidirectional bipolar transistors
9,048,118	6/02/2015	Systems, circuits, devices, and methods with bidirectional bipolar transistors
9,035,350	5/19/2015	Lateral transistors with low-voltage drop shunt to body diode
9,029,909	5/12/2015	Systems, circuits, devices, and methods with bidirectional bipolar transistors
		Systems, circuits, devices, and methods with bidirectional bipolar transistors
9,024,379	5/5/2015	Trench transistors and methods with low-voltage-drop shunt to body diode
9,018,833	4/28/2015	Apparatus with Light Emitting or Absorbing Diodes
8,940,627	1/27/2015	Conductive Iink for Filling Vias
8,937,502	1/20/2015	Lateral Insulated Gate Turn-off Devices
8,890,238	11/18/2014	Power Semiconductor Devices, structures and related methods
8,878,238	11/4/2014	MCT device with base-width-determined latching and non-latching states
8,878,237	11/4/2014	Active edge structures providing uniform current flow in insulated gate turn-off thyristors
8,877,101	11/4/2014	Method of manufacturing a light emitting, power generating or other electronic apparatus
8,852,467	10/7/2014	Method of Manufacturing a printable composition of a liquid or gel suspension of diodes
8,847,307	9/30/2014	Power semiconductor devices, methods, and structures with embedded dielectric layers containing permanent charges
8,846,457	9/30/2014	Printable composition of a liquid or gel suspension of diodes
8,809,126	8/19/2014	Printable composition of a liquid or gel suspension of diodes
8,803,191	8/12/2014	Systems, Devices, and Methods with Integrable FET-Controlled Lateral Thyristors
8,753,947	6/17/2014	Method of Manufacturing a Light Emitting. Photovoltaic or other Electronic Apparatus and Systems
8,753,946	6/17/2014	Method of Manufacturing a Light Emitting. Photovoltaic or other Electronic Apparatus and Systems
8,742,912	06/03/2014	Self-powered sensor system for monitoring tire pressure
8,742,456	06/03/2014	Integrating a Trench-gated Thyristor with a Trench-gated Rectifier
8,723,408	05/13/2014	Diode for Printable Composition
8,704,301	04/22/2014	Devices, Methods, and systems with MOS-gated Trench-to-trench Lateral Current Flows
8,704,295	04/22/2014	Schottky and MOSFET+Schottky Structures, Devices and Methods
8,679,903	03/25/2014	Vertical quadruple conduction channel insulated gate transistor
8,674,593	03/18/2014	Diode for a printable composition
8,669,612 B2	03/11/2014	Technique for Forming the Deep Doped Columns in Superjunction
8,643,055 B2	02/14/2014	Series Current Limiter Device
8,581,341 B2	11/12/2013	Power MOSFET with Embedded Recessed Field Plate and Methods

		of Fabrication
8,580,644 B2	11/12/2013	Multi-Level Lateral floating Coupled Capacitor Transistor Structures
8,575,688 B2	11/5/2013	Trench Device Structure and Fabrication
8,569,117 B2	10/29/2013	Systems and Methods Integrating Trench-Gated Thyristor with Trench-Gated Rectifier
8,513,732 B2	08/20/2013	High Voltage Power MOSFET having low on-resistance
8,456,393	06/04/2013	Method of Manufacturing a Light Emitting, Photovoltaic or other Electronic Apparatus and System
8,456,392	06/04/2013	Method of Manufacturing a Light Emitting, Photovoltaic or other Electronic Apparatus and System
8,450,795	05/28/2013	Technique for Forming the Deep Doped Columns in Superjunction
8,415,879	04/09/2013	Diode for Printable Composition
8,395,568	03/12/2013	Light Emitting, Photovoltaic or other Electronic Apparatus and System
8,390,060	03/05/2013	Power Semiconductor Devices, Structures, and Related Methods
8,384,630	02/26/2013	Light Emitting Photovoltaic or other Electronic Apparatus and System
8,354,711	01/15/2013	Power MOSFET and its Edge Termination
8,330,217	12/11/2012	Devices, Methods, and Systems with MOS-Gated Trench-to-Trench Lateral, Current Flow
8,330,213	12/11/2012	Power Semiconductor Devices, Methods, and Structures with Embedded Dielectric Layers Containing Permanent Charges
8,319,278	11/27/2012	Power Device Structures and Methods Using Empty Space Zones
8,310,006	11/13/2012	Devices, Structures, and Methods using Self-aligned Resistive Source Extensions
8,193,565	06/05/2012	Multi-level Lateral Floating Coupled Capacitor Transistor Structures
8,133,768	03/13/2012	Method of Manufacturing a Light Emitting Photovoltaic or Other Electronic Apparatus and System
8,049,271	11/01/2011	Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Formation of Floating Islands
7,989,293	08/02/2011	Trench Device Structure and Fabrication
7,825,492	11/02/2010	Isolated Vertical Power Device Structure with Both N-Doped and P-Doped Trenches
7,745,885	06/29/2010	High Voltage Power MOSFET Having Low On-Resistance
7,736,976	06/15/2010	Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands
7,705,397	04/27/2010	Devices, Methods, and Systems with MOS-Gated Trench-to-Trench Lateral Current Flow
7,704,842	04/27/2010	Lateral High-Voltage Transistor with Vertically-Extended Voltage-Equalized Drift Region
7,586,165	09/08/2009	Microelectromechanical Systems (MEMS) Device Including a Superlattice

7,586,148	09/08/2009	Power Semiconductor Device Having a Voltage Sustaining Region that Includes Doped Columns Formed by Terraced Trenches
7,557,394	07/07/2009	High-Voltage Transistor Fabrication with Trench Etching Technique
7,544,544	06/09/2009	Low Capacitance Two-Terminal Barrier Controlled TVS Diodes
7,535,041	05/19/2009	Method for Making a Semiconductor Device Including Regions of Band-Engineered Semiconductor Superlattice to Reduce Device-On Resistance
7,531,850	05/12/2009	Semiconductor Device Including a Memory Cell with a Negative Differential Resistance (NDR) Device
7,531,829	05/12/2009	Semiconductor Device Including Regions of Band-Engineered Semiconductor Superlattice to Reduce Device-On Resistance
7,504,305	03/17/2009	Technique for Forming the Deep Doped Regions in Superjunction Devices
7,473,966	01/06/2009	Oxide-Bypassed Lateral High Voltage Structures and Methods
7,442,584	10/28/2008	Isolated Vertical Power Device Structure with Both N-Doped and P-Doped Trenches
7,411,249	08/12/2008	Lateral High-Voltage Transistor with Vertically-Extended Voltage-Equalized Drift Region
7,397,097	07/08/2008	Integrated Released Beam Layer Structure Fabricated in Trenches and Manufacturing Method Thereof
7,339,252	03/04/2008	Semiconductor Having Thick Dielectric Regions
7,304,347	12/04/2007	Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands
7,244,970	07/17/2007	Low Capacitance Two-Terminal Barrier Controlled TVS Diodes
7,224,027	05/29/2007	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Diffusion from Regions of Oppositely Doped Polysilicon
7,202,494	04/10/2007	FinFET Including a Superlattice
7,199,427	04/03/2007	DMOS Device with a Programmable Threshold Voltage
7,138,289	11/21/2006	Technique for Fabricating Multilayer Color Sensing Photodetectors
7,094,621	08/22/2006	Fabrication on Diaphragms and "Floating" Regions of Single Crystal Semiconductor for MEMS Devices
7,091,552	08/15/2006	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Ion Implantation
7,084,455	08/01/2006	Power Semiconductor Device Having a Voltage Sustaining Region that Includes Terraced Trench with Continuous Doped Columns Formed in an Epitaxial Layer
7,067,376	06/27/2006	High Voltage power MOSFET Having Low On-Resistance
7,061,072	06/13/2006	Integrated Circuit Inductors Using Driven Shields
7,023,069	04/04/2006	Method for Forming Thick Dielectric Regions Using Etched Trenches
7,019,360	03/28/2006	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching Using an Etchant Gas that is also a Doping Source

7,015,104	03/21/2006	Technique for Forming the Deep Doped Columns in Superjunction
6,992,350	01/31/2006	High Voltage Power MOSFET Having Low On-Resistance
6,949,432	09/27/2005	Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface
6,921,938	07/26/2005	Double Diffused Field Effect Transistor Having Reduced On-Resistance
6,906,529	06/14/2005	Capacitive Sensor Device With Electrically Configurable Pixels
6,882,573	04/19/2005	DMOS Device with a Programmable Threshold Voltage
6,861,337	03/01/2005	Method for Using a Surface Geometry for a MOS-Gated Device in the Manufacture of Dice Having Different Sizes
6,812,526	11/02/2004	Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface
6,812,056	11/02/2004	Technique for Fabricating MEMS Devices Having Diaphragms of "Floating" Regions of Single Crystal Material
6,794,251	09/21/2004	Method of Making a Power Semiconductor Device
6,790,745	09/14/2004	Fabrication of Dielectrically Isolated Regions of Silicon in a Substrate
6,777,745	08/17/2004	Symmetric Trench MOSFET Device and Method of Making Same
6,750,523	06/15/2004	Photodiode Stacks for Photovoltaic Relays and the Method of Manufacturing the Same
6,750,104	06/15/2004	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching Using an Etchant Gas that is also a Doping Source
6,734,495	05/11/2004	Two Terminal Programmable MOS-Gated Current Source
6,730,963	05/04/2004	Minimum Sized Cellular MOS-Gated Device Geometry
6,724,044	04/20/2004	MOSFET Device Having Geometry that Permits Frequent Body Contact
6,724,039	04/20/2004	Semiconductor Device Having a Schottky Diode
6,713,351	03/30/2004	Double Diffused Field Effect Transistor Having Reduced On-Resistance
6,710,414	03/23/2004	Surface Geometry for a MOS-Gated Device that Allows the Manufacture of Dice Having Different Sizes
6,710,400	03/23/2004	Method for Fabricating a High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Rapid Diffusion
6,689,662	02/10/2004	Method of Forming a High Voltage Power MOSFET Having Low On-Resistance
6,686,244	02/03/2004	Power Semiconductor Device Having a Voltage Sustaining Region that Includes Doped Columns Formed with a Single Ion Implantation Step
6,660,571	12/09/2003	High Voltage Power MOSFET Having Low On-Resistance
6,656,797	12/02/2003	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Ion Implantation
6,649,477	11/18/2003	Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands

6,627,949	09/30/2003	High Voltage Power MOSFET Having Low On-Resistance
6,624,494	09/23/2003	Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer
6,621,107	09/16/2003	Trench DMOS Transistor with Embedded Trench Schottky Rectifier
6,593,619	07/15/2003	High Voltage Power MOSFET Having Low On-Resistance
6,593,174	07/15/2003	Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same
6,576,516	06/10/2003	High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Diffusion from Regions of Oppositely Doped Polysilicon
6,566,201	05/20/2003	Method for Fabricating a High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Rapid Diffusion
6,538,279	03/25/2003	High-Side Switch with Depletion-Mode Device
6,492,663	12/10/2002	Universal Source Geometry for MOS-Gated Power Devices
6,479,352	11/12/2002	Method of Fabricating High Voltage Power MOSFET Having Low On-Resistance
6,472,709	10/29/2002	Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface
6,468,866	10/22/2002	Single Feature Size MOS Technology Power Device
6,465,304	10/15/2002	Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer
6,432,775	08/13/2002	Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface
6,420,764	07/16/2002	Field Effect Transitor (sic. Transistor) Having Dielectrically Isolated Sources and Drains and Methods for Making Same
6,403,427	06/11/2002	Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same
6,399,961	06/04/2002	Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same
6,369,426	04/09/2002	Transistor with Integrated Photodetector for Conductivity Modulation
6,368,918	04/09/2002	Method of Fabricating Nan (sic. an) Embedded Flash EEPROM with a Tunnel Oxide Grown on a Textured Substrate
6,331,794	12/18/2001	Phase Leg with Depletion-Mode Device
6,316,336	11/13/2001	Method for Forming Buried Layers with Top-Side Contacts and the Resulting Structure
6,291,845	09/18/2001	Fully-Dielectric-Isolated FET Technology
6,272,050	08/07/2001	Method and Apparatus for Providing an Embedded Flash-EEPROM Technology
6,239,752	05/29/2001	Semiconductor Chip Package that is also an Antenna
6,225,662	05/01/2001	Semiconductor Structure with Heavily Doped Buried Breakdown Region
6,215,170	04/10/2001	Structure for Single Conductor Acting as Ground and Capacitor Plate Electrode Using Reduced Area
6,198,114	03/06/2001	Field Effect Transistor Having Dielectrically Isolated Sources and

		Drains and Method for Making Same
6,069,385	05/30/2000	Trench MOS-Gated Device
6,064,109	05/16/2000	Ballast Resistance for Producing Varied Emitter Current Flow Along the Emitter's Injecting Edge
6,046,473	04/04/2000	Structure and Process for Reducing the On-Resistance of MOS-Gated Power Devices
6,011,298	01/04/2000	High Voltage Termination with Buried Field-Shaping Region
5,985,721	11/16/1999	Single Feature Size MOS Technology Power Device
5,981,998	11/09/1999	Single Feature Size MOS Technology Power Device
5,981,318	11/09/1999	Fully-Dielectric-Isolated FET Technology
5,960,277	09/28/1999	Method of Making a Merged Device with Aligned Trench FET and Buried Emitter Patterns
5,897,355	05/27/1999	Method of Manufacturing Insulated Gate Semiconductor Device to Improve Ruggedness
5,869,371	02/09/1999	Structure and Process for Reducing the On-Resistance of MOS-gated Power Devices
5,856,696	01/05/1999	Field Effect Transistor Having Dielectrically Isolated Sources and Drains
5,821,136	10/13/1998	Inverted Field-Effect Device with Polycrystalline Silicon/Germanium Channel
5,801,396	09/01/1998	Inverted Field-Effect Device with Polycrystalline Silicon/Germanium Channel
5,798,549	08/25/1998	Conductive Layer Overlaid Self-Aligned MOS-Gated Semiconductor Devices
5,773,328	06/30/1998	Method Of Making A Fully-Dielectric-Isolated FET
5,756,386	05/26/1998	Method of Making Trench MOS-Gated Device with A Minimum Number of Masks
5,710,443	01/20/1998	Merged Device with Aligned Trench FET and Buried Emitter Patterns
5,708,289	01/13/1998	Pad Protection Diode Structure
5,701,023	12/23/1997	Insulated Gate Semiconductor Device Typically Having Subsurface-Peaked Portion of Body Region for Improved Ruggedness
5,691,555	11/25/1997	Integrated Structure Current Sensing Resistor For Power Devices Particularly For Overload Self-Protected Power MOS Devices
5,668,025	09/16/1997	Method of Making a FET with Dielectrically Isolated Sources and Drains
5,663,079	09/02/1997	Method of Making Increased Density MOS-Gated Semiconductor Devices
5,648,670	07/15/1997	Trench MOS-Gated Device with a Minimum Number of Masks
5,640,037	06/17/1997	Cell with Self-Aligned Contacts
5,637,889	06/10/1997	Composite Power Transistor Structures Using Semiconductor Materials With Different Bandgaps
5,591,655	01/07/1997	Process for Manufacturing a Vertical Switched-Emitter Structure with Improved Lateral Isolation
5,589,415	12/31/1996	Method for Forming a Semiconductor Structure with Self-Aligned Contacts

5,576,245	11/19/1996	Method of Making Vertical Current Flow Field Effect Transistor
5,574,301	11/12/1996	Vertical Switched-Emitter Structure with Improved Lateral Isolation
5,528,063	06/18/1996	Conductive-Overlaid Self-Aligned MOS-Gated Semiconductor Devices
5,485,027	01/16/1996	Isolated DMOS IC Technology
5,298,781	03/29/1994	Vertical Current Flow Field Effect Transistor with Thick Insulator Over Non-Channel Areas
5,237,481	08/17/1993	Temperature Sensing Device for Use in a Power Transistor
5,218,228	06/08/1993	High Voltage MOS Transistors with Reduced Parasitic Current Gain
5,164,325	11/17/1992	Method of Making a Vertical Current Flow Field Effect Transistor
5,156,989	10/20/1992	Complementary, (sic) Isolated DMOS IC Technology
5,132,235	07/21/1992	Method for Fabricating a High Voltage MOS Transistor
5,034,785	07/23/1991	Planar Vertical Channel DMOS Structure
4,983,535	01/08/1991	Vertical DMOS Transistor Fabrication Process
4,978,631	12/18/1990	Current Source with a Process Selectable Temperature Coefficient
4,958,204	09/18/1990	Junction Field-Effect Transistor with a Novel Gate
4,956,700	09/11/1990	Integrated Circuit with High Power, Vertical Output Transistor Capability
4,952,992	08/28/1990	Method and Apparatus for Improving the On-Voltage Characteristics of a Semiconductor Device
4,929,991	05/29/1990	Rugged Lateral DMOS Transistor Structure
4,920,388	04/24/1990	Power Transistor with Integrated Gate Resistor
4,916,509	04/10/1990	Method for Obtaining Low Interconnect Resistance on a Grooved Surface and the Resulting Structure
4,914,058	04/03/1990	Grooved DMOS Process with Varying Gate Dielectric Thickness
4,896,196	01/23/1990	Vertical DMOS Power Transistor with an Integral Operating Condition Sensor
4,893,160	01/09/1990	Method for Increasing the Performance of Trenched Devices and the Resulting Structure
4,868,537	09/19/1989	Doped SiO_2 Resistor and Method of Forming Same
4,851,366	07/25/1989	Method for Providing Dielectrically Isolated Circuit
4,845,051	07/04/1989	Buried Gate JFET
4,835,586	05/30/1989	Dual-Gate High Density FET
4,827,324	05/02/1989	Implantation of Ions into an Insulating Layer to Increase Planar PN Junction Breakdown Voltage
4,824,795	04/25/1989	Method for Obtaining Regions of Dielectrically Isolated Single Crystal Silicon
4,816,882	03/28/1989	Power MOS Transistor with Equipotential Ring
4,799,100	01/17/1989	Method and Apparatus for Increasing Breakdown of a Planar Junction
4,798,810	01/17/1989	Method for Manufacturing a Power MOS Transistor
4,794,436	12/27/1988	High Voltage Drifted-Drain MOS Transistor
4,791,462	12/13/1988	Dense Vertical J-MOS Transistor
4,774,196	09/27/1988	Method of Bonding Semiconductor Wafers

4,767,722	08/30/1988	Method for Making Planar Vertical Channel DMOS Structures
4,759,836	07/26/1988	Ion Implantation of Thin Film $CrSi_2$ and SiC Resistors
4,707,909	11/24/1987	Manufacture of Trimmable High Value Polycrystalline Silicon Resistors
4,682,405	07/28/1987	Methods for Forming Lateral and Vertical DMOS Transistors
4,402,003	08/30/1983	Composite MOS/Bipolar Power Device
4,398,339	08/16/1983	Fabrication Method for High Power MOS Device
4,393,391	07/12/1983	Power MOS Transistor With a Plurality of Longitudinal Grooves to Increase Channel Conducting Area
4,345,265	08/17/1982	MOS Power Transistor with Improved High-Voltage Capability
4,344,081	08/10/1982	Combined DMOS and a Vertical Bipolar Transistor Device and Fabrication Method Therefor (sic)
4,145,703	03/20/1979	High Power MOS Device and Fabrication Method Therefor (sic)

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