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[54] **DIFFUSION BARRIER TRILAYER FOR MINIMIZING REACTION BETWEEN METALLIZATION LAYERS OF INTEGRATED CIRCUITS**

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[21] Appl. No.: **685,159**

[22] Filed: **Jul. 23, 1996**

Related U.S. Application Data

[60] Continuation of Ser. No. 474,286, Jun. 7, 1995, abandoned, which is a division of Ser. No. 412,473, Mar. 28, 1995, abandoned.

[51] **Int. Cl.**[6] **H01L 21/44**; H01L 29/43

[52] **U.S. Cl.** **257/751**; 257/915; 438/653

[58] **Field of Search** 257/751, 915; 437/190, 195

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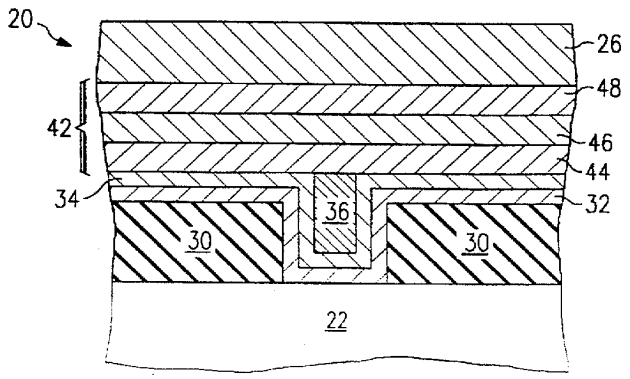
[57] **ABSTRACT**

A diffusion barrier trilayer **42** is comprised of a bottom layer **44**, a seed layer **46** and a top layer **48**. The diffusion barrier trilayer **42** prevents reaction of metallization layer **26** with the top layer **48** upon heat treatment, resulting in improved sheet resistance and device speed.

15 Claims, 3 Drawing Sheets



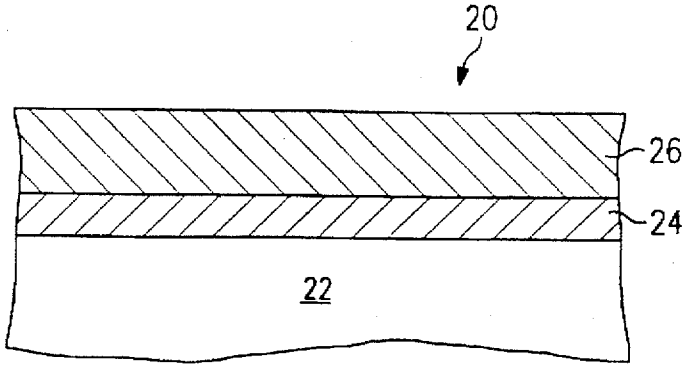


FIG. 1
(PRIOR ART)

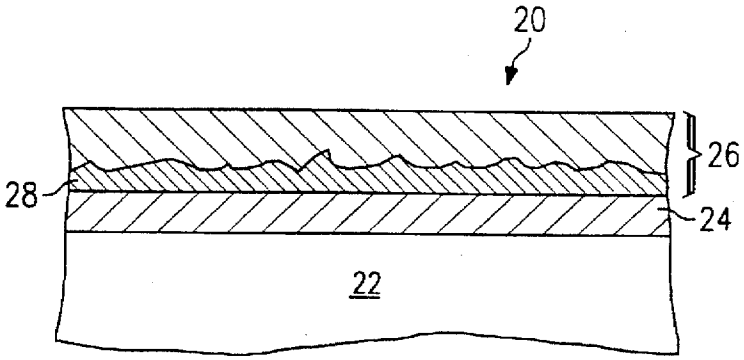


FIG. 2
(PRIOR ART)

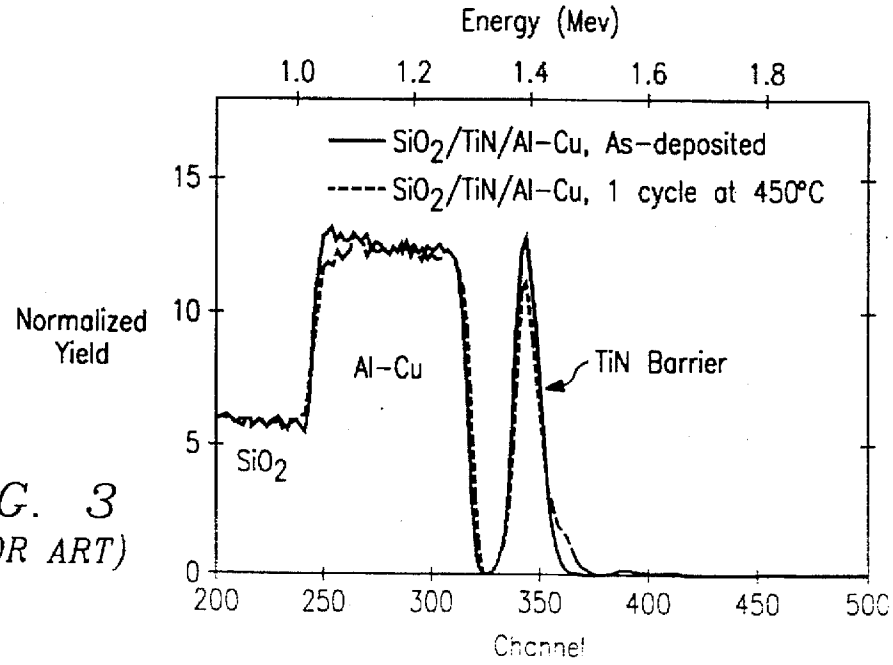


FIG. 3
(PRIOR ART)

FIG. 4
(PRIOR ART)

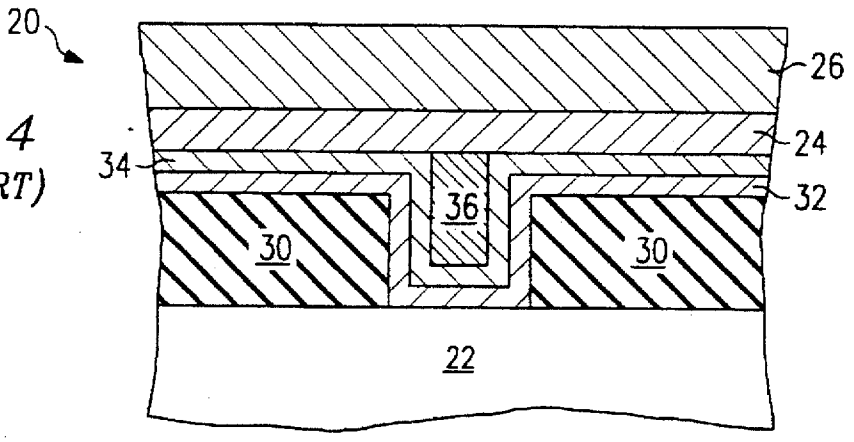


FIG. 5
(PRIOR ART)

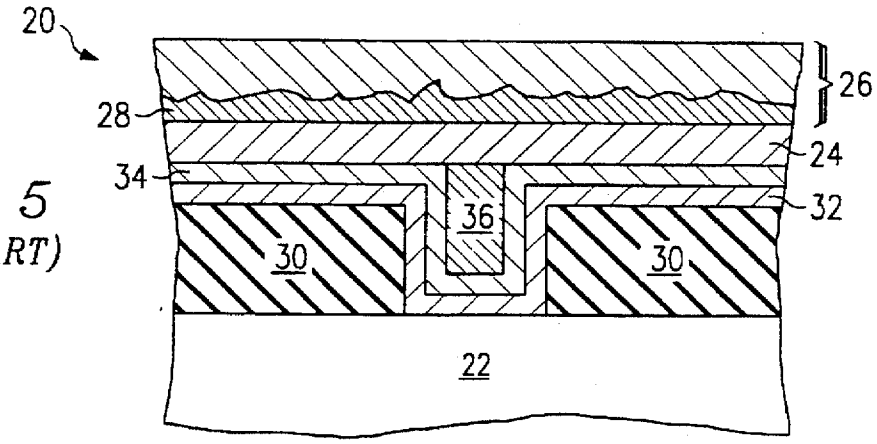


FIG. 6
(PRIOR ART)

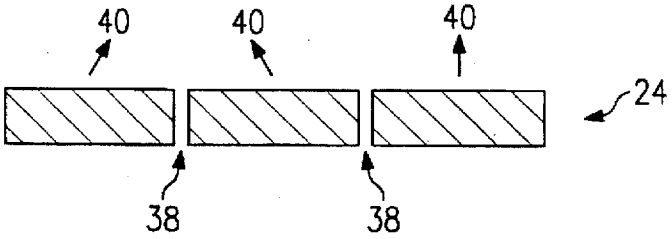


FIG. 7

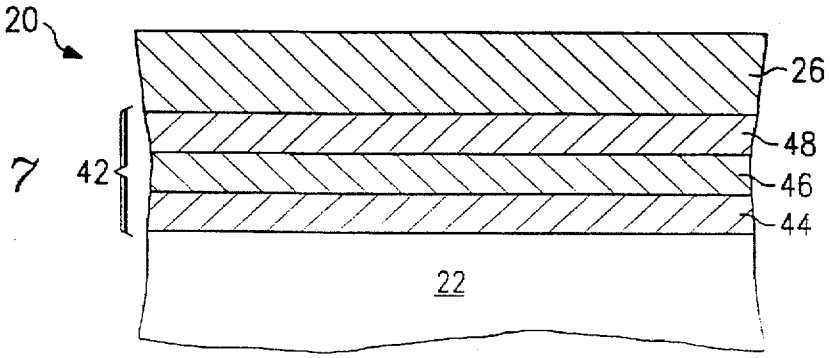
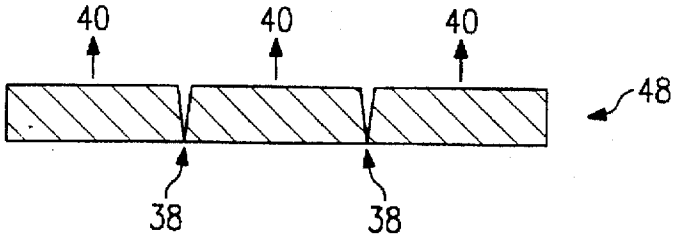


FIG. 8



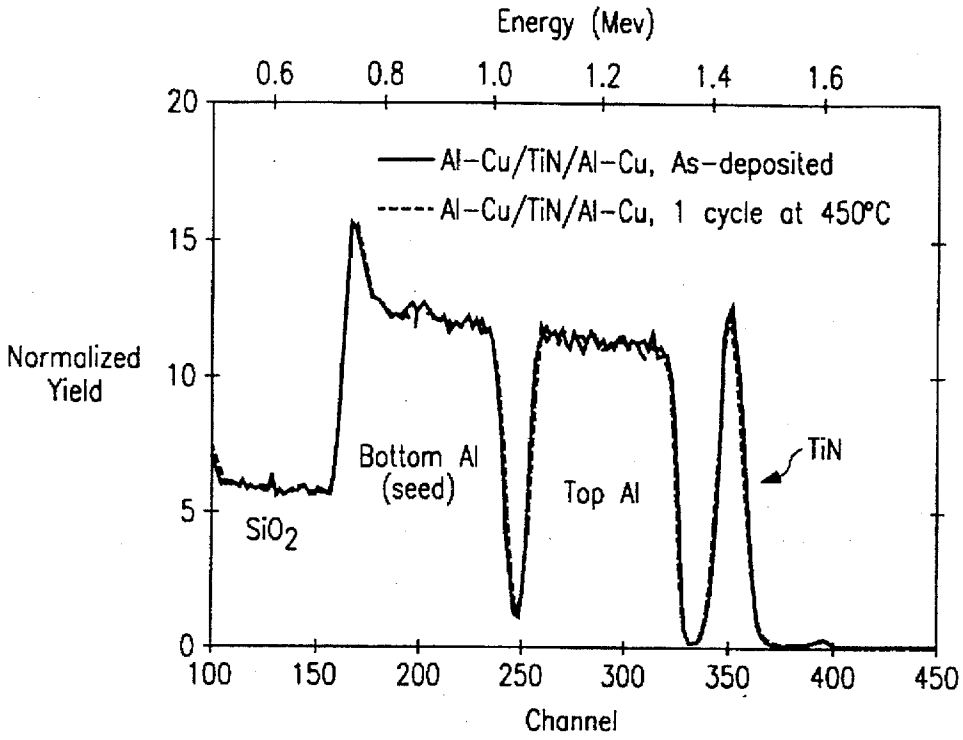


FIG. 9

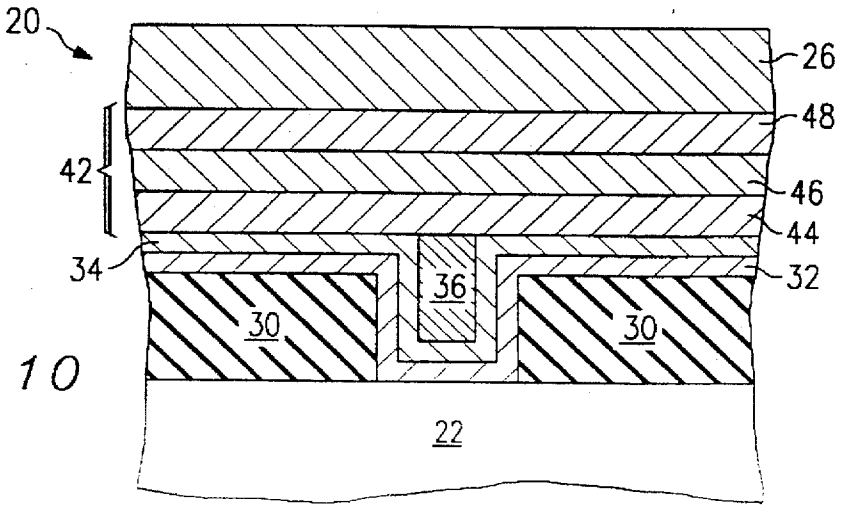


FIG. 10

DIFFUSION BARRIER TRILAYER FOR MINIMIZING REACTION BETWEEN METALLIZATION LAYERS OF INTEGRATED CIRCUITS

This is a continuation of application Ser. No. 08/474,286 filed Jun. 2, 1995, now abandoned, which is a division of application Ser. No. 08/412,473, filed Mar, 28, 1995, now abandoned.

FIELD OF THE INVENTION

This invention relates generally to the fabrication of semiconductor devices, and more specifically to metallization layers of integrated circuits.

BACKGROUND OF THE INVENTION

Semiconductors are widely used in integrated circuits for electronic applications, including radios, computers, televisions, and high definition televisions. Such integrated circuits typically use multiple transistors fabricated in single crystal silicon. Many integrated circuits now contain multiple levels of metallization for interconnections.

Aluminum-copper (AlCu) alloys are typically used in VLSI (very large scale integration) metallization. To enhance the speed of devices, a low and stable sheet resistance is required for AlCu. However, AlCu can react with other metals (e.g. W) thereby increasing its sheet resistance. Sheet resistance is a measurement of a conductive material with a magnitude proportional to resistivity and inverse of thickness. TiN has been applied as a diffusion barrier between AlCu and the other metals to suppress their reactions. However, heat treatment of AlCu/TiN layered structures at 450° C. induces reactions between the AlCu and TiN, leading to an increase in the sheet resistance of the AlCu.

Several attempts have been made to improve the barrier properties of TiN in Al/TiN/Si, Al/TiN/silicide/Si and Al/TiN/W structures. In the past, the improvement of TiN barriers have mostly been achieved by optimizing the parameters during TiN deposition, such as introducing oxygen flow during deposition, changing the substrate temperature, or adding a substrate voltage bias. Other attempts have included post-deposition treatments such as thermal annealing and exposure to air.

SUMMARY OF THE INVENTION

The present invention is a method and structure for a diffusion barrier trilayer comprising a bottom layer deposited on a substrate, a seed layer deposited on the bottom layer, a top layer deposited on the seed layer, and a metallization layer deposited on the top layer. Reaction of the metallization layer with the top layer, which may occur upon heat treatment, is minimized due to the improved properties of the top layer of the diffusion barrier trilayer. This results in no degradation of sheet resistance of the metallization layer upon heat treatment, and no loss of integrated circuit device speed.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, which form an integral part of the specification and are to be read in conjunction therewith, and in which like numerals and symbols are employed to designate similar components in various views unless otherwise indicated:

FIG. **1** is a prior art drawing of a cross-sectional view of a semiconductor wafer having a TiN diffusion barrier between the metallization layer and the substrate;

FIG. **2** is a prior art drawing showing the wafer of FIG. **1** after heat treatment, where the metallization layer has reacted with the diffusion barrier;

FIG. **3** is a Rutherford Backscattering Spectroscopy (RBS) of a prior art wafer before and after heat treatment;

FIG. **4** is a prior art drawing showing a typical via plug structure used to connect a metallization layer to underlying circuitry or metal layers;

FIG. **5** shows the wafer of FIG. **4** after heat treatment, with a portion of the metallization layer reacted with the diffusion barrier;

FIG. **6** demonstrates the crystal structure of the diffusion barrier of prior art, having a polycrystalline structure with high-angle grain boundaries;

FIG. **7** is a cross-sectional view of the present invention, a diffusion barrier trilayer;

FIG. **8** demonstrates the crystal structure of the top layer of the diffusion barrier trilayer, having a single-crystal-like appearance;

FIG. **9** is a Rutherford Backscattering Spectroscopy (RBS) of an experimental wafer having a diffusion barrier bilayer, before and after heat treatment; and

FIG. **10** shows the present invention implemented on the structure shown in FIG. **4**.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

It has been found that the methods used in the past to improve the barrier properties of TiN are inadequate. Changing deposition temperature may induce change in other properties of TiN, such as stress and grain size, making it difficult to optimize these parameters at the same time. Adding substrate bias induces ion bombardment of the TiN layer, which may result radiation damage to existing devices. Post-deposition treatments involve additional processing steps, increasing process cycle time. Moreover, thermal annealing (densification) of TiN is possible only at the contact level on the integrated circuitry where AlCu is not present. Dosing with oxygen during deposition is undesirable, since oxygen may contaminate the Ti sputtering target, form oxide particles and increase the sheet resistance of TiN. Exposure of TiN to air for 24 hours has not been found to improve the barrier properties of TiN.

The making and use of the presently preferred embodiments are discussed below in detail. However, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not delimit the scope of the invention.

The following is a description of a preferred embodiment of the present invention, including manufacturing methods. Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated. Table 1 below provides an overview of the elements of the embodiments and the drawings.

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