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# United States Patent [19]

Lee et al.

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[45] Date of Patent: *Feb. 9, 1999

[54] **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF**

[75] Inventors: **Sang-in Lee**; **Chang-soo Park**, both of Kyungki-do, Rep. of Korea

[73] Assignee: **Samsung Electronics Co., Ltd.**, Kyungki-Do, Rep. of Korea

[ * ] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,355,020.

[21] Appl. No.: **612,792**

[22] Filed: **Mar. 11, 1996**

**Related U.S. Application Data**

[60] Division of Ser. No. 8,775, Jan. 25, 1993, Pat. No. 5,534,463, which is a continuation-in-part of Ser. No. 897,294, May 11, 1992, Pat. No. 5,318,923, which is a continuation-in-part of Ser. No. 585,218, Sep. 19, 1990, abandoned.

[30] **Foreign Application Priority Data**

Jan. 23, 1992 [KR] Rep. of Korea ..... 92-904

[51] **Int. Cl.**[6] ..... **H01L 23/48**; H01L 23/52; H01L 29/40

[52] **U.S. Cl.** ..... **257/773**; 257/751; 257/752; 257/758; 257/763; 257/764; 257/765; 257/767; 257/770; 257/774; 257/775

[58] **Field of Search** ..... 257/751, 752, 257/758, 763, 764, 765, 767, 770, 771, 774, 775

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*Assistant Examiner*—Jhihan B. Clark
*Attorney, Agent, or Firm*—Pillsbury Madison & Sutro LLP

[57] **ABSTRACT**

A wiring layer of a semiconductor device having a novel contact structure is disclosed. The semiconductor device includes a semiconductor substrate, an insulating layer having an opening (contact hole or via), a reactive spacer formed on the sidewall of the opening or a reactive layer formed on the sidewall and on the bottom surface of the opening and a first conductive layer formed on the insulating layer which completely fills the opening. Since the reactive spacer or layer is formed on the sidewall of the opening, when the first conductive layer material is deposited, large islands will form to become large grains of the sputtered Al film. Also, providing the reactive spacer or layer improves the reflow of the first conductive layer during a heat-treating step for filling the opening at a high temperature below a melting temperature. Thus, complete filling of the opening with sputtered Al can be ensured. All the contact holes, being less than 1 $\mu$m in size and having an aspect ratio greater than 1.0, can be completely filled with Al, to thereby enhance the reliability of the wiring of a semiconductor device.

**38 Claims, 9 Drawing Sheets**

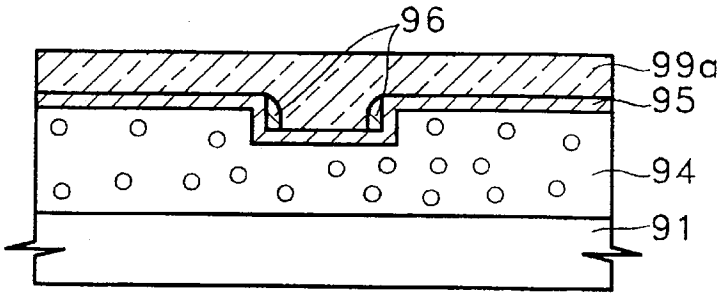

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FIG. 1 (PRIOR ART)

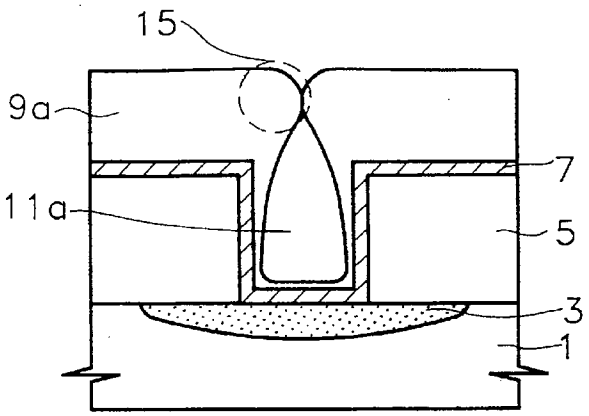



FIG. 2 (PRIOR ART)

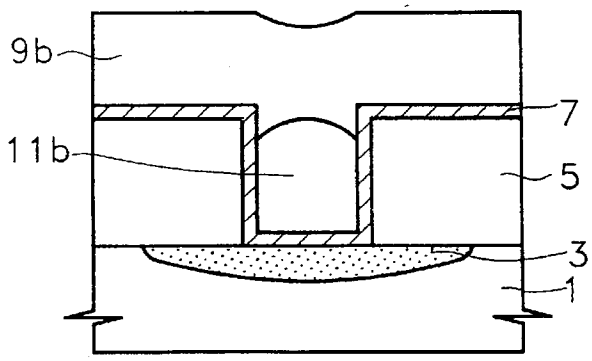



FIG. 3 (PRIOR ART)

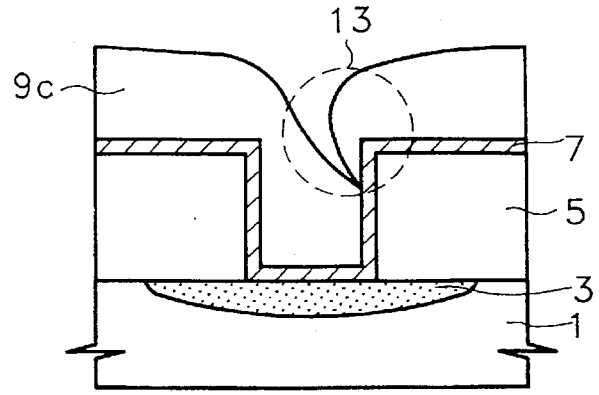


FIG. 4

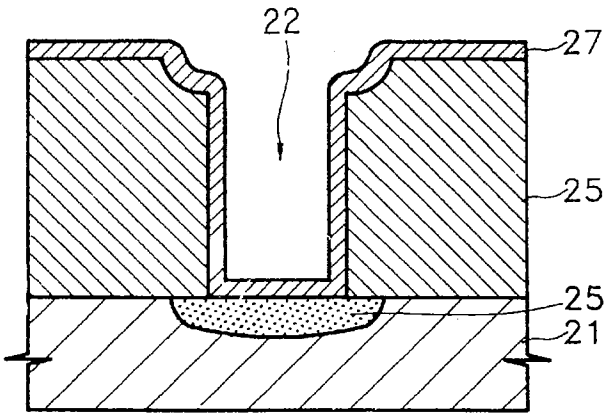



FIG. 5

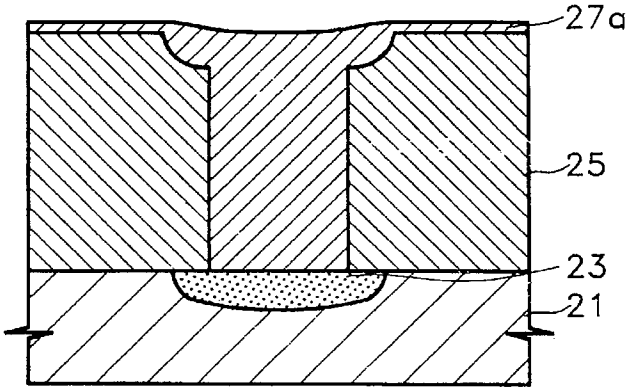



FIG. 6

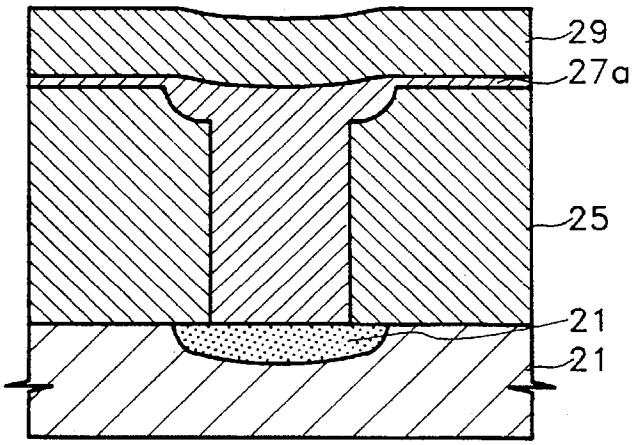


FIG. 7

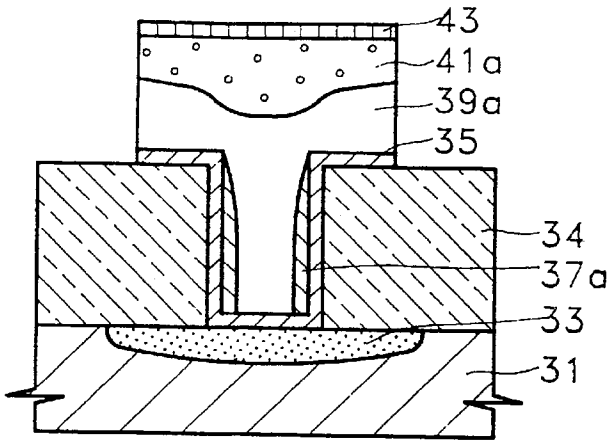



FIG. 8

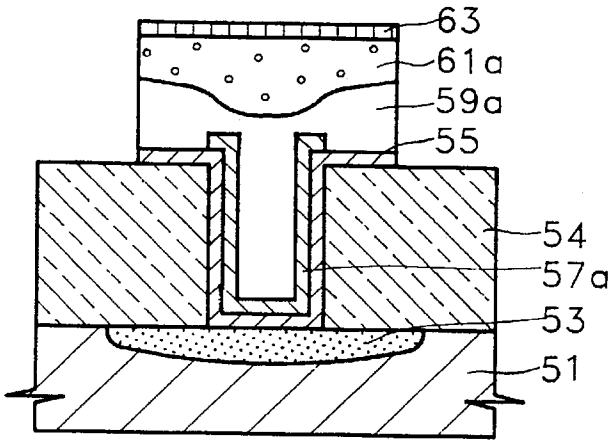
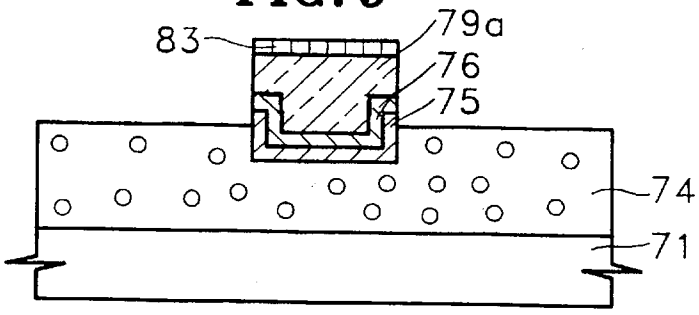



FIG. 9



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