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VERIFICATION OF TRANSLATION

I, Rumiko Whitehead

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declare that I am well acquainted with both the Japanese and English languages, and that the attached is an accurate translation, to the best of my knowledge and ability, of Japanese Unexamined Patent Application Publication No. H08-274098, published October 18, 1996.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-captioned application or any patent issued thereon.

Signature Rumiko Whitehead Date 8/2/2017

Rumiko Whitehead

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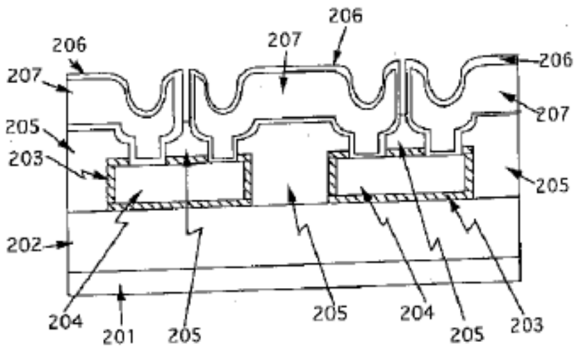
(54) [Title of Invention] Semiconductor Device and Manufacture Method of Semiconductor Device

(57) [Abstract]

[Structure] A wiring structure of a multi-layered wiring semiconductor device characterized by the entire upper portion, lower portion, and side walls of a metal wiring being covered by a barrier metal. A semiconductor device characterized by a first metal wiring layer formed on a first insulating film formed on a semiconductor substrate, in which the first metal wiring layer is formed such that the side walls, lower portion and upper portion thereof are covered by a second metal wiring layer, and in which the second and subsequent wiring layers of a semiconductor device having a multi-layered wiring structure are similarly formed, and a manufacturing method thereof.

[Purpose] To dramatically improve the reliability, and in particular the electromigration resistance, of metal wiring layers. Even when a high current is applied, metal, such as aluminum and the like from wiring materials, is prevented from moving and flowing out from side walls that are not in contact with TiN and causing disconnection failure. In addition to aluminum, the first metal wiring layer may be primarily composed of copper, gold, silver, zinc, platinum or iron; a second metal wiring layer may be primarily composed of titanium, tungsten, molybdenum, titanium nitride, tungsten nitride or molybdenum nitride.



[Scope of Claims]
[Claim 1] A semiconductor device characterized by a first metal wiring layer formed on a first insulating film formed on a semiconductor substrate, in which the first metal wiring layer is formed so that side walls and a lower portion and an upper portion thereof are covered by a second metal wiring layer, and in which the second and subsequent wiring layers of a semiconductor device having a multi-layered wiring structure are similarly formed.

[Claim 2] In the semiconductor device according to the aforementioned Claim 1, a first primary component metal is at least aluminum, copper, gold, silver, zinc, platinum, or iron, and a second primary component metal is at least titanium, tungsten, molybdenum, titanium nitride, tungsten nitride, or molybdenum nitride.

[Claim 3] With respect to a manufacturing method of a semiconductor device, a manufacturing method of a semiconductor device characterized by including at least a process of forming a first insulating film, a process of forming TiN, a process of forming aluminum, a process of patterning the aforementioned aluminum, a process of again forming TiN, and a process of forming the aforementioned TiN to be larger than the aluminum.

[Claim 4] With respect to a manufacturing method of a semiconductor device, a manufacturing method of a semiconductor device characterized by including at least a process of forming a first insulating film, a process of forming TiN, a process of forming aluminum, a process of patterning the aforementioned aluminum, a process of again forming TiN to be thick, and a process of subjecting the aforementioned TiN to anisotropic etching.

[Detailed Description of Invention]
[0001]
[Field of Industrial Application] The present invention relates to a structure of, and a manufacturing method of, a semiconductor device having a multi-layered wiring structure.

[002]
[Prior Art] Conventionally, as shown in Fig. 3, a barrier metal, the aforementioned first metal wiring layer, and a barrier metal are formed in this order on a first insulating film formed on the aforementioned semiconductor substrate, and then formed into a desired pattern through photolithography and etching processes. Thereafter, a first interlayer insulating film is formed. In this structure, only the lower and upper portions of the metal wiring are in contact with the barrier metal and the barrier metal is not formed on a side wall portion.

[0003]
[Problem to Be Solved by the Invention] However, as wiring structures have become increasingly multi-layered and finer in size, it is becoming difficult to sufficiently ensure reliability of metal wiring with conventional technology. When a high current is applied to metal wiring according to the conventional technology in order to test the reliability thereof, there is an issue in which a portion of the metal wiring moves and takes on a form as if it melted out from the side wall portion of the metal wiring that is not in contact with the barrier metal made of Ti or TiN, causing disconnection failures.

[0004] The present invention solves this issue and the purpose thereof is to enable improvement of the reliability of metal wiring by covering the entire surface of metal wiring with a barrier metal.

[0005]
[Means of Solving the Problem] A semiconductor device according to the present invention is characterized by a barrier metal covering the side walls and upper and lower sides of the aforementioned metal wiring formed on the aforementioned first insulating film formed on the aforementioned semiconductor substrate.

[0006]
[Embodiments] Fig. 3 is a cross-sectional view of a conventional semiconductor device. Fig. 2 is a cross-sectional view of a semiconductor device according to one embodiment of the present invention. Figs. 1(a) through (d) are main cross-sectional views of each manufacturing process of a manufacturing method according to another embodiment (Claim 2) of the present invention. Figs. 4(a) through (d) are main cross-sectional views of each manufacturing process of a manufacturing method according to another embodiment (Claim 3) of the present invention. In all of the figures of the embodiments, parts having the same function are indicated by identical reference numerals, and redundant explanations thereof are omitted. Below, the manufacturing method (Claim 2) will be explained step by step with reference to Figs. 1(a) through (d).

[0007] (Embodiment 1) A first embodiment is described with reference to Fig. 1. First, as shown in Fig. 1(a), using a chemical vapor deposition (CVD) method, an insulating film 102 composed of silicon dioxide film is formed [in a thickness of] approximately 500 nm on a semiconductor substrate 101. Next, as shown in Fig. (b), using a sputtering method, a second metal wiring layer 103 having a thickness of about 40 nm and a metal wiring layer (composed of aluminum, copper and the like) having a thickness of 500 nm are formed. Next, as shown in Fig. (c), by applying photolithography, in which photoresist is used as a masking material, and an etching process, a first wiring layer 104 having a width of approximately 1.2 μm is formed. Thereafter, again using the sputtering method, a second metal wiring layer 105 is formed on the entire surface in a thickness of about 40 nm. Next, as shown in Fig. (d), by applying the photolithography and etching methods, the aforementioned second wiring layer is formed to have a width of approximately 1.6 μm, so as to have a width wider than the width of the aforementioned first metal wiring layer (approximately 1.2 μm).

[0008] Up to the second wiring layer is formed as described above; third and subsequent wiring layers are similarly formed.

[0009] Fig. 2 shows a cross-sectional view of a semiconductor device in which up to the third wiring layer is formed.

[0010] First, using a chemical vapor deposition (CVD) method, an insulating film 202 composed of silicon dioxide film is formed [in a thickness of] approximately 500 nm on a semiconductor substrate 201. Next, using a sputtering method, a second metal wiring layer 203 having a thickness of about 40 nm and a metal wiring layer (the material thereof being aluminum, copper and the like) having a thickness of 500 nm are formed, and then, by applying photolithography, in which photoresist is used as a masking material, and an etching process, a first wiring layer 204 having a width of approximately 1.2 μm is formed. Thereafter, again using the sputtering method, the second metal wiring layer is formed on the entire surface in a thickness of about 40 nm. By applying the photolithography and etching methods, the aforementioned second wiring layer is formed to have a width of approximately 1.6 μm, so as to have a width wider than the width of the aforementioned first metal wiring layer (approximately 1.2 μm). Next, using the CVD method, an interlayer insulating film 205 composed of silicon dioxide film is formed in a thickness of approximately 800 nm. After forming the aforementioned first interlayer insulating film, a hole of about 0.7 μm is formed by applying the photolithography and etching processes. Thereafter, using the sputtering method, the second metal wiring layer having a thickness of about 40 nm and a metal wiring layer having a thickness of 500 nm are formed on the entire surface, and then a third wiring layer

207 is formed by applying photolithography, in which photoresist is used as the masking material, and the etching process. Thereafter, again using the sputtering method, the second metal wiring layer is formed on the entire surface in a thickness of about 40 nm. Using the photolithography and etching methods, the aforementioned barrier metal is formed so as to have a width that is slightly wider (by about 0.4 μm) than the width of the aforementioned second wiring layer.

[0011] (Embodiment 2) Next, a second embodiment is described with reference to Fig. 4. First, as shown in Fig. 4(a), using a chemical vapor deposition (CVD) method, an insulating film 402 composed of silicon dioxide film is formed [in a thickness of] approximately 500 nm on a semiconductor substrate 401. Next, as shown in Fig. (b), using a sputtering method, a second metal wiring layer 403 having a thickness of about 40 nm and a first metal wiring layer (the material thereof being aluminum, copper and the like) 404 having a thickness of 500 nm are formed, and then a second metal wiring layer 405 is again formed in a thickness of 40 nm. By applying photolithography, in which photoresist is used as a masking material, and the etching process, the first metal wiring layer 404 having a width of approximately 1.2 μm is formed. Thereafter, again using the sputtering method, the second metal wiring layer is formed on the entire surface in a thickness of about 500 nm. The aforementioned barrier metal is subjected to anisotropic etching by an etch-back method.

[0012] The foregoing describes a manufacturing method characterized by covering the entire surface, such as the side walls, upper portion and lower portion, of the aforementioned first metal wiring layer 404, with the aforementioned second metal wiring layer.

[0013] The invention created by the present inventor is described in detail above based on the aforementioned embodiments; however, the present invention is not limited to the aforementioned embodiments, and modifications are of course possible to the extent that they do not depart from the scope of the present invention. For example, the multi-layered wiring can be three layers or more. Also, in addition to aluminum, similar effects are obtained even when the first metal wiring layer is primarily composed of copper, gold, silver, zinc, platinum, or iron. Further, similar effects are obtained when the second metal wiring layer is primarily composed of titanium, tungsten, molybdenum, titanium nitride, tungsten nitride, or molybdenum nitride.

[0014]
[Effects of the Invention] As stated above, according to the present invention, since the side walls, the lower portion and the upper portion of the first metal wiring layer are covered by the second metal wiring layer, even when a high current is applied to the metal wiring layers, aluminum and the like which are used in the first metal wiring layer will not move and flow out from the side walls that are not in contact with the second metal wiring layer. Thus, the reliability, and in particular the electromigration resistance, of metal wiring layers is improved dramatically, which makes it possible to accommodate, in particular, the increasing miniaturization and multi-layering of metal wiring.

[Brief Description of Drawings]
[Fig. 1] are main cross-sectional views to describe, step by step, an example of a manufacturing method of a semiconductor device according to the present invention.
[Fig. 2] is a main cross-sectional view of an embodiment of a semiconductor device according to the present invention.
[Fig. 3] is a main cross-sectional view of a conventional semiconductor device.
[Fig. 4] are main cross-sectional views to describe, step by step, another example of a manufacturing method of a semiconductor device according to the present invention.

[Description of Reference Numerals]
101 ...semiconductor substrate

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