This report describes the development and integration of a blanket CVD copper film into advanced microprocessor devices. The insitu deposition of sputtered Tantalum based or CVD Titanium based barrier layers and PVD Cu under and overlayers has been demonstrated to improve film adhesion and device electrical performance.

Introduction

Copper has proven to be the material of choice for sub-quarter micron interconnection because of its superior resistance against electromigration, higher electrical conductivity and lower interconnect delay compared to aluminium [1 - 3]. With copper metallization, the inlaid technique is being applied to reduce potential copper corrosion and processing cost as compared with conventional metallization integration schemes. This patterning technique requires good step coverage of the copper barrier and seed at high aspect ratios in order to provide extendibility through several generation shrinks of technology.

Results and Discussion

In this work, Cu(I)hfac(TMVS) blended with 2.5% excess VTMS and 0.4% excess hydrated hfac was chosen as the copper precursor for the CVD depositions. The process utilizes hydrogen as the mixing gas with a direct liquid injected source line. A wafer temperature of 200 °C and chamber pressure of 1.1 Torr resulted in a deposition rate of 2000Å/min. The CVD chamber was mounted on a cassette to cassette staged vacuum system and fully integrated with ionized plasma PVD tantalum nitride, CVD titanium nitride, and copper reflow sputtering chambers. The CVD Cu films deposited are relatively pure as evidenced from the near bulk resistivity of 1.9 μΩ-cm. However, SIMS analysis shows low levels of flourine within the film. Also, when deposited on TaN or TiN substrates, strong signals of flourine and oxygen were detected at the interface by TOFSIMS analysis (Figure 1). The CVD Cu films show a strong wire texture in the <111> direction. The grain size was investigated with the use of focused ion beam technique and significant grain growth was seen after a 400 °C, 3min anneal. This grain growth led to a densification of the film and a subsequent decrease in resistivity on both TaN and Copper substrates (Figure 2). The larger grains also lead to films with higher reflectivity and reduced roughness. (Figures 3 &4). Because the CVD film is to be used as a via fill material as well as the interconnect, the step coverage of the film is critical. Excellent step coverage is evident from Figure 5, a TEM of CVD Cu in a dual inlaid via/trench hole with aspect ratio of ~3.5:1. The individual grains are defined in the via cavity and there is no evidence of a seam. A key aspect for the integration of CVD Cu is in the selection of a suitable based substrate ... adhesion. This is at least partially due to flourine interactions from the Cu precursor and refractory barrier layers as is shown in the TEM in Figure 6. The electrical performance of structures using CVD Cu as both the interconnect and via fill material have been evaluated on short flow test vehicles. The addition of a thin PVD copper layer between the barrier and CVD Cu improves via resistance and adhesion dramatically. Figure 7 is a probability plot of a via structure of 0.4 μm size showing that the Cu underlayer structures have a via resistance at least an order of magnitude lower than structures without the copper underlayer. An optimum thickness of the PVD copper underlayer has been determined which protects the barrier material from the CVD precursor and is thin enough to eliminate excessive pinchoff at the top of the trench structures. Figure 8 is a probability plot of via resistance of 0.4 μm dimension for varying thicknesses of PVD Cu underlayer. Further considerations for deposition of the copper layer on the barrier material include the necessity of insitu processing of the barrier and copper films. Evidence of the importance of maintaining a clean interface between the barrier material and subsequent copper layer on device performance is increased via resistances of via chain structures obtained with air exposed barrier/copper processing. Several integration schemes have been investigated for the copper filling of the vias and metal lines. These include full fill with CVD copper, CVD copper seed with Electroplated fill, and CVD copper with insitu PVD copper reflow. Figure 9 shows SEM cross sections for the three fill techniques. The current integration of choice includes sputtered copper at <380°C for simultaneous grain growth and void-free reflow into the device structures. Electromigration performance has been evaluated on 0.25 μm logic test vehicles with an optimized stack and will be discussed.

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References

1. Hu, C.K, et. al., *Proc. VLSI Multilevel Interconnection Conference*., Santa Clara, Ca. p 181, 1986.
2. Pai, P.L and Ting, C.H., *IEEE Elec. Dev. Lett.*, 10(9), p.423, 1989.
3. Aweya, N. and Arita,Y., *Proc. Tech. Paper symp. on VLSI Technology*., Kyota, Japan, p103. 1989.
4. Rober, J, et.al., *Appl. Surf. Sci.*, 91, p 134-138, 1995.
5. Norman, J.A., et. al., *Thin Solid Films*, 262, p46-51, 1995.

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0.5

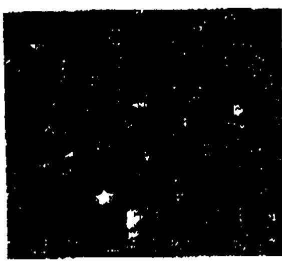
1.5 As Deposit /5 min

26 PVD Cu PVD TaN

Figure 1. TOFSIMS of CVD Cu/TaN interface

Figure 2. Resistivity of CVD Cu

Figure 3. Reflectivity of CVD copper on TaN &Cu - Al reference



3kÅ CVD Cu on PVD Cu
Zrange 158nm RMS 16.6nm

After 5min-400°C anneal
Zrange 83.1 nm RMS 12.0 nm

Figure 4. AFM micrographs of CVD Copper

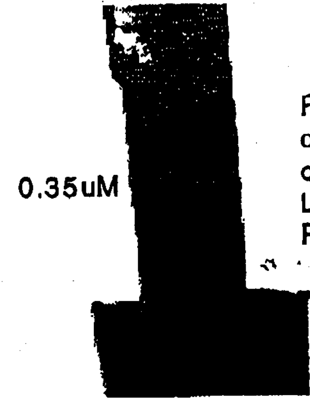


Figure 5. TEM of CVD copper seed/reflow fill of dual inlaid structure. Lower metal line is conv. PVD seed/EP fill.

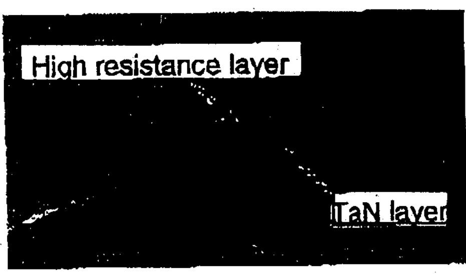


Figure 6. High mag TEM showing TaN/CVD copper iinterface layer suspected of causing high resistance

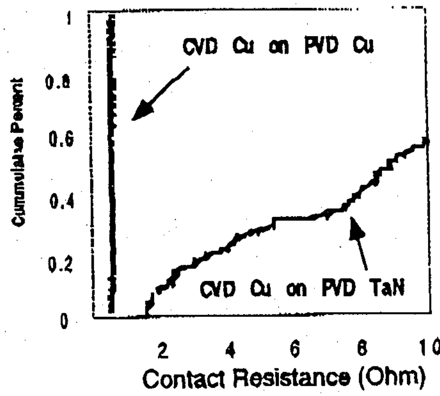


Figure 7. Resistance of 0.4uM via

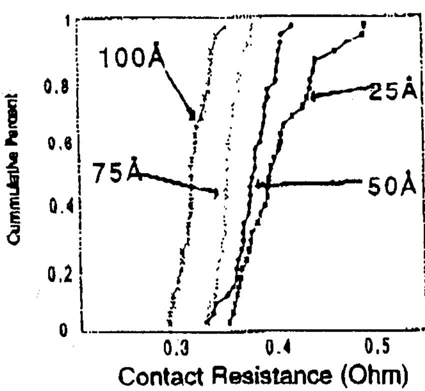


Figure 8. Resistance of 0.4uM via chain which is 4350 vias in length

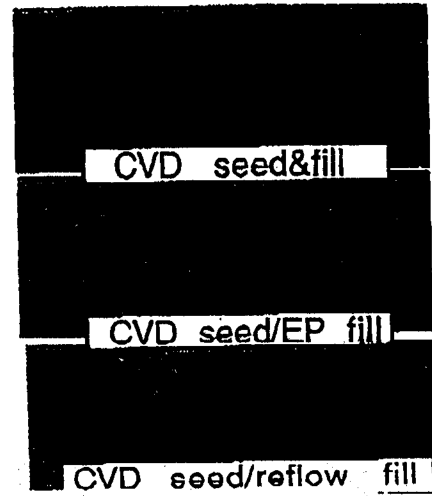


Figure 9. FIB/SEM of integrated CVD copper in dual inlaid features

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