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Young

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(54) **LOCALIZED DOPING AND/OR ALLOYING OF METALLIZATION FOR INCREASED INTERCONNECT PERFORMANCE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 258 days.

(21) Appl. No.: **10/288,974**

(22) Filed: **Nov. 6, 2002**

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(51) **Int. Cl.**
H01L 21/4763 (2006.01)
H01L 21/44 (2006.01)

(52) **U.S. Cl.** **438/625**; 438/626; 438/638; 438/654; 438/687

(58) **Field of Classification Search** 438/625, 438/626, 638, 654, 687; 385/100, 135, 136, 385/137, 123; 242/159, 47, 176
See application file for complete search history.

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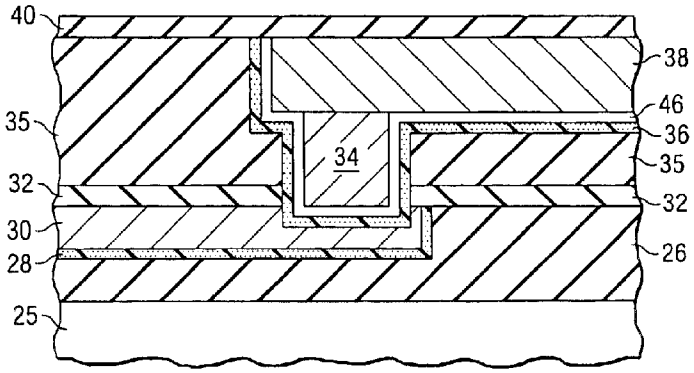
(57) **ABSTRACT**

Methods and compositions are disclosed for modifying a semiconductor interconnect layer to reduce migration problems while minimizing resistance increases induced by the modifications. One method features creating trenches in the interconnect layer and filling these trenches with compositions that are less susceptible to migration problems. The trenches may be filled using traditional vapor deposition methods, or electroplating, or alternately by using electroless plating methods. Ion implantation may also be used as another method in modifying the interconnect layer. The methods and compositions for modifying interconnect layers may also be limited to the via/interconnect interface for improved performance. A thin seed layer may also be placed on the semiconductor substrate prior to applying the interconnect layer. This seed layer may also incorporate similar dopant and alloying materials in the otherwise pure metal.

17 Claims, 3 Drawing Sheets



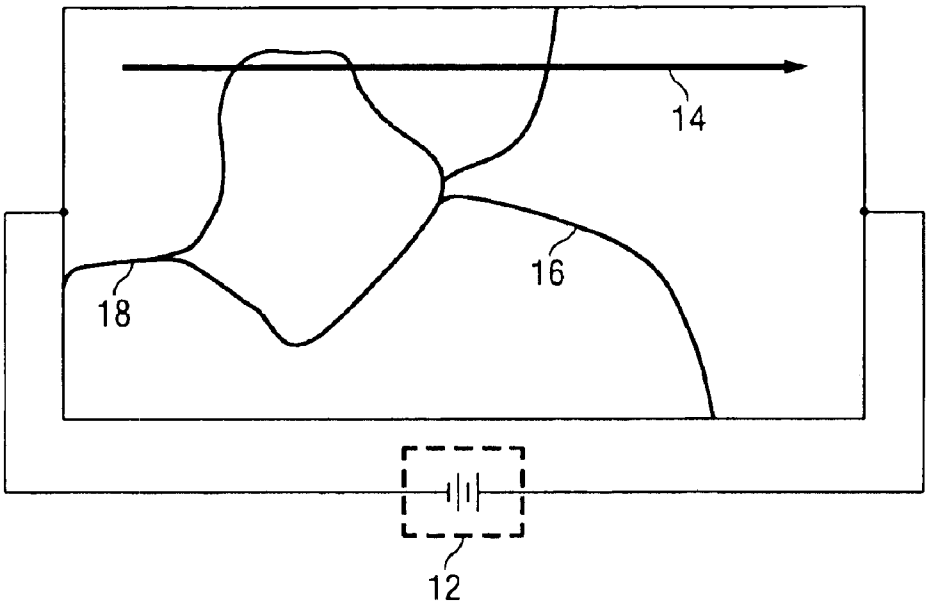


FIG. 1A
(PRIOR ART)

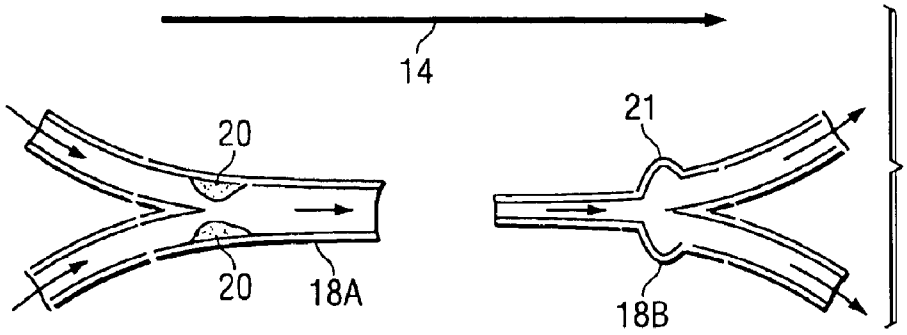


FIG. 1B
(PRIOR ART)

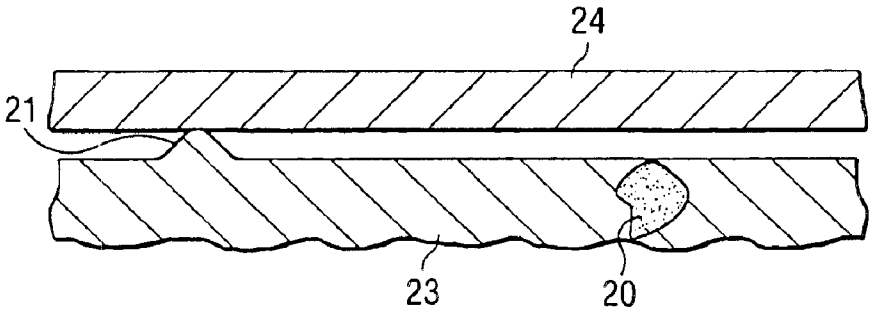


FIG. 2
(PRIOR ART)

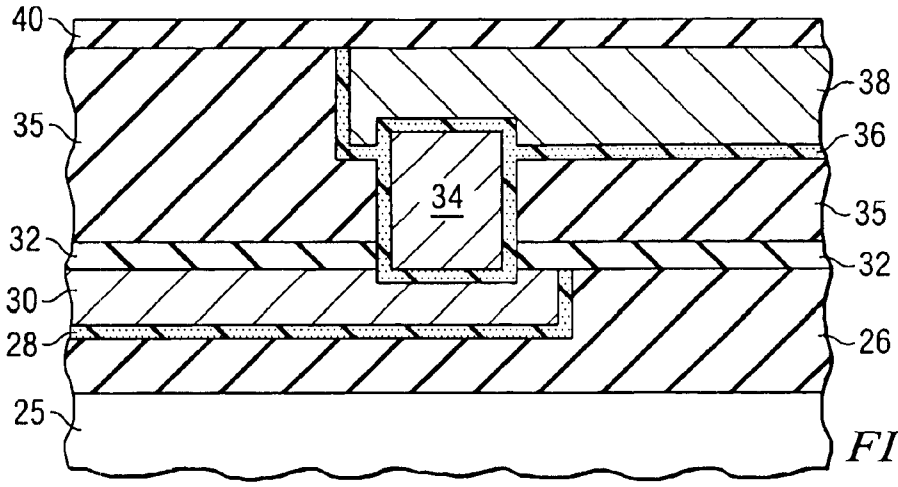


FIG. 3A

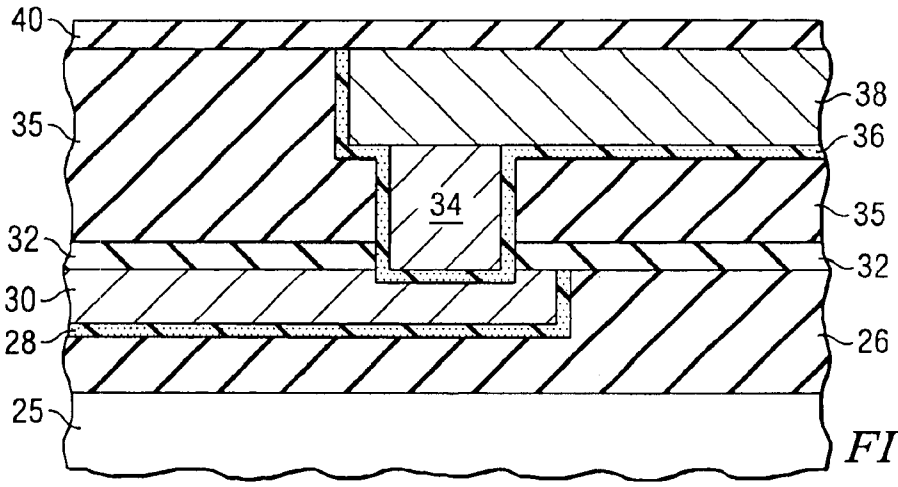


FIG. 3B

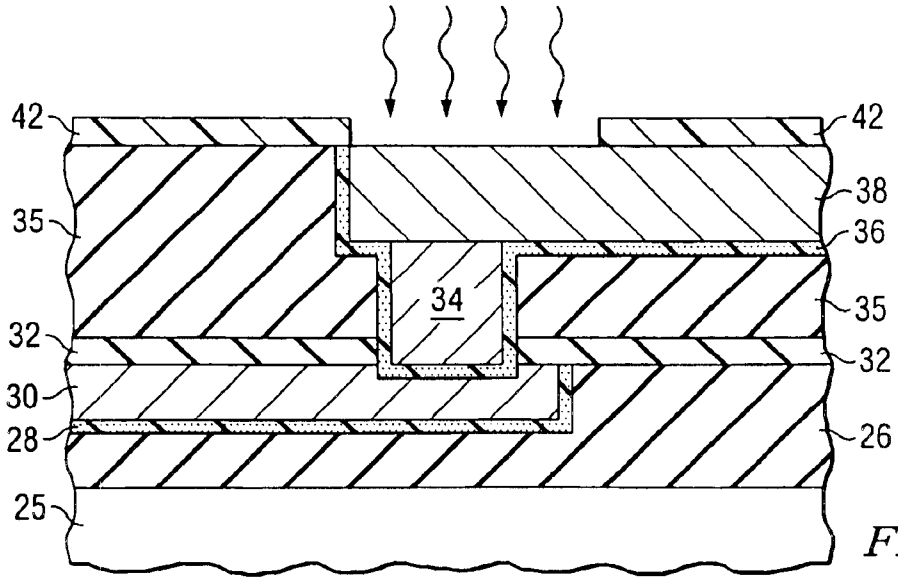


FIG. 4

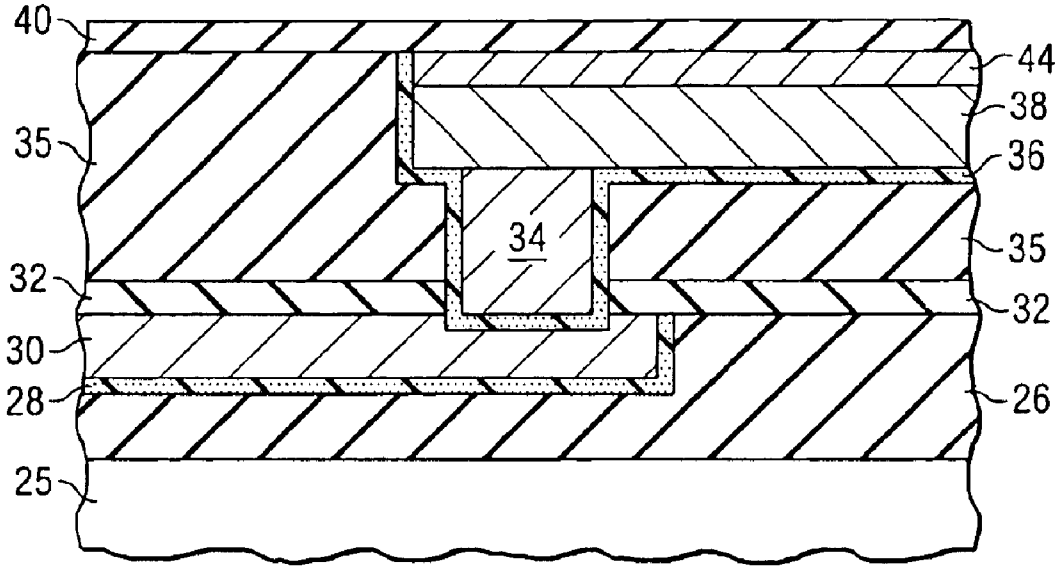


FIG. 5

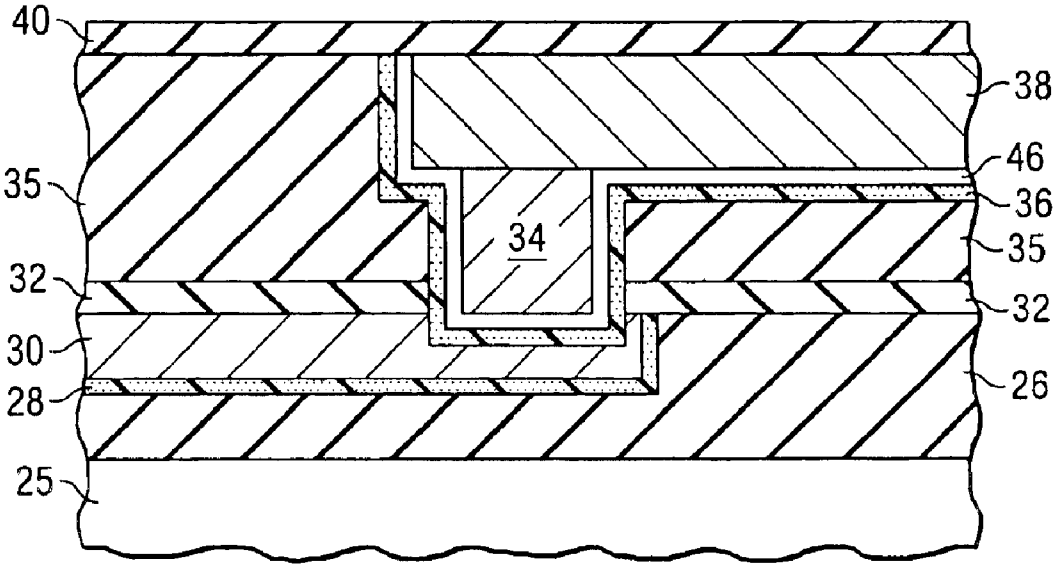


FIG. 6

LOCALIZED DOPING AND/OR ALLOYING OF METALLIZATION FOR INCREASED INTERCONNECT PERFORMANCE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is entitled to the benefit of a provisional patent application Ser. No. 60/392,715 filed Jun. 28, 2002.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not applicable.

BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

The present invention generally relates to semiconductor processing techniques. More particularly, the present invention relates to selective modification of the interconnects of an integrated circuit to achieve improved mechanical and electrical properties.

2. Description of Related Art

The semiconductor technology central to the modern integrated circuit ("IC") has been developing for over a century. In the late nineteenth century, the special properties of the semiconductor selenium were first observed and recognized. The field of semiconductor physics advanced rapidly and the first transistor was proposed in the 1930s. However, not until the late 1940s was a functional point contact transistor constructed. The IC, which employs a plurality of circuit elements in a monolithic semiconductor substrate rather than using discrete components, was first developed in the late 1950s by Jack Kilby at Texas Instruments, Inc. and by Robert Noyce at Fairchild Semiconductor Corporation.

Since the late 1950s, IC technology has evolved rapidly and has revolutionized virtually every industry and capacity in which ICs are used. Today's ICs frequently employ hundreds of thousands or even millions of transistors and highly complex, multi-layered architectures. The proliferation of electronics in general, and ICs in particular, has resulted in large part from the ability to increase circuit functionality while simultaneously reducing device cost and size. An important catalyst for these improvements has been advances in semiconductor processing technologies. Although a wide array of semiconductor companies and products exist, for the most part, semiconductor processing is completed through a series of common steps. Semiconductor processing begins with a wafer or substrate, upon which various processing techniques are used to construct circuit elements such as transistors, resistors and capacitors. The formation of circuit elements comprises a process called doping—i.e., deliberately introducing impurities into certain regions of the monolithic crystalline substrate. After the circuit elements are formed, a series of conductive and insulating layers are used to form connections, called interconnects, between the appropriate circuit elements.

As increasingly complex ICs utilize an increasing number of circuit elements, more electrical interconnects between circuit elements and a greater number of conductor-insulator layers are required. A chief objective of semiconductor processing is the minimization of interconnect electrical resistance. Increased resistance is undesirable because as the interconnect resistance between two electrical devices

overall speed at which the IC functions. Additionally, increased resistance also increases the amount of overall power consumed by the IC.

Another important consideration is the mechanical stability of the interconnects, which is negatively impacted by a phenomenon known as electromigration, the migration of atoms in the interconnect induced by applying an electric potential across the interconnect. The principle of electromigration is depicted graphically in FIGS. **1**A, **1**B and **2**. FIG. **1**A shows an electron flow **14** in a conductor **10** due to a potential difference supplied by a battery **12**. The momentum of the electrons in the electron flow **14** causes atoms in the conductor **10** to migrate in the same direction as the electron flow **14**. Grain boundaries occur at the intersection between two crystalline grains. The intersection of three or more crystalline grains may be susceptible to electromigration. Consequently, grain boundary **16** and intersection point **18** are likely places for electromigration damage, but usually at higher activation energy than surface diffusion in the case of Cu metallization.

FIG. **1**B shows electron flow **14** through grain boundary intersection points **18**A and **18**B. In intersection point **18**A, electron flow **14** from two grains is merging into a single grain, resulting in the formation of void **20**. In intersection point **18**B, in contrast, electron flow **14** from a single grain is diverging into two different grains, resulting in the formation of hillock **21**.

Conductors are often processed using aluminum with a small concentration (i.e., less than about 2% by weight), of Copper ("Cu"). More recently, pure Cu has been the metal of choice for producing metal interconnect on ICs. To contain the Cu and keep it from entering and moving within the glass dielectric layers and the active areas of the substrate, barrier layers surround the Cu. These barriers are carefully chosen so as to not cause adhesion problems between the metallization and the encapsulating/insulating dielectric layers. With the advancement of technology, new materials are sought to reduce parasitic capacitance and resistance for greater circuit performance and lower power consumption. These new materials possess lower dielectric constants but also lower thermal conductance. This reduces the efficiency with which heat is transferred to the substrate. Also, these material are more brittle and mechanically less robust than the more traditional silicone dioxide. Lower mechanical strength means less resistance to cracking and possibly a greater tendency toward electromigration, due to tensile forces on the metallization or lower strength in general. The surface between the Cu lead and the barrier is observed to be a path for metal movement of relatively low activation energy. Voids can nucleate and/or grow at this surface, and the other interfacial surfaces. Metal will electromigrate, that is, drift or diffuse in the direction of electron flow under electrical bias. Voids, depletion of metal in an area, can form near the electron source. These voids are usually paired downstream with hillocks, an accumulation of metal. Hillocks can cause the formation of metal filaments into the dielectric, that is, unwanted paths of current leakage, and even cracking of the barrier and/or dielectric.

The impact on circuit performance of void **20** and hillock **21** in FIG. **1** is depicted graphically in FIG. **2**. FIG. **2** shows interconnect **23** and parallel interconnect **24**, which is desirably electrically isolated from interconnect **23**. Proper circuit performance requires not only high electrical conductance along interconnect **23** and interconnect **24** but a high electrical resistance between them. Void **20** and hillock **21**

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