DEP/REF

Docket No.: 071971-0012 2007 MAR 21 PM 4:59 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mizuki SEGAWA, et al.	:	Confirmation Number: 5361
Application No.: 10/995,283 Patent No. 7,126,174 Issue Date: October 24, 2006	:	Group Art Unit: 2822
	:	Examiner: POTTER, Roy K.
Filed: November 24, 2004	:	

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

REQUEST FOR REFUND

Mail Stop Request for Refund
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A refund in the amount of $120.00 is hereby requested in the above-identified application for the following reason:

The Petition for Extension of Time in the amount of $120.00 filed on February 20, 2007 was inadvertently filed in this case.

Please immediately credit Deposit Account number 500417 in this amount.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Ramyar M. Farid
Registration No. 46,692
Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 RMF:MaM
Facsimile: 202.756.8087
Date: March 20, 2007

WDC99 1363893-1.071971.0012

Adjustment Date: 04/05/2007 MGEBREM1
02/26/2007 AWONDAF1 00000045 500417 10995283
01 FC:1251 120.00 CR

ATTENTION ATTENTION ATTENTION

Method of Refund:

- [ ] **ACH/EFT**
- [ ] **Credit Card**
- [x] **Deposit Account #** 50-0417
- [ ] **Treasury Check**

Patent/TM/App/Serial # 10/995,283

Program Area Tech Center 2822

Date Processed 3/27/2007

ATTENTION ATTENTION ATTENTION

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 5361

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/995,283	11/24/2004 RULE	257	2822	71971-012

APPLICANTS

Mizuki Segawa, Osaka, JAPAN;
Isao Miyanaga, Osaka, JAPAN;
Toshiki Yabu, Osaka, JAPAN;
Takashi Nakabayashi, Osaka, JAPAN;
Takashi Uehara, Osaka, JAPAN;
Kyoji Yamashita, Osaka, JAPAN;
Takaaki Ukeda, Osaka, JAPAN;
Masatoshi Arai, Osaka, JAPAN;
Takayuki Yamada, Osaka, JAPAN;
Michikazu Matsumoto, Osaka, JAPAN;

** **CONTINUING DATA** *************************

This application is a DIV of 10/454,682 06/05/2003 PAT 6,967,409
which is a DIV of 09/902,157 07/11/2001 PAT 6,709,950
which is a DIV of 08/685,726 07/24/1996 PAT 6,281,562

** **FOREIGN APPLICATIONS** ********************

JAPAN 7-192181 07/27/1995
JAPAN 7-330112 12/19/1995

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 01/21/2005

Foreign Priority claimed ☐ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged ____ Examiner's Signature Initials	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
	JAPAN	21	14	1

ADDRESS
20277

TITLE

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

FILING FEE RECEIVED		
1090	FEES: Authority has been given in Paper No. _________ to charge/credit DEPOSIT ACCOUNT No. _________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ____________

		☐ Credit

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

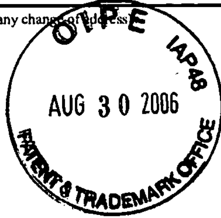
INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 07/17/2006

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, DC 20005-3096

"CUSTOMER NO.: 20277"



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/995,283	11/24/2004	Mizuki Segawa	71971-012	5361

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/17/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
POTTER, ROY KARL	2822	257-288000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 McDERMOTT WILL & EMERY LLP
2 ____
3 ____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

08/31/2006 MBERHE1 00000089 500417 10995283
01 FC:1501 1400.00 DA
02 FC:1504 300.00 DA
03 FC:8001 12.00 DA

(A) NAME OF ASSIGNEE: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): OSAKA, JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies FOUR

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 500417 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ____ Date August 30, 2006

Typed or printed name Michael E. Fogarty Registration No. 36,139

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 07/17/2006

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
POTTER, ROY KARL	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/17/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/995,283	11/24/2004	Mizuki Segawa	71971-012	5361

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/17/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

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Commissioner for Patents
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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/995,283	11/24/2004	Mizuki Segawa	71971-012	5361

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EXAMINER	ART UNIT	CLASS-SUBCLASS
POTTER, ROY KARL	2822	257-288000

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   - ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
   (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1 ____________________
   2 ____________________
   3 ____________________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies ____________________

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number ____________ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ____________________ Date ____________________

Typed or printed name ____________________ Registration No. ____________________

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/995,283	11/24/2004	Mizuki Segawa	71971-012	5361

7590 07/17/2006

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
POTTER, ROY KARL	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/17/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Notice of Allowability	**Application No.** 10/995,283	**Applicant(s)** SEGAWA ET AL.	
	Examiner Roy K. Potter	**Art Unit** 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment of 5/31/06*.
2. ☒ The allowed claim(s) is/are *39-43,45-47 and 49-60*.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☒ Certified copies of the priority documents have been received in Application No. *10454682* .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

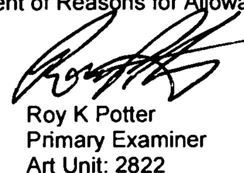
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.



Roy K Potter
Primary Examiner
Art Unit: 2822

SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 071971-0012	SERIAL NO. 10/995,283
	APPLICANT Mizuki SEGAWA, et al.	
	FILING DATE November 24, 2004	GROUP 2822

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US			
		US			
		US			
		US			
		US			
		US			
		US			
		US			
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		US			

FOREIGN PATENT DOCUMENTS

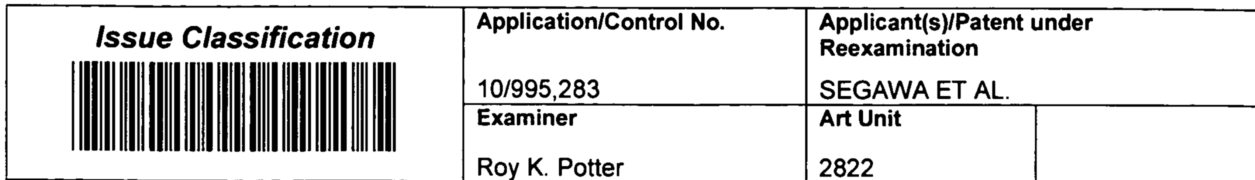
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3 -Number4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
[initials]		JP 06-21208	01/28/1994	Sony Corp.			
[initials]		JP 07-142726	06/02/1995	Oki Electric Ind. Co. Ltd.			
[initials]		JP 06-196495	07/15/1994	Matsushita Electric Ind. Co. Ltd.			
[initials]		JP 06-177237	06/24/1994	SGS Thomson Microelectron Inc.			
[initials]		JP 07-153939	06/16/1995	Oki Electric Ind. Co. Ltd.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

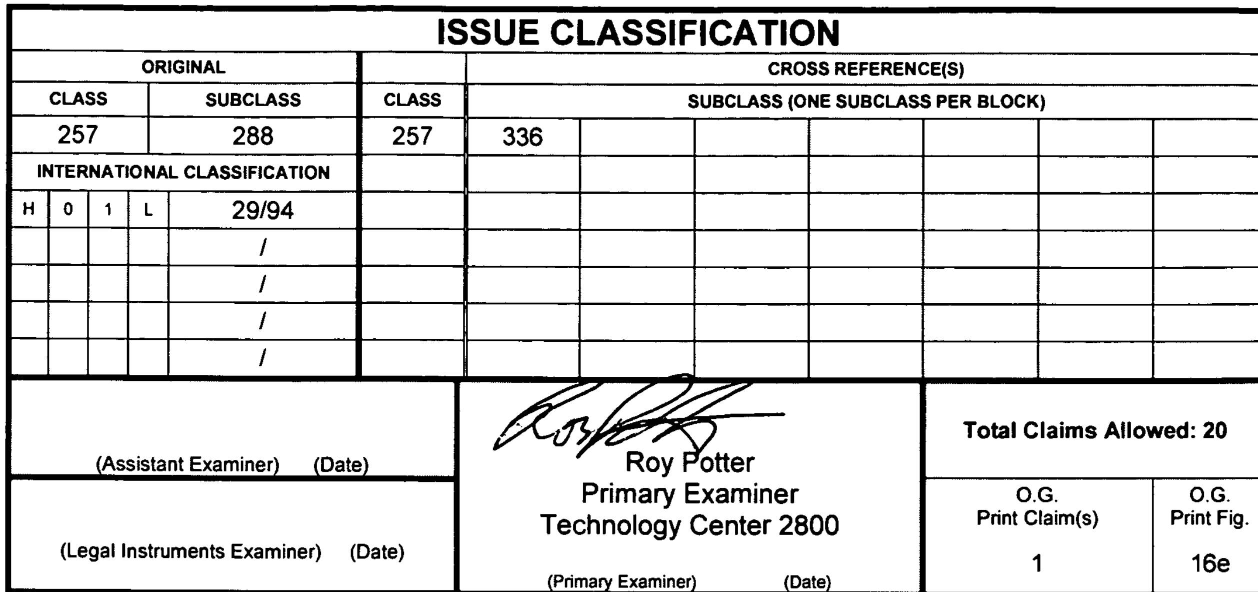
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	

EXAMINER [signature]	6/23/06 DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.



Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/995,283	SEGAWA ET AL.
	Examiner	Art Unit
	Roy K. Potter	2822



ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
257	288	257	336						

INTERNATIONAL CLASSIFICATION				
H	0	1	L	29/94
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(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

Roy Potter
Primary Examiner
Technology Center 2800

(Primary Examiner) (Date)

Total Claims Allowed: 20

O.G. Print Claim(s)	O.G. Print Fig.
1	16e

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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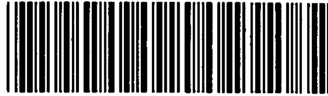
Search Notes 	Application/Control No. 10/995,283	Applicant(s)/Patent under Reexamination SEGAWA ET AL.	
	Examiner Roy K. Potter	Art Unit 2822	

SEARCHED			
Class	Subclass	Date	Examiner
257	384	6/24/2006	RP
257	336	6/24/2006	RP
257	288	6/24/2006	RP
257	333	6/24/2006	RP
257	396	6/24/2006	RP
257	386	6/24/2006	RP
257	401	6/24/2006	RP

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
257	**401,386**	6/25/2006	**RP**
	396,333	6/25/2006	**RP**
	336,288	6/25/2006	**RP**
257/384		6/25	**RP**

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST SEARACH	6/25/2006	RP

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 5361

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/995,283	11/24/2004 RULE	257	2822	71971-012

APPLICANTS

Mizuki Segawa, Osaka, JAPAN;
Isao Miyanaga, Osaka, JAPAN;
Toshiki Yabu, Osaka, JAPAN;
Takashi Nakabayashi, Osaka, JAPAN;
Takashi Uehara, Osaka, JAPAN;
Kyoji Yamashita, Osaka, JAPAN;
Takaaki Ukeda, Osaka, JAPAN;
Masatoshi Arai, Osaka, JAPAN;
Takayuki Yamada, Osaka, JAPAN;
Michikazu Matsumoto, Osaka, JAPAN;

** **CONTINUING DATA** *************************

This application is a DIV of 10/454,682 06/05/2003 PAT 6,967,409 which is a DIV of 09/902,157 07/11/2001 PAT 6,709,950
which is a DIV of 08/685,726 07/24/1996 PAT 6,281,562

** **FOREIGN APPLICATIONS** ********************

JAPAN 7-192181 07/27/1995
JAPAN 7-330112 12/19/1995

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 01/21/2005

Foreign Priority claimed: ☑ yes ☐ no 35 USC 119 (a-d) conditions met: ☑ yes ☐ no ☐ Met after Allowance Verified and Acknowledged: Examiner's Signature / Initials	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
	JAPAN	21	14	1

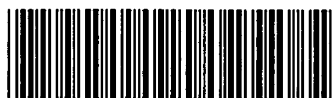
ADDRESS
McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, DC20005-3096

TITLE

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
790	No. _________ to charge/credit DEPOSIT ACCOUNT No. _________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue)

Index of Claims



Application/Control No.	Applicant(s)/Patent under Reexamination
10/995,283	SEGAWA ET AL.
Examiner	**Art Unit**
Roy K. Potter	2822

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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EAST Search History

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L2	1753	257/336	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L3	1732	257/288	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L4	485	257/333	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L5	410	257/396	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L6	279	257/386	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L7	238	257/389	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:23
L8	254145	"L shaped" or "L-shaped"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:23

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	909	257/384	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:21
L2	1753	257/336	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L3	1732	257/288	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L4	485	257/333	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L5	410	257/396	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L6	279	257/386	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:22
L7	238	257/389	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:23
L8	254145	"L shaped" or "L-shaped"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:23

EAST Search History

L9	5128	l1 or l2 or l3 or l4 or l5 or l6 or l7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:24
L10	83	l8 and l9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:24
L11	17693	sidewall and l8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:24
L12	49	l10 and l11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:33
L13	2149	257/401	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:34
L14	43	l8 and l13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:34

EAST Search History

L9	5128	l1 or l2 or l3 or l4 or l5 or l6 or l7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:24
L10	83	l8 and l9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:24
L11	17693	sidewall and l8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:24
L12	49	l10 and l11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/25 20:24

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004 6/14/06

Application or Docket Number: 10/995283

RCE **CLAIMS AS FILED - PART I**

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	14 minus 20=	* –
INDEPENDENT CLAIMS	1 minus 3 =	* –
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	150.00	OR	BASIC FEE	300.00
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL		OR	TOTAL	790 pd.

CLAIMS AS AMENDED - PART II

AMENDMENT A

6/14/06	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 20	Minus	** 20	=
Independent	* 1	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

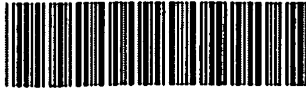
	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 10/04)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Index of Claims 	Application/Control No. 10/995,283	Applicant(s)/Patent under Reexamination SEGAWA ET AL.
	Examiner Roy K. Potter	Art Unit 2822

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Docket No.: 71971-012

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mizuki SEGAWA, et al.	:	Confirmation Number: 5361
Application No.: 10/995,283	:	Group Art Unit: 2822
Filed: November 24, 2004	:	Examiner: Roy K. POTTER

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

AMENDMENT

Mail Stop Amendment
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicant respectfully requests reconsideration in accordance with the filing of the RCE, amendments and remarks for the reasons set forth below.

AMENDMENT TO CLAIMS

Listing of Claims

Claims 1 – 38 (Cancelled)

39. (Currently amended) A semiconductor device, comprising:

[[an]] a trench isolation ~~insulating area~~ surrounding an active area of a semiconductor substrate;

a gate insulating film formed over the active area;

a gate electrode formed over the gate insulating film;

first L-shaped sidewalls formed over the side surfaces of the gate electrode; [[and]]

first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area

an interconnection formed on the trench isolation; and

second L-shaped sidewalls formed over the side surfaces of the interconnection.

40. (Previously presented) The semiconductor device of Claim 39, wherein the first L-shaped sidewalls are made of a silicon nitride film.

41. (Previously presented) The semiconductor device of Claim 39, further comprising first protection oxide films formed between the gate electrode and the first L-shaped sidewalls.

42. (Previously presented) The semiconductor device of Claim 39, further comprising a second silicide layer formed on the gate electrode.

43. (Previously presented) The semiconductor device of Claim 39, further comprising source/drain regions formed on both sides of the gate electrode within the active area,

wherein the first silicide layers are formed on the source/drain regions.

44. (Cancelled)

45. (Currently amended) The semiconductor device of Claim [[44]] 39, the second L-shaped sidewalls are made of a silicon nitride film.

46. (Currently amended) The semiconductor device of Claim [[44]] 39, further comprising second protection oxide films formed between the interconnection and the second L-shaped sidewalls.

47. (Currently amended) The semiconductor device of Claim [[44]] 39, further comprising a third silicide layer formed on the interconnection.

48. (Cancelled)

49. (Currently amended) The semiconductor device of Claim [[48]] 39, the trench isolation has an upper surface higher than the surface of the active area.

50. (Currently amended) The semiconductor device of Claim [[48]] 39, wherein a lower portion of the interconnection provided on the upper surface of the trench isolation is located higher than the surface of the active area.

51. (Currently amended) The semiconductor device of Claim [[44]] 39, wherein the interconnection is composed of the same material as the gate electrode.

52. (Currently amended) The semiconductor device of Claim [[51]] 39, wherein the gate electrode and the interconnection has at least a polysilicon film.

53. (New) The semiconductor device of Claim [[39]] 41, wherein a channel stop region of the same conductivity as that of the semiconductor substrate is formed below the trench isolation.

54. (New) The semiconductor device of Claim 39, wherein the first and second L-shaped sidewalls are made of the same insulating film.

55. (New) The semiconductor device of Claim 41, wherein the first protection oxide film is a CVD oxide film.

56. (New) The semiconductor device of Claim 43, wherein the source/drain regions include low-concentration source/drain regions and high-concentration source/drain regions, and the first silicide layers are formed on the high-concentration source/drain regions.

57. (New) The semiconductor device of Claim 46, wherein the second protection oxide film is a CVD oxide film.

58. (New) The semiconductor device of Claim 46, wherein the second protection oxide films are L-shaped films.

59. (New) The semiconductor device of Claim 39, wherein the first silicide layers are formed so as to be located apart from the trench isolations.

60. (New) The semiconductor device of Claim 56, wherein the source/drain regions are formed so as to be located apart from the trench isolations.

REMARKS

In the foregoing amendment, claims 39, 46, 47 and 49-52 have been amended and new claims 54-60 have been added to further clarify the intended subject matter of the present invention. No new matter has been added. In addition, claims 44 and 48 have been cancelled. Entry of the foregoing amendment is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:MaM
Facsimile: 202.756.8087
Date: May 31, 2006i

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WDC99 1239964-1.071971.0012

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Request for Continued Examination (RCE) Transmittal

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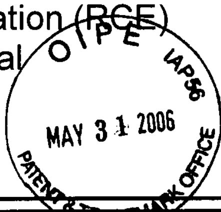

Application Number	10/995,283
Filing Date	November 24, 2004
First Named Inventor	Mizuki SEGAWA, et al.
Art Unit	2822
Examiner Name	POTTER, Roy K.
Attorney Docket Number	071971-0012

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Education (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on ________
      ii. ☐ Other ________

   b. ☒ Enclosed
      i. ☒ Amendment/Reply
      ii. ☐ Affidavit(s)/Declaration(s)
      iii. ☒ Information Disclosure Statement (IDS)
      iv. ☐ Other ________

2. Miscellaneous
   a. ☐ Suspension of action of the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   b. ☐ Other ________

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 500417. I have enclosed a duplicate copy of this sheet.
      i. ☒ RCE fee required under 37 CFR 1.17(e) $790
      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
      iii. ☐ Other ________
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Signature		Date	May 31, 2006
Name (Print/Type)	Michael E. Fogarty	Registration No.	36,139

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This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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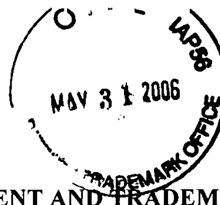

Docket No.: 071971-0012

PATENT

RCE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277

Mizuki SEGAWA, et al. : Confirmation Number: 5361

Application No.: 10/995,283 : Group Art Unit: 2822

Filed: November 24, 2004 : Examiner: POTTER, Roy K.

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an Amendment in the above-identified application.

☐ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	20	20	0	$50.00 =	$0.00
Independent Claims	1	3	0	$200.00 =	$0.00
		Multiple dependent claims newly presented			$0.00
		Fee for extension of time			$0.00
		RCE			$790.00
		Total of Above Calculations			$790.00

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Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:MaM
Facsimile: 202.756.8087
Date: May 31, 2006

WDC99 1240005-1.071971.0012

Docket No.: 071971-0012 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mizuki SEGAWA, et al.	:	Confirmation Number: 5361
Application No.: 10/995,283	:	Group Art Unit: 2822
Filed: November 24, 2004	:	Examiner: POTTER, Roy K.

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

INFORMATION DISCLOSURE STATEMENT

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Each non-English language reference was first cited in a corresponding foreign application search report or office action and its relevance discussed therein. A copy of the

foreign search report or office action, together with an English language version thereof, is attached for the Examiner's information.

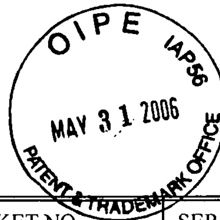
Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139
Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:MaM
Facsimile: 202.756.8087
Date: May 31, 2006



SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 071971-0012	SERIAL NO. 10/995,283
	APPLICANT **Mizuki SEGAWA, et al.**	
	FILING DATE **November 24, 2004**	GROUP **2822**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 *(if known)*		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Code5 *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	No
		JP 06-21208	01/28/1994	Sony Corp.			
		JP 07-142726	06/02/1995	Oki Electric Ind. Co. Ltd.			
		JP 06-196495	07/15/1994	Matsushita Electric Ind. Co. Ltd.			
		JP 06-177237	06/24/1994	SGS Thomson Microelectron Inc.			
		JP 07-153939	06/16/1995	Oki Electric Ind. Co. Ltd.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

PATENT ABSTRACTS OF JAPAN

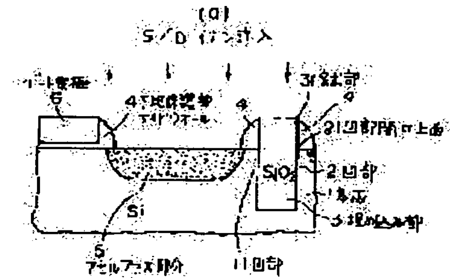
(11)Publication number : 06-021208
(43)Date of publication of application : 28.01.1994

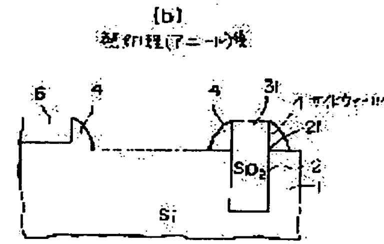
(51)Int.CI. H01L 21/76

(21)Application number : 04-078348
(22)Date of filing : 28.02.1992
(71)Applicant : SONY CORP
(72)Inventor : TOKUNAGA KAZUHIKO

(54) SEMICONDUCTOR DEVICE AND BURYING METHOD OF RECESSED PART ON SUBSTRATE

(57)Abstract:
PURPOSE: To provide a semiconductor device wherein a defect is not caused near a recessed part and a trouble that a leakage current becomes large or the like is not caused when a heat treatment is executed after various kinds of substrate treatments (ion implantation and the like) have been executed and to provide a method wherein a recessed part on a substrate is buried.
CONSTITUTION: (1) In a semiconductor device, a burying material is buried in a recessed part 2 on a substrate 1 and buried parts 3, 3a, 3b are formed. In the semiconductor device, each buried part is formed as a structure in which it protrudes from the opening surface of the recessed part and in which sidewalls 4 are formed on side parts of a protrusion part 31. (2) In a method, a recessed part on a substrate is buried. The method is provided with a process wherein a substrate treatment is executed and, after that, a heat treatment is executed after having executed a process wherein a burying material is buried in the recessed part on the substrate. In the method wherein the burying material is formed as a structure in which the burying material protrudes from the opening surface of the recessed part, substrate protective parts 4 are formed on side parts of the protrusion part, the subatrate treatment is executed and the recessed part is buried.





LEGAL STATUS

[Date of request for examination]	23.02.1999
[Date of sending the examiner's decision of rejection]	19.06.2001
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3277383
[Date of registration]	15.02.2002
[Number of appeal against examiner's decision of rejection]	2001-12625
[Date of requesting appeal against examiner's decision of rejection]	19.07.2001
[Date of extinction of right]	

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(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平6－21208

(43)公開日　平成6年(1994)1月28日

(51)Int.Cl.⁵	識別記号	庁内整理番号	F I	技術表示箇所
H01L　21/76	L	9169－4M		

審査請求　未請求　請求項の数2(全　6　頁)

(21)出願番号　特願平4－78348

(22)出願日　平成4年(1992)2月28日

(71)出願人　000002185
ソニー株式会社
東京都品川区北品川6丁目7番35号

(72)発明者　徳永　和彦
東京都品川区北品川6丁目7番35号　ソニー株式会社内

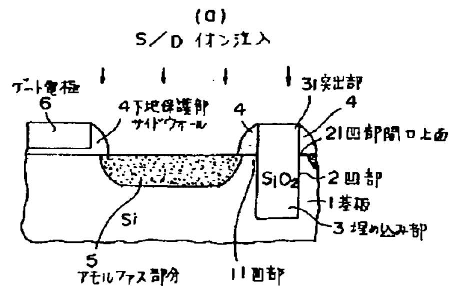
(74)代理人　弁理士　高月　亨

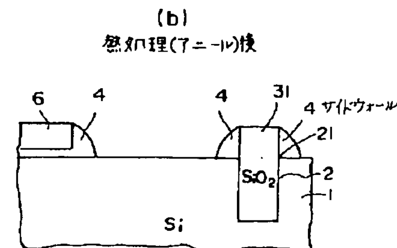
(54)【発明の名称】　半導体装置及び基板上の凹部の埋め込み方法

(57)【要約】

【目的】　各種の基板処理（イオン注入など）の処理を行った後、熱処理を行う場合についても、凹部近傍に欠陥が生じず、リーク電流が大きくなるなどの不都合の生じない半導体装置、及び基板の凹部の埋め込み方法を提供する。

【構成】　①基板１上の凹部２に埋め込み材料を埋め込んで埋め込み部３，３ａ，３ｂを形成した半導体装置であって、該埋め込み部は凹部の開口上面よりも突出する構成で形成し、該突出部３１の側部にはサイドウォール４を形成した構成の半導体装置。②基板上の凹部に埋め込み材料を埋め込む工程を行った後、基板処理を行い、その後熱処理を施す工程を備える基板上の凹部の埋め込み方法において、埋め込み材料を凹部の開口上面よりも突出する構成で形成し、この突出部の側部に下地保護部４を形成し、その後基板処理を行う凹部の埋め込み方法。





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【特許請求の範囲】
【請求項1】基板上の凹部に埋め込み材料を埋め込んで埋め込み部を形成した半導体装置であって、
該埋め込み部は凹部の開口上面よりも突出する構成で形成し、
該突出部の側部にはサイドウォールを形成した構成であることを特徴とする半導体装置。
【請求項2】基板上の凹部に埋め込み材料を埋め込む工程を行った後、基板処理を行い、その後熱処理を施す工程を備える基板上の凹部の埋め込み方法において、
埋め込み材料を凹部の開口上面よりも突出する構成で形成し、
この突出部の側部に下地保護部を形成し、
その後基板処理を行うことを特徴とする基板上の凹部の埋め込み方法。
【発明の詳細な説明】
【0001】
【産業上の利用分野】本発明は、半導体装置、及びこの半導体装置の製造に用いることができる基板上の凹部の埋め込み方法に関する。
【0002】
【従来の技術】半導体装置等の形成の際、基板に形成した凹部に埋め込み材料を埋め込み、各種の構造を形成することが行われている。例えば、トレンチアイソレーションの形成、トレンチキャパシタの形成、埋め込み配線（プラグ）の形成などである。
【0003】ところで、基板には各種の処理、例えばイオン注入などの処理が施される。更に、基板には熱処理が行われることが多い。
【0004】ところが、上記のように凹部を埋め込む構成のものについては、上記基板処理、及び熱処理により、凹部に欠陥が生じることがある。
【0005】以下に、この問題について、アスペクト比の大きいトレンチ（溝）を埋め込んで素子分離を行う構成の半導体基板を形成する場合で、かつ、基板には基板処理としてイオン注入を行い、更に熱処理を行う場合を例にとって説明する。
【0006】図5（a）に示すように、基板1上に形成した凹部2（トレンチ）を絶縁材で埋め込んで埋め込み部3を形成し、これを素子分離として用いる場合、ソース／ドレイン（S／D）形成のためのイオン注入（図5（a））を行った後、熱処理（アニール）を行う（図5（b））と、図5（b）に略示するように、凹部2のコーナー部に欠陥Dが生じることがある（なお図中、6はゲート、61はLDD形成用のサイドウォールである）。即ち、一般に半導体装置形成の際に行われているように、通常のLDD（Ｌｉｇｈｔｌｙ　Ｄｏｐｅｄ　Ｄｒａｉｎ）構造のトランジスタを形成後、ソース／ドレイン領域形成のための高濃度の不純物の注入（イオン注入）を行い、シリコンのアモルファス化した部分5を

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形成し（図5（a）参照）、その後拡散層活性化のためのアニール（回復アニール）を行うと、トレンチコーナーのエッヂに図5（b）に示したように欠陥Dが発生する傾向がある。この原因は、以下の理由によるものと考えられる。
【0007】①ソース／ドレインイオン注入時のダメージと、埋め込み材料（例えばSiO_2）の応力の相乗により、欠陥が生じる。
②固相成長過程で、結晶方位（例えば（100）の方向での成長）であるとか、結晶性の問題で、アモルファス化する部分5において、トレンチコーナーのエッヂが最後に固相成長するため、ここでミスフィット、つまりアモルファス化する時にエッヂ部がしわよせを受ける如く成長することになる現象を起こし、これが欠陥となる。
【0008】このため、この欠陥部Dでリーク電流が発生しやすくなる。一般に、上記のように凹部2を埋め込んで素子分離を行う構成にあっては、リーク電流は、通常のLOCOS構造の素子分離に比べ、1～2桁多い。
【0009】
【発明の目的】本発明は、上記問題点を解決して、各種の基板処理、例えばイオン注入などの処理を行った後、熱処理を行う場合についても、凹部近傍に欠陥が生じず、リーク電流が大きくなるなどの不都合の生じない半導体装置、及び基板の凹部の埋め込み方法を提供しようとするものである。
【0010】
【問題点を解決するための手段】本出願の請求項1の発明は、基板上の凹部に埋め込み材料を埋め込んで埋め込み部を形成した半導体装置であって、該埋め込み部は凹部の開口上面よりも突出する構成で形成し、該突出部の側部にはサイドウォールを形成した構成であることを特徴とする半導体装置であって、これにより上記目的を達成するものである。
【0011】本出願の請求項2の発明は、基板上の凹部に埋め込み材料を埋め込む工程を行った後、基板処理を行い、その後熱処理を施す工程を備える基板上の凹部の埋め込み方法において、埋め込み材料を凹部の開口上面よりも突出する構成で形成し、この突出部の側部に下地保護部を形成し、その後基板処理を行うことを特徴とする基板上の凹部の埋め込み方法であって、これにより上記目的を達成するものである。
【0012】
【作用】本発明によれば、埋め込み部の突出部の側壁にサイドウォールを形成し、これが下地保護部となるので、基板処理の際にその下地部分が欠陥を生じ得る状態になることが防がれる。この結果、欠陥の生じないように凹部の埋め込み7が達成され、また欠陥のない半導体装置が得られる。
【0013】
【実施例】以下本発明の実施例について、図面を参照し

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て説明する。但し当然のことではあるが、本発明は以下の実施例により限定を受けるものではない。

【0014】実施例1

本実施例は、凹部の埋め込みによりトレンチアイソレーション（溝型素子分離）を形成する場合であって、かつ、基板処理としてソース／ドレイン領域形成用のイオン注入を行い、更に熱処理として回復アニールを行う場合について、本発明を適用したものである。

【0015】図1を参照する。本実施例の方法にあっては、基板1上の凹部2に埋め込み材料を埋め込む工程を行って埋め込み部3を形成した後、ここではイオン注入である基板処理を行い（図1（a））、その後熱処理（ここではアニール、図1（b））を施す工程を備える基板1上の凹部2の埋め込み方法において、埋め込み材料を凹部2の開口上面21よりも突出する構成で形成して埋め込み部3を形成し、この埋め込み部3の突出部31の側部に下地保護部（サイドウォール）4を形成し、その後イオン注入である基板処理や、アニールである熱処理を行うものである。

【0016】得られた半導体装置は、図1（b）に示すように、基板1上の凹部2に埋め込み材料を埋め込んで埋め込み部3を形成した半導体装置であって、該埋め込み部3は凹部2の開口上面21よりも突出する構成で形成し、該突出部31の側部にはサイドウォール4を形成した構成になる。

【0017】本実施例は、凹部2であるトレンチコーナーのエッヂ11にソース／ドレイン領域形成用イオン注入時のダメージが加わらないようにするものであり、具体的には上記したように、トレンチの埋め込みSiO_2（埋め込み材料3）の高さが、Si基板表面（凹部開口21）より高くなるように形成し、LDD構造のトランジスタを作るとき、トレンチの埋め込みSiO_2の側面にも、同時にサイドウォールを形成する。こうすれば、ソース／ドレイン領域形成のためのイオン注入時に、トレンチコーナーのエッヂにはダメージが加わらず、アモルファス化もしないので、結晶回復時に欠陥も発生しない。なおこの例のように、LDD形成のためのサイドウォール形成と保護部としてのサイドウォール4形成とを同時に行うことは、好ましい態様である。

【0018】本実施例により、図2（A）に示すようなアモルファス化部分5が形成され、コーナー部に不都合をもたらすおそれのある図2（B）に示すアモルファス化部分5（コーナー部11にかかる）の生成が防止できる。

【0019】このように図1（a）の如くトレンチの埋め込みSiO_2（埋め込み部3）の高さがSi基板1表面より高くなるように形成し、LDD構造のトランジスタを作る時、埋め込みSiO_2の側面にも同時にサイドウォールを形成するようにしたので、次の作用がもたらされる。

【0020】（1）トレンチコーナー11は、イオン注入時のダメージが無いので、当然欠陥は発生しない。

（2）イオン注入後の固相成長では、トレンチコーナーの単結晶部分が種結晶となるので、アモルファス領域は単結晶で回復する。

【0021】より具体的には、本実施例においては、図2（a）〜（h）に示す工程を行った。

【0022】まず、図3（a）に示すように、基板1であるSi基板上に、熱酸化により酸化膜12を形成し（例えば10〜20nm）、更にCVD等により、PolySi13を形成する（例えば100〜300nm）。

【0023】次に、通常のリソグラフィー技術を用いて、RIEにより、素子分離領域形成用の凹部2（トレンチ）を形成し、図3（b）の構造とする。

【0024】次に、埋め込み材料を埋め込んで埋め込み部3を形成し、図3（c）の構造とする。埋め込み材料は、トレンチアイソレーションを形成できるものなら任意であり、SiO_2やBPSGその他の不純物含有ガラス（平坦化材料）を用いることができ、例えばバイアスECR−CVDでSiO_2を埋め込んだり、あるいは各種手段でポリSiや不純物含有ガラスを埋め込み、平坦化することができる。ここではSiO_2を埋め込んで、図3（c）の構造とした。

【0025】次に、RIEにより、PolySi13、酸化膜12であるSiO_2を除去する。これにより、図3（d）に示すように、埋め込み部3が、基板1の表面である凹部2の開口上面21よりも高く、突出部31を有する構成で得られる。突出部の突出の大きさ、つまり開口上面21より上に出っぱる高さは、PolySi13の膜厚により調整できる。

【0026】次に、熱酸化膜14、PolySiCVD膜を形成し、更にフォトリソグラフィー工程、つまりレジスト工程及びRIEにより、通常のポリシリコンゲート電極15を形成する。これによって、図3（e）の構造を得る。

【0027】次に、一般的な手法に従い、SiO_2−CVDとRIEにより、ゲート電極をなすPolySi15の側壁に通常のサイドウォール41を形成する。この時、素子分離のSiO_2である埋め込み材料3は、突出部31が形成されている結果、ゲート電極と同程度位、上に出っぱっているので、この横にもサイドウォール4が形成される。このサイドウォールを、下地保護部として用いる。

【0028】即ち、上記保護部4となるサイドウォール、及びポリシリコン電極15のサイドウォールー41形成後、通常のソース／ドレイン領域形成用イオン注入を行うと、図3（g）に示すように、アモルファス領域となったアモルファス部5が形成される。ここで、下地保護部4となるサイドウォールが形成されているので、

図の（A）の領域（トレンチコーナーのエッヂ）は、イオン注入によるダメージを受けず、完全な単結晶のままである。

【0029】その後、熱処理である回復アニールを行う。図3（h）に示すように、5′で示す如く結晶の回復が行われ、上記図3（g）で説明したところから、欠陥の無い構造が得られることになる。

【0030】ここで、埋め込み部3の突出部31の高さ、つまりここでは埋め込みSiO_2の高さ（Si基板表面から出っぱる高さ）の適正値は、ソース／ドレイン領域形成用イオン注入の条件（イオン種、エネルギー、ドーズ量）により異なる。一般に、このイオン注入によりSi基板がアモルファス化される深さより、高くすれば良い。

【0031】例えば、以下の表1に示す如くである。

【表1】

ソース／ドレイン用イオン注入条件	アモルファス部の深さ	埋め込みSiO_2の高さ
As 20keV 5E15 cm^{-2}	40～45　nm	45nm以上
As 50keV 5E15 cm^{-2}	85～90　nm	90nm以上

【0032】実施例2

本実施例では、埋め込み材料として、PolySiを用いた。即ち図4に示すように、PolySiから成る埋め込み部3bを凹部2内に形成し、その周囲はSiO_2部3aとした。その他は実施例1と同様にして、同様の効果を得た。

【0033】

【発明の効果】本出願の発明によると、凹部の埋め込み構造を備える構成の基板について各種の基板処理、例えば、イオン注入などの処理を行った後、熱処理を行う場合についても、凹部近傍に欠陥が生じず、リーク電流が大きくなるなどの不都合の生じない半導体装置、及び基板の凹部の埋め込み方法を提供することができる。

【図面の簡単な説明】

【図1】実施例1の工程の概略を示す図である。

【図2】本発明の作用説明のための図である。

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【図3】実施例1の工程を示す図である。

【図4】実施例2を示す図である。

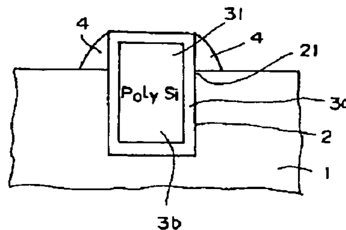
【図5】従来技術を示す図である。

【符号の説明】

1	基板
2	凹部
3，3a，3b	埋め込み部
31	突出部
4	下地保護部（サイドウォール）
5	アモルファス部分

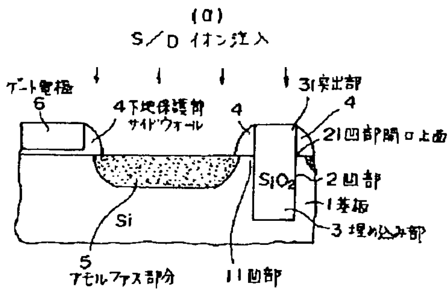
【図4】

実施例2

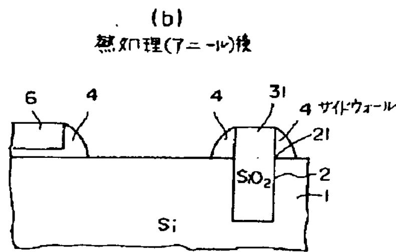


【図1】

(a)
S／D イオン注入



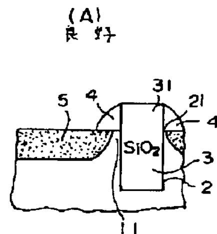
(b)
熱処理(アニール)後



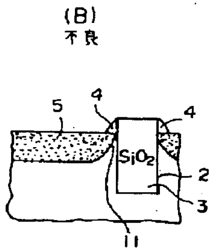
【図2】

作用説明図

(A)
良好



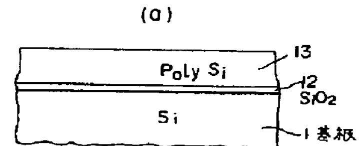
(B)
不良



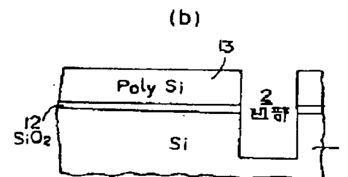
【図3その1】

実施例1の工程

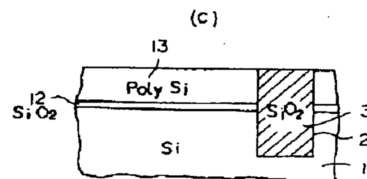
(a)



(b)

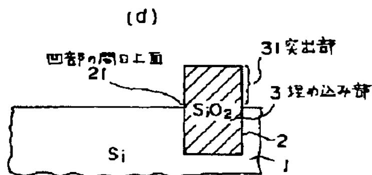


(c)

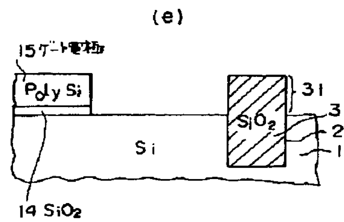


【図3その2】

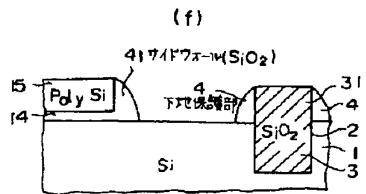
(d)



(e)

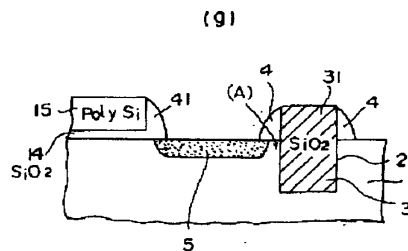


(f)

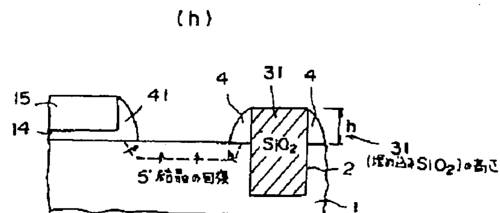


【図3その3】

(g)

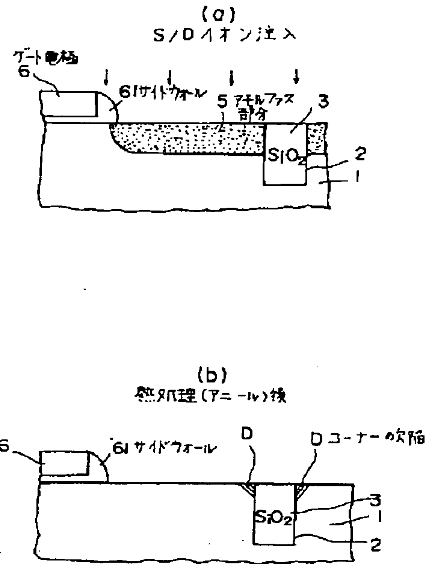


(h)



【図5】

従来技術



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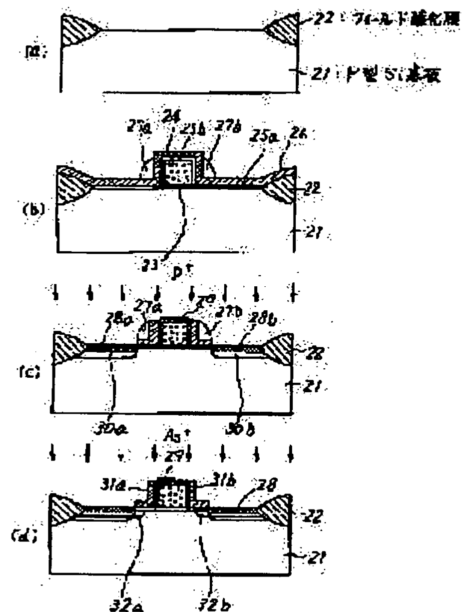
(71)Applicant : OKI ELECTRIC IND CO LTD
(72)Inventor : WAKAMATSU HIDETOSHI

(54) MANUFACTURE OF FIELD EFFECT TRANSISTOR

(57)Abstract:
PURPOSE: To provide a manufacturing method for FETs capable of suppressing leakage currents, parasitic resistances, the short channel effect and the hot carrier effect.
CONSTITUTION: A gate electrode 24 is formed on a semiconductor substrate, and on its sides double walls 31a, 31b, and 27a, 27b are formed. Using these double side walls as masks, deep n- diffusion layers 30a and 30b are formed in source and drain regions. Then only side walls 27a and 27b are removed by etching leaving the L-shaped side walls 31a and 31b unremoved, and shallow n+ diffusion layers 32a and 32b are formed in the source and drain regions. Next the L-shaped side walls 31a and 31b are removed by etching, and an n- layer for LDD is formed by ion implantation using the gate electrode 24 as a mask. Besides, a layer insulating film is formed and heat treatment is performed for smoothing it and activating the source and drain diffusion layers. Gate electrode wiring and laminated metal wiring containing barrier metals are brought into contact.



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(71)出願人　000000295
沖電気工業株式会社
東京都港区虎ノ門１丁目７番12号

(72)発明者　若松　秀利
東京都港区虎ノ門１丁目７番12号　沖電気工業株式会社内

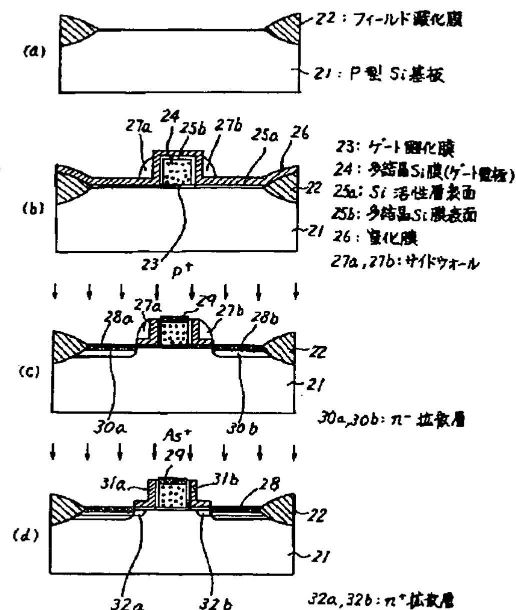
(74)代理人　弁理士　清水　守　（外１名）

(54)【発明の名称】　電界効果型トランジスタの製造方法

(57)【要約】　（修正有）

【目的】　漏れ電流、寄生抵抗、短チャネル効果及びホットキャリア効果を抑制したＦＥＴの製法を提供する。

【構成】　半導体基板上にゲート電極２４、その側面に３１ａ，３１ｂ、及び２７ａ，２７ｂの２重サイドウォールを形成し、この２重サイドウォールをマスクにしてソース・ドレイン領域に深いｎ－ 拡散層３０ａ，３０ｂを形成する。サイドウォール２７ａ，２７ｂだけをエッチング除去し、Ｌ型サイドウォール３１ａ，３１ｂは残して、ソース・ドレイン領域に浅いｎ+拡散層３２ａ，３２ｂを形成し、次にＬ型サイドウォール３１ａ，３１ｂをエッチング除去し、ゲート電極２４をマスクにしイオン注入法により、ＬＤＤ用ｎ－ 層を形成する。また層間絶縁膜を形成し、その平滑化と、ソース・ドレイン拡散層の活性化のために熱処理を行う。ゲート電極配線とバリアメタルを含む積層メタル配線とコンタクトをとる。



【特許請求の範囲】

【請求項1】　サリサイド構造を有する電界効果型トランジスタの製造方法において、

（a）半導体基板上のアクティブ領域にゲート電極を形成する工程と、

（b）該ゲート電極の側面に第1のL型サイドウォール及びその上に堆積される第2のサイドウォールを有する2重サイドウォールを形成する工程と、

（c）ソース・ドレイン領域及び前記ゲート電極上に高融点金属シリサイド膜を形成する工程と、

（d）前記2重サイドウォールをマスクにしてソース・ドレイン領域に深い接合の不純物拡散層を形成する工程と、

（e）前記2重サイドウォールの第2のサイドウォールをエッチング除去し、前記第1のL型サイドウォールを残した状態で、ソース・ドレイン領域に浅い接合の不純物拡散層を形成する工程と、

（f）前記第1のL型サイドウォールをエッチング除去し、ゲート電極をマスクにして大斜角斜め回転イオン注入法により、LDD用の不純物拡散層を形成する工程と、

（g）多層の層間絶縁膜を形成し、該層間絶縁膜の平滑化と、ソース・ドレイン拡散層を活性化するための熱処理を行う工程と、

（h）ゲート電極配線とソース・ドレイン領域をバリアメタルを含む積層メタル配線とコンタクトをとる工程とを順に施すことを特徴とする電界効果型トランジスタの製造方法。

【請求項2】　サリサイド構造を有する電界効果型トランジスタの製造方法において、

（a）半導体基板上のアクティブ領域にゲート電極を形成する工程と、

（b）該ゲート電極の側面に幅の広いサイドウォールを形成する工程と、

（c）ソース・ドレイン領域及び前記ゲート電極上に高融点金属シリサイド膜を形成する工程と、

（d）前記サイドウォールをマスクにしてソース・ドレイン領域に深い接合の不純物拡散層を形成する工程と、

（e）前記サイドウォールをエッチング除去し、ソース・ドレイン領域に浅い接合の不純物拡散層を形成する工程と、

（f）ゲート電極をマスクにして大斜角斜め回転イオン注入法により、LDD用の不純物拡散層を形成する工程と、

（g）多層の層間絶縁膜を形成し、該層間絶縁膜の平滑化と、ソース・ドレイン拡散層を活性化するための熱処理を行う工程と、

（h）ゲート電極配線とソース・ドレイン領域をバリアメタルを含む積層メタル配線とコンタクトをとる工程とを順に施すことを特徴とする電界効果型トランジスタの製造方法。

【請求項3】　サリサイド構造を有する電界効果型トランジスタの製造方法において、

（a）半導体基板上のアクティブ領域にゲート電極を形成する工程と、

（b）該ゲート電極の側面に第1のL型サイドウォール及びその上に堆積される第2のサイドウォールを有する2重サイドウォールを形成する工程と、

（c）ソース・ドレイン領域及び前記ゲート電極上に高融点金属シリサイド膜を形成する工程と、

（d）前記2重サイドウォールをマスクにしてソース・ドレイン領域に深い接合の不純物拡散層を形成する工程と、

（e）前記2重サイドウォールの第2のサイドウォールをエッチング除去し、前記第1のL型サイドウォールを残した状態で、ソース・ドレイン領域に浅い接合の不純物拡散層を形成する工程と、

（f）前記第1のL型サイドウォール及びゲート電極をマスクにして大斜角斜め回転イオン注入法により、LDD用の不純物拡散層を形成する工程と、

（g）多層の層間絶縁膜を形成し、該層間絶縁膜の平滑化と、ソース・ドレイン拡散層を活性化するための熱処理を行う工程と、

（h）ゲート電極配線とソース・ドレイン領域をバリアメタルを含む積層メタル配線とコンタクトをとる工程とを順に施すことを特徴とする電界効果型トランジスタの製造方法。

【請求項4】　前記LDD用の不純物拡散層を形成した後にゲート電極及びソース・ドレイン領域全面をN_2あるいはNH_3ガス雰囲気中で窒化することを特徴とする請求項1、2又は3項記載の電界効果型トランジスタの製造方法。

【請求項5】　前記多層の層間絶縁膜は、下層から順にシリコン酸化膜、シリコン窒化膜、シリコン酸化膜及び不純物を含むシリコン酸化膜の4層からなることを特徴とする請求項1、2又は3項記載の電界効果型トランジスタの製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、電界効果型トランジスタの製造方法に係り、、特に、MOSFETを有するCMOSデバイスの、主としてそのnチャネルMOSFETの製造方法に関するものである。

【0002】

【従来の技術】近年、半導体素子の微細化が進み、それとともに、MOSFETが縮小化されるにしたがい、そのゲート長が短くなり、また、短チャネル効果を抑制するため、ソース・ドレイン領域の接合深さ（xj）は浅くせざるを得なくなってきている。

【0003】このように、ゲート長が短くなり、MOS

ＦＥＴのオン抵抗は下がり、一方でｘｊが浅くなるため、ソース・ドレインのシート抵抗は増大する。したがって、ゲート長がサブミクロン領域のＭＯＳＦＥＴでは、ソース・ドレインのシート抵抗が、ＭＯＳＦＥＴのオン抵抗に対して無視し得なくなり、ＭＯＳＦＥＴの駆動力が、ソース・ドレイン領域の寄生抵抗により低下する問題が顕著となる。

【０００４】かかる問題に対してソース・ドレイン及びゲートを自己整合的でシリサイド化し、シート抵抗を下げるためにサリサイド技術が存在している。図３はかかる従来のサリサイド構造を有するＭＯＳＦＥＴの製造工程断面図である。

（１）まず、図３（ａ）に示すように、Ｐ型１００Ｓｉ基板１上の一部に、通常のホトリソグラフィ（以下、ホトリソと略す）とエッチング及びイオン注入法を用いて、Ｎ型不純物（リン等）を導入し、Ｎウエル領域２を形成する。次に、通常のＬＯＣＯＳ法により、フィールド酸化膜３を形成する。ドライ酸化雰囲気中で熱酸化し、Ｓｉ基板１表面にゲート酸化膜４を形成し、ゲート電極となる多結晶シリコン膜を全面に堆積し、通常のホトリソ・エッチング技術を用いたゲート電極５のパターニングを行う。

【０００５】通常のホトリソ工程により、Ｐｃｈ（Ｐチャネル）ＭＯＳＦＥＴ形成領域をホトレジスト６で被い、全面にＬＤＤ（Ｌｉｇｈｔｌｙ　Ｄｏｐｅ）層（低濃度拡散層）n^- 層７となるリンまたはヒ素を、加速エネルギー３０～５０ｋｅＶで$1〜4×10^{13}$ｉｏｎｓ／cm^2 イオン注入法により注入することで、Ｎｃｈ（ＮチャネルＭＯＳＦＥＴ領域のみn^- 層７を形成する。

【０００６】次いで、全面に常圧ＣＶＤ（化学的気相成長）法により、シリコン酸化膜もしくはボロン、リン等を含むシリコン酸化膜を形成し、異方性イオンエッチング法により、図３（ｂ）に示すように、ゲート電極５側壁にサイドウォール膜８を形成する。次いで、上記と同様に、ホトレジストにより、ＰｃｈＭＯＳＦＥＴ、ＮｃｈＭＯＳＦＥＴ側を各々被い、Ｎｃｈ側、Ｐｃｈ側に各々イオン注入法により、ソース・ドレイン領域となる不純物のヒ素打ち込み領域９（n^+ 層）及びボロン打ち込み領域９′（p^+ 層）を注入する。

【０００７】次に、図３（ｃ）に示すように、８００～１０００℃の熱処理を行い、ソース・ドレイン領域９の不純物の活性化を行った後、高融点金属膜１０を形成する。次いで、６００～１０００℃の範囲内で、２段階短時間熱処理法を施すと、図３（ｄ）に示すように、高融点金属膜１０とゲート電極５の多結晶シリコン膜、及びソース・ドレイン領域９のシリコン活性層との間にシリサイド化反応が生じ、自己整合的に高融点金属シリサイド膜１１が形成される。

【０００８】この工程の間には、アンモニア水と過酸化水素水の混合液を用いて、未反応高融点金属１２を選択

的にエッチング除去することにより、図３（ｅ）に示すように、サリサイド構造を有するＭＯＳＦＥＴが完成する。

【０００９】

【発明が解決しようとする課題】しかしながら、以上述べた従来のサリサイド構造を有するＭＯＳＦＥＴの製造方法では、素子の微細化に伴い、短チャネル効果抑制のため、そのソース・ドレイン領域の拡散層の接合深さ（ｘｊ）が浅くなり、シリサイド化した層の底面と接合との間隔が短くなり、接合リーク電流が増大するという問題があった。

【００１０】また、ソース・ドレイン領域及びゲート電極上のシリサイド表面は、大気に晒されたときに酸化物が生成され、メタル配線との接続のときに十分なオーミックコンタクトがとれないという問題があった。また、ソース・ドレイン領域を形成した後に、シリサイド化を行っているため、シリサイドと拡散層の界面の不純物濃度が層間絶縁膜の平坦化熱処理によって低下し、寄生抵抗が生じ、ＭＯＳトランジスタの電流駆動能力が低下するという問題があった。

【００１１】また、ソース・ドレイン領域を形成するときに、サイドウォールが形成された状態でイオン注入を行っているためと、そのサイドウォールがプロセスの最後まで除去されずに残っているために、後工程の熱処理によってサイドウォール膜中の不純物が、ソース・ドレイン領域に拡散し、ゲート電極端のソース・ドレイン領域の不純物プロファイルを不均一にし、短チャネル効果及びホットキャリア耐性の劣化を生じるという問題があった。

【００１２】また、ソース・ドレイン領域とゲート電極上をシリサイド化するときに、サイドウォール上部は殆どシリサイド化はしないが、わずかにサイドウォール表面部はシリサイド化反応が生じるため、その後の選択エッチングのときに、その反応層を十分除去しきれずに、ゲート電極とソース・ドレイン領域をショートさせるという問題点があった。

【００１３】本発明は、上記問題点を解決するために、以上述べた接合リーク電流及び寄生抵抗の増大をなくし、また、効果的に短チャネル効果を抑制し、さらにホットキャリア効果を抑制できるようにしたサリサイド構造を有する電界効果型トランジスタの製造方法を提供することを目的とする。

【００１４】

【課題を解決するための手段】本発明は、上記目的を達成するために、サリサイド構造を有する電界効果型トランジスタの製造方法において、

〔Ａ〕半導体基板上のアクティブ領域にゲート電極を形成する工程と、該ゲート電極の側面に第１のＬ型サイドウォール及びその上に堆積される第２のサイドウォールを有する２重サイドウォールを形成する工程と、ソース

・ドレイン領域及び前記ゲート電極上に高融点金属シリサイド膜を形成する工程と、前記２重サイドウォールをマスクにしてソース・ドレイン領域に深い接合の不純物拡散（n⁻）層を形成する工程と、前記２重サイドウォールの第２のサイドウォールをエッチング除去し、前記第１のＬ型サイドウォールを残した状態で、ソース・ドレイン領域に浅い接合の不純物拡散（n⁺）層を形成する工程と、前記第１のＬ型サイドウォールをエッチング除去し、ゲート電極をマスクにして大斜角斜め回転イオン注入法により、ＬＤＤ用の不純物拡散（n⁻）層を形成する工程と、多層の層間絶縁膜を形成し、該層間絶縁膜の平滑化と、ソース・ドレイン拡散層を活性化するための熱処理を行う工程と、ゲート電極配線とソース・ドレイン領域をバリアメタルを含む積層メタル配線とコンタクトをとる工程とを順に施すようにしたものである。

【００１５】〔B〕半導体基板上のアクティブ領域にゲート電極を形成する工程と、該ゲート電極の側面に幅の広いサイドウォールを形成する工程と、ソース・ドレイン領域及び前記ゲート電極上に高融点金属シリサイド膜を形成する工程と、前記サイドウォールをマスクにしてソース・ドレイン領域に深い接合の不純物拡散（n⁻）層を形成する工程と、前記サイドウォールをエッチング除去し、ソース・ドレイン領域に浅い接合の不純物拡散（n⁺）層を形成する工程と、ゲート電極をマスクにして大斜角斜め回転イオン注入法により、ＬＤＤ用の不純物拡散（n⁻）層を形成する工程と、多層の層間絶縁膜を形成し、該層間絶縁膜の平滑化と、ソース・ドレイン拡散層を活性化するための熱処理を行う工程と、ゲート電極配線とソース・ドレイン領域をバリアメタルを含む積層メタル配線とコンタクトをとる工程とを順に施すようにしたものである。

【００１６】〔C〕半導体基板上のアクティブ領域にゲート電極を形成する工程と、該ゲート電極の側面に第１のＬ型サイドウォール及びその上に堆積される第２のサイドウォールを有する２重サイドウォールを形成する工程と、ソース・ドレイン領域及び前記ゲート電極上に高融点金属シリサイド膜を形成する工程と、前記２重サイドウォールをマスクにしてソース・ドレイン領域に深い接合の不純物拡散（n⁻）層を形成する工程と、前記２重サイドウォールの第２のサイドウォールをエッチング除去し、前記第１のＬ型サイドウォールを残した状態で、ソース・ドレイン領域に浅い接合の不純物拡散（n⁺）層を形成する工程と、前記第１のＬ型サイドウォール及びゲート電極をマスクにして大斜角斜め回転イオン注入法により、ＬＤＤ用の不純物拡散（n⁻）層を形成する工程と、多層の層間絶縁膜を形成し、該層間絶縁膜の平滑化と、ソース・ドレイン拡散層を活性化するための熱処理を行う工程と、ゲート電極配線とソース・ドレイン領域をバリアメタルを含む積層メタル配線とコンタクトをとる工程とを順に施すようにしたものである。

【００１７】

【作用】本発明によれば、上記のように、比較的長いサイドウォールの外側で、ソース・ドレイン領域がシリサイド化され、しかもその領域のみ拡散層深さが深くなっているため、トランジスタの短チャネル効果を増大させることなく、接合リーク電流の増大を抑制できる。

【００１８】また、ソース・ドレイン領域の拡散層を形成する前に、その領域のシリサイド化を行っているので、自然酸化膜の影響を受けずに、低温でシリサイド化反応を安定に生じさせることができ、十分な低抵抗化を再現性よく安定に実現することができる。更に、ソース・ドレイン領域にイオン注入時のマスク酸化膜による酸素のノックオンがないので、シリサイド化反応の熱処理において、低温下でシリサイド化反応を均一に生じさせることができる。

【００１９】また、より具体的には、ソース・ドレイン形成用イオン注入ドーズ量が接合深さを十分浅くし、しかも電流駆動力駆を低下させないような範囲に抑制されているため、微細なＭＯＳＦＥＴにおいても、十分な短チャネル効果が抑制され、しかも高駆動力なＭＯＳＦＥＴが実現可能となる。更に、シリサイド化領域の深い拡散層形成は、シリサイド膜からの固相拡散を利用しているため、シリサイド界面や拡散層界面が凹凸にならないスムーズな界面が得られ、かつシリサイドと拡散層界面の不純物濃度が高濃度に保たれ、オーミック接合が再現性よく安定に実現できる。

【００２０】また、シリサイド化後に、浅い拡散層形成と、ＬＤＤ（n⁻）層形成のためのイオン注入を行っているので、そのイオン注入の不純物の活性化を層間絶縁膜の平坦化アニールと同時に行うようにしても、シリサイドと拡散層界面の不純物濃度が低下するのを補うことができ、十分なオーミック接合がシリサイドと拡散層の間で実現できる。

【００２１】

【実施例】以下、本発明の実施例について図面を参照しながら詳細に説明する。図１は本発明の第１の実施例を示す電界効果型トランジスタの製造工程断面図（その１）、図２はその電界効果型トランジスタの製造工程断面図（その２）である。

【００２２】（１）まず、図１（ａ）に示すように、ｐ型の面方位（１００）面のシリコン基板２１上に、ＬＯＣＯＳ法により素子分離領域を形成するためにフィールド酸化膜２２を４０００Å程度形成する。

（２）次に、図１（ｂ）に示すように、高清浄度なドライ酸化雰囲気中でゲート酸化膜２３を１００Å程度形成する。次に、減圧ＣＶＤ法を用いて、多結晶シリコン膜を３０００Å程度形成する。次に、通常のホトリソ技術とエッチング技術を用いて、多結晶シリコン膜からなるゲート電極２４配線を形成する。次に、シリコン活性層表面２５ａ、多結晶シリコン膜表面２５ｂ上に、８００

℃程度の温度のドライ酸化雰囲気中で酸化膜を形成する。

【0023】次に、LPCVD法を用いて、全面にシリコン窒化膜26を500～1000Å程度形成する。次に、LPCVD法かあるいは常圧CVD法を用いて、シリコン酸化膜を2000～3000Å程度形成する。次いで、反応性（異方性）イオンエッチング法を用いて、シリコン酸化膜のみをエッチングし、ゲート電極24側壁にシリコン酸化膜からなるサイドウォール27a，27bを形成する。

【0024】（3）次に、図1（c）に示すように、ウェットエッチング法あるいは反応性イオンエッチング法を用いてゲート電極24側壁以外のシリコン窒化膜26をエッチング除去し、L型のサイドウォールを含む2重サイドウォール31a，31b，27a，27bを形成し、これをマスクにして、界面活性剤入りのバッファードフッ酸溶液を用いて、シリコン活性層表面25aと多結晶シリコン膜表面25b上の酸化膜をエッチング除去する。次に、シリコン活性層表面25aと多結晶シリコン膜表面25b上の自然酸化膜を、Ar＋H_2 ガス混合のガス雰囲気中でプラズマ表面クリーニングによってエッチング除去する。

【0025】次いで、連続的にシリコン基板を大気に晒さないで、全面にプラズマスパッタリング法を用いて、高融点金属（Ti，Co，W，Ni，Mo等）膜を200～500Å程度形成する。次に、2段階短時間熱処理法を用いて、多結晶シリコン膜からなるゲート電極24上と、ソース・ドレイン領域となるシリコン活性層表面25aに、自己整合的に高融点金属シリサイド膜、例えば$TiSi_2$ 膜を600Å程度形成する。なお、1段階目の短時間熱処理は、600～700℃程度でN_2 ガス雰囲気中で30秒間行う。

【0026】次いで、アンモニア水（NH_3 OH）と過酸化水素水（H_2 O_2 ）と水（H_2O）の混合液を用いて、室温でシリサイド上のTiNとサイドウォール上及びフィールド酸化膜上の未反応TiとTiNをエッチング除去する。次に、2段階目の短時間熱処理を700～900℃程度でN_2 ガス雰囲気中で30秒間行い、化学量論的に安定な$TiSi_2$ 膜28a，28b，29を形成する。

【0027】次に、ソース・ドレイン領域形成用不純物（P）を、加速エネルギー40keV、ドーズ量1×10^{14}～1×10^{15}ions／cm^2 と、通常使用される（3～5×10^{15}）ions／cm^2 より低いドーズ量で、シリサイド膜とシリコン基板界面付近にイオン注入し、接合の深いn^- 拡散層30a，30bを形成する。

【0028】（4）次に、図1（d）に示すように、シリコン酸化膜のサイドウォール27a，27bを、反応性イオンエッチング法を用いてエッチング除去する。次に、L型サイドウォール31a，31bをマスクにして、サイドウォール下に加速エネルギー110keV、ドーズ量3～5×10^{15}ions／cm^2 の条件で、接合の浅いn^+ 拡散層32a，32bのソース・ドレイン領域を形成するためのイオン、例えばAsのイオン注入をする。

【0029】（5）次に、L型サイドウォール31a，31bを、図2（a）に示すように、反応性イオンエッチング法を用いてエッチング除去する。次いで、シリコン活性層表面と多結晶シリコン膜側壁のシリコン酸化膜を、界面活性剤入りのバッファードフッ酸を用いてエッチング除去する。次いで、ホットキャリア効果抑制用のLDD層（n^- 層）33a，33bを形成するための不純物（P）を大斜角（45°程度）斜め回転イオン注入法により、2～4×10^{13}ions／cm^2 程度のドーズ量、加速エネルギー30keVの条件でイオン注入する。次に、800℃程度でN_2 （又はNH_3 ）ガス雰囲気中で30秒間短時間熱処理を行い、シリサイド膜表面及び多結晶シリコン膜側壁を窒化する（図示なし）。

【0030】（6）次に、図2（b）に示すように、LPCVD法を用いて、全面にシリコン酸化膜34を500Å程度形成する。次に、LPCVD法を用いて、全面にシリコン窒化膜35を500Å程度形成する。次に、常圧CVD法を用いて全面にシリコン酸化膜36と、不純物（B，P）を含むシリコン酸化膜37を連続的に形成する。次に、不純物を含むシリコン酸化膜37を平坦にするためとソース・ドレイン領域の不純物を活性化するためのアニールを行う。

【0031】（7）次に、図2（c）に示すように、通常のホトリソ技術とエッチング技術を用いて、ソース・ドレイン領域上あるいはゲート電極24配線上にコンタクト穴38を形成する。次に、スパッタリング法を用いて、2層あるいはそれ以上の積層膜で形成された金属を形成し、通常のホトリソ技術とエッチング技術により、メタル配線39を形成する。

【0032】次に、本発明の第2実施例について図を用いて説明する。図4は本発明の第2実施例を示す電界効果型トランジスタの製造工程断面図である。この第2の実施例は、比較的長いサイドウォール1層を用いて、第1の実施例と同様のソース・ドレイン領域を形成するようにしたものである。

【0033】（1）まず、図4（a）に示すように、p型の面方位（100）面のシリコン基板41上に、LOCOS法により素子分離領域を形成するためにフィールド酸化膜42を4000Å程度形成する。次に、高清浄度なドライ酸化雰囲気中でゲート酸化膜43を100Å程度形成する。次に、減圧CVD法を用いて、多結晶シリコン膜を3000Å程度形成する。次に、通常のホトリソ技術とエッチング技術を用いて、多結晶シリコン膜からなるゲート電極44配線を形成する。次に、シリコン活性層表面45a、多結晶シリコン膜表面45bに、

８００℃程度の温度のドライ酸化雰囲気中で酸化膜を形成する。次に、ＬＰＣＶＤ法かあるいは常圧ＣＶＤ法を用いて、シリコン酸化膜を２５００～４０００Å程度形成する。次いで、反応性イオンエッチング法を用いて、シリコン酸化膜のみをエッチングし、ゲート電極４４側壁にサイドウォール４６ａ，４６ｂを形成する。

【００３４】（２）次いで、図４（ｂ）に示すように、サイドウォール４６ａ，４６ｂをマスクにして、ウェットエッチング法あるいは反応性イオンエッチング法を用いてゲート電極４４側壁以外のシリコン酸化膜をエッチング除去する。次いで、界面活性剤入りのバッファードフッ酸溶液を用いて、シリコン活性層表面４５ａと多結晶シリコン膜表面４５ｂ上の酸化膜をエッチング除去する。次に、シリコン活性層表面４５ａと多結晶シリコン膜表面４５ｂ上の自然酸化膜をＡｒ＋H_2 ガス混合のガス雰囲気中でプラズマ表面クリーニングによってエッチング除去する。

【００３５】次いで、連続的にシリコン基板を大気に晒さないで、全面にプラズマスパッタリング法を用いて、高融点金属（Ｔｉ，Ｃｏ，Ｗ，Ｎｉ，Ｍｏ等）膜を２００～５００Å程度形成する。次に、２段階短時間熱処理法を用いて、ゲート電極４４上と、ソース・ドレイン領域となるシリコン活性層表面４５ｂに、自己整合的に高融点金属シリサイド膜、例えば$TiSi_2$ 膜を６００Å程度形成する。なお、１段階目の短時間熱処理は、６００～７００℃程度でN_2 ガス雰囲気中で３０秒間行う。

【００３６】次いで、アンモニア水（NH_3OH）と過酸化水素水（H_2O_2 ）と水（H_2O）の混合液を用いて、室温でシリサイド上のＴｉＮとサイドウォール上及びフィールド酸化膜上の未反応ＴｉとＴｉＮをエッチング除去する。次に、２段階目の短時間熱処理を７００～９００℃程度でN_2 ガス雰囲気中で３０秒間行い、化学量論的に安定なシリサイド膜、つまり$TiSi_2$ 膜４７ａ，４７ｂ，４８を形成する。

【００３７】次に、ソース・ドレイン領域形成用不純物（Ｐ）を、加速エネルギー４０ｋｅＶ、ドーズ量1×10^{14}～1×10^{15} ｉｏｎｓ／cm^2 と、通常使用される（$3\sim5\times10^{15}$）ｉｏｎｓ／cm^2 より低いドーズ量で、シリサイド膜とシリコン膜基板界面付近にイオン注入し、接合の深いn^- 拡散層４９ａ，４９ｂを形成する。

【００３８】（３）次いで、図４（ｃ）に示すように、シリコン酸化膜のサイドウォール４６ａ，４６ｂを、反応性イオンエッチング法を用いてエッチング除去する。更に、シリコン活性層表面と多結晶シリコン膜側壁のシリコン酸化膜を界面活性剤入りのバッファードフッ酸を用いてエッチング除去する。次に、加速エネルギー６０ｋｅＶ、ドーズ量$3\sim5\times10^{15}$ ｉｏｎｓ／cm^2 の条件で、接合の浅いn^+拡散層５０ａ，５０ｂのソース・ドレイン領域を形成するためのイオン、例えば、As^+ のイオン注入をする。

【００３９】（４）次いで、図４（ｄ）に示すように、ホットキャリア効果抑制用のＬＤＤ層（n^- 層）５１ａ，５１ｂを形成するための不純物（Ｐ）を大斜角（４５°程度）斜め回転イオン注入法により、$2\sim4\times10^{13}$ ｉｏｎｓ／cm^2 程度のドーズ量、加速エネルギー３０ｋｅＶの条件でイオン注入する。次に、８００℃程度でN_2 （又はNH_3 ）ガス雰囲気中で３０秒間短時間熱処理を行い、シリサイド膜表面及び多結晶シリコン膜側壁を窒化する（図示なし）。

【００４０】（５）その後は、第１実施例の図２（ｂ）及び図２（ｃ）に示す工程を施し、電界効果型トランジスタを完成する。このように、第２実施例においては、第１の実施例で用いたＬ型サイドウォールを用いずに、ＬＤＤ構造のソース・ドレイン領域を形成する。シリサイド膜の形成後のシリサイド膜下の接合の深いn^- 拡散層４９ａ，４９ｂは第１の実施例と同じである。ゲート電極４４をマスクにして入射角０°で、接合の浅いn^+拡散層５０ａ，５０ｂを形成し、その後、大斜角斜め回転イオン注入法を用いて、ＬＤＤ層（n^- 層）５１ａ，５１ｂを形成するようにしたことが特徴である。

【００４１】次に、本発明の第３実施例について図を用いて説明する。図５は本発明の第３実施例を示す電界効果型トランジスタの製造工程断面図である。

（１）まず、図５（ａ）に示すように、ｐ型の面方位（１００）面のシリコン基板６１上に、ＬＯＣＯＳ法により素子分離領域を形成するためにフィールド酸化膜６２を４０００Å程度形成する。次に、高清浄度なドライ酸化雰囲気中でゲート酸化膜６３を１００Å程度形成する。次に、減圧ＣＶＤ法を用いて、多結晶シリコン膜を３０００Å程度形成する。次に、通常のホトリソ技術とエッチング技術を用いて、多結晶シリコン膜からなるゲート電極６４配線を形成する。

【００４２】次に、シリコン活性層表面６５ａ、多結晶シリコン膜表面６５ｂ上に、８００℃程度の温度のドライ酸化雰囲気中で酸化膜を形成する。次に、ＬＰＣＶＤ法を用いて、全面にシリコン窒化膜６６を５００～１０００Å程度形成する。次に、ＬＰＣＶＤ法かあるいは常圧ＣＶＤ法を用いて、シリコン酸化膜を２０００～３０００Å程度形成する。次いで、反応性（異方性）イオンエッチング法を用いて、不純物を含むシリコン酸化膜６７のみをエッチングし、ゲート電極側壁にサイドウォール６７ａ，６７ｂを形成する。

【００４３】（２）次いで、図５（ｂ）に示すように、Ｌ型のサイドウォールを含む２重サイドウォール７１ａ，７１ｂ，６７ａ，６７ｂをマスクにして、ウエットエッチング法あるいは反応性イオンエッチング法を用いて、ゲート電極６４側壁以外のシリコン窒化膜６６をエッチング除去する。次いで、界面活性剤入りのバッファードフッ酸溶液を用いて、シリコン活性層表面６５ａと

多結晶シリコン膜表面65b上の酸化膜をエッチング除去する。次に、シリコン活性層表面65aと多結晶シリコン膜表面65b上の自然酸化膜を、Ar＋H_2 ガス混合のガス雰囲気中でプラズマ表面クリーニングによってエッチング除去する。

【0044】次いで、連続的にシリコン基板を大気に晒さないで、全面にプラズマスパッタリング法を用いて、高融点金属（Ti，Co，W，Ni，Mo等）膜を200～500Å程度形成する。次に、2段階短時間熱処理法を用いて、多結晶シリコン膜からなるゲート電極64上と、ソース・ドレイン領域となるシリコン活性層表面65aに、自己整合的に高融点金属シリサイド膜、例えば$TiSi_2$ 膜を600Å程度形成する。なお、1段階目の短時間熱処理は、650℃程度でN_2 ガス雰囲気中で30秒間行う。

【0045】次いで、アンモニア水（NH_3OH）と過酸化水素水（H_2O_2）と水（H_2O）の混合液を用いて、室温でシリサイド上のTiNとサイドウォール上及びフィールド酸化膜上の未反応TiとTiNをエッチング除去する。次に、2段階目の短時間熱処理を700～900℃程度N_2 ガス雰囲気中で30秒間行い、化学量論的に安定な$TiSi_2$ 膜68a，68b，69を形成する。

【0046】次に、ソース・ドレイン領域形成用不純物（P）を、加速エネルギー40keV、ドーズ量1×10^{14}～1×10^{15} ions／cm^2 と、通常使用される（3～5×10^{15}）ions／cm^2 より低いドーズ量で、シリサイド膜とシリコン膜基板界面付近にイオン注入し、接合の深いn^- 拡散層70a，70bを形成する。

【0047】（3）次に、図5（c）に示すように、シリコン酸化膜からなるサイドウォール67a，67bを反応性イオンエッチング法を用いてエッチング除去する。次に、L型サイドウォール71a，71bをマスクにして、サイドウォール下に加速エネルギー110keV、ドーズ量3～5×10^{15} ions／cm^2 の条件で接合の浅いn^+ 拡散層72a，72bのソース・ドレイン領域を形成するためのイオン、例えばAsのイオン注入をする。

【0048】（4）次いで、図5（d）に示すように、ホットキャリア効果抑制用のLDD層（n^- 層）73a，73bを形成するための不純物（P）を大斜角（45°程度）斜め回転イオン注入法により、2～4×10^{13} ions／cm^2 程度のドーズ量、加速エネルギー30keVの条件でイオン注入する。次いで、800℃程度でN_2（又はNH_3）ガス雰囲気中で30秒間短時間熱処理を行い、シリサイド膜表面及び多結晶シリコン膜側壁を窒化する（図示なし）。

【0049】（5）その後は、第1実施例の図2（b）及び図2（c）に示す工程を施し、電界効果型トランジ

スタを完成する。このように、第3の実施例は、L型のサイドウォールを含む2重サイドウォールを用いた第1の実施例を変形したものである。第1の実施例との違いは、ホットキャリア効果抑制用のLDD層（n^- 層）73a，73bを形成する工程である。

【0050】すなわち、L型サイドウォール71a，71bを残した状態で、まず、入射角0°のイオン注入により、接合の浅いn^+ 拡散層72a，72bを形成し、更に、L型サイドウォール71a，71bを残した状態で、大斜角斜めイオン注入法を用いて、LDD層（n^- 層）73a，73bを、ゲート電極64にオーバーラップするように形成する。

【0051】なお、上記実施例においては、nチャネルMOSFETについて説明したが、pチャネルMOSFETの場合にも同様に適用できることは言うまでもない。また、本発明は上記実施例に限定されるものではなく、本発明の趣旨に基づいて種々の変形が可能であり、これらを本発明の範囲から排除するものではない。

【0052】

【発明の効果】以上、詳細に説明したように、本発明によれば、

（1）比較的長いサイドウォールの外側で、ソース・ドレイン領域がシリサイド化され、しかもその領域のみ拡散層深さが深くなっているため、トランジスタの短チャネル効果を増大させることなく、接合リーク電流の増大を抑制できる。

【0053】（2）ソース・ドレイン領域の拡散層を形成する前に、その領域のシリサイド化を行っているので、自然酸化膜の影響を受けずに、低温でシリサイド化反応を安定に生じさせることができ、十分な低抵抗化を再現性よく安定に実現することができる。

（3）ソース・ドレイン領域にイオン注入時のマスク酸化膜による酸素のノックオンがないので、シリサイド化反応の熱処理において、低温下でシリサイド化反応を均一に生じさせることができる。

【0054】（4）より具体的には、ソース・ドレイン形成用イオン注入ドーズ量が接合深さを十分浅くし、しかも電流駆動力を低下させないような範囲に制御されているため、微細なMOSFETにおいても、十分な短チャネル効果が抑制され、しかも高駆動力なMOSFETが実現可能となる。

（5）シリサイド化領域の深い拡散層形成は、シリサイド膜からの固相拡散を利用しているため、シリサイド界面や拡散層界面が凹凸にならないスムーズな界面が得られ、かつシリサイドと拡散層界面の不純物濃度が高濃度に保たれるオーミック接合が再現性よく安定に実現できる。

【0055】（6）シリサイド化後に、浅い拡散層形成と、LDD（n^-）層形成のためのイオン注入を行っているので、そのイオン注入の不純物の活性化を層間絶縁

膜の平坦化アニールと同時に行うようにしても、シリサイドと拡散層界面の不純物濃度が低下するのを補うことができ、十分なオーミック接合がシリサイドと拡散層の間で実現できる。

【0056】また、特に、請求項1及び3によれば、上記効果に加えて、L型サイドウォールは、エッチングによるサイドウォール幅のばらつきが生じないため、電気的なゲート長のばらつきがなくなり、閾値電圧のばらつきの小さいMOSFETを安定に形成することができる。また、LDD（n^-）層形成のイオン注入は、マスク酸化膜なしにシリコン活性層表面に直接大斜角斜めに回転イオン注入法により行っているため、マスク酸化膜中の酸素のシリコン基板へのノックオンによる不純物の不活性化を防止できる。

【0057】更に、特に、請求項2によれば、上記効果に加えて、浅いn^+の接合の拡散層領域を、ゲート電極とオーバーラップさせることにより、バンド間トンネルによるドレインリーク電流の発生を回避させることが可能である。また、特に、請求項4によれば、ソース・ドレイン領域のn^-層とn^+層及びLDD（n^-）層を形成した後に、低温短時間熱処理によるシリサイド表面と多結晶シリコン膜表面及びシリコン活性層表面を膜応力緩和のための窒化とシリサイド膜結晶回復を同時に行っているため、後の熱処理によって拡散層の不純物の再分布が生じないだけでなく、シリサイド膜の凝集も起こらなくなり、十分な低抵抗拡散層とオーミック接合が形成できる。

【0058】更に、特に、請求項5によれば、層間絶縁膜を下層よりシリコン酸化膜、シリコン窒化膜、シリコン酸化膜及び不純物を含むシリコン酸化膜の4層構造にしたため、シリサイド膜への膜応力が緩和され、その後の熱プロセスに対するシリサイド膜の耐熱性が十分となる。また、層間絶縁膜の構成膜の中にLPCVD法かあるいはプラズマCVD法によるシリコン窒化膜が含まれているので、層間絶縁膜の表面平坦化熱処理雰囲気としてN_2、O_2、ウェットO_2ガスの全ての雰囲気に対して対応できる。特にウェットO_2ガス雰囲気にすることにより、N_2処理より低温で平坦化が可能になる。

【0059】また、シリサイド膜表面がＴｉＮ化されているため、コンタクト穴を形成した後、ＴｉＮ表面が酸化されなくなり、メタル配線との接合において、十分なオーミックコンタクトが得られる。更に、現行のコンタクト穴形成後のHFディップにより微小コンタクト穴底部の自然酸化膜を除去する工程をそのまま使うことができる。ここでHFとしては、界面活性剤の入っているバッファードフッ酸溶液が望ましい。

【図面の簡単な説明】

【図1】本発明の第1の実施例を示す電界効果型トランジスタの製造工程断面図（その1）である。

【図2】本発明の第1の実施例を示す電界効果型トランジスタの製造工程断面図（その2）である。

【図3】従来のサリサイド構造を有するMOSFETの製造工程断面図である。

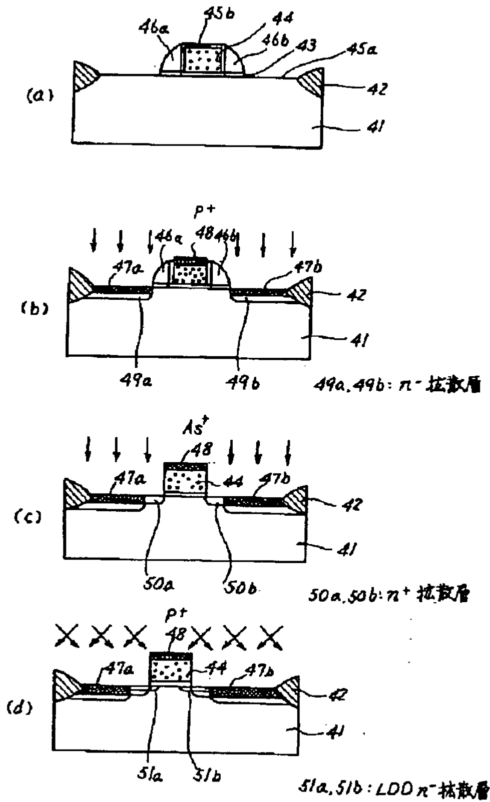
【図4】本発明の第2の実施例を示す電界効果型トランジスタの製造工程断面図である。

【図5】本発明の第3の実施例を示す電界効果型トランジスタの製造工程断面図である。

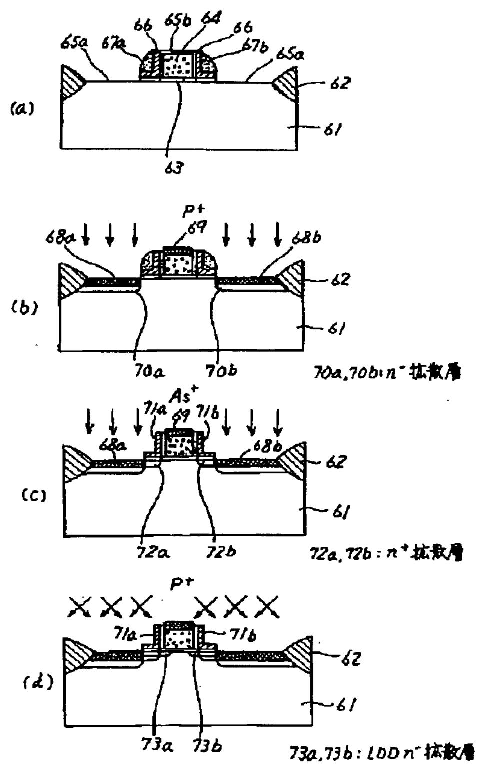
【符号の説明】

21，41，61　シリコン基板
22，42，62　フィールド酸化膜
23，43，63　ゲート酸化膜
24，44，64　ゲート電極
26，35，66　シリコン窒化膜
27a，27b，46a，46b，67a，67b　サイドウォール
28a，28b，29，47a，47b，48，68a，68b，69　$TiSi_2$膜
30a，30b，49a，49b，70a，70b　接合の深いn^-拡散層
31a，31b，71a，71b　L型サイドウォール
32a，32b，50a，50b，72a，72b　接合の浅いn^+拡散層
33a，33b，51a，51b，73a，73b　LDD層（n^-層）
34，36，37　シリコン酸化膜
38　コンタクト穴
39　メタル配線

【図4】



【図5】



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(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(72)Inventor : HIROKI AKIRA
KURIMOTO KAZUMI
ODANAKA SHINJI

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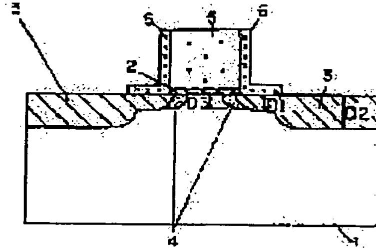
(54) SEMICONDUCTOR DEVICE, COMPLEMENTARY SEMICONDUCTOR DEVICE, AND MANUFACTURE THEREOF

(57)Abstract:
PURPOSE: To provide a semiconductor device which is excellent in resistance to a short channel effect and high in operational speed and reliability.
CONSTITUTION: The junction depth D1 of a high concentration source.drain diffusion layer 3 under an L-shaped side wall 6 is set smaller than the junction depth D2 of the high concentration source.drain diffusion layer 3 outside the L-shaped side wall 6, and the junction depth D3 of a low concentration diffusion layer 4 is set equal to or smaller than the junction depth D1 of the high concentration source.drain diffusion layer 3 under an L-shaped side wall 6. Therefore, a potential is more effectively restrained from expanding from a source.drain diffusion layer toward a channel than that in a conventional overlapped LDD structure, so that a problem or a reduction in Vt peculiar to a MOSFET is effectively prevented when a device is microminiaturized to a size of the order of half-micron or below.



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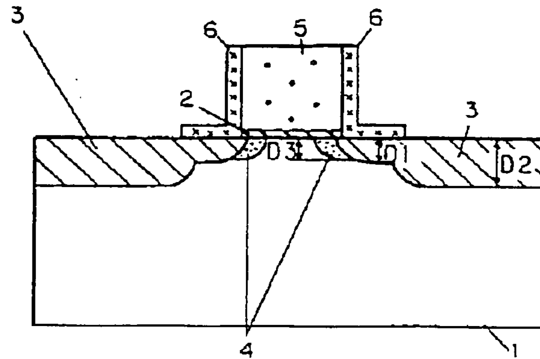
(71)出願人　000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地
(72)発明者　広木　彰
大阪府門真市大字門真1006番地　松下電器産業株式会社内
(72)発明者　栗本　一実
大阪府門真市大字門真1006番地　松下電器産業株式会社内
(72)発明者　小田中　紳二
大阪府門真市大字門真1006番地　松下電器産業株式会社内
(74)代理人　弁理士　小鍜治　明　（外２名）

(54)【発明の名称】　半導体装置及び相補型半導体装置並びにそれらの製造方法

(57)【要約】
【目的】　短チャネル効果に強く、高速で高信頼性の半導体装置を提供する。
【構成】　Ｌ型側壁６下部の高濃度ソース・ドレイン拡散層３の接合深さＤ１が、Ｌ型側壁６の外側の高濃度ソース・ドレイン拡散層３の接合深さＤ２よりも浅く形成され、かつ低濃度ソース・ドレイン拡散層４の接合深さＤ３がＬ型側壁６下部のソース・ドレイン拡散層３の接合深さＤ１と同等かそれよりも浅く形成されている。このため、従来のオーバラップＬＤＤ構造よりもソース・ドレイン拡散層からのポテンシャルのチャネル方向への広がりが効果的に抑えられ、ハーフミクロン領域以下の微細化に問題となるＭＯＳＦＥＴ特有のＶｔの低下が効果的に抑制される。



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【特許請求の範囲】

【請求項１】第１導電型不純物がドープされた第１導電型領域を含み、かつ、主面を有する半導体基板と、該第１導電型領域に設けられたＭＯＳトランジスタと、を備えた半導体装置であって、
該ＭＯＳトランジスタは、
該第１導電型領域内に形成された第２導電型ソース領域と、
該第１導電型領域内に形成され、該第２導電型ソース領域から一定距離だけ離れた第２導電型ドレイン領域と、
該第１導電型領域内に形成され、該第２導電型ソース領域と該第２導電型ドレイン領域との間に位置するチャネル領域と、
該チャネル領域の両端部に形成され、該第２導電型ソース領域の不純物濃度よりも低い不純物濃度を有する一対の第２導電型不純物拡散層と、
該半導体基板の該主面上に形成されたゲート絶縁膜であって、該チャネル領域及び該第２導電型不純物拡散領域を直接に覆っているゲート絶縁膜と、
該ゲート絶縁膜上に形成されたゲート電極と、
該ゲート電極の側面に設けられたサイドウォールと、
を備えており、
該サイドウォールは、該ゲート電極の該側面から基板の該主面に沿って伸びる部分を有する形状を有しており、
該第２導電型ソース領域及びドレイン領域は、該サイドウォールの該主面に沿って伸びる部分に覆われている第１部分と、該サイドウォールの該主面に沿って伸びる部分に覆われていない第２部分とを有しており、該第１部分の厚さは該第２部分の厚さよりも薄い、半導体装置。

【請求項２】前記第２導電型ソース領域及びドレイン領域の前記第１部分は、前記ゲート電極の端部の真下の領域にまで達している請求項１に記載の半導体装置。

【請求項３】前記ゲート絶縁膜は、前記一対の第２導電型不純物領域上の部分の厚さが前記チャネル領域上の部分の厚さよりも厚い請求項１に記載の半導体装置。

【請求項４】前記ゲート絶縁膜は、前記一対の第２導電型不純物領域上の部分の厚さが前記チャネル領域上の部分の厚さよりも厚い請求項２に記載の半導体装置。

【請求項５】第１導電型不純物がドープされた第１導電型領域を含み、かつ、主面を有する半導体基板と、該第１導電型領域に設けられたＭＯＳトランジスタと、を備えた半導体装置であって、
該ＭＯＳトランジスタは、
該第１導電型領域内に形成された第２導電型ソース領域と、
該第１導電型領域内に形成され、該第２導電型ソース領域から一定距離だけ離れた第２導電型ドレイン領域と、
該第２導電型ソース領域と該第１導電型領域との間の接合、及びドレイン領域と該第１導電型領域との間の接合を覆うように設けられ、該第２導電型ソース領域及びドレイン領域の不純物濃度よりも低い不純物濃度を有する一対の第２導電型不純物拡散層と、
該第１導電型領域内に形成され、該一対の第２導電不純物拡散層の間に位置するチャネル領域と、
該半導体基板の該主面上に形成されたゲート絶縁膜であって、該チャネル領域を直接に覆っているゲート絶縁膜と、
該ゲート絶縁膜上に形成されたゲート電極と、
該ゲート電極の側面に設けられたサイドウォールと、
を備えており、
該サイドウォールは、該ゲート電極の該側面から基板の該主面に沿って伸びる部分を有する形状を有しており、
該部分は、該第２導電型不純物拡散層を直接に覆っている、半導体装置。

【請求項６】前記第２導電型ソース領域及びドレイン領域は、前記サイドウォールの前記主面に沿って伸びる前記部分の外側端部の真下の領域にまで達している、請求項５に記載の半導体装置。

【請求項７】前記第２導電型不純物拡散層領域は、前記ゲート電極の端部の真下の領域にまで達している請求項５に記載の半導体装置。

【請求項８】前記ゲート絶縁膜は、前記一対の第２導電型不純物領域上の部分の厚さが前記チャネル領域上の部分の厚さよりも厚い請求項６に記載の半導体装置。

【請求項９】前記ゲート絶縁膜は、前記一対の第２導電型不純物領域上の部分の厚さが前記チャネル領域上の部分の厚さよりも厚い請求項７に記載の半導体装置。

【請求項１０】第１導電型不純物がドープされた第１導電型領域を含み、かつ、主面を有する半導体基板と、該第１導電型領域に設けられたＭＯＳトランジスタと、を備えた半導体装置を製造する方法であって、
該第１導電型領域を覆うように、該トランジスタのゲート絶縁膜となる第１絶縁膜及び該トランジスタのゲート電極となる導電材料膜をこの順番で該半導体基板上に堆積する工程と、
該導電材料膜をパターニングし、それによって該ゲート電極を形成する工程と、
該ゲート電極を覆うように、第２絶縁膜及び、酸化種を透過しにくい第３絶縁膜をこの順番で該半導体基板上に堆積する工程と、
異方性エッチング技術を用いて、該第３及び第２絶縁膜をこの順番でエッチングすることによって、該第３及び第２絶縁膜の一部を該ゲート電極の側面に残置させる工程と、
選択性エッチング技術を用いて、該第３絶縁膜を選択的に除去することによって、該第２絶縁膜からなるＬ字型サイドウォールを形成する工程と、
該ゲート電極を注入マスクとして、第２導電型不純物イオンを該半導体基板に注入し、それによって、第２導電型不純物拡散層を形成する第１イオン注入工程と、

該ゲート電極を注入マスクとして、第２導電型不純物イオンを該半導体基板に注入し、それによって、該第２導電型不純物拡散層の不純物濃度よりも高濃度の不純物を含み、しかも、該サイドウォールに覆われている第１部分と該サイドウォールに覆われていない第２部分とを有し、該第１部分の厚さが該第２部分の厚さよりも薄い、第２導電型ソース及びドレイン領域を形成する第２イオン注入工程と、
を包含する製造方法。

【請求項１１】前記選択性エッチング技術を用いて前記Ｌ字型サイドウォールを形成する前記工程の前に、前記ゲート絶縁膜の端部を更に厚くする酸化工程を包含する、請求項１０に記載の製造方法。

【請求項１２】第１導電型不純物がドープされた第１導電型領域を含み、かつ、主面を有する半導体基板と、該第１導電型領域に設けられたMOSトランジスタと、を備えた半導体装置を製造する方法であって、
該第１導電型領域を覆うように、ゲート絶縁膜となる第１絶縁膜及びゲート電極となる導電材料膜をこの順番で該半導体基板上に堆積する工程と、
該導電材料膜をパターニングし、それによってゲート電極を形成する工程と、
該ゲート電極を覆うように、第２絶縁膜及び、酸化種を透過しにくい第３絶縁膜をこの順番で該半導体基板上に堆積する工程と、
異方性エッチング技術を用いて、該第３及び第２絶縁膜をこの順番でエッチングすることによって、該第３及び第２絶縁膜の一部を該ゲート電極の側面に残置させる工程と、
選択性エッチング技術を用いて、該第３絶縁膜を選択的に除去することによって、第２絶縁膜からなるＬ字型サイドウォールを形成する工程と、
該ゲート電極及び該サイドウォールを注入マスクとして、該サイドウォールを透過し得ない加速エネルギにて第２導電型不純物イオンを該半導体基板に注入し、それによって、該ゲート電極及び該サイドウォールに実質的に覆われてない領域に第２導電型ソース及びドレイン領域を形成する第１イオン注入工程と、
該ゲート電極を注入マスクとして、該サイドウォールを透過し得る加速エネルギにて第２導電型不純物イオンを該半導体基板に注入し、それによって、該第２導電型ソース及びドレイン領域の不純物濃度よりも低濃度の不純物を含み、しかも、該第２導電型ソース及びドレイン領域の厚さよりも厚い第２導電型不純物拡散層を形成する第２イオン注入工程と、
を包含する製造方法。

【請求項１３】前記選択性エッチング技術を用いて前記Ｌ字型サイドウォールを形成する前記工程の前に、前記ゲート絶縁膜の端部を更に厚くする酸化工程を包含する、請求項１２に記載の製造方法。

【請求項１４】ｎ型不純物がドープされたｎ型領域及び第ｐ型不純物がドープされたｐ型領域を含み、かつ、主面を有する半導体基板と、該ｐ型領域に設けられたｎチャネル型MOSトランジスタと、該ｎ型領域に設けられたｐチャネル型MOSトランジスタと、を備えた相補型半導体装置であって、
該ｎチャネル型MOSトランジスタは、
該ｐ型領域内に形成されたｎ型ソース領域と、
該ｐ型領域内に形成され、該ｎ型ソース領域から一定距離だけ離れたｎ型ドレイン領域と、
該ｐ型領域内に形成され、該ｎ型ソース領域と該ｎ型ドレイン領域との間に位置するチャネル領域と、
該チャネル領域の両端部に形成され、該ｎ型ソース領域の不純物濃度よりも低い不純物濃度を有する一対のｎ型不純物拡散層と、
該半導体基板の該主面上に形成されたゲート絶縁膜であって、該チャネル領域及び該一対のｎ型不純物領域を直接に覆い、該一対のｎ型不純物領域上の部分の厚さが、該チャネル領域上の部分の厚さよりも厚いゲート絶縁膜と、
該ゲート絶縁膜上に形成されたゲート電極と、
を備えており、
該ｐチャネル型MOSトランジスタは、
該ｎ型領域内に形成されたｐ型ソース領域と、
該ｎ型領域内に形成され、該ｐ型ソース領域から一定距離だけ離れたｐ型ドレイン領域と、
該ｎ型領域内に形成され、該ｐ型ソース領域と該ｐ型ドレイン領域との間に位置するチャネル領域と、
該半導体基板の該主面上に形成されたゲート絶縁膜であって、均一な厚さを有するゲート絶縁膜と、
該ゲート絶縁膜上に形成されたゲート電極と、
を備えている相補型半導体装置。

【請求項１５】前記ｎチャネル型MOSトランジスタ及び前記ｐチャネル型MOSトランジスタの少なくとも一方は、前記ゲート電極の側面に設けられたサイドウォールであって、該ゲート電極の該側面から前記半導体基板の前記主面に沿って伸びる部分を有する形状を有するサイドウォールを備えており、
前記ソース領域及びドレイン領域は、該サイドウォールの該主面に沿って伸びる部分に覆われている第１部分と、該サイドウォールの該主面に沿って伸びる部分に覆われていない第２部分とを有しており、該第１部分の厚さは該第２部分の厚さよりも薄い、請求項１４に記載の相補型半導体装置。

【請求項１６】前記第２導電型ソース領域及びドレイン領域の前記第１部分は、前記ゲート電極の端部の真下の領域にまで達している請求項１５に記載の半導体装置。

【請求項１７】前記ｐチャネル型MOSトランジスタの前記チャネル領域は、ｐ型の埋め込み型チャネル構造を有し、該チャネル領域の両端部に形成され、該ｐ型ソー

ス領域の不純物濃度よりも低い不純物濃度を有する一対のｐ型不純物拡散層を有している請求項１４に記載の半導体装置。

【請求項１８】前記ｐチャネル型ＭＯＳトランジスタの前記ゲート電極は、第１導電型ゲート電極である、請求項１４に記載の半導体装置。

【請求項１９】ｎ型不純物がドープされたｎ型領域及び第ｐ型不純物がドープされたｐ型領域を含み、かつ、主面を有する半導体基板と、該ｐ型領域に設けられたｎチャネル型ＭＯＳトランジスタと、該ｎ型領域に設けられたｐチャネル型ＭＯＳトランジスタと、を備えた相補型半導体装置を製造する方法であって、
該ｐ型領域及び該ｎ型領域を覆うように、該トランジスタのゲート絶縁膜となる第１絶縁膜及び該トランジスタのゲート電極となる導電材料膜をこの順番で該半導体基板上に堆積する工程と、
該導電材料膜をパターニングし、それによって該ゲート電極を形成する工程と、
該ゲート電極を覆うように、第２絶縁膜及び、酸化種を透過しにくい第３絶縁膜をこの順番で該半導体基板上に堆積する工程と、
該ｐチャネル型ＭＯＳトランジスタの該ゲート電極を覆うレジストを該ｎ型領域上に形成する工程と、
異方性エッチング技術を用いて、該第３及び第２絶縁膜のうちの該レジストに覆われてない部分をこの順番でエッチングすることによって、該第３及び第２絶縁膜の一部を該ｎチャネル型ＭＯＳトランジスタの該ゲート電極の側面及び該ｎ型領域上に残置させる工程と、
該レジストを除去する工程と、
該ｎチャネル型ＭＯＳトランジスタの該ゲート絶縁膜の端部を更に厚くする酸化工程と、
異方性エッチング技術を用いて、該第３及び第２絶縁膜をこの順番でエッチングすることによって、該第３及び第２絶縁膜の一部を該ｐチャネル型ＭＯＳトランジスタの該ゲート電極の側面に残置させる工程と、
選択性エッチング技術を用いて、該第３絶縁膜を選択的に除去することによって、該第２絶縁膜からなるＬ字型サイドウォールを形成する工程と、
を包含する製造方法。

【請求項２０】前記ｐチャネル型ＭＯＳトランジスタを覆うレジストを前記ｎ型領域上に形成する工程と、
該レジスト及び前記ｎチャネル型ＭＯＳトランジスタのゲート電極を注入マスクとして、ｎ型不純物イオンを前記ｐ型領域に注入し、それによって、ｎ型不純物拡散層を形成する第１のｎ型イオン注入工程と、
該レジスト及び該ｎチャネル型ＭＯＳトランジスタの該ゲート電極を注入マスクとして、ｎ型不純物イオンを該ｐ型領域に注入し、それによって、該ｎ型不純物拡散層の不純物濃度よりも高濃度の不純物を含み、しかも、該サイドウォールに覆われている第１部分と該サイドウォールに覆われていない第２部分とを有し、該第１部分の厚さが該第２部分の厚さよりも薄い、ｎ型ソース及びドレイン領域を形成する第２のｎ型イオン注入工程と、
を更に包含する、請求項１９に記載の製造方法。

【請求項２１】前記ｎチャネル型ＭＯＳトランジスタを覆うレジストを前記ｐ型領域上に形成する工程と、
該レジスト及び前記ｐチャネル型ＭＯＳトランジスタのゲート電極を注入マスクとして、ｐ型不純物イオンを前記ｎ型領域に注入し、それによって、前記サイドウォールに覆われている第１部分と該サイドウォールに覆われていない第２部分とを有し、該第１部分の厚さが該第２部分の厚さよりも薄い、ｐ型ソース及びドレイン領域を形成するｐ型イオン注入工程を更に包含する、請求項２０に記載の製造方法。

【請求項２２】前記ｐ型領域を覆うレジストと前記ｐチャネル型ＭＯＳトランジスタの前記ゲート電極を注入マスクとして、ｐ型不純物イオンを前記ｎ型領域に注入し、それによって、該サイドウオールに覆われている第１部分と該サイドウオールに覆われていない第２部分とを有し、該第１部分の厚さが該第２部分の厚さよりも薄く、しかも、該ゲート電極の端部の真下の領域にまで達しているｐ型ソース及びドレイン領域を形成するｐ型イオン注入工程と、
を更に包含する、請求項２０に記載の製造方法。

【請求項２３】ｎ型不純物がドープされたｎ型領域及び第ｐ型不純物がドープされたｐ型領域を含み、かつ、主面を有する半導体基板と、該ｐ型領域に設けられたｎチャネル型ＭＯＳトランジスタと、該ｎ型領域に設けられたｐチャネル型ＭＯＳトランジスタと、を備えた相補型半導体装置を製造する方法であって、
該ｐ型領域及び該ｎ型領域を覆うように、該トランジスタのゲート絶縁膜となる第１絶縁膜及び該トランジスタのゲート電極となる導電材料膜をこの順番で該半導体基板上に堆積する工程と、
該導電材料膜をパターニングし、それによって該ゲート電極を形成する工程と、
該ゲート電極を覆うように、第２絶縁膜及び、酸化種を透過しにくい第３絶縁膜をこの順番で該半導体基板上に堆積する工程と、
該ｐチャネル型ＭＯＳトランジスタの該ゲート電極を覆うレジストを該ｎ型領域上に形成する工程と、
異方性エッチング技術を用いて、該第３及び第２絶縁膜のうちの該レジストに覆われてない部分をこの順番でエッチングすることによって、該第３及び第２絶縁膜の一部を該ｎチャネル型ＭＯＳトランジスタの該ゲート電極の側面及び該ｎ型領域上に残置させる工程と、
該レジストを除去する工程と、
該ｎチャネル型ＭＯＳトランジスタの該ゲート絶縁膜の端部を更に厚くする酸化工程と、
異方性エッチング技術を用いて、該第３及び第２絶縁膜

をこの順番でエッチングすることによって、該第3及び第2絶縁膜の一部を該pチャネル型MOSトランジスタの該ゲート電極の側面に残置させる工程と、
選択性エッチング技術を用いて、該第3絶縁膜を選択的に除去することによって、該第2絶縁膜からなるL字型サイドウォールを形成する工程と、
該pチャネル型MOSトランジスタを覆うレジストを前記n型領域上に形成する工程と、
該レジスト及び前記nチャネル型MOSトランジスタのゲート電極を注入マスクとして、n型不純物イオンを前記p型領域に注入し、それによって、n型不純物拡散層を形成する第1のn型イオン注入工程と、
該イオン注入工程と連続して、該レジスト及び該nチャネル型MOSトランジスタの該ゲート電極を注入マスクとして、n型不純物イオンを該p型領域に注入し、それによって、該n型不純物拡散層の不純物濃度よりも高濃度の不純物を含み、しかも、該サイドウォールに覆われている第1部分と該サイドウォールに覆われていない第2部分とを有し、該第1部分の厚さが該第2部分の厚さよりも薄い、n型ソース及びドレイン領域を形成し、同時に，n型ゲート電極を形成する第2のn型イオン注入工程と、
該nチャネル型MOSトランジスタを覆うレジストを該p型領域上に形成する工程と、
該レジスト及び前記pチャネル型MOSトランジスタのゲート電極を注入マスクとして、p型不純物イオンを前記n型領域に注入し、それによって、p型不純物拡散層を形成する第1のp型イオン注入工程と、
該イオン注入工程と連続して、該レジスト及び該pチャネル型MOSトランジスタの該ゲート電極を注入マスクとして、p型不純物イオンを該n型領域に注入し、それによって、該p型不純物拡散層の不純物濃度よりも高濃度の不純物を含み、しかも、該サイドウォールに覆われている第1部分と該サイドウォールに覆われていない第2部分とを有し、該第1部分の厚さが該第2部分の厚さよりも薄い、p型ソース及びドレイン領域を形成し、同時に，p型ゲート電極を形成する第2のp型イオン注入工程と、
を包含する製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、微細化された半導体装置及びその製造方法に関する。より詳細には、微細化されたMOS型半導体装置及び相補MOS型半導体装置並びにそれらの製造方法に関する。

【0002】

【従来の技術】VLSIを更に高集積化するために、VLSIに使用されるMOS型半導体装置のサイズは益々微細化され、現在、装置の最小寸法はハーフミクロン領域に迄達している。このような装置の微細化に伴い、装置の電気特性がホットキャリアによって劣化するということが、装置の信頼性上、深刻な問題となっている。ホットキャリアによる装置の劣化に対する耐性を向上し、しかも、駆動能力を向上させるために、ゲート・ドレインオーバラップLDD構造が提案されている。例えばｱｲ､ｲ､ｲ､ｲ､1986ｱｲ､ｲ､ﾃﾞｲ､ｴﾑ(I.E.E.E.1986 I.E.D.M.)Technical Digest pp742-745にT. Y. Hung等によってITLDD構造。また、ｱｲ､ｲ､ｲ､ｲ ﾄﾗﾝｽﾞｱｸｼｮﾝ ｴﾚｸﾄﾛﾝ ﾃﾞﾊﾞｲｽ(I.E.E.E.Transaction on Electron Devices) vol.35, pp2088-2093, 1988にR. Izawa等によってGOLD構造が提案されている。

【0003】図16は、ゲート・ドレインオーバラップLDD構造を有するMOS型トランジスタの断面を示している。

【0004】このトランジスタは、基板31中に形成された高濃度n型ソース・ドレイン拡散層33及び低濃度n型拡散層34と、基板31上に形成されたゲート酸化膜32と、ゲート酸化膜32上に設けられたゲート電極35と、ゲート電極35の両側面に設けられたゲート側壁36とを有している。高濃度ソース・ドレイン拡散層33は、ゲート電極35の端部真下にまで拡散するように形成されており、低濃度n型拡散層34は、ゲート酸化膜32を介してゲート電極と完全にオーバラップしている。従って、低濃度n型拡散層34内の横方向の電界の強度は、ゲート電極35に印加された電位によって充分に緩和され、これによって、ホットキャリアの発生率が減少する。また、低濃度n型拡散層34内のキャリアは完全にゲート電極によって制御されねので、低濃度n型拡散層34のソース抵抗は低減し、素子の駆動能力が向上する。

【0005】

【発明が解決しようとする課題】しかしながら、これらの構造は、ハーフミクロン領域以下のサイズのMOS型トランジスタには適していない。図16に示したMOS型トランジスタは、以下の問題点を有しているからである。

【0006】(1) ゲート電極35がゲート酸化膜32を介して低濃度拡散層34と完全にオーバラップしているので、実効チャネル長L_{eff}は、次の関係を有している。

【0007】$L_{eff} < L_g - 2 \times L_{ldd}$

ここで、L_gはゲート長、L_{ldd}は低濃度拡散層34の幅（チャネル方向に沿って測ったもの）である。

【0008】低濃度n型拡散層34の幅L_{ldd}は、少なくとも0．1μmは必要であるので、ゲート・ドレインオーバラップLDD構造の実効チャネル長L_{eff}は、ゲート長L_gよりも0．2μmは短くなる。従って、ハーフミクロン領域以下のサイズのMOS型トランジスタにおいては、実効チャネル長L_{eff}が0．3μm以下になり、短チャネル効果による素子の初期特性劣化が従来の

ＬＤＤ構造に比べて顕著になる。
【０００９】（２）ゲート電極３５が低濃度拡散層３４とゲート酸化膜３２を介して完全にオーバラップしているのでトランジスタの駆動能力は改善されるが、ゲート・ドレインオーバラップ容量が増大し、ＭＯＳトランジスタを含む回路の動作特性を著しく劣化させる。
【００１０】（３）ゲート酸化膜３２の厚さが１０ｎｍ以下になると、ゲート電圧に誘因するバンド間トンネル電流がリーク電流の新たな原因となる。
【００１１】（４）低濃度ｎ型拡散層と高濃度ソース・ドレイン拡散層を形成するために、少なくとも２回のマスク工程を必要とする。ＣＭＯＳ回路においては、ｐチャネルーＭＯＳ型トランジスタを形成するための同様のマスク工程を含めて、合計４回以上のマスク工程が必要となる。
【００１２】以上の点から、ゲート・ドレインオーバラップ構造を、ハーフミクロン領域以下のサイズを持つＭＯＳ型トランジスタに適用しても、良好なトランジスタ特性を得ることが困難であり、また、ＣＭＯＳ製造工程全体がますます複雑化するという問題がある。
【００１３】一方、従来のＬＤＤ構造のＭＯＳ型半導体装置の製造方法の問題点を、図１７（ａ）～（ｃ）を参照しながら説明する。図１７（ａ）に示すように、ゲート電極３５をマスクとして第２導電型の不純物、例えば、リンイオンを半導体基板表面にイオン注入し、低濃度のソース・ドレイン拡散層３４を形成する。その後、図１７（ｂ）に示すように、酸化膜を２００－２５０ｎｍ程度堆積する。その後、異方性ドライエッチングにより前記酸化膜をゲート電極側部のみに残置させる。ところが、ゲート電極側部に残置する酸化膜３６の幅はドライエッチングの条件に極端に左右され精度良く形成することは困難である。そのため、図１７（ｃ）に示すようにゲート電極側部の酸化膜３６の幅が厚く残置した場合、第２導電型の不純物、例えば、ヒ素イオン注入によって形成されたソース・ドレイン拡散層３３はゲート電極３５の下部に達するように拡散せずオフセット状態になる。
【００１４】その場合、
（１）オーバラップＬＤＤ構造よりも、短チャネル効果は改善されるがホットキャリア耐性は悪くなる。
【００１５】（２）ゲート・ドレインオーバラップ容量は改善されるが、駆動能力は低減する。
【００１６】（３）低濃度拡散層と高濃度拡散層を形成するために２回のマスク工程を必要とする。ｐ－ＭＯＳＦＥＴの形成工程も考えれば４回も必要である。
【００１７】本発明は、上記事情に鑑みてなされたものであり、その目的とするところは、高速で動作し得、しかも短チャネル効果に強く高い信頼性を有する半導体装置（ＭＯＳ型半導体装置及び相補型半導体装置）、並びにその製造方法を提供することにある。
【００１８】
【課題を解決するための手段】本発明による半導体装置は、第１導電型不純物がドープされた第１導電型領域を含み、かつ、主面を有する半導体基板と、該第１導電型領域に設けられたＭＯＳトランジスタと、を備えた半導体装置であって、該ＭＯＳトランジスタは、該第１導電型領域内に形成された第２導電型ソース領域と、該第１導電型領域内に形成され、該第２導電型ソース領域から一定距離だけ離れた第２導電型ドレイン領域と、該第１導電型領域内に形成され、該第２導電型ソース領域と該第２導電型ドレイン領域との間に位置するチャネル領域と、該チャネル領域の両端部に形成され、該第２導電型ソース領域の不純物濃度よりも低い不純物濃度を有する一対の第２導電型不純物拡散層と、該半導体基板の該主面上に形成されたゲート絶縁膜であって、該チャネル領域及び該第２導電型不純物拡散領域を直接に覆っているゲート絶縁膜と、該ゲート絶縁膜上に形成されたゲート電極と、該ゲート電極の側面に設けられたサイドウォールと、を備えており、該サイドウォールは、該ゲート電極の該側面から基板の該主面に沿って伸びる部分を有する形状を有しており、該第２導電型ソース領域及びドレイン領域は、該サイドウォールの該主面に沿って伸びる部分に覆われている第１部分と、該サイドウォールの該主面に沿って伸びる部分に覆われていない第２部分とを有しており、該第１部分の厚さは該第２部分の厚さよりも薄く、それによって上記目的が達成される。
【００１９】前記第２導電型ソース領域及びドレイン領域の前記第１部分は、前記ゲート電極の端部の真下の領域にまで達していることが好ましい。
【００２０】ある実施例では、前記ゲート絶縁膜は、前記一対の第２導電型不純物領域上の部分の厚さが前記チャネル領域上の部分の厚さよりも厚い。
【００２１】本発明による他の半導体装置は、第１導電型不純物がドープされた第１導電型領域を含み、かつ、主面を有する半導体基板と、該第１導電型領域に設けられたＭＯＳトランジスタと、を備えた半導体装置であって、該ＭＯＳトランジスタは、該第１導電型領域内に形成された第２導電型ソース領域と、該第１導電型領域内に形成され、該第２導電型ソース領域から一定距離だけ離れた第２導電型ドレイン領域と、該第２導電型ソース領域と該第１導電型領域との間の接合、及びドレイン領域と該第１導電型領域との間の接合を覆うように設けられ、該第２導電型ソース領域及びドレイン領域の不純物濃度よりも低い不純物濃度を有する一対の第２導電型不純物拡散層と、該第１導電型領域内に形成され、該一対の第２導電不純物拡散層の間に位置するチャネル領域と、該半導体基板の該主面上に形成されたゲート絶縁膜であって、該チャネル領域及を直接に覆っているゲート絶縁膜と、該ゲート絶縁膜上に形成されたゲート電極と、該ゲート電極の側面に設けられたサイドウォール

と、を備えており、該サイドウォールは、該ゲート電極の該側面から基板の該主面に沿って伸びる部分を有する形状を有しており、該部分は、該第２導電型不純物拡散層を直接に覆っており、そのことにより上記目的が達成される。

【００２２】前記第２導電型ソース領域及びドレイン領域は、前記サイドウォールの前記主面に沿って伸びる前記部分の外側端部の真下の領域にまで達していることが好ましい。

【００２３】前記第２導電型不純物拡散層領域は、前記ゲート電極の端部の真下の領域にまで達していることが好ましい。

【００２４】ある実施例では、前記ゲート絶縁膜は、前記一対の第２導電型不純物領域上の部分の厚さが前記チャネル領域上の部分の厚さよりも厚い。

【００２５】本発明による半導体装置の製造方法は、第１導電型不純物がドープされた第１導電型領域を含み、かつ、主面を有する半導体基板と、該第１導電型領域に設けられたMOSトランジスタと、を備えた半導体装置を製造する方法であって、該第１導電型領域を覆うように、該トランジスタのゲート絶縁膜となる第１絶縁膜及び該トランジスタのゲート電極となる導電材料膜をこの順番で該半導体基板上に堆積する工程と、該導電材料膜をパターニングし、それによって該ゲート電極を形成する工程と、該ゲート電極を覆うように、第２絶縁膜及び、酸化種を透過しにくい第３絶縁膜をこの順番で該半導体基板上に堆積する工程と、異方性エッチング技術を用いて、該第３及び第２絶縁膜をこの順番でエッチングすることによって、該第３及び第２絶縁膜の一部を該ゲート電極の側面に残置させる工程と、選択性エッチング技術を用いて、該第３絶縁膜を選択的に除去することによって、該第２絶縁膜からなるL字型サイドウォールを形成する工程と、該ゲート電極を注入マスクとして、第２導電型不純物イオンを該半導体基板に注入し、それによって、第２導電型不純物拡散層を形成する第１イオン注入工程と、該ゲート電極を注入マスクとして、第２導電型不純物イオンを該半導体基板に注入し、それによって、該第２導電型不純物拡散層の不純物濃度よりも高濃度の不純物を含み、しかも、該サイドウォールに覆われている第１部分と該サイドウォールに覆われていない第２部分とを有し、該第１部分の厚さが該第２部分の厚さよりも薄い、第２導電型ソース及びドレイン領域を形成する第２イオン注入工程と、を包含し、そのことによって上記目的が達成される。

【００２６】ある実施例では、前記選択性エッチング技術を用いて前記L字型サイドウォールを形成する前記工程の前に、前記ゲート絶縁膜の端部を更に厚くする酸化工程を包含する。

【００２７】本発明による半導体装置の他の製造方法は、第１導電型不純物がドープされた第１導電型領域を含み、かつ、主面を有する半導体基板と、該第１導電型領域に設けられたMOSトランジスタと、を備えた半導体装置を製造する方法であって、該第１導電型領域を覆うように、ゲート絶縁膜となる第１絶縁膜及びゲート電極となる導電材料膜をこの順番で該半導体基板上に堆積する工程と、該導電材料膜をパターニングし、それによってゲート電極を形成する工程と、該ゲート電極を覆うように、第２絶縁膜及び、酸化種を透過しにくい第３絶縁膜をこの順番で該半導体基板上に堆積する工程と、異方性エッチング技術を用いて、該第３及び第２絶縁膜をこの順番でエッチングすることによって、該第３及び第２絶縁膜の一部を該ゲート電極の側面に残置させる工程と、選択性エッチング技術を用いて、該第３絶縁膜を選択的に除去することによって、第２絶縁膜からなるL字型サイドウォールを形成する工程と、該ゲート電極及び該サイドウォールを注入マスクとして、該サイドウォールを透過し得ない加速エネルギにて第２導電型不純物イオンを該半導体基板に注入し、それによって、該ゲート電極及び該サイドウォールに実質的に覆われてない領域に第２導電型ソース及びドレイン領域を形成する第１イオン注入工程と、該ゲート電極を注入マスクとして、該サイドウォールを透過し得る加速エネルギにて第２導電型不純物イオンを該半導体基板に注入し、それによって、該第２導電型ソース及びドレイン領域の不純物濃度よりも低濃度の不純物を含み、しかも、該第２導電型ソース及びドレイン領域の厚さよりも厚い第２導電型不純物拡散層を形成する第２イオン注入工程と、を包含し、そのことにより上記目的が達成される。

【００２８】ある実施例では、前記選択性エッチング技術を用いて前記L字型サイドウォールを形成する前記工程の前に、前記ゲート絶縁膜の端部を更に厚くする酸化工程を包含する。

【００２９】本発明による相補形半導体装置は、n型不純物がドープされたn型領域及び第p型不純物がドープされたp型領域を含み、かつ、主面を有する半導体基板と、該p型領域に設けられたnチャネル型MOSトランジスタと、該n型領域に設けられたpチャネル型MOSトランジスタと、を備えた相補型半導体装置であって、該nチャネル型MOSトランジスタは、該p型領域内に形成されたn型ソース領域と、該p型領域内に形成され、該n型ソース領域から一定距離だけ離れたn型ドレイン領域と、該p型領域内に形成され、該n型ソース領域と該n型ドレイン領域との間に位置するチャネル領域と、該チャネル領域の両端部に形成され、該n型ソース領域の不純物濃度よりも低い不純物濃度を有する一対のn型不純物拡散層と、該半導体基板の該主面上に形成されたゲート絶縁膜であって、該チャネル領域及び該一対のn型不純物領域を直接に覆い、該一対のn型不純物領域上の部分の厚さが、該チャネル領域上の部分の厚さよりも厚いゲート絶縁膜と、該ゲート絶縁膜上に形成され

たゲート電極と、を備えており、該pチャネル型MOSトランジスタは、該n型領域内に形成された第1導電型ソース領域と、該n型領域内に形成され、該p型ソース領域から一定距離だけ離れたp型ドレイン領域と、該n型領域内に形成され、該p型ソース領域と該p型ドレイン領域との間に位置するチャネル領域と、該半導体基板の該主面上に形成されたゲート絶縁膜であって、均一な厚さを有するゲート絶縁膜と、該ゲート絶縁膜上に形成されたゲート電極と、を備えており、そのことにより上記目的が達成される。

【0030】ある実施例では、前記nチャネル型MOSトランジスタ及び前記pチャネル型MOSトランジスタの少なくとも一方は、前記ゲート電極の側面に設けられたサイドウォールであって、該ゲート電極の該側面から前記半導体基板の前記主面に沿って伸びる部分を有する形状を有するサイドウォールを備えており、前記n型ソース領域及びドレイン領域は、該サイドウォールの該主面に沿って伸びる部分に覆われている第1部分と、該サイドウォールの該主面に沿って伸びる部分に覆われていない第2部分とを有しており、該第1部分の厚さは該第2部分の厚さよりも薄い。

【0031】前記第2導電型ソース領域及びドレイン領域の前記第1部分は、前記ゲート電極の端部の真下の領域にまで達していることが好ましい。

【0032】ある実施例では、前記pチャネル型MOSトランジスタの前記チャネル領域は、第1導電型の埋め込み型チャネル構造を有している。

【0033】ある実施例では、前記pチャネル型MOSトランジスタの前記ゲート電極は、第1導電型ゲート電極である。

【0034】本発明による相補形半導体装置の製造方法は、n型不純物がドープされたn型領域及び第p型不純物がドープされたp型領域を含み、かつ、主面を有する半導体基板と、該p型領域に設けられたnチャネル型MOSトランジスタと、該n型領域に設けられたpチャネル型MOSトランジスタと、を備えた相補型半導体装置を製造する方法であって、該p型領域及び該n型領域を覆うように、該トランジスタのゲート絶縁膜となる第1絶縁膜及び該トランジスタのゲート電極となる導電材料膜をこの順番で該半導体基板上に堆積する工程と、該導電材料膜をパターニングし、それによって該ゲート電極を形成する工程と、該ゲート電極を覆うように、第2絶縁膜及び、酸化種を透過しにくい第3絶縁膜をこの順番で該半導体基板上に堆積する工程と、該pチャネル型MOSトランジスタの該ゲート電極を覆うレジストを該n型領域上に形成する工程と、異方性エッチング技術を用いて、該第3及び第2絶縁膜のうちの該レジストに覆われてない部分をこの順番でエッチングすることによって、該第3及び第2絶縁膜の一部を該nチャネル型MOSトランジスタの該ゲート電極の側面及び該n型領域上に残置させる工程と、該レジストを除去する工程と、該nチャネル型MOSトランジスタの該ゲート絶縁膜の端部を更に厚くする酸化工程と、異方性エッチング技術を用いて、該第3及び第2絶縁膜をこの順番でエッチングすることによって、該第3及び第2絶縁膜の一部を該pチャネル型MOSトランジスタの該ゲート電極の側面に残置させる工程と、選択性エッチング技術を用いて、該第3絶縁膜を選択的に除去することによって、該第2絶縁膜からなるL字型サイドウォールを形成する工程と、を包含し、そのことにより上記目的が達成される。

【0035】前記pチャネル型MOSトランジスタを覆うレジストを前記n型領域上に形成する工程と、該レジスト及び前記nチャネル型MOSトランジスタのゲート電極を注入マスクとして、n型不純物イオンを前記p型領域に注入し、それによって、n型不純物拡散層を形成する第1のn型イオン注入工程と、該レジスト及び該nチャネル型MOSトランジスタの該ゲート電極を注入マスクとして、n型不純物イオンを該p型領域に注入し、それによって、該n型不純物拡散層の不純物濃度よりも高濃度の不純物を含み、しかも、該サイドウォールに覆われている第1部分と該サイドウォールに覆われていない第2部分とを有し、該第1部分の厚さが該第2部分の厚さよりも薄い、n型ソース及びドレイン領域を形成する第2のn型イオン注入工程と、を更に包含することが好ましい。

【0036】前記nチャネル型MOSトランジスタを覆うレジストを前記p型領域上に形成する工程と、該レジスト及び前記pチャネル型MOSトランジスタのゲート電極を注入マスクとして、p型不純物イオンを前記n型領域に注入し、それによって、前記サイドウォールに覆われている第1部分と該サイドウォールに覆われていない第2部分とを有し、該第1部分の厚さが該第2部分の厚さよりも薄い、p型ソース及びドレイン領域を形成するp型イオン注入工程を更に包含することが好ましい。

【0037】

【実施例】以下に、図面を参照しながら、本発明による半導体装置およびその製造方法を説明する。

【0038】（実施例1）図1は、本発明の半導体装置（第1の実施例）の断面図である。この半導体装置は、p型（第1導電型）不純物がドープされているp型半導体基板1に設けられたMOSトランジスタを含む半導体装置である。

【0039】このMOSトランジスタは、半導体（シリコン）基板1中に形成された高濃度n型ソース・ドレイン拡散層3と、ソース拡散層3とドレイン拡散層3との間に位置するチャネル領域と、を有している。チャネル領域の両端部には、ソース・ドレイン拡散層3のn型不純物濃度よりも低いn型不純物濃度を有する一対の低濃度n型不純物拡散層（低濃度n型ソース・ドレイン拡散層）4が形成されている。

【００４０】半導体基板１の主面上には、チャネル領域及び低濃度ｎ型不純物拡散層４を直接に覆うように、ゲート絶縁膜２が形成されている。ゲート絶縁膜２上には、ゲート電極５が形成されている。ゲート電極５の両側面にはＬ型側壁６が形成されている。このＬ型側壁６は、ゲート電極５の側面から半導体基板１１の主面に沿って伸びる部分を有する形状を有している。高濃度ｎ型ソース・ドレイン拡散層３のそれぞれは、Ｌ型側壁の主面に沿って伸びる部分によって覆われている第１部分と、覆われていない第２部分とを有している。図１に示されているように、この第１部分の厚さ（接合深さＤ１）は、第２部分の厚さ（接合深さＤ２）よりも薄くなっている。

【００４１】本実施例の特徴的なことの一つは、接合深さＤ１が、接合深さＤ２よりも浅く形成され、かつ低濃度ｎ型ソース・ドレイン拡散層４の接合深さＤ３が接合深さＤ１と同等かそれよりも浅く形成されていることである。このため、従来のオーバラップＬＤＤ構造よりもソース・ドレイン拡散層からチャネル方向へのポテンシャルの広がりが効果的に抑えられる。その結果、ハーフミクロン領域以下の微細化に問題となるＭＯＳＦＥＴ特有のＶｔの低下が効果的に抑制される。

【００４２】また、ソース・ドレイン拡散層３は、ゲート電極５の端部の真下にまで拡散しており、低濃度ｎ型不純物拡散層４は、ゲート絶縁膜２を介してゲート電極５と完全にオーバラップする位置にある。このため、オーバラップＬＤＤ構造と同様に、低濃度ｎ型ソース・ドレイン拡散層４内の横方向の電界はゲート電極に印加された電位によって充分に緩和される。

【００４３】また、Ｌ型側壁６を通してイオン注入された高濃度のソース・ドレイン拡散層の不純物濃度は、Ｌ型側壁の真下で$10^{19}cm^{-3}$程度の低い値となる。このため、横方向電界の強度はさらに緩和され、オーバラップ量を減少させることができる。

【００４４】また、ゲート電極５の外側に位置する酸化膜（Ｌ型側壁６）内にトラップされた電子やそこに発生した界面準位は、高濃度拡散層３の上に位置するため、素子特性の劣化を加速することはない。これによって、ホットキャリアの発生率が減少する。また、低濃度ｎ型不純物拡散層４内のキャリアは、ゲート電極によて完全に制御され、しかも、低濃度ｎ型不純物拡散層４の抵抗（ソース抵抗）は低減され、それによって、素子の駆動能力が向上する。

【００４５】図９は、本発明の第１の実施例における不純物濃度分布等高線図である。これは、以下に示す条件の基でシミュレーションを行った結果得られたものである。すなわち、図９の例では、ゲート側部の幅が５０ｎｍで、半導体基板に接する部分の長さが１５０ｎｍで、厚さが４０ｎｍのＬ型側壁を透過して、ヒ素イオンを注入エネルギーが８０ＫｅＶ、注入ドーズ量が$6\times10^{15}cm^{-2}$でイオン注入し、それによって高濃度ソース・ドレイン拡散層を形成している。また、ヒ素注入に連続して、リンイオンを注入エネルギーが６０ＫｅＶ、注入ドーズ量$4\times10^{13}cm^{-2}$で注入し、それによって低濃度ソース・ドレイン拡散層を形成している。

【００４６】図９から分かるように、Ｌ型側壁の真下の高濃度ソース・ドレイン拡散層の接合深さは、Ｌ型側壁の外側の高濃度ソース・ドレイン拡散層の接合深さよりも浅く形成され、Ｌ型側壁直下では高濃度ソース・ドレイン拡散層の濃度は、$10^{19}cm^{-3}$程度に低下している。また、ゲート電極下部における低濃度ソース・ドレイン拡散層は、そのの接合深さがＬ型側壁下部の高濃度ソース・ドレイン拡散層の接合深さと同程度になるように、形成されている。

【００４７】（実施例２）図２は、本発明の半導体装置（第２の実施例）の断面図である。

【００４８】図２の半導体装置と図１の半導体装置との間の構造上の主要な相違点は、図２の半導体装置のゲート電極５ｂが下に凸な構造を有している点にある。言い替えれば、ゲート酸化膜２の端部の厚さが、中央部の厚さよりも厚くなっている。なお、ゲート電極５ｂの端部は、ゲート酸化膜２を介して低濃度拡散層４にオーバラップしている。低濃度ｎ型不純物拡散層４とゲート電極５ｂとの間のゲート酸化膜２の厚さが、チャネル領域上部のゲート酸化膜２の厚さよりも厚いため、ゲート・ドレインオーバラップ容量は、従来のゲート・ドレインオーバラップＬＤＤ構造のオーバラップ容量よりも小さい。従って、回路動作の速度が向上し、高速で動作し得る半導体集積回路が実現される。さらに、ゲート電圧に誘因するバンド間トンネル電流を低減することができる。しかも、第１の実施例と同様に、短チャネル効果に強くホットキャリア劣化耐性に強い高信頼性半導体装置を得ることができる。

【００４９】（実施例３）図３は、本発明の他の半導体装置（第３の実施例）の断面図を示す。

【００５０】図３の実施例で特徴的なことの一つは、第２導電型の低濃度拡散層４がゲート酸化膜２を介してゲート電極５の端部に達するように形成されていることである。このため、本実施例のＭＯＳ型半導体装置の実効チャネル長は、ゲート電極５の長さとほぼ等しくなる。また、第２導電型の高濃度ソース・ドレイン拡散層３の接合深さが低濃度拡散層４の接合深さよりも浅く形成され、かつ、Ｌ型ゲート側壁６の端部に達するように形成されていることで、ソース・ドレイン拡散層からのポテンシャルのチャネル方向への広がりを効果的に抑え、ハーフミクロン領域いかの微細化に問題となる初期特性のしきい値の劣化（Ｖｔ低下）を抑制している。

【００５１】（実施例４）図４は、本発明の半導体装置（第４の実施例）の断面図を示す。

【００５２】図４の半導体装置と図３の半導体装置との

間の構造上の主要な相違点は、図４の半導体装置のゲート電極５ｂが下に凸の構造を持っていることである。そのため、ゲート酸化膜２の厚みはゲート電極端部で厚くなっている。さらにゲート電極５ｂの凸部の端部がゲート酸化膜２を介して低濃度拡散層４に達している。このため、低濃度拡散層４とゲート電極５ｂの間の酸化膜２はチャネル上部の酸化膜よりも厚くなりゲート・ドレインオーバラップ容量は、従来のゲート・ドレインオーバラップＬＤＤ構造のオーバラップ容量よりも小さくなる。従って、回路速度を向上し高速な半導体回路を実現できる。さらに、ゲート電圧に誘因するバンド間トンネル電流を低減することができる。しかも、図３の実施例と同様に、短チャネル効果に強くハーフミクロン領域以下の微細化に適した半導体装置を得る。

【００５３】第１及び第２の従来例と実施例１から４の半導体装置とについて、各特性の評価を行った。下記の表１は、その評価結果を示している。この表１において、記号◎は「非常に良い」を意味し、○は「良い」を意味し、△は「良くも悪くもない」を意味し、×は「悪い」を意味している。

【００５４】

【表１】

	短チャネル効果抑制	回路特性（オーバラップ容量）	駆動能力	ホットキャリア抑制	バンド間トンネルリーク抑制	マスク工程改善
実施例1	◎	○	◎	◎	×	◎
実施例2	◎	◎	○	◎	◎	◎
実施例3	○	○	×	△	○	◎
実施例4	◎	○	×	△	◎	◎
従来例1（オーバラップLDD）	×	○	◎	◎	×	×
従来例2（LDD）	×	×	×	△	○	×

【００５５】（実施例５）図５（ａ）～（ｃ）を参照しながら、図１に示す半導体装置を製造する方法の実施例を説明する。

【００５６】まず、図５（ａ）に示すように、ｐ型半導体基板１の一主面上にゲート酸化膜２を形成した後、ゲート酸化膜２上にゲート電極５を形成する。この後、酸化膜（厚さ：４０ｎｍ程度）６’を半導体基板１上に堆積して、ゲート電極５を覆うようにする。更に、酸化膜６’の材質とは異なる材質の絶縁膜、たとえば、窒化膜（厚さ：１００ｎｍ程度）７を酸化膜６’上に堆積する。

【００５７】次に、図５（ｂ）に示すように、異方性ドライエッチングによって酸化膜６’及び窒化膜７をエッチングすることにより、ゲート電極５の側面にのみ酸化膜６’及び窒化膜７の一部を残置させる。

【００５８】次に、選択性エッチング、例えば、熱リン酸溶液を用いたエッチングによって、残置されたされた窒化膜７を完全に除去し、それによってＬ型側壁６’を形成する。このとき、プラズマ等を用いた異方性ドライエッチングではなく、選択性エッチングを行うことによって、窒化膜７のみを選択的に除去し、酸化膜６’をほとんどエッチングしないようにする。このようにして、特別マスクを使用せずに、酸化膜からなるＬ型側壁６をゲート電極５の側壁に形成することができる。Ｌ型側壁６は、図５（ｂ）に示されるように、ゲート電極５の側面から半導体基板１の主面に沿って外方に伸びている部分を有している。この部分をチャネル方向に沿って計測したサイズは、窒化膜７の堆積厚さを制御することにより高い精度で調整される。

【００５９】次に、図５（ｃ）に示すように、第２導電型の不純物、例えば、注入ドーズ量6×10^{15}ｃｍ$^{-2}$程度のヒ素イオンを加速エネルギー８０ＫｅＶで半導体基板１に注入し、それによって高濃度ソース・ドレイン拡散層３を形成する。このイオン注入工程で、ヒ素イオンの一部は、Ｌ型側壁６のゲート電極５側面から半導体基板１の主面に沿って外方に伸びている部分を透過して、半導体基板１内に注入され、それによって高濃度ソース・ドレイン拡散層３の相対的に薄い部分が形成される。また、このとき同時に、ヒ素イオンの他の部分は、Ｌ型側壁６を透過することなく、直接に半導体基板１内に注入され、それによって高濃度ソース・ドレイン拡散層３の相対的に厚い部分が形成される。こうして、Ｌ型側壁６の真下のソース・ドレイン拡散層３の接合深さは、Ｌ型側壁６の外側の接合深さよりも浅く形成される。Ｌ型側壁６の幅は、窒化膜７の厚さを制御することによって、高い精度で所望の幅に調整されているので、ソース・ドレイン拡散層３の端部の位置は、ゲート電極５の端部の真下にまで達するように高い精度で拡散され得る。

【0060】前記ヒ素イオン注入工程に連続して、第2導電型の不純物、例えば、ドーズ量4×1013cm-2程度のリンイオンを加速エネルギー70KeVで半導体基板1中に注入し、低濃度拡散層4を形成する。この注入は、注入イオンビームと半導体基板1の主面との間の角度が45度になるように行われる。この注入に際して、リンイオンの一部は、L型側壁6を透過して、大仰角（＝45度）で半導体基板1に注入されるので、低濃度拡散層4の接合深さはL型側壁6の真下部のソース・ドレイン拡散層3の接合深さと同等かそれよりも浅く形成される。

【0061】図9は本発明の半導体装置についてシミュレーションを行った結果得られた不純物濃度分布等高線図である。図9の例では、L型側壁を透過して、6×1015cm-2のドーズ量のヒ素イオンを加速エネルギー80KeVで半導体基板1に注入し、それによって高濃度ソース・ドレイン拡散層3を形成した。また、連続してドーズ量4×1013cm-2のリンイオンを加速エネルギー60KeVで注入し、それによって低濃度ソース・ドレイン拡散層を形成した。

【0062】図9からわかるように、L型側壁下部の高濃度ソース・ドレイン拡散層の接合深さは、L型側壁の外側の高濃度ソース・ドレイン拡散層の接合深さよりも浅く形成され、L型側壁直下では濃度が1019cm-3程度に低下している。また、ゲート電極下部の低濃度ソース・ドレイン拡散層の接合深さは、L型側壁下部の高濃度ソース・ドレイン拡散層の接合深さと同程度に形成されている。

【0063】図10は、本実施例の方法により製造された半導体装置の断面TEM写真に基づいて作成した図である。図10で、1は半導体基板（p型）、5はゲート電極、6はL型の側壁である。図10から分かるように、L型側壁が精度良く形成されている。

【0064】本実施例によれば、図1の半導体装置を精度良く、しかも1回のマスキングステップで高濃度ソース・ドレイン拡散層と低濃度ソース・ドレン拡散層を効率良く形成することができる。

【0065】（実施例6）図6（a）～（d）を参照しながら、図2の半導体装置を製造する方法の実施例を説明する。

【0066】まず、図6（a）に示すように、p型半導体基板1の一主面上にゲート酸化膜2を形成した後、ゲート酸化膜2上にゲート電極5bを形成する。この後、酸化膜（厚さ：40nm程度）6’を半導体基板1上に堆積して、ゲート電極5bを覆うようにする。更に、酸素を透過しない絶縁膜、たとえば、窒化膜（厚さ：100nm程度）7を酸化膜6’上に堆積する。この後、異方性ドライエッチングによって酸化膜6’及び窒化膜7をエッチングすることにより、ゲート電極5の側面にのみ酸化膜6’及び窒化膜7の一部を残置させる。

【0067】次に、図6（b）に示すようにウエット酸化工程により酸化膜（厚さ：30nm程度）8を形成する。この時、酸化種を透過させない窒化膜7がゲート電極5a側面に残置しているので、ゲート電極5bの側部はほとんど酸化されず、ゲート電極側部の酸化膜6が露出している部分から透過した酸化種によってゲート電極5bは下に凸に酸化される。

【0068】次に、図6（c）に示すように、選択性エッチング、例えば、熱リン酸溶液を用いたエッチングによって、残置されたされた窒化膜7を完全に除去し、それによってL型側壁6’を形成する。このとき、プラズマ等を用いた異方性ドライエッチングではなく、選択性エッチングを行うことによって、窒化膜7のみを選択的に除去し、酸化膜6’をほとんどエッチングしないようにする。このようにして、特別マスクを使用せずに、酸化膜からなるL型側壁6をゲート電極5bの側壁に形成することができる。L型側壁6は、図6（b）に示されるように、ゲート電極5bの側面から半導体基板1の主面に沿って外方に伸びている部分を有している。この部分をチャネル方向に沿って計測したサイズは、窒化膜7の堆積厚さを制御することにより高い精度で調整される。

【0069】次に、第2導電型の不純物、例えば、注入ドーズ量6×1015cm-2程度のヒ素イオンを加速エネルギー80KeVで半導体基板1に注入し、それによって高濃度ソース・ドレイン拡散層3を形成する。このイオン注入工程で、ヒ素イオンの一部は、L型側壁6のゲート電極5bの側面から半導体基板1の主面に沿って外方に伸びている部分を透過して、半導体基板1内に注入され、それによって高濃度ソース・ドレイン拡散層3の相対的に薄い部分が形成される。また、このとき同時に、ヒ素イオンの他の部分は、L型側壁6を透過することなく、直接に半導体基板1内に注入され、それによって高濃度ソース・ドレイン拡散層3の相対的に厚い部分が形成される。こうして、L型側壁6の真下のソース・ドレイン拡散層3の接合深さは、L型側壁6の外側の接合深さよりも浅く形成される。L型側壁6の幅は、窒化膜7の厚さを制御することによって、高い精度で所望の幅に調整されているので、ソース・ドレイン拡散層3の端部の位置は、ゲート電極5の端部の真下にまで達するように高い精度で拡散され得る。

【0070】前記ヒ素イオン注入工程に連続して、第2導電型の不純物、例えば、ドーズ量4×1013cm-2程度のリンイオンを加速エネルギー70KeVで半導体基板1中に注入し、低濃度拡散層4を形成する。この注入は、注入イオンビームと半導体基板1の主面との間の角度が45度になるように行われる。この注入に際して、リンイオンの一部は、L型側壁6を透過して、大仰角（＝45度）で半導体基板1に注入されるので、低濃度拡散層4の接合深さはL型側壁6の真下部のソース・ド

レイン拡散層3の接合深さと同等かそれよりも浅く形成される。

【0071】以上より、本実施例によれば、ゲート電極側部を酸化することなく下に凸なゲート電極を効果的に形成することができる。しかも1回のマスキングステップで高濃度ソース・ドレイン拡散層と低濃度ソース・ドレイン拡散層を効率良く形成することができる。

【0072】（実施例7）図7（a）～（c）を参照しながら、図3に示す半導体装置を製造する方法の実施例を説明する。

【0073】まず、図7（a）に示すように、p型半導体基板1の一主面上にゲート酸化膜2を形成した後、ゲート酸化膜2上にゲート電極5を形成する。この後、酸化膜（厚さ：40nm程度）6’を半導体基板1上に堆積して、ゲート電極5を覆うようにする。更に、酸化膜6’の材質とは異なる材質の絶縁膜、たとえば、窒化膜（厚さ：100nm程度）7を酸化膜6’上に堆積する。

【0074】次に、図7（b）に示すように、異方性ドライエッチングによって酸化膜6’及び窒化膜7をエッチングすることにより、ゲート電極5の側面にのみ酸化膜6’及び窒化膜7の一部を残置させる。

【0075】次に、選択性エッチング、例えば、熱リン酸溶液を用いたエッチングによって、残置されたされた窒化膜7を完全に除去し、それによってL型側壁6’を形成する。このとき、プラズマ等を用いた異方性ドライエッチングではなく、選択性エッチングを行うことによって、窒化膜7のみを選択的に除去し、酸化膜6’をほとんどエッチングしないようにする。このようにして、特別マスクを使用せずに、酸化膜からなるL型側壁6をゲート電極5の側壁に形成することができる。L型側壁6は、図7（b）に示されるように、ゲート電極5の側面から半導体基板1の主面に沿って外方に伸びている部分を有している。この部分をチャネル方向に沿って計測したサイズは、窒化膜7の堆積厚さを制御することにより高い精度で調整される。

【0076】次に、図7（c）に示すように、第2導電型の不純物、例えば、注入ドーズ量6×1015cm-2程度のヒ素イオンを加速エネルギー40KeVで半導体基板1に注入し、それによって高濃度ソース・ドレイン拡散層3を形成する。このイオン注入工程で、ヒ素イオンの一部は、L型側壁6のゲート電極5側面から半導体基板1の主面に沿って外方に伸びている部分によってブロックされる。このとき同時に、ヒ素イオンの他の部分は、L型側壁6を透過することなく、直接に半導体基板1内に注入され、それによって高濃度ソース・ドレイン拡散層3が形成される。上記ヒ素イオン注入は、低加速エネルギにて行われるため、L型側壁6の真下には、ソース・ドレイン拡散層3が形成されず、また、ソース・ドレイン拡散層3の接合深さは0．1μm程度に浅く形成される。

【0077】次に図7（d）に示すように、前記ヒ素イオン注入に連続して、第2導電型の不純物、例えば、注入ドーズ量4×1013cm-2程度のリンイオンを加速エネルギー60KeVで半導体基板2内に注入し、低濃度拡散層4を形成する。この時、リンイオンは、前記ヒ素イオンよりも高い加速エネルギーで半導体基板1に注入されるので、L型側壁6を透過し得て、低濃度拡散層4はゲート電極5の端部真下にまで達する。

【0078】以上より、本実施例によれば、精度良く、しかも1回のマスキングステップで高濃度ソース・ドレイン拡散層と低濃度ソース・ドレイン拡散層を効率良く形成することができる。

【0079】（実施例8）図8（a）～（d）を参照しながら、図4の半導体装置を製造する方法の実施例を説明する。

【0080】まず、図8（a）に示すように、p型半導体基板1の一主面上にゲート酸化膜2を形成した後、ゲート酸化膜2上にゲート電極5bを形成する。この後、酸化膜（厚さ：40nm程度）6’を半導体基板1上に堆積して、ゲート電極5を覆うようにする。更に、酸素を透過しない絶縁膜、たとえば、窒化膜（厚さ：100nm程度）7を酸化膜6’上に堆積する。この後、異方性ドライエッチングによって酸化膜6’及び窒化膜7をエッチングすることにより、ゲート電極5の側面にのみ酸化膜6’及び窒化膜7の一部を残置させる。

【0081】次に、図8（b）に示すようにウエット酸化工程により酸化膜（厚さ：30nm程度）8を形成する。この時、酸化種を透過させない窒化膜7がゲート電極5b側面に残置しているので、ゲート電極5bの側部はほとんど酸化されず、ゲート電極側部の酸化膜6が露出している部分から透過した酸化種によってゲート電極5bは下に凸に酸化される。

【0082】次に、図8（c）に示すように、選択性エッチング、例えば、熱リン酸溶液を用いたエッチングによって、残置されたされた窒化膜7を完全に除去し、それによってL型側壁6を形成する。このとき、プラズマ等を用いた異方性ドライエッチングではなく、選択性エッチングを行うことによって、窒化膜7のみを選択的に除去し、酸化膜6’をほとんどエッチングしないようにする。このようにして、特別マスクを使用せずに、酸化膜からなるL型側壁6をゲート電極5bの側壁に形成することができる。L型側壁6は、図8（b）に示されるように、ゲート電極5bの側面から半導体基板1の主面に沿って外方に伸びている部分を有している。この部分をチャネル方向に沿って計測したサイズは、窒化膜7の堆積厚さを制御することにより高い精度で調整される。

【0083】次に、図8（c）に示すように、第2導電型の不純物、例えば、注入ドーズ量6×1015cm-2程度のヒ素イオンを加速エネルギー40KeVで半導体基

板1に注入し、それによって高濃度ソース・ドレイン拡散層3を形成する。このイオン注入工程で、ヒ素イオンの一部は、L型側壁6のゲート電極5b側面から半導体基板1の主面に沿って外方に伸びている部分によってブロックされる。このとき同時に、ヒ素イオンの他の部分は、L型側壁6を透過することなく、直接に半導体基板1内に注入され、それによって高濃度ソース・ドレイン拡散層3が形成される。上記ヒ素イオン注入は、低加速エネルギにて行われるため、L型側壁6の真下には、ソース・ドレイン拡散層3が形成されず、また、ソース・ドレイン拡散層3の接合深さは0．1μm程度に浅く形成される。

【0084】次に図8（d）に示すように、前記ヒ素イオン注入に連続して、第2導電型の不純物、例えば、注入ドーズ量4×1013cm-2程度のリンイオンを加速エネルギ60KeVで半導体基板2内に注入し、低濃度拡散層4を形成する。この時、リンイオンは、前記ヒ素イオンよりも高い加速エネルギーで半導体基板1に注入されるので、L型側壁6を透過し得て、低濃度拡散層4はゲート電極5bの端部真下にまで達する。

【0085】以上より、本実施例によれば、ゲート電極側部を酸化することなく下に凸なゲート電極5bを効果的に形成することができる。しかも1回のマスキングステップで高濃度ソース・ドレイン拡散層と低濃度ソース・ドレイン拡散層を効率良く形成することができる。

【0086】以下に、図面を参照しながら、本発明による相補型半導体装置およびその製造方法を説明する。

【0087】（実施例9）図11は、本発明の相補型半導体装置の断面を示している。

【0088】半導体基板19は、n型不純物がドープされたn型領域（nウェル）18及びp型不純物がドープされたp型領域を含んでいる。半導体基板19の素子分離領域には、トランジスタを相互に電気的に分離するためのLOCOS分離13が形成されている。

【0089】半導体基板19のp型領域には、nチャネル型MOSトランジスタが形成され、nウェル18にはpチャネル型MOSトランジスタが形成されている。nチャネル型MOSトランジスタは、半導体基板19のp型領域中に形成されたn型高濃度ソース・ドレイン拡散層14と、半導体基板19上に形成されたゲート絶縁膜20と、ゲート絶縁膜20上に形成されたゲート電極11と、ゲート電極11の側壁に設けられたL型ゲート側壁酸化膜12とを備えている。また、n型高濃度ソース・ドレイン拡散層14のチャネル側端部には、n型低濃度ソース・ドレイン拡散層16が設けられている。ゲート絶縁膜20は、チャネル領域を覆う比較的薄い部分と、n型低濃度ソース・ドレイン拡散層6’を覆う比較的厚い部分とを有している。このnチャネル型MOSトランジスタの構成は、図2に示されているものと実質的に同じである。

【0090】一方、pチャネル型MOSトランジスタは、半導体基板19のnウェル18中に形成されたp型高濃度ソース・ドレイン拡散層16と、nウェル18上に形成されたゲート絶縁膜20と、ゲート絶縁膜20上に形成されたゲート電極11と、ゲート電極11の側壁に設けられたL型ゲート側壁酸化膜12とを備えている。また、p型高濃度ソース・ドレイン拡散層15のチャネル側端部には、p型低濃度ソース・ドレイン拡散層17が設けられている。このpチャネル型MOSトランジスタのゲート絶縁膜20は、nチャネル型MOSトランジスタのゲート絶縁膜20とは異なり、均一な厚さを有している。

【0091】高濃度ソース・ドレイン拡散層14、15のL型側壁2の真下における接合深さD1は、L型側壁12の下部以外の接合深さD2よりも浅く形成され、かつ、低濃度拡散層16、17の接合深さD3がL型側壁2下部の高濃度ソース・ドレイン拡散層14、15の接合深さD1と同等かそれよりも浅く形成されている。このため、ソース・ドレイン拡散層からのポテンシャルのチャネル方向への広がりが効果的に抑えられ、微細MOSトランジスタ特有のVtの低下が効果的に抑制される。

【0092】また、nチャネル型MOSトランジスタの低濃度ソース・ドレイン拡散層16がゲート絶縁膜20の両端の厚いゲート酸化膜10の下面に拡散していることにより、ドレイン電流を下げることなくゲート・ドレイン容量とゲート・ソース容量を減少させ、ゲート電極1による垂直電界により低濃度ソース・ドレイン拡散層6の水平電界の緩和を行なうことができる。一方、ホットキャリア劣化耐性が良く、駆動力が低く、短チャネル効果を誘発しやすいp型MOSトランジスタでは、均一なゲート絶縁膜20を持ち、低濃度ソース・ドレイン拡散層を小さくとり、実効チャネル長を長くとることによって寄生抵抗の減少と短チャネル効果の抑制を行なうことができる。

【0093】（実施例10）図12は、本発明の他の相補型半導体装置の断面を示している。

【0094】半導体基板19は、n型不純物がドープされたn型領域（nウェル）18及びp型不純物がドープされたp型領域を含んでいる。半導体基板19の素子分離領域には、トランジスタを相互に電気的に分離するためのLOCOS分離13が形成されている。

【0095】半導体基板19のp型領域には、nチャネル型MOSトランジスタが形成され、nウェル18にはpチャネル型MOSトランジスタが形成されている。nチャネル型MOSトランジスタは、半導体基板19のp型領域中に形成されたn型高濃度ソース・ドレイン拡散層14と、半導体基板19上に形成されたゲート絶縁膜20と、ゲート絶縁膜20上に形成されたゲート電極11aと、ゲート電極11aの側壁に設けられたL型ゲー

ト側壁酸化膜１２とを備えている。また、ｎ型高濃度ソース・ドレイン拡散層１４のチャネル側端部には、ｎ型低濃度ソース・ドレイン拡散層１６が設けられている。ゲート絶縁膜２０は、チャネル領域を覆う比較的厚さ薄い部分と、ｎ型低濃度ソース・ドレイン拡散層１６を覆う比較的厚い部分とを有している。

【００９６】一方、ｐチャネル型ＭＯＳトランジスタは、半導体基板１９のｎウエル１８中に形成されたｐ型高濃度ソース・ドレイン拡散層１８と、ｎウエル１８上に形成されたゲート絶縁膜２０と、ゲート絶縁膜２０上に形成されたゲート電極１１と、ゲート電極１１の側壁に設けられたＬ型ゲート側壁酸化膜１２とを備えている。また、ｐ型高濃度ソース・ドレイン拡散層１５のチャネル側端部には、ｐ型低濃度ソース・ドレイン拡散層１７が設けられている。

【００９７】図１２の相補型半導体装置と図１１の相補型半導体装置との間にある構造上の主要な差異は、ｐ型ＭＯＳトランジスタがｐ型ゲート電極１１ｂを持つ表面チャネル型であることである。表面チャネル構造を持つことによって埋め込みチャネル型より優れた耐短チャネル効果特性と耐ホットキャリア劣化特性を有する。また、電界を緩和させ、ホットキャリア劣化を改善するｐ型低濃度ソース・ドレイン拡散層のない構造を適応することができる。またｐ型低濃度ソース・ドレイン拡散層による寄生抵抗を解消することができる。

【００９８】実施例９と同様にｎ、ｐ型ＭＯＳトランジスタのＬ型側壁１２下部の高濃度ソース・ドレイン拡散層４、５の接合深さＤ１が、Ｌ型側壁１２下部以外の高濃度ソース・ドレイン拡散層４、５の接合深さＤ２よりも浅く形成されることと、加えてｎ型ＭＯＳトランジスタで低濃度拡散層６の接合深さＤ３がＬ型側壁１２下部の高濃度ソース・ドレイン拡散層４の接合深さＤ１と同等かそれよりも浅く形成されていることによって、ソース・ドレイン拡散層４、５からのポテンシャルのチャネル方向への広がりが効果的に抑えられ、微細ＭＯＳトランジスタ特有のＶｔの低下が効果的に抑制される。

【００９９】（実施例１１）図１３（ａ）から（ｆ）及び図１４（ａ）から（ｅ）を参照しながら、本発明による相補型半導体装置の製造方法を以下に説明する。

【０１００】まず、１３（ａ）に示されるように、ｐ型半導体基板１９の一部にｎウエル領域１８を形成することによって、ｐ型領域とｎ型領域とを導体基板１９中に形成する。

【０１０１】次に、半導体基板１９の主面を熱酸化することによって、半導体基板１９の表面にＬＯＣＯＳ分離１３を形成する。

【０１０２】ｐ型領域及びｎウエル領域１８上にゲート酸化膜２０を介してゲート電極１１を形成した後、図１３（ｂ）に示されるように、第１の酸化膜（厚さ：約５ｎｍ）２３がゲート電極１１を覆うようにして半導体基板１９の主面上に形成される。

【０１０３】この後、図１３（ｃ）に示されるように、第２の酸化膜（厚さ：４０ｎｍ程度）２５が第１の酸化膜２３上に堆積される。第２の酸化膜２５は、例えば、ＣＶＤ法に形成されたシリコン酸化膜である。次に、酸素を透過させにくい絶縁膜、たとえば、窒化膜（１００ｎｍ程度）２４が第２の酸化膜２５上に堆積される。

【０１０４】次に、図１３（ｄ）に示されるように、レジスト２６がフォトリソグラフィ工程によってｎウエル１８上にのみ選択的に堆積される。

【０１０５】垂直方向に強い異方性を有するドライエッチングにより、ｎ型ＭＯＳトランジスタが形成される領域に位置する酸化膜２３と窒化膜２４とをエッチングし、それによって、図１３（ｅ）に示されるように、これらの膜２３及び２４からなるサイドウォールをゲート電極２１の側面に形成する。

【０１０６】レジスト２６を除去した後、図１３（ｆ）に示されるように、熱酸化工程、例えば８５０℃のウエット酸化工程によって、第３の酸化膜（厚さ：約３０ｎｍ）２７がｎ型ＭＯＳトランジスタが形成される領域上に形成される。ゲート電極端部のゲート酸化膜２０を厚くする。このときｐ型ＭＯＳＦＥＴ領域のｐウエル１８上は窒化膜に覆われているため酸化されない。

【０１０７】この後、図１４（ａ）に示されるように、垂直方向に強い異方性をもつドライエッチングにより、窒化膜２４をゲート電極２１の側面に残置させる。この異方性エッチングにより、ｎ型ＭＯＳトランジスタ領域のゲート電極２１の側部の窒化膜２４の高さは、さらに低くなる。また同時に第３の酸化膜２７と第２の酸化膜２５が１０～２０ｎｍエッチングされる。

【０１０８】選択性エッチング、例えば、熱リン酸溶液のエッチングにより、窒化膜２４を完全に除去し、図１４（ｂ）に示されるように、Ｌ型の側壁１２を形成する。このとき、従来方法の異方性ドライエッチングではなく、選択性エッチングにより窒化膜２４を除去するので、酸化膜２５、２７はほとんどエッチングされずＬ型の側壁が精度良くゲート電極２１の側壁に形成される。

【０１０９】次に、図１４（ｃ）に示されるように、フォトリソグラフィ工程によってレジスト２６をｎウエル上に選択的に堆積させる。この後、レジスト２６とＬ型側壁１２とゲート電極１１とをマスクとして、ｎ型の不純物、例えば、ドーズ量$6\times10^{15}cm^{-2}$程度のヒ素イオンを加速エネルギー８０ＫｅＶで注入し、ｎ型高濃度ソース・ドレイン拡散層１４とｎ型ゲート電極１１ａを形成する。この時、Ｌ型側壁１２をマスクとして高濃度ソース・ドレイン拡散層４を形成するので、Ｌ型側壁１２下部のソース・ドレイン拡散層１４の接合深さはＬ型側壁１２下部以外の接合深さよりも浅く形成される。さらにＬ型側壁１２の幅が精度良く形成されているのでソース・ドレイン拡散層１４は精度良くｎ型ゲート電極１

１ａ端部まで達するように拡散させている。

【０１１０】さらに、ｎ型の不純物、例えば、ドーズ量４×10^{13}ｃｍ$^{-2}$程度のリンイオンを加速エネルギー８０ＫｅＶで、しかも、４５度の入射角度で注入し、ｎ型低濃度拡散層１６を形成する。Ｌ型側壁１２をマスクとして大仰角でイオン注入するため、低濃度拡散層１６の接合深さはＬ型側壁１２下部の高濃度ソース・ドレイン拡散層１４の接合深さと同等かそれよりも浅く形成される。

【０１１１】図１４（ｄ）に示されるように、フォトリソグラフィ工程によってｎ型ＭＯＳトランジスタ領域上に選択的にレジスト２６を堆積させる。このレジスト２６とＬ型の側壁１２とゲート電極１１とをマスクとして、ｐ型の不純物、例えば、ドーズ量４×10^{15}ｃｍ$^{-2}$程度のBF_2イオンを、加速ネルギー４０ＫｅＶで注入し、ｐ型高濃度ソース・ドレイン拡散層１５とｐ型ゲート電極１１ｂとを形成する。

【０１１２】図１４（ｅ）に示されるように、レジスト２６を除去した後、絶縁膜２８を堆積する。

【０１１３】上記製造方法は、自己整合性的な工程を多く含み、現在のＬＳＩ技術で容易に実現され得る。この製造方法により、比較少ない工程数で、図１１の相補型半導体装置を歩留り良く製造することができる。

【０１１４】（実施例１２）図１５（ａ）及び（ｂ）を参照しながら、本発明による相補型半導体装置の他の製造方法を以下に説明する。

【０１１５】本製造方法は、図１３（ａ）から（ｆ）及び図１４（ａ）～（ｃ）に示される工程と同様の工程を含んでおり、図１５（ａ）に示される工程は、図１４（ｃ）に示される工程の後に行なわれる。なお、図１５（ａ）及び（ｂ）において、実施例１１の相補型半導体装置の各要素に対応する要素には、実施例１１に使用されている図番号と同じ図番号が使用される。

【０１１６】図１４（ｃ）に示される工程が終了した後、図１５（ａ）に示されるように、フォトリソグラフィ工程によって選択的にｎ型ＭＯＳトランジスタ領域上にレジスト２６を堆積させる。このレジスト２６とＬ型側壁１２とゲート電極１１とをマスクとしてｐ型の不純物、例えば、ドーズ量４×10^{15}ｃｍ$^{-2}$程度のBF_2イオンを加速エネルギー４０ＫｅＶで注入し、ｐ型高濃度ソース・ドレイン拡散層１５を形成すると同時に、大仰角イオン注入によりｐ型の不純物、例えば、注入ドーズ量４×10^{13}ｃｍ$^{-2}$程度のボロンイオンを注入エネルギー３０ＫｅＶで、しかも４５度の入射角度で注入し、ｐ型低濃度拡散層１７を形成する。この時、Ｌ型側壁１２をマスクとして大仰角でイオン注入するので低濃度拡散層１７はゲート電極１１端に達し、しかも接合深さはＬ型側壁１２下部の高濃度ソース・ドレイン拡散層１７の接合深さと同等かそれよりも浅く形成される。

【０１１７】次に、図１５（ｂ）に示されるように、レ

ジスト２６を除去した後、絶縁膜２８を堆積させる。

【０１１８】このように、本製造方法によっても、前述の製造方法と同様に、図１１の相補型半導体装置が簡単に製造される。

【０１１９】

【発明の効果】以上のように、本発明の半導体装置によれば、ゲート電極側部のＬ型側壁下部のソース・ドレイン拡散層の接合深さが前記Ｌ型側壁の外側の接合深さよりも浅く形成され、かつ、第２導電型の低濃度ソース・ドレイン拡散層の接合深さがＬ型側壁下部のソース・ドレイン拡散層の接合深さと同等かそれよりも浅く形成されていることで、従来のオーバラップＬＤＤ構造よりもソース・ドレイン拡散層からのポテンシャルのチャネル方向への広がりを効果的に抑え、ハーフミクロン領域以下の微細化に問題となる初期特性のしきい値電位の劣化（Ｖｔ低下）を抑制している。

【０１２０】また、高濃度ソース・ドレイン拡散層がゲート酸化膜を介してゲート電極端部まで拡散するように形成され、かつ、第２導電型の低濃度拡散層が完全にゲート電極とオーバラップするように形成されていることで、オーバラップＬＤＤ構造と同様に低濃度拡散層内の横方向の電界はゲート電極に印加された電位によって充分に緩和される。また、Ｌ型側壁を通してイオン注入された高濃度のソース・ドレイン拡散層はＬ型側壁直下では10^{19}ｃｍ$^{-3}$程度に低下しさらに横方向電界は緩和されオーバラップ量を減少させることができる。また、ゲート電極の外側の酸化膜内にトラップされた電子や発生した界面準位は高濃度拡散層のために素子特性の劣化を加速することはない。これによって、ホットキャリアの発生率が減少する。また、低濃度拡散層内のキャリアは完全にゲート電極によって制御され、低濃度拡散層のソース抵抗は低減し、素子の駆動能力が向上する。

【０１２１】また、ゲート電極が下に凸の構造を持ちゲート電極凸部の端部がゲート酸化膜を介して低濃度第２導電型拡散層に達するように形成されていることで、オーバラップ部のゲート酸化膜がチャネル部よりも厚くなり、ゲート・ドレインオーバラップ容量が減少し、素子の回路特性を改善している。また、ゲート電圧誘因のバンド間トンネル電流を減少させる。

【０１２２】従って、本発明は、電気特性の劣化や駆動能力の低下を招くことなく、短チャネル効果に強くハーフミクロン領域以下の微細化が可能で、高速で高信頼性なＭＯＳ型半導体装置を提供する。

【０１２３】また、第３の絶縁膜を選択性エッチングにより除去しＬ型の第２の絶縁膜を形成する工程と、ゲート電極をマスクとし前記第２の絶縁膜の底部を透過して第２導電型の高濃度ソース・ドレイン拡散層を形成するイオン注入工程を有することで、１回のイオン注入工程で効果的に請求項１に記載のＭＯＳ型半導体装置の高濃度のソース・ドレイン拡散層を形成できる。また、高濃

度ソース・ドレイン拡散層とゲート電極のオーバラップ量を確実に制御することができる。

【0124】また、このイオン注入工程と連続してL型側壁を透過させて第2導電型の低濃度拡散層をイオン注入により形成することで、1回のマスキング工程で高濃度ソース・ドレイン拡散層と低濃度ソース・ドレイン拡散層を形成することができる。

【0125】さらに、酸化工程により、ゲート電極側部を酸化させることなく効果的にゲート酸化膜端部を厚くし、本発明の半導体装置を効率よく形成することができる。

【0126】従って、本発明の半導体装置は、ハーフミクロン領域以下のＶＬＳＩ技術に要求される短チャネル効果を抑制しホットキャリア劣化耐性が高い高信頼性で高性能な半導体装置である。さらに、本発明の半導体装置の製造方法は、前記半導体装置を高精度に効果的に得る製造方法であり、その工業的価値はきわめて高い。

【0127】また、本発明の相補型半導体装置によれば、ゲート電極側部のＬ型側壁下部の高濃度ソース・ドレイン拡散層の接合深さが前記Ｌ型側壁の外側の接合深さよりも浅く形成され、かつ低濃度拡散層の接合深さがＬ型側壁下部の高濃度ソース・ドレイン拡散層の接合深さと同等かそれよりも浅く形成されていることで、ソース・ドレイン拡散層からのポテンシャルのチャネル方向への広がりを効果的に抑え、ハーフミクロン領域以下の微細に問題となる初期特性のしきい値電位の劣化（Ｖｔ低下）を抑制している。

【0128】また、第１導電型半導体基板上の第２導電型の低濃度拡散層がゲート電極と十分にオーバラップするように形成されていることで、オーバラップＬＤＤ構造と同様に第２導電型の低濃度拡散層内の横方向の電界はゲート電極に印加された電位によって充分に緩和され、ホットキャリアの発生率が減少する。また、低濃度拡散層内のキャリアは完全にゲート電極によって制御され、低濃度拡散層のソース抵抗は低減し、素子の駆動能力が向上する。

【0129】さらに第１導電型半導体基板上の第２導電型の低濃度拡散層上に厚いゲート酸化膜を形成することでオーバラップ部のゲート酸化膜がチャネル部よりも厚くなり、ゲート・ドレインオーバラップ容量が減少し、素子の回路特性を改善している。

【0130】また、本発明の他の相補型半導体装置は、第２導電型のウエル上のゲート絶縁膜が均一な膜厚を持つことで第１導電型の低濃度拡散層とゲート電極の重なりを最小にすることができ寄生抵抗を増加させることなしに、ゲート長に対して最大の実効チャネル長を設定することができる。

【0131】従って、本発明は電気特性の劣化や駆動力の低下を招くことなく、短チャネル効果に強くハーフミクロン領域以下の微細化が可能で、高速で高信頼性の相補型相補型半導体装置を提供する。

【0132】また、酸化種を通し難い第３の絶縁膜を第２導電型のウエル上と第１導電型半導体基板上のゲート電極側面に残留させる工程と酸化工程により、ゲート電極側面と第２導電型のウエル上のゲート電極端部を酸化することなく、第１導電型半導体基板上のゲート電極端部のゲート絶縁膜を厚く形成することができる。

【0133】従って、本発明の相補型半導体装置は、ハーフミクロン領域以下のＶＬＳＩ技術に要求される短チャネル効果を抑制しホットキャリア劣化耐性が高い高信頼性で高性能な相補型相補型半導体装置である。さらに、本発明の相補型半導体装置の製造方法は、前記相補型半導体装置を容易に得る製造方法であり、その工業的価値はきわめて高い。

【図面の簡単な説明】

【図１】本発明による半導体装置の断面図

【図２】本発明による他の半導体装置の断面図

【図３】本発明による更に他の半導体装置の断面図

【図４】本発明による更に他の半導体装置の断面図

【図５】本発明による半導体装置の製造方法を示す工程断面図

【図６】本発明による半導体装置の他の製造方法を示す工程断面図

【図７】本発明による半導体装置の更に他の製造方法を示す工程断面図

【図８】本発明による半導体装置の更に他の製造方法を示す工程断面図

【図９】本発明の第１の実施例における不純物分布の一例を示す不純物分布等高線図

【図１０】本発明による半導体装置製造方法により形成された半導体装置の断面ＴＥＭ写真に基づく図

【図１１】本発明による相補型半導体装置の断面図

【図１２】本発明による他の相補型半導体装置の断面図

【図１３】本発明による相補型半導体装置の製造方法を示す工程断面図

【図１４】本発明による相補型半導体装置の製造方法を示す工程断面図

【図１５】本発明による相補型半導体装置の他の製造方法を示す工程断面図

【図１６】従来例の半導体装置の断面図

【図１７】従来例の半導体装置の製造方法の工程断面図

【符号の説明】

1　第１導電型半導体基板（ｐ型）
2　ゲート酸化膜
3　高濃度ソース・ドレイン拡散層（ｎ型）
4　低濃度ソース・ドレイン拡散層（ｎ型）
5　ゲート電極
6　Ｌ型側壁
１１　ゲート電極
１１ａ　ｎ型ゲート電極

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１１ｂ　ｐ型ゲート電極
１２　Ｌ型側壁
１３　ＬＯＣＯＳ分離
１４　ｎ型高濃度拡散層
１５　ｐ型高濃度拡散層
１６　ｎ型低濃度拡散層
１７　ｐ型低濃度拡散層
１８　ｎウエル
１９　半導体基板

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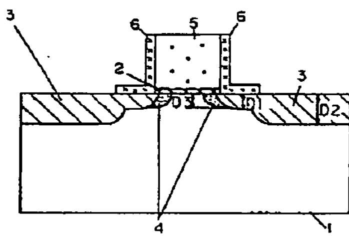
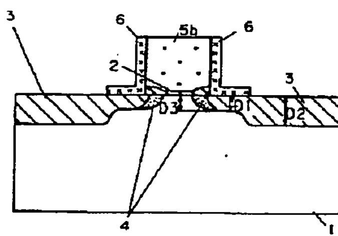
２０　ゲート絶縁膜
２３　第１の酸化膜
２４　窒化膜
２５　第２の酸化膜
２６　レジスト
２７　第３の酸化膜
２８　絶縁膜
２９　埋め込みチャネル部ｐ型低濃度層

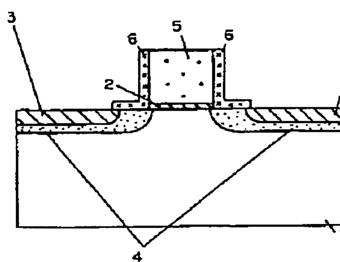
【図１】



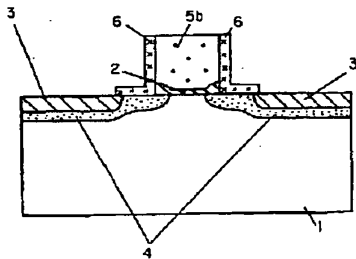
【図２】



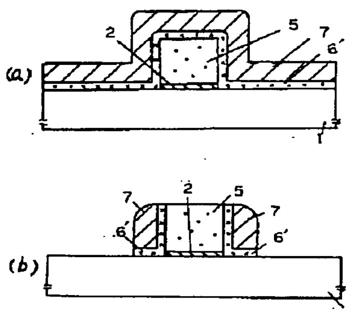
【図３】

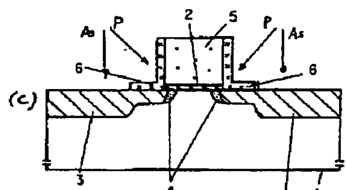


【図４】

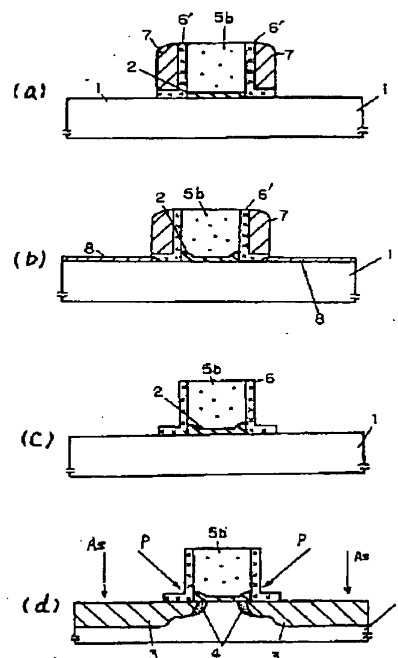


【図５】

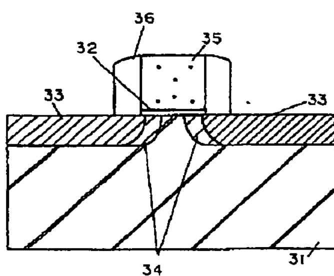




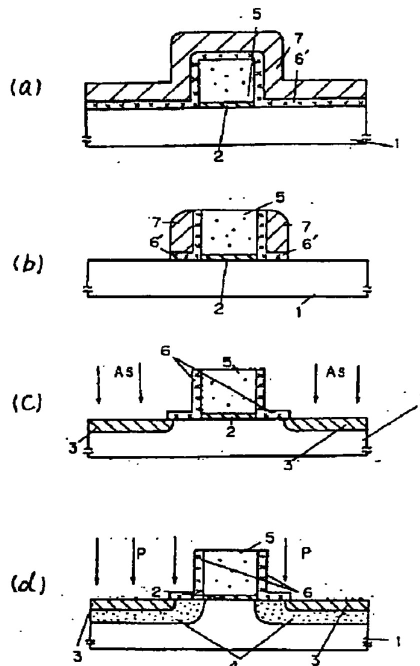
【図６】



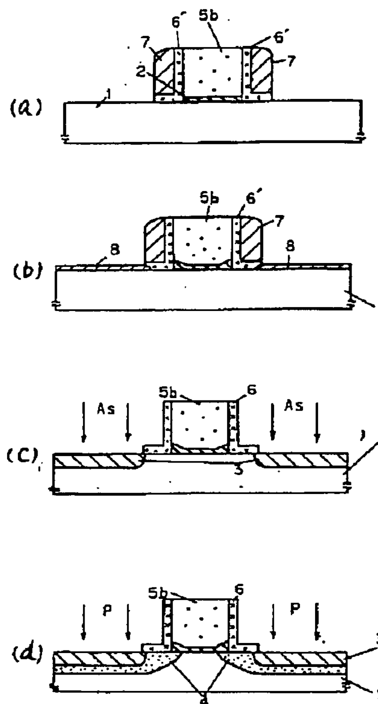
【図１６】



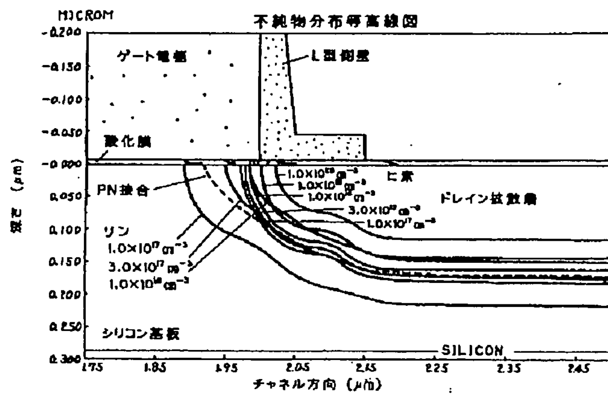
【図7】



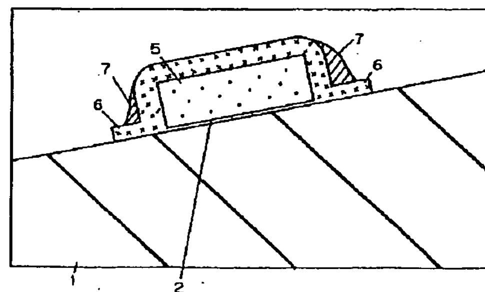
【図8】



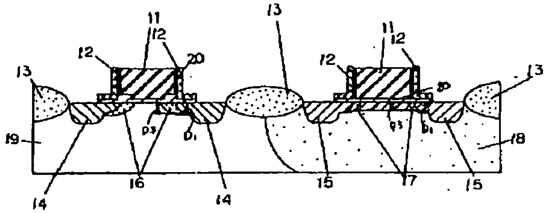
【図9】



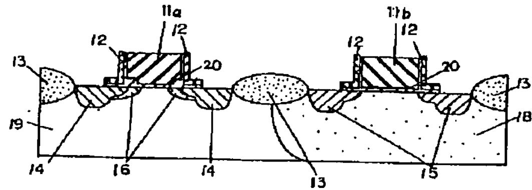
【図10】



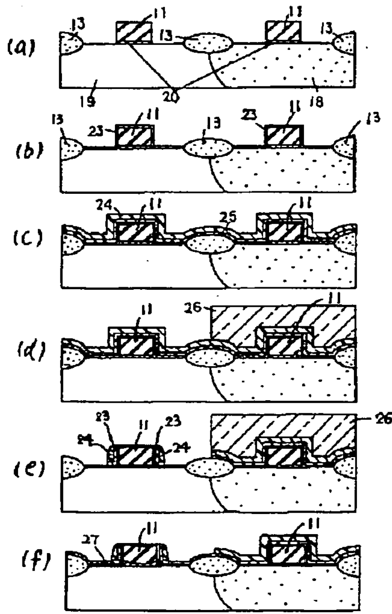
【図11】



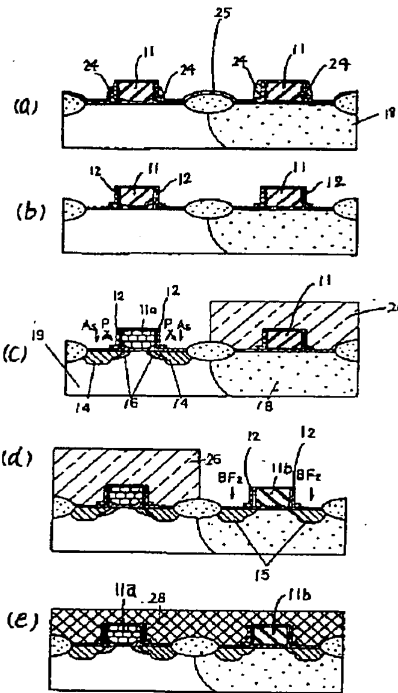
【図12】



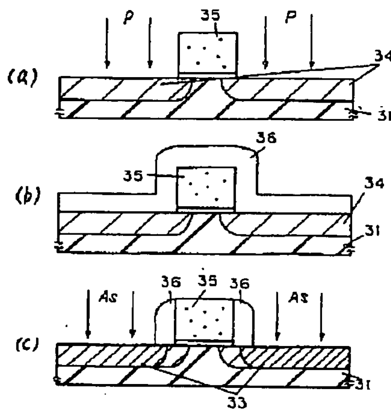
【図13】



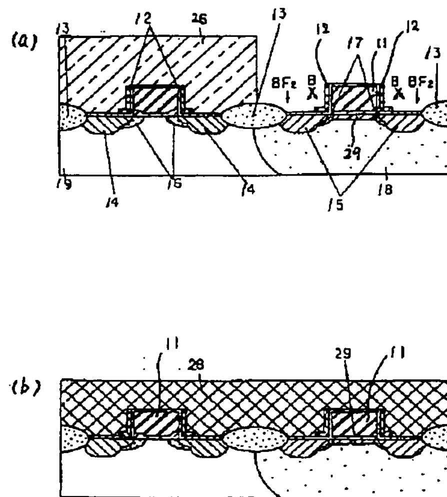
【図14】



【図17】



【図１５】



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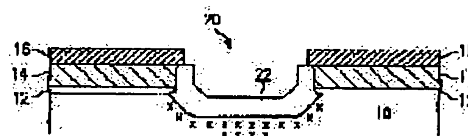
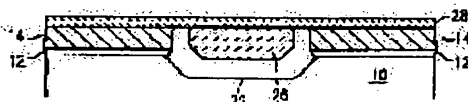
(71)Applicant : SGS THOMSON MICROELECTRON INC
(72)Inventor : BRYANT FRANK

(30)Priority
Priority number : 92 889822 Priority date : 29.05.1992 Priority country : US

(54) MOSFET CONSTITUTION BODY PROVIDED WITH FLAT SURFACE

(57)Abstract:
PURPOSE: To provide a separation structure body provided with the surface practically in the same surface shape as the surface of an adjacent active area by forming a flat silicide layer layer on a conductive layer and an insulation area on a substrate.
CONSTITUTION: A gate oxidized film 12, a polysilicon layer 14 and a silicon nitride layer 16 are formed on the substrate 10. Then, a photoresist layer is formed and patterned. The silicon nitride layer 16, the polysilicon layer 14 and a gate oxide layer 12 are etched, an opening 20 is formed and the substrate 10 is exposed. Then, photoresist is removed, the exposed substrate 10 and a part of the polysilicon layer 14 are oxidized and an oxidized area 22 is formed. A flattened insulation layer is formed on the silicon nitride layer 16 and inside the opening 20, the flattened insulation layer is etched back and the silicon nitride 16 is exposed. In this case, the upper surface of the insulation layer is turned to the same surface shape as the upper surface of the polysilicon layer 14. Then, the silicon nitride layer 16 is removed and the flat silicide layer 28 is formed on the polysilicon layer 14.





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(71)出願人　591236448
エスジーエスートムソン　マイクロエレクトロニクス，インコーポレイテッド
SGS－THOMSON MICROELECTRONICS, INCORPORATED
アメリカ合衆国，テキサス 75006，カーロルトン，エレクトロニクス ドライブ 1310

(72)発明者　フランク　ブライアント
アメリカ合衆国，テキサス 76201，デントン，クレストウッド 2125

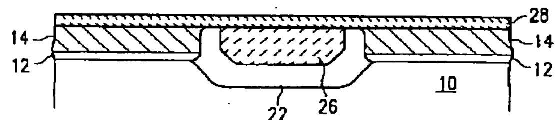
(74)代理人　弁理士　小橋　一男　（外1名）

(54)【発明の名称】　平坦な表面を具備するMOSFET構成体

(57)【要約】　　（修正有）

【目的】　隣接する活性領域の表面と実質的に、同一面状の表面を具備する分離構成体及びその製造方法を提供する。

【構成】　基板上に導電層を形成し、その上に窒化シリコン層を形成する。次いでホトレジスト層を形成し且つパターン化する。窒化シリコン層と導電層をエッチングして基板の一部を露出させる開口を形成する。次いで、ホトレジストを除去し、露出された基板及び開口内の側壁に沿って露出された導電層の一部を酸化する。スピンオンガラス等の平坦化用絶縁層を窒化シリコン層上及び開口内に形成する。絶縁層をエッチバックして窒化シリコンを露出させ、その場合に絶縁層の上表面が導電層の上表面と同一面状となる。次いで、窒化シリコン層を除去し、次いで導電層上に平坦なシリサイド層を形成する。



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【特許請求の範囲】
【請求項１】　半導体集積回路の平坦な表面を形成する方法において、
基板上に導電層を形成し、
前記基板の一部を露出させるために前記導電層を貫通して開口を形成し、
前記開口内の前記基板の一部及び前記開口内の側壁に沿っての前記導電層の一部を酸化し、
前記開口内に絶縁性領域を形成し、
前記絶縁性領域及び前記導電層上に平坦なシリサイド層を形成する、
上記各ステップを有することを特徴とする方法。
【請求項２】　請求項１において、前記導電層を形成するステップが、更に、
前記基板上にゲート酸化物層を形成し、
前記ゲート酸化物層上にポリシリコン層を形成し、
前記ポリシリコン層上に窒化シリコン層を形成し、
前記窒化シリコン層上にホトレジスト層を形成すると共にパターン化し、
前記窒化シリコン層とポリシリコン層とゲート酸化物層とをエッチングして前記基板の一部を露出させる開口を形成し、
前記ホトレジスト層を除去する、
上記各ステップを有することを特徴とする方法。
【請求項３】　請求項２において、更に、
酸化の前に前記窒化シリコン層の一部と前記窒化シリコン層の一部の下側に存在するポリシリコン層の一部とを除去するステップを有しており、残存するポリシリコン層の上表面が前記酸化ステップ期間中に酸化されることを特徴とする方法。
【請求項４】　請求項１において、前記絶縁性領域を形成するステップが、更に、
前記窒化シリコン層上及び前記開口内にスピンオンガラス層を形成し、
前記スピンオンガラス層をエッチバックして前記窒化シリコン層を露出させ、その場合に前記スピンオンガラス層の上表面が前記ポリシリコン層の上表面と同一面状にある、
上記各ステップを有することを特徴とする方法。
【請求項５】　請求項２において、更に、
前記シリサイド層を形成する前に前記窒化シリコン層を除去する、
上記ステップを有することを特徴とする方法。
【請求項６】　請求項４において、更に、
前記スピンオンガラス層を形成した後にそれを硬化する、
上記ステップを有することを特徴とする方法。
【請求項７】　請求項１において、更に、
酸化の前に露出された基板内にドーパントを注入する、
上記ステップを有することを特徴とする方法。

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【請求項８】　請求項３において、更に、
前記基板の一部を酸化する前に前記開口内に露出された基板の一部をエッチングする、
上記ステップを有することを特徴とする方法。
【請求項９】　請求項３において、更に、
前記平坦なシリサイド層と導電層をパターン化し且つエッチングして導電性構成体を形成する、
上記ステップを有することを特徴とする方法。
【請求項１０】　半導体集積回路の平坦な表面を形成する方法において、
基板上に導電層を形成し、
前記導電層上に窒化シリコン層を形成し、
前記窒化シリコン層上にホトレジスト層を形成すると共にパターン化し、
前記窒化シリコン層及び導電層をエッチングして前記基板の一部を露出する開口を形成し、
前記ホトレジスト層を除去し、
前記露出された基板及び前記開口内の側壁に沿って露出された導電層の一部を酸化し、
前記窒化シリコン層上及び開口内に絶縁層を形成し、
前記絶縁層の上表面が前記導電層の上表面と同一面状であるように前記絶縁層をエッチバックして前記窒化シリコンを露出させて、
前記窒化シリコン層を除去し、
前記導電性構成体上に平坦なシリサイド層を形成する、
上記各ステップを有することを特徴とする方法。
【請求項１１】　請求項１０において、更に、
酸化の前に前記窒化シリコン層及びその下側に存在する導電層の一部を除去する、
上記ステップを有しており、その場合に残存する導電層の部分の上表面が酸化ステップ期間中に酸化されることを特徴とする方法。
【請求項１２】　請求項１０において、更に、
前記ホトレジスト層を除去する前に前記開口内に露出された基板の一部をエッチングする、
上記ステップを有することを特徴とする方法。
【請求項１３】　請求項１２において、前記基板が約２０００Åエッチングされることを特徴とする方法。
【請求項１４】　請求項１０において、前記絶縁層がスピンオンガラスであり、且つ前記スピンオンガラスは、形成された後に、硬化されることを特徴とする方法。
【請求項１５】　請求項１０において、更に、
酸化の前に露出された基板内にドーパントを注入する、
上記ステップを有することを特徴とする方法。
【請求項１６】　請求項１０において、前記導電性構成体が酸化物層上に配設したポリシリコン層を有していることを特徴とする方法。
【請求項１７】　請求項１６において、前記ポリシリコン層が約１５００Åの厚さを有していることを特徴とする方法。

【請求項１８】　請求項１０において、前記窒化シリコン層が約５００Åの厚さを有していることを特徴とする方法。

【請求項１９】　請求項１０において、酸化前に開口内の側壁に沿っての導電層の部分の間の距離が約０．６ミクロンの幅であることを特徴とする方法。

【請求項２０】　請求項１０において、酸化後の開口内の側壁に沿っての導電層の部分の間の距離が約０．７ミクロンの幅であることを特徴とする方法。

【請求項２１】　請求項１０において、前記基板が約１０００Åの厚さに酸化されることを特徴とする方法。

【請求項２２】　集積回路装置の一部からなる構成体において、
基板、
前記基板の一部の上側に位置しておりそれを貫通しており前記基板の一部を露出させる開口を具備する導電性構成体、
前記露出された基板の上表面の一部と前記開口内の側壁に沿っての導電性構成体の一部とからなる酸化領域、
前記開口内の絶縁性領域、
前記導電性構成体及び前記絶縁性領域の上の平坦なシリサイド層、
を有することを特徴とする構成体。

【請求項２３】　請求項２２において、前記絶縁性領域がスピンオンガラスを有することを特徴とする構成体。

【請求項２４】　請求項２２において、前記酸化領域が、更に、前記導電性構成体の一部の上表面を有することを特徴とする構成体。

【請求項２５】　請求項２２において、前記導電性構成体がゲート酸化物層の上に配設したポリシリコン層を有することを特徴とする構成体。

【請求項２６】　請求項２２において、更に、前記酸化領域の下側に位置し前記基板内に注入したドーパントが設けられていることを特徴とする構成体。

【請求項２７】　請求項２２において、前記酸化領域が約１０００Åの厚さを有することを特徴とする構成体。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、大略、半導体集積回路及びその処理技術に関するものであって、更に詳細には、平坦な表面を有するＭＯＳＦＥＴ構成体及びその製造方法に関するものである。

【０００２】

【従来の技術】集積回路の製造コストは、所望の機能を実現するのに必要とされるチップ面積にかなりの部分が依存する。このチップ面積は、例えば金属－酸化物－半導体（ＭＯＳ）技術におけるゲート電極等のアクティブな構成要素や、例えばＭＯＳ装置のソース及びドレイン領域やバイポーラ装置のエミッタ及びベース領域等の拡散領域の幾何学的形状及び寸法により画定される。これらの幾何学的形状及び寸法は、しばしば、特定の製造設備に対して得られるホトリソグラフィの分解能に依存することが多い。種々の装置及び回路の水平方向の寸法を確立する場合のホトリソグラフィの目標は、設計条件にかなうパターンを形成すると共に、ウエハの表面上に回路パターンを正確に整合させることである。ライン幅がサブミクロンホトリソグラフィにおいて益々小さくなるに従って、ホトレジスト内にライン及びコンタクト孔をプリントするためのプロセスは益々困難なものとなっている。

【０００３】回路が超大規模集積化（ＶＳＬＩ）レベルに進むと共に、ウエハの表面にはより多くの層が付加される。これらの付加的な層は、ウエハ表面上により多くのステップ即ち段差を形成する。従って、ホトリソグラフィにおける小さな画像寸法の分解能は、光の反射及びこれらの段差においてのホトレジストの薄層化のために、これらの付加的な段差においてより一層困難なものとなる。変化されるトポグラフィ即ち地形的構成の影響を取除くために平坦化技術が一般的に使用されている。

【０００４】ホトリソグラフィの分解能を向上させるために平坦化技術が使用されることに加えて、チップ面積は、更に、使用される分離技術にも依存する。リーク電流が機能的又は仕様上の障害を発生させないように、アクティブな回路要素間には充分なる電気的分離が与えられねばならない。例えば、より高い密度のメモリアレイに使用するより小型のメモリセルに対する要求と共に、益々厳しくなる仕様条件は、メモリ装置及びその他の最近の集積回路においての分離技術に著しい圧力をかけている。

【０００５】公知の広く使用されている分離技術は、通常ＬＯＣＯＳとして呼ばれるシリコンの局所酸化技術である。このＬＯＣＯＳプロセスは、分離領域に対して必要とされる面積を減少させ且つある寄生要領を減少させる上で優れた技術的改良であった。ＬＯＣＯＳフィールド酸化膜は、通常、最大回路電圧へバイアスされた場合に、フィールド酸化膜上に設けられた導体がその下側のチャンネルを反転させることがないように充分な厚さに形成される。しかしながら、ＬＯＣＯＳフィールド酸化膜及びその他の分離技術は、集積回路表面に対してトポグラフィ即ち凹凸のある地形的形状を発生させる。この付加的なトポグラフィ即ち地形的構成は、シリコンの酸素に対する反応のために、シリコンが酸化する前の体積よりも、二酸化シリコンは必然的により大きな体積を占めるものとなることの結果である。その結果、従来のＬＯＣＯＳフィールド酸化膜の表面はアクティブ領域の表面上であり、該酸化膜の厚さの約半分はアクティブ領域表面の上方に位置している。このトポグラフィは、上側に存在する導体がフィールド酸化膜の端部において段差を被覆することを必要とし、そのことは、導体層をエッチングする場合及び導体層の信頼性において問題となる

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蓋然性を与えている。更に、サブミクロンホトリソグラフィに対するフィールドの深さは、ウエハ表面のトポグラフィにより超えることが可能である。

【0006】

【発明が解決しようとする課題】従って、本発明の目的とするところは、隣接するアクティブ即ち活性な領域の表面と実質的に同一面状の表面を具備する分離構成体及びその製造方法を提供することである。

【0007】本発明の別の目的とするところは、幅広及び幅狭の両方の分離位置に対して使用することの可能な分離構成体を形成する方法を提供することである。

【0008】本発明の更に別の目的とするところは、分離用の物質として熱二酸化シリコンを使用する分離構成体を形成する方法を提供することである。

【0009】本発明の更に別の目的とするところは、分離用の凹所を平坦化用絶縁層で実質的に充填する分離構成体を形成する方法を提供することである。

【0010】

【課題を解決するための手段】本発明は、基板上に導電層を形成することによる、半導体装置構成体の製造方法及びその際に製造される半導体装置構成体に組込むことが可能である。導電層を貫通して開口を形成し基板の一部を露出させる。露出された基板の一部を該開口内においてエッチング除去する。開口内の側壁に沿っての導電層の一部と共に、該開口内に残存する露出された基板を酸化する。該開口内に平坦化用絶縁性領域を形成する。次いで、平坦化用絶縁性領域及び導電層の上に平坦なシリサイド層を形成する。

【0011】

【実施例】以下に説明する処理ステップ及び構成は、集積回路を製造するための完全な処理の流れを構成するものではない。本発明は、当該技術分野において現在使用されている集積回路製造技術に関連して実施することが可能なものであり、本発明の重要な特徴を理解するのに必要と思われる重要なステップについて重点的に説明する。尚、添付の図面は製造過程中における集積回路の一部の概略断面を示したものであるが、これらの図面は縮尺通りに画いたものではなく適宜拡縮して示してあることに注意すべきである。

【0012】図1を参照すると、シリコン基板10の上に集積回路を形成すべき状態が示されている。シリコン基板10の上にゲート酸化物層12を形成する。ゲート酸化物層の上にポリシリコン層14を形成する。ポリシリコン層14は、典型的には、適宜ドープされて、電界効果トランジスタのゲート電極を形成する。典型的には、ポリシリコン層14は約1500Åの厚さを有している。ポリシリコン層14の上に約500Åの厚さに窒化シリコン層16を形成する。次いで、窒化シリコン上にホトレジスト層を形成し且つパターン化して約0．6ミクロンの幅を持った下側に存在する層を貫通して延在

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する開口を形成する。窒化シリコン層16、ポリシリコン層14及びゲート酸化物層12をエッチングして開口20を形成し、該開口内にシリコン基板層10を露出させる。種々の層の形成及びエッチングは従来のプロセスに従って行なわれる。注意すべきことであるが、本発明は、単一セルCMOSプロセス、ツインウエル即ちツインタブCMOSプロセス、及びその他のバイポーラ、Nチャンネル及びPチャンネルMOS及びBiCMOS技術を包含するその他の技術においても適用可能なものである。このような技術では、それらのアクティブな装置は、直接的にモノリシック基板内に又は基板の表面においてエピタキシャル層内に形成する場合がある。本発明は、このようなその他の技術に適用可能であり且つそのようなその他の技術に実現される場合に効果的であると考えられる。

【0013】図2を参照すると、開口内において基板10の一部がエッチング除去されている。好適には、従来のプロセスを使用して約2000Åがエッチング除去される。ホトレジスト層18を除去する。Xで示したチャンネルストップ注入をシリコン基板内に付与して、寄生スレッシュホールド電圧を増加させることにより電気的分離を改善させることが可能である。このチャンネルストップ注入は、開口内の領域に適切なドーピングを与え、それは分離構成体として作用する。基板のエッチングの後に形成される基板10内の凹所の側部にイオン注入することによっても分離が改善される。このことは、凹所及びトレンチの側部のイオン注入に対しての角度回転型注入により達成することが可能である。

【0014】開口内の露出されたシリコン基板10は熱酸化によって酸化領域22を形成する。この酸化プロセスは、通常、30分間の間900℃の温度で行なわれる。熱酸化は、開口20内の側壁に沿ってポリシリコン層14の一部をも酸化させる。注意すべきことであるが、シリコン基板10及び開口20内の側壁に沿ってポリシコンの熱酸化は、窒化シリコン層16がアクティブ即ち活性な装置の表面の上にマスクとして作用する状態で行なわれる。

【0015】

【実施例】窒化シリコンは、ポリシリコン層14の上表面の酸化を防止するための酸化バリアとして作用する。酸化された区域、即ち現在ポリシリコン層14を離隔させる分離区域の幅は、元が0．6ミクロンの幅であったのと比較し、約0．7ミクロンである。この分離区域の厚さは、典型的に、約4000Åである。シリコン基板とポリシリコン層14との間にはそのエッジに沿って酸化ステップの期間中に小さなバードビークが形成される。このバードビークは活性領域の尖った角部を丸めた形状とさせ、そのことはポリシリコンゲート電極の角部によって形成される高い電界を減少させ且つ寄生フィールド酸化物トランジスタのリークの傾向を減少させるこ

とに貢献する。

【0016】図3を参照すると、窒化シリコン層26上及び開口20内に絶縁層24を形成する。絶縁層24は、好適には、例えばスピンオンガラス（SOG）のような平坦化層である。説明の便宜上絶縁層24のことをSOGとして呼称する。

【0017】図4を参照すると、SOGをエッチバックしてSOG領域26を形成し、従ってそれはほぼポリシリコン層14と同一面状である。開口内にSOGを形成することにより分離区域開口が充填され且つポリシリコン層14のレベルにおいて集積回路を平坦化させる。次いで、窒化シリコン層16を除去し、且つポリシリコン層14、酸化領域22の一部及びSOG26の上に適合性シリサイド層28を形成する。シリサイド層28は平面状乃至は平坦状である。何故ならば、下側に存在するポリシリコン層及びSOG層が実質的に同一面状だからである。次いで、ポリシリコン層14及びシリサイド層28を従来の方法に従ってパターン化し且つエッチングしてゲート電極を形成する。

【0018】ゲート電極を形成する前に導電層を実質的に平坦化させる方法は、従来技術と比較し著しい利点を提供している。このプロセスは、サブミクロンの分離区域を形成するのに適している。酸化領域22とSOG26とを有する活性区域分離構成体を形成することは、サブミクロンの分離区域を維持しながらゲート電極のパターン化をする前に集積回路のより良好な平坦性を確保する。このような平坦な表面は、一様な画像ライン及び空間をプリントする能力を改善する。

【0019】しかしながら、図5を参照すると、大きな分離区域を形成することも可能である。基板の酸化を行なう前に、分離区域として作用する大きな区域にわたり窒化シリコンを除去する。残存されるべき窒化シリコンの上にホトレジスト層（不図示）即ちマスクを形成する。除去されるべき窒化シリコンの部分の下側に存在するポリシリコン層の一部も除去することが可能である。例えば、ポリシリコン層14のうちの500Åを除去し、ゲート酸化物層12の上側に位置するポリシリコン層30の薄い層を有する区域を残存させることが可能である。一方、除去する窒化シリコン層の下側に存在する全てのポリシリコンを除去することも可能である。熱酸化領域22を形成する基板の熱酸化は、更に、開口20内の側壁に沿って残存するポリシリコン層30の一部を

酸化させる。窒化シリコン層の一部は除去されているので、露出されたポリシリコン層30の上表面も酸化して領域32を形成する。

【0020】より大きな分離区域においてポリシリコンを残存させることは、例えば、より薄いポリシリコン層30をクロスオーバー即ち交差する信号ラインを持った装置の性能に著しい影響を与えることはない。このことは、その大きな区域は種々のデバイス即ち装置を電気的に分離する酸化領域22及びSOG26を有するトレンチによって取囲まれているからである。更に、より大きな分離区域内に残存するポリシリコンは、酸化領域及びSOG領域の平坦性を向上させる。例えば500Åのポリシリコンの幾分かを残存させることの付加的な利点としては、オプションとしてポリシリコン層30をVssへ接続させてラジエーション（RAD）保護を与えることが可能であるということである。

【0021】以上、本発明の具体的実施の態様について詳細に説明したが、本発明は、これら具体例にのみ限定されるべきものではなく、本発明の技術的範囲を逸脱することなしに種々の変形が可能であることは勿論である。

【図面の簡単な説明】

【図1】　本発明の一実施例に基づいて半導体集積回路を製造する一段階における状態を示した概略断面図。

【図2】　本発明の一実施例に基づいて半導体集積回路を製造する一段階における状態を示した概略断面図。

【図3】　本発明の一実施例に基づいて半導体集積回路を製造する一段階における状態を示した概略断面図。

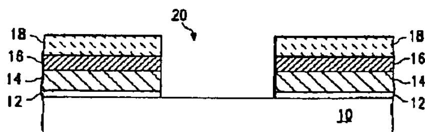
【図4】　本発明の一実施例に基づいて半導体集積回路を製造する一段階における状態を示した概略断面図。

【図5】　本発明の別の実施例に基づいて半導体集積回路を製造する一段階における状態を示した概略断面図。

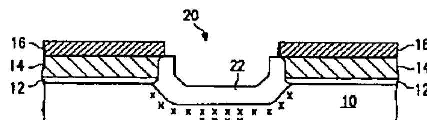
【符号の説明】

10　シリコン基板
12　ゲート酸化物層
14　ポリシリコン層
16　窒化シリコン層
20　開口
22　酸化領域
24　絶縁層
26　SOG領域

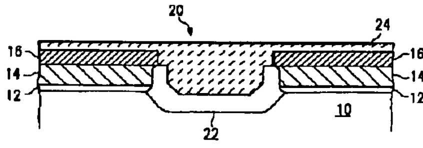
【図1】



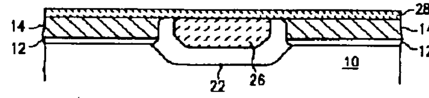
【図2】



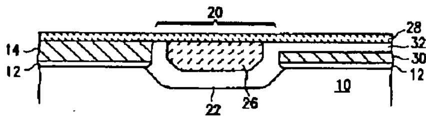
【図3】



【図4】



【図5】



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PATENT ABSTRACTS OF JAPAN

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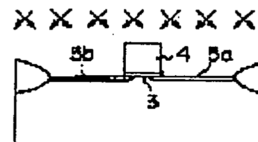
(71)Applicant : OKI ELECTRIC IND CO LTD
(72)Inventor : WAKAMATSU HIDETOSHI

(54) SEMICONDUCTOR ELEMENT AND MANUFACTURE THEREOF

(57)Abstract:
PURPOSE: To inhibit a short channel effect by forming source-drain while forming structure, in which junction depth can be shallowed sufficiently, in an ion- implanting dose for forming the source-drain.
CONSTITUTION: Gate oxide films 3 in sections except a gate electrode 4, sections as source-drain regions, are removed through etching by a buffered hydrofluoric acid containing a surface-active agent. The ions of impurities (As, P, etc.,) are implanted under oblique ion implanting conditions in the large inclination of approximately 45° in the does of approximately 2 × 1013ions/cm2 for forming the N layers 5a, 5b of an LDD type source-drain layers for inhibiting a hot carrier effect. Accordingly, the N layers 5a, 5b are formed in a shape that the N layers 5a, 5b are overlapped under the gate electrode 4. Junction depth is shallowed sufficiently in an ion implanting dose for forming source-drain, and the dose is controlled within a range that driving force is not lowered, thus suppressing a sufficient short channel effect in a fine MOSFET.



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(71)出願人　000000295
沖電気工業株式会社
東京都港区虎ノ門1丁目7番12号

(72)発明者　若松　秀利
東京都港区虎ノ門1丁目7番12号　沖電気工業株式会社内

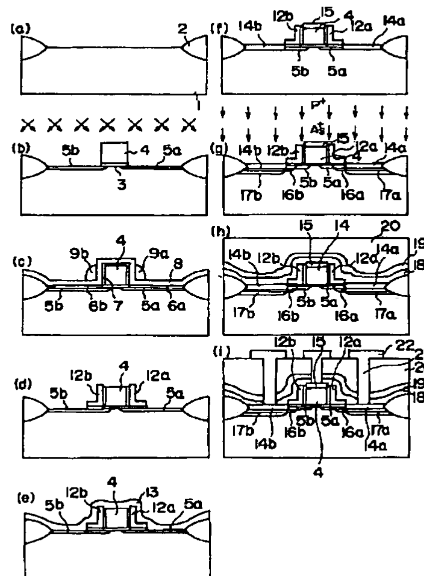
(74)代理人　弁理士　鈴木　敏明

(54)【発明の名称】　半導体素子およびその製造方法

(57)【要約】

【目的】　本発明は、半導体装置の中でも特にサリサイド構造でＬＤＤ型ＭＯＳＦＥＴの製法と構造に関するもので、従来のサリサイドプロセスでは、素子の微細化に伴い短チャネル効果抑制のため、ソース・ドレインの接合深さが浅くなり、シリサイド化した層の底面と接合との間隔が短くなり、接合リーク電流が発生するという問題点があり、これを解消することを目的とする。

【構成】　本発明は、ＬＤＤ型のトランジスタのソース・ドレインの最も浅い拡散層n⁻層５ａ，５ｂを形成する際、斜めイオン注入法でゲート電極４下にオーバーラップするようにし、ゲート電極４の側壁にＬ字型の窒化膜のサイドウォール１２ａ，１２ｂを形成し、それをマスクにして、次に深いn⁺拡散層１６ａ，１６ｂを前記サイドウォール１２ａ，１２ｂの下部まで形成し、最も深いn⁻拡散層１７ａ，１７ｂを前記サイドウォール１２ａ，１２ｂの外側に形成するようにしたものである。



本発明の第１の実施例の工程説明図

【特許請求の範囲】

【請求項１】　半導体基板上に設けるＬＤＤ型のＭＯＳ型トランジスタの構造として、

（ａ）半導体基板上に、前記トランジスタのゲート電極が有り、該ゲート電極の両側壁に耐酸化性膜のサイドウォールが設けられており、

（ｂ）前記ゲート電極の両側の前記基板に、前記ＬＤＤ型のトランジスタのソース・ドレインとしての多重拡散層のうち、最も浅い拡散層は前記ゲート電極の下部の一部まで延在し、それより深い次の拡散層は前記サイドウォール下部まで延在し、最も深い拡散層は前記サイドウォールの端部下より外側に有り、

（ｃ）少なくとも前記ゲート電極とそのサイドウォールの下部以外に存在するソース・ドレインの拡散層の表面がシリサイド膜となっていることを特徴とする半導体素子。

【請求項２】　半導体装置におけるＬＤＤ型のＭＯＳ型トランジスタ部の製造方法として、

（ａ）半導体基板上にゲート電極を形成した後、該ゲート電極をマスクにして、トランジスタのソース・ドレインとなる拡散層を形成する不純物の注入を、斜イオン注入法により注入し、前記ゲート電極下部まで前記拡散層が形成されるようにする工程、

（ｂ）前記ゲート電極の側壁に少なくとも耐酸化性膜のサイドウォールを形成する工程、

（ｃ）前記ソース・ドレイン領域とゲート電極上とに、自己整合的にシリサイド膜を形成する工程、

（ｄ）前記サイドウォールをマスクにして、ソース・ドレインとしての浅い拡散層を前記サイドウォール下に不純物を注入して形成し、次に該浅い拡散層より不純物濃度の低い濃度の不純物を注入してソース・ドレインの深い拡散層を前記ソース・ドレイン領域のシリサイド膜界面下に形成する工程、

（ｅ）前記までの構造の上に絶縁膜を形成し、熱処理を行なうことにより、該絶縁膜の平滑化と前記ソース・ドレイン領域の各拡散層の不純物活性化とを同時に行う工程、以上の工程を含むことを特徴とする半導体素子の製造方法。

【請求項３】　半導体装置におけるサリサイド構造でＬＤＤ型のＭＯＳ型トランジスタ部の製造方法として、

（ａ）半導体基板上にゲート電極を形成した後、該ゲート電極をマスクにして、トランジスタのソース・ドレインとなる拡散層を形成する不純物の注入を、斜イオン注入法により注入し、前記ゲート電極下部まで前記拡散層が形成されるようにする工程、

（ｂ）前記ゲート電極の側壁に少なくとも耐酸化性膜のサイドウォールを形成する工程、

（ｃ）前記ソース・ドレイン領域とゲート電極上とに、自己整合的にシリサイド膜を形成する工程、

（ｄ）前記サイドウォールをマスクにして、ソース・ドレインとしての浅い拡散層形成のための不純物を、前記サイドウォール下に注入して形成する工程、

（ｅ）前記ソース・ドレイン領域に形成されたシリサイド膜に不純物を注入する工程、

（ｆ）前記までの構造の上に絶縁膜を形成し、熱処理を行なうことにより、該絶縁膜の平滑化と前記不純物を注入したシリサイド膜からの固相拡散によりソース・ドレインの深い拡散層の形成とを同時に行う工程、以上の工程を含むことを特徴とする半導体素子の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明は、半導体素子の中でも特にＬＤＤ型の電界効果型トランジスタ（主にＭＯＳＦＥＴ）を有するＣＭＯＳデバイスの、主としてそのＦＥＴ部の構造とその形成方法に関するものである。

【０００２】

【従来の技術】半導体素子の微細化が進み、それとともにＭＯＳＦＥＴが縮小化されるに従い、そのゲート長が短くなり、また、短チャネル効果を抑制するため、ソース・ドレイン領域の接合深さ（Ｘｊ）は、浅くせざるを得ない。ゲート長が短くなり、ＭＯＳＦＥＴのオン抵抗は下がり、一方でＸｊが浅くなるため、ソース・ドレインのシート抵抗は増大する。従って、ゲート長がサブミクロン領域のＭＯＳＦＥＴでは、ソース・ドレインのシート抵抗が、ＭＯＳＦＥＴのオン抵抗に対して無視し得なくなり、ＭＯＳＦＥＴの駆動力が、ソース・ドレイン領域の寄生抵抗により低下する問題が顕著となる。

【０００３】上記問題に対して、ソース・ドレイン及びゲートをセルフ・アライメントでシリサイド化し、シート抵抗を下げるサリサイド・プロセスがある。図３に、従来より使われて来たサリサイド・プロセスを示し、以下に説明する。なお、この図はＣＭＯＳデバイスの例であり、従って周知のようにＰｃｈＭＯＳＦＥＴ領域（同図右半分）とＮｃｈＭＯＳＦＥＴ領域（同図左半分）が形成される。

【０００４】まず、図３（ａ）のように、Ｐ型Ｓｉ基板３１の一部に、通常のホトリソグラフィ（以下ホトリソと略す）・エッチング及びイオン注入法を用いて、Ｎ型不純物（リン等）を導入し、Ｎウェル領域３２を形成する。次に、通常のＬＯＣＯＳ（Ｌｏｃａｌ　Ｏｘｉｄａｔｉｏｎ　ｏｆ　Ｓｉｌｉｃｏｎ）法により、フィールド酸化膜３３を形成する。次に熱酸化により、Ｓｉ基板３１表面に、ゲート酸化膜３４を形成し、ゲート電極となるポリシリコン３５を全面に堆積し、通常のホトリソ・エッチング技術を用い、ゲート電極３５のパターニングを行なう。次いで、通常のホトリソ工程により、ＰｃｈＭＯＳＦＥＴ形成領域をホトレジスト３６で被い、全面にＬＤＤ（Ｌｉｇｈｔｌｙ　Ｄｏｐｅｄ　Ｄｒａｉｎ）層（N^-層）３７となるリン又はヒ素を３０～５０ｋｅＶ、$1〜4×10^{13}$ ｉｏｎｓ／cm^2 イオン注入法

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により、注入することでＮｃｈＭＯＳＦＥＴ領域にのみ、Ｎ⁻層３７を形成する。この後、前記ホトレジスト３６は除去する。

【０００５】その後、図３（ｂ）のように、全面にＣＶＤ（化学的気相成長）法により酸化膜もしくは、ボロン、リン等を含む酸化膜を堆積し、ＲＩＥ（ＲｅａｃｔｉｖｅＩｏｎ　Ｅｔｃｈｉｎｇ）法により異方性エッチングを行なうことによりゲート電極３５側壁に、サイドウォール３８を残す。このとき、サイドウォール３８下以外の前記酸化膜３４は除去され、そこに再度酸化膜３４ａを形成する。その後、上記と同様に、ホトレジストによりＰｃｈＭＯＳＦＥＴ側、ＮｃｈＭＯＳＦＥＴ側を各々、交互に被い、Ｎｃｈ側、Ｐｃｈ側に各々、イオン注入法によりソース・ドレインとなる不純物のヒ素（Ｎ⁺層）３７ａ及びボロン（Ｐ⁺層）３７ｂ（図３（ｃ））を注入し（図３（ｂ）はＰｃｈＭＯＳＦＥＴ側を被った例示である）、ホトレジストを除去し、また前記酸化膜３４ａを除去して図３（ｃ）の形状を得る。

【０００６】その後、図３（ｃ）のように、８００～１０００℃の熱処理を行ない、ソース・ドレイン部の不純物の活性化を行なった後、高融点金属３９を堆積させる。その後、図３（ｄ）のように、６００～１０００℃の熱処理を施すと、高融点金属３９と、ゲート電極３５のポリシリコン膜とソース・ドレイン領域（３７ａ，３７ｂ）のシリコン活性層との間に、シリサイド化反応が生じ、自己整合的に、ゲート電極３５及び、ソース・ドレイン部に、高融点金属３９のシリサイド４０が形成される。その後、未反応高融点金属４１を除去することにより、図３（ｅ）に示すサリサイド構造が完成する。

【０００７】

【発明が解決しようとする課題】しかしながら、以上述べた従来のサリサイドプロセスおよびその結果できた構造では、素子の微細化に伴い、短チャネル効果抑制のため、そのソース・ドレイン接合深さ（Ｘｊ）が浅くなり、シリサイド化した層の底面と接合との間隔が短かくなり接合リーク電流が発生するという問題があった。

【０００８】本発明は、前述した接合リーク電流が発生するといった問題点を除去するとともに、短チャネル効果を抑制し、ホットキャリア効果を抑制できるようにしたサリサイド化ＭＯＳＦＥＴ（特にＮｃｈ側）の製造方法とその構造を提供することを目的とする。

【０００９】

【課題を解決するための手段】前記目的達成のため、本発明は以下に述べる製造方法および構造を主要点としたものである。なお、本発明は主として前記トランジスタのうちＮｃｈ側に関するものである。これはＰｃｈ側も同じような製法で作ってもよいが、周知のように、Ｐｃｈ側は特にＬＤＤ構造にする必要はないからであり、本発明の説明からは除いた。

【００１０】（１）ＬＤＤ型構造（以下一々ＬＤＤ型と

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記述しない）としてのソース・ドレインの最初のｎ⁻層を形成する際、常にゲート電極の下にオーバーラップした構造となるよう、斜めにイオン注入法によりマスク酸化膜なしで行なうようにした。

（２）ゲート電極側壁にＬ型サイドウォールを形成し、それをマスクにしてソース・ドレイン層のｎ⁺の浅い層とｎ⁻の深い拡散層とを同時または片方（ｎ⁻層）を固相拡散で形成するようにした。このとき、深い拡散層は、ソース・ドレイン部をシリサイド化したシリサイド膜を通して形成するようにした。

【００１１】（３）ソース・ドレイン領域の不純物の活性化熱処理は（このとき第２の実施例では固相拡散も行なう）、層間絶縁膜の平滑化熱処理と同時に行うようにした。

【００１２】

【作用】本発明は、前述した点を中心にした製造方法でＭＯＳＦＥＴを形成、つまり、ソース・ドレイン形成用イオン注入ドーズ量が接合深さを十分浅くできる構造としてソース・ドレインを形成したので、短チャネル効果を十分抑制できるとともに、サイドウォールの外側でソース・ドレインの表面がシリサイド膜となっており、その領域のみ接合が深くなっているため、トランジスタの短チャネル効果を増大させることなく、接合リーク電流の増大を抑制できる。

【００１３】

【実施例】図１に、本発明の第１の実施例の製造工程を断面図で示し、以下に説明する。なお、第１の実施例も後述する第２の実施例も、前述したようにＮｃｈ側のみの製法であり、図１も図２もその部分のみ表示してある。

【００１４】まず、図１（ａ）に示すように、半導体基板（この場合、Ｐ型で面方位（１００）面のシリコン基板、以下、単に基板と称す）１上に、従来同様ＬＯＣＯＳ法により素子分離領域としてのフィールド酸化膜２を４０００Å程度の厚さ（以下一々厚さと記述しない）形成する。以下の各工程での形成は、言うまでもなくフィールド酸化膜２で素子分離された素子形成領域に行なうものである。

【００１５】次いで、図１（ｂ）に示すように、高清浄度なドライ酸化雰囲気中で、ゲート酸化膜３を１００Å程度形成し、その上にＬＰＣＶＤ（減圧化学的気相成長）法でポリシリコン（多結晶シリコン）膜４を３０００Å程度形成し、通常のホトリソ（ホトリソグラフィ）・エッチング技術により、ゲート電極としての所定のパターン４を形成する。ここまでもその形成方法は従来同様である。また、ゲート電極４以外、つまりソース・ドレイン領域となる部分の前記ゲート酸化膜３は界面活性剤入りのバッファードフッ酸でエッチング除去する。次いで、ホットキャリア効果抑制用のＬＤＤ型のソース・ドレイン層のｎ⁻層５ａ，５ｂを形成するための不純物

（As，P等）のイオン注入を2×10^{13} ions／cm^{2}程度のドーズ量で45°程度の大傾斜の斜めイオン注入条件で行なう。すると、前記n^-層5a，5bが図のようにゲート電極4の下にオーバーラップした形状に形成される。

【0016】次いで、図1（c）に示すように、ソース・ドレイン領域5a，5bのイオン注入ダメージ回復のために、ドライ酸化雰囲気中で850℃、30minの条件で熱処理を行ない、ゲート電極4表面とソース・ドレイン領域5a，5b表面に酸化膜7，6a，6bを形成する。次ぎに、LPCVD法により耐酸化性膜であるシリコン窒化膜（以下、単に窒化膜と称す）8を全面に500Å程度形成する。次いで、LPCVD法により絶縁膜であるシリコン酸化膜（以下、単に酸化膜と称す）を形成し、それを比較的イオンエネルギーの高い異方性の反応性イオンエッチング法（RIE）によりエッチングし、ゲート電極4側壁にサイドウォール酸化膜9a，9bを形成する。

【0017】次いで、図1（d）に示すように、ウエットエッチング法あるいは比較的イオンエネルギーの低いRIE法で、前記サイドウォールの酸化膜9a，9bをマスクにして、前記窒化膜8をエッチング除去する。その後、前記酸化膜6a，6bを界面活性剤入りのバッファードフッ酸にて基板1表面があれないようにエッチング除去する。このとき、前記サイドウォール酸化膜9a，9bも同時にエッチング除去される。すると、図1（d）に示すように、ゲート電極4の側壁に前記窒化膜8がL字型のサイドウォールとして残る。図1（d）ではこれを12a，12bと表示してある。

【0018】次いで、図1（e）に示すように、全面にプラズマスパッタリング法により、高融点金属（例えば、コバルト（Co）、チタニウム（Ti）、タングステン（W）など、本実施例はTiとする）13を100～500Å程度形成する。

【0019】次ぎに、図1（f）に示すように、2段階短時間熱処理法により、ゲート電極4上とソース・ドレイン領域5a，5bの露出部を自己整合的にシリサイド（$TiSi_2$）化させて、高融点金属シリサイド膜15，14a，14bを形成する。まず、第1段階目の短時間熱処理は、600～700℃の範囲で10～60秒間、N_2雰囲気中で行なう。次ぎに、サイドウォール12a，12b上部およびフィールド酸化膜2上の未反応TiおよびTiN膜を選択的にウエットエッチング法（例えばアンモニア水（NH_3OH）と過酸化水素水（H_2O_2）の混合液）により、室温でエッチング除去する。次ぎに、第2段階目の短時間熱処理は、700～900℃の範囲で10～60秒間、N_2雰囲気あるいはAr雰囲気中で行なう。このとき、ゲート電極4上のシリサイド膜15とソース・ドレイン領域のシリサイド膜14a，14bは完全な$TiSi_2$を形成する。一般に

このようなシリサイド膜を形成するプロセスでできた形状をサリサイド構造と言う。

【0020】次ぎに、図1（g）に示すように、前記L字型サイドウォール12a，12bをマスクにして、ソース・ドレイン領域にn^+層の浅い拡散層16a，16bと深い拡散層17a，17bを形成する。このn^+層の浅い拡散層16a，16bは、ヒ素（As）を3×10^{15}～1×10^{16} ions／cm^{2}のドーズ量で50keV加速エネルギーの条件で、前記L字型サイドウォール12a，12bの下部にイオン注入する。また、n^+層の深い拡散層17a，17bは、リン（P）をドーズ量1×10^{14}～1×10^{15} ions／cm^2（前記Asより濃度が薄い）、加速エネルギー100keVの条件で前記シリサイド膜14a，14b界面下にイオン注入する。つまり、最初の不純物（本例の場合As）より2番目の不純物（この場合P）の濃度を薄くするのである。

【0021】次いで、図1（h）に示すように、全面にLPCVD法により窒化膜18を500Å程度形成し、その上に、常圧CVD法により酸化膜19を1000Å、さらにその上にボロンとリンを含む酸化膜20を7000Å程度、連続的に形成する。そして、ドライN_2雰囲気中あるいはウエットO_2雰囲気中で、800～900℃の温度範囲で20～60分間熱処理を行ない、前記ボロン、リンを含む酸化膜20表面の平滑化とソース・ドレイン領域のn^+，n^-拡散層5a，5b，16a，16b，17a，17bの不純物活性化を同時に行う。

【0022】次ぎに、図1（i）に示すように、通常のホトリソ・エッチング技術により、ソース・ドレイン領域上、あるいはゲート電極4上にコンタクトホール21を形成し、次いで、スパッタリング法により2層あるいはそれ以上積層した金属膜を形成し、ホトリソ・エッチング技術でパターニングしてメタル配線22を形成してNch側のMOSFET構造を得る。

【0023】次ぎに、本発明の第2の実施例の製造工程を図2に断面図で示し、以下に説明する。説明および表示の主旨は第1の実施例で述べた通りである。また、第1の実施例の図1と同じ機能部分には同じ符号を付してある。

【0024】本第2の実施例の図2の（a）ないし（c）の工程は、第1の実施例の図1の（a）ないし（c）の工程と全く同じであるので、あらためて説明することは割愛する。従って、以下の説明は図2（c）の工程の後の工程である図2（d）の工程から記述する。

【0025】前記工程後、図2（d）に示すように、サイドウォール酸化膜9a，9bをマスクにして、第1の実施例同様の方法でゲート電極4側壁以外の窒化膜8をエッチング除去する。すると、前記窒化膜8はゲート電極4側壁にL字型12a，12bとして残る。

【0026】次いで、これも第1の実施例同様、前述した酸化膜6a，6bおよびサイドウォール酸化膜9a，9bを除去し、基板1上にできた自然酸化膜などの不純物をAr＋H_2ガス雰囲気中のプラズマ表面クリーニングを行なった後、図2（e）に示すように、高融点金属13を第1の実施例同様形成する。

【0027】次いで、図2（f）に示すように、これも第1の実施例と同じように、2段階短時間熱処理法により、ゲート電極4上の15とソース・ドレイン領域の14a，14bに示す高融点金属シリサイド膜を形成する。勿論、第1の実施例同様、不要な高融点金属は除去する。

【0028】次ぎに、図2（g）に示すように、ソース・ドレイン形成用不純物（リン）を加速エネルギー100keV、ドーズ量1×10^{14}～1×10^{15}ions／cm^2と通常使用されるドーズ量（3×10^{15}～5×10^{15}ions／cm^2）より低いドーズ量とで前記L字型窒化膜サイドウォール12a，12b下に注入し、n^+拡散層16a，16bを形成する。引き続き、ソース・ドレイン形成用不純物（ヒ素）を加速エネルギー50keV、ドーズ量3×10^{15}～5×10^{15}ions／cm^2の条件で、前記ソース・ドレイン領域に形成されたシリサイド膜14a，14b中に注入する。

【0029】次いで、図2（h）に示すように、第1の実施例同様、全面に窒化膜15、その上に酸化膜19、さらにその上にボロン、リンを含む酸化膜20を形成し、熱処理を行なうと、前記ボロン、リンを含む酸化膜20の平滑化とともに、前記シリサイド膜14a，14bからの固相拡散により、その下にn^-の深い層17a，17bが形成される。

【0030】後は、第1の実施例同様、図2（i）に示すように、コンタクトホール21を形成し、メタル配線22を形成してNch側のMOSFETの構造を得る。

【0031】第1、第2の実施例とも最終的な構造としては、ゲート電極4の側壁に耐酸化性膜のサイドウォール12a，12bがあり、ソース・ドレインの拡散層は、最も浅い層5a，5bがゲート電極4の下部にオーバーラップしており、次の層16a，16bが前記サイドウォール12a，12bの下部まであり、一番深い層17a，17bが前記サイドウォール12a，12bの外側にある。また、ソース・ドレインの最も深い層17a，17bの上部、つまり、前記サイドウォール12a，12bの外側の前記ソース・ドレイン上（およびゲート電極4上）にシリサイド膜14a，14b（および15）が存在しているものである。

【0032】

【発明の効果】以上詳細に説明したように、本発明の製造方法によれば以下に述べるような効果がある。

【0033】（1）ソース・ドレイン形成用イオン注入ドーズ量が接合深さを十分に浅くし、しかも駆動力を低下させない様な範囲に制御されるため、微細なMOSFETにおいて十分な短チャネル効果が抑制され、しかも高駆動力のMOSFETが実現可能となる。また、ホットキャリア耐性の向上が期待できる。

【0034】（2）比較的長いサイドウォールの外側でソース・ドレイン領域の表面をシリサイド膜としており、しかも、その領域のみ接合が深くなっているため、トランジスタの短チャネル効果を増大させることなく、接合リーク電流の増大を抑制できる。さらに、ソース・ドレインのイオン注入を比較的低ドーズとし、ソース・ドレインのシート抵抗増大をサリサイド化により抑え、十分な低抵抗化を実現できる。

【0035】（3）シリコンと高融点金属を反応させるシリサイド化工程では、そのシリコン中の不純物が従来より非常に低いため、すなわち、n^+層ソース・ドレイン領域を形成する前にシリサイド化しているため、シリサイド化工程も再現性よく安定して行なえる。

【0036】（4）深いn^-拡散層は、シリサイド化後、シリサイド界面にイオン注入するか、シリサイド膜からの固相拡散で形成しているため、シリサイド界面や拡散層界面が凸凹にならないスムーズな界面が得られ、かつ、シリサイドと拡散層界面の濃度が高濃度に保たれ、オーミック接合が再現性よく安定して形成できる。

【0037】（5）LDD構造を形成するのに、サイドウォールエッチングのときのプラズマダメージを抑えるエッチングストッパー膜が形成されているため、トランジスタ特性が信頼性よく再現性よく安定に得られる。

【0038】（6）ソース・ドレイン、LDD構造形成のための不純物注入は、それぞれマスク酸化膜なしにシリコン基板表面に直接行なうようにしているため、マスク酸化膜中の酸素のシリコン基板へのノックオンによる拡散層不純物の不活性化を防止でき、その後の熱処理において低温で活性化アニールが可能となる。

【0039】（7）LDD構造を形成するのに、L型の窒化膜サイドウォールマスク膜だけで、イオン注入領域の打ち分けを行なうため、マスクステップ数が簡略化でき、工程を簡略化できる。

【0040】（8）n^+層となる領域がゲート電極とオーバーラップすることをさけることにより、バンド間トンネルによるドレインリーク電流の発生を回避することが可能である。

【0041】（9）サイドウォールのエッチングに影響しないL型の前記サイドウォールによって、LDD構造の浅いn^+拡散層を形成したので、ゲート長のバラツキを決める主要因であったサイドウォールエッチングのバラツキをゲート長のバラツキ要因より省くことができ、バラツキの小さいMOSFETの特性を安定に得ることができる。

【0042】（10）ソース・ドレイン領域の高融点金属シリサイド膜上には、シリコン窒化膜という熱による

膜ストレス緩和のためのバッファ層が形成されているため、その後の熱処理によるシリサイド膜の耐熱性向上および膜ストレスによるシリコン基板への結晶誘起欠陥の発生防止が可能となり、高密度でかつ高速化が可能な信頼性の高いＬＳＩが実現できる。

【００４３】（１１）サイドウォール側壁膜として、高誘電率のシリコン窒化膜を用いているため、ソース・ドレイン領域のゲート電極近傍の電界が緩和され、ホットエレクトロン耐性の向上が期待でき、信頼性の高いＬＳＩが実現できる。

【図面の簡単な説明】

【図１】本発明の第１の実施例の工程説明図

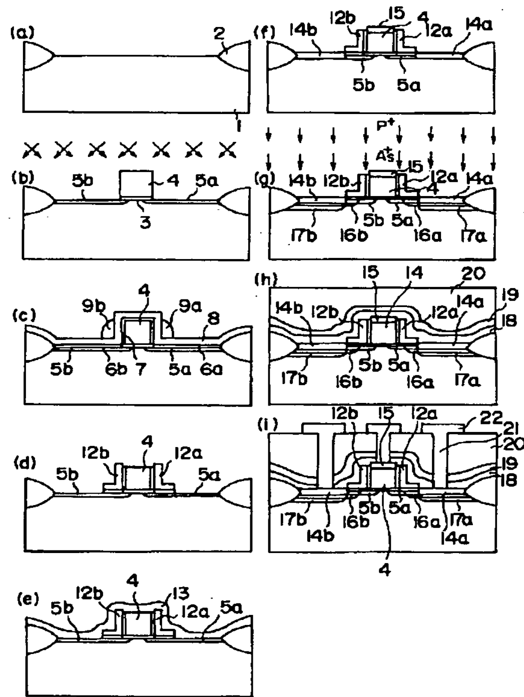
【図２】本発明の第２の実施例の工程説明図

【図３】従来例の工程説明図

【符号の説明】

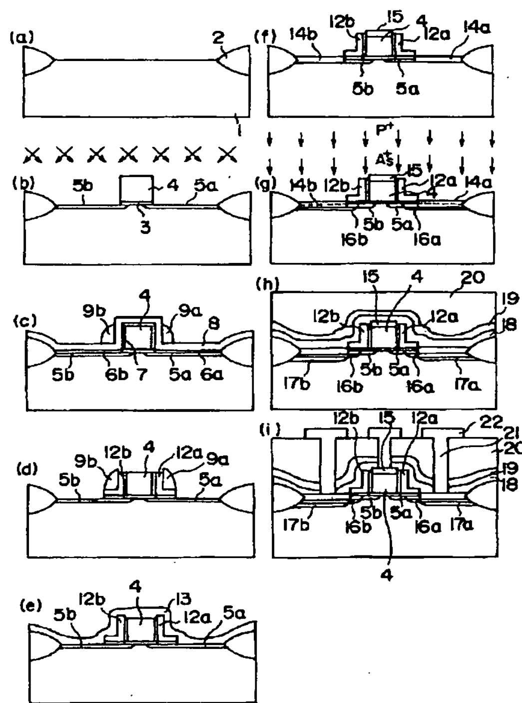
１　基板
４　ゲート電極
５ａ，５ｂ　ソース・ドレインのｎ⁻層
６ａ，６ｂ，７，１９　酸化膜
８，１８　窒化膜
９ａ，９ｂ　サイドウォール酸化膜
１２ａ，１２ｂ　Ｌ字型窒化膜サイドウォール
１３　高融点金属膜
１４ａ，１４ｂ，１５　シリサイド膜
１６ａ，１６ｂ　ソース・ドレインの浅いｎ⁺層
１７ａ，１７ｂ　ソース・ドレインの深いｎ⁻層

【図１】



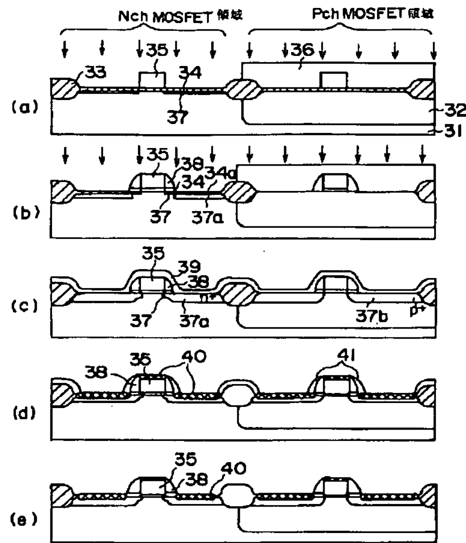
本発明の第１の実施例の工程説明図

【図２】



本発明の第２の実施例の工程説明図

【図3】



従来例の工程説明図

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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 03/10/2006

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
POTTER, ROY KARL	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/10/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/995,283	11/24/2004	Mizuki Segawa	71971-012	5361

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	06/12/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 01/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 03/10/2006

McDermott Will & Emery LLP
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Washington, DC 20005-3096

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/995,283	11/24/2004	Mizuki Segawa	71971-012	5361

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	06/12/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
POTTER, ROY KARL	2822	257-288000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
   (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1 ______________________
   2 ______________________
   3 ______________________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies ______________

4b. Payment of Fee(s):
- ☐ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number ______________ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ______________________ Date ______________________

Typed or printed name ______________________ Registration No. ______________________

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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7590 03/10/2006

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
POTTER, ROY KARL	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/10/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 01/06) Approved for use through 04/30/2007.

H·A

Notice of Allowability	Application No. 10/995,283	Applicant(s) SEGAWA ET AL.	
	Examiner Roy K. Potter	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Applicant's response of 12/21/05*.
2. ☒ The allowed claim(s) is/are *39-52*.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☒ Certified copies of the priority documents have been received in Application No. *10/454,682* .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

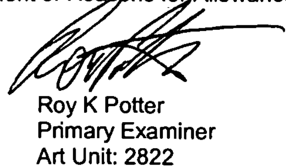
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

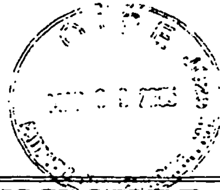
   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.



Roy K Potter
Primary Examiner
Art Unit: 2822



SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
71971-012	10/995,283
APPLICANT	
Mizuki SEGAWA, et al.	
FILING DATE	GROUP
November 24, 2004	2812

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Codes (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
[initials]		US	4,966,870	10/30/1990	Barber et al.	
[initials]		US	5,384,281	01/24/1995	Kenney et al.	
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	No
[initials]		EP 0 706 206 A2	04/10/1996	MOTOROLA, INC.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	

EXAMINER	DATE CONSIDERED
[signature]	1/28/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 71971-012	SERIAL NO. Divisional of Application No. 10/454,682
	APPLICANT Mizuki SEGAWA, et al.	
	FILING DATE November 24, 2004	GROUP Not yet assigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
			4,578,128	03/1986	Mundt et al.	
		US	5,177,028	01/1993	Manning	
		US	5,196,910	03/1993	Moriuchi et al.	
		US	5,286,674	02/1994	Roth et al.	
		US	5,319,235	06/1994	Kihara et al.	
		US	5,393,708	02/1995	Hsia et al.	
		US	5,397,910	03/1995	Ishimaru	
		US	5,401,673	03/1995	Urayama	
		US	5,413,881	05/1995	Kim	
		US	5,433,794	07/1995	Fazan et al.	
		US	5,497,016	03/1996	Koh	
		US	5,521,422	05/1996	Mandelman et al.	
		US	5,561,311	10/1996	Hamamoto et al.	
		US	5,777,370	07/1998	Omid-Zohoor et al.	
			5,804,862	09/1998	Matumoto	
		US	6,022,781	02/2000	Noble, Jr.	
		US	6,077,344	06/2000	Shoup et al.	
		US	6,278,138 B1	08/2001	Suzuki	
		US	6,281,562	08/2001	Segawa et al.	

FOREIGN PATENT DOCUMENTS

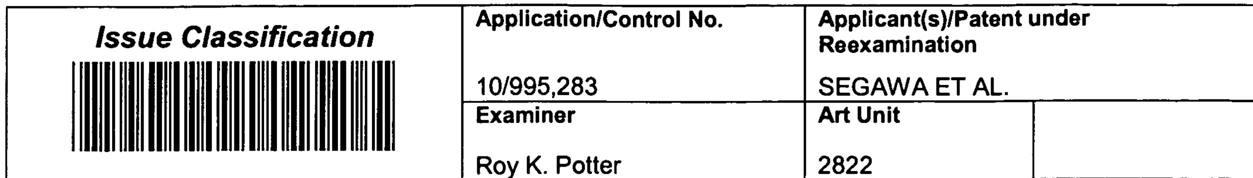
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code-Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
		JP 59181062 A	10/1984				
		JP 62-85461	04/1987				
		EP 0234988-A1	04/1987				
		EPA 0 243 988	11/1987				
		JP 03079033 A	04/1991				
		JP 4-48647	02/1992				
		JP 4-68564	03/1992				
		JP 4-305922	10/1992				
		EPA 0 513 639	11/1992				
		JP 6-45432	02/1994				
		JP 6-163843	06/1994				
		JP 7-273330	10/1995				
		JP 09162392 A	06/1997				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

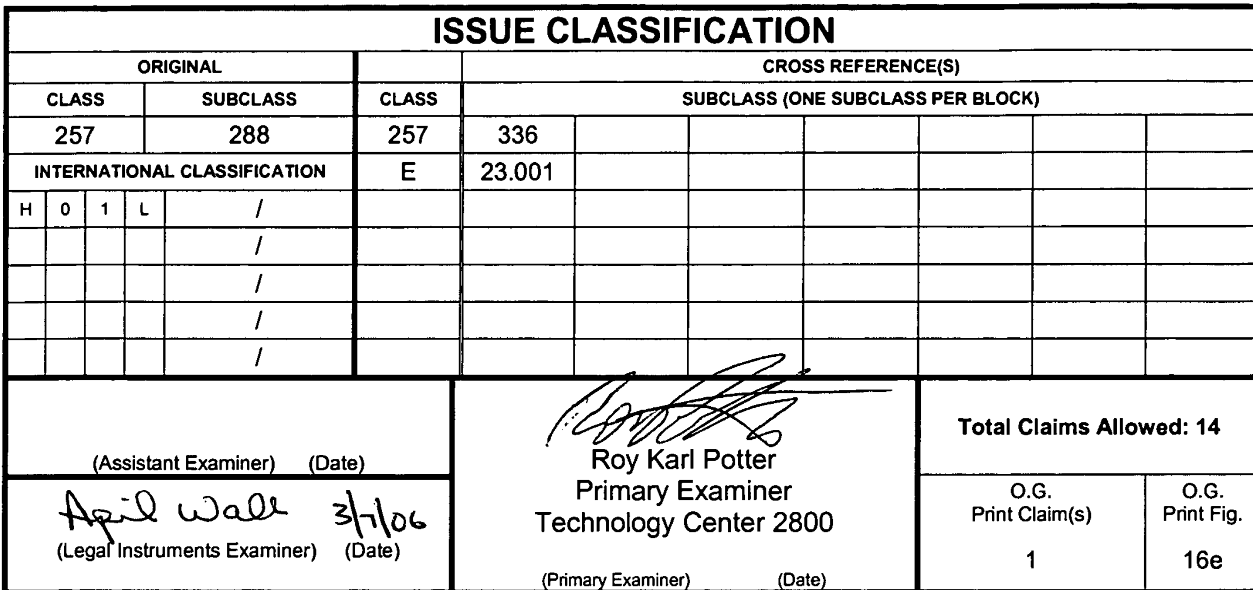
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER	DATE CONSIDERED 9/15/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.



Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/995,283	SEGAWA ET AL.	
	Examiner	Art Unit	
	Roy K. Potter	2822	



ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
257	288	257	336					
INTERNATIONAL CLASSIFICATION		E	23.001					
H 0 1 L	/							
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	/							
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	/							

(Assistant Examiner) (Date)

April Wall 3/7/06
(Legal Instruments Examiner) (Date)

Roy Karl Potter
Primary Examiner
Technology Center 2800
(Primary Examiner) (Date)

Total Claims Allowed: 14

O.G. Print Claim(s)	O.G. Print Fig.
1	16e

☐ **Claims renumbered in the same order as presented by applicant** ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9	1	39		69		99		129		159		189
	10	2	40		70		100		130		160		190
	11	3	41		71		101		131		161		191
	12	4	42		72		102		132		162		192
	13	5	43		73		103		133		163		193
	14	6	44		74		104		134		164		194
	15	7	45		75		105		135		165		195
	16	8	46		76		106		136		166		196
	17	9	47		77		107		137		167		197
	18	10	48		78		108		138		168		198
	19	11	49		79		109		139		169		199
	20	12	50		80		110		140		170		200
	21	13	51		81		111		141		171		201
	22	14	52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Index of Claims	Application/Control No. 10/995,283	Applicant(s)/Patent under Reexamination SEGAWA ET AL.
	Examiner Roy K. Potter	Art Unit 2822

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim Final	Claim Original	Date 3/6/06
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Claim Final	Claim Original	Date 3/6/06
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Claim Final	Claim Original	Date
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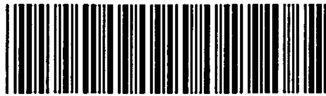
U.S. Patent and Trademark Office | Part of Paper No. 20060306

Search Notes 	Application/Control No. 10/995,283	Applicant(s)/Patent under Reexamination SEGAWA ET AL.	
	Examiner Roy K. Potter	Art Unit 2822	

SEARCHED			
Class	Subclass	Date	Examiner
257	384, 336	3/6/2006	RP
257	288, 333	3/6/2006	RP
257	386, 389	3/6/2006	RP
257	401	3/6/2006	RP

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
257	**384, 336**	3/6/2006	**RP**
	288, 333	3/6/2006	RP
	386, 389	3/6/2006	RP
257/401		3/6/2006	RP

SEARCH NOTES (INCLUDING SEARCH STRATEGY)	DATE	EXMR
EAST SEARCH	3/5/2006	RP

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 5361

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/995,283	11/24/2004 RULE	257	2822	71971-012

APPLICANTS

Mizuki Segawa, Osaka, JAPAN;

Isao Miyanaga, Osaka, JAPAN;
Toshiki Yabu, Osaka, JAPAN;Takashi Nakabayashi, Osaka, JAPAN;
Takashi Uehara, Osaka, JAPAN;
Kyoji Yamashita, Osaka, JAPAN;
Takaaki Ukeda, Osaka, JAPAN;
Masatoshi Arai, Osaka, JAPAN;
Takayuki Yamada, Osaka, JAPAN;
Michikazu Matsumoto, Osaka, JAPAN;

** CONTINUING DATA *************************
This application is a DIV of 10/454,682 06/05/2003 PAT 6,967,409
which is a DIV of 09/902,157 07/11/2001 PAT 6,709,950
which is a DIV of 08/685,726 07/24/1996 PAT 6,281,562

** FOREIGN APPLICATIONS ********************
JAPAN 7-192181 07/27/1995
JAPAN 7-330112 12/19/1995

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 01/21/2005

Foreign Priority claimed ☑ yes ☐ no 35 USC 119 (a-d) conditions met ☑ yes ☐ no ☐ Met after Allowance Verified and Acknowledged ____ Examiner's Signature ____ Initials	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
	JAPAN	21	14	1

ADDRESS
McDermott Will & Emery LLP
600 13th Street, N.W.
Washington , DC
20005-3096

TITLE

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"E23.001"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 11:21
L2	0	sidewall and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 11:21

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	21	"l-shaped" with sidewall same gate same active	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/28 12:17
L2	433	(257/384).CCLS.	USPAT	OR	OFF	2006/02/28 12:18
L3	595	(257/336).CCLS.	USPAT	OR	OFF	2006/02/28 12:18
L4	560	(257/288).CCLS.	USPAT	OR	OFF	2006/02/28 12:19
L5	202	(257/333).CCLS.	USPAT	OR	OFF	2006/02/28 12:21
L6	141	(257/386).CCLS.	USPAT	OR	OFF	2006/02/28 12:21
L7	142	(257/389).CCLS.	USPAT	OR	OFF	2006/02/28 12:21
L8	1076	(257/401).CCLS.	USPAT	OR	OFF	2006/02/28 12:21

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

Application or Docket Number: 10/995283

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	* –
INDEPENDENT CLAIMS	minus 3 =	* –
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	150.00	OR	BASIC FEE	300.00
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

12/30/05	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 14	Minus	** 20	=
Independent	* 1	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

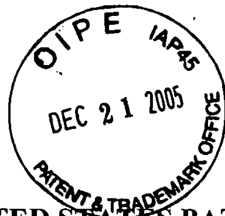
	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 10/04)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE



Docket No.: 71971-012 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mizuki SEGAWA, et al.	:	Confirmation Number: 5361
Application No.: 10/995,283	:	Group Art Unit: 2822
Filed: November 24, 2004	:	Examiner: Roy K. POTTER

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

RESPONSE UNDER 37 C.F.R. § 1.111

Mail Stop Amendment
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Office Action dated October 5, 2005, having a shortened statutory period for response set to expire January 5, 2006, Applicant respectfully requests reconsideration of the pending rejections for the reasons set forth below.

REMARKS

In response to the pending Office Action, Applicants respectfully submit that the pending rejections must be withdrawn because the cited prior art reference does not constitute valid prior art to the above-identified application for the reasons set forth below. Applicants note with appreciation the indication of allowance of claims 40-42 and 44-52.

Turning to the rejection of claims 39 and 43, as set forth on page 2 of the Office Action, these claims were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 5,817,562 to Chang. The above-identified application claims priority to USP No. 6,281,562 (application Ser. No. 08/685,726), which has a filing date of July 24, 1996. Chang has an effective filing date of January 24, 1997. As such, because the effective filing date of the instant application precedes the effective filing date of Chang, Chang does not constitute valid prior art relative to the instant applicaton. As a result, the pending rejection must be withdraw.

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ete:dmd
Facsimile: 202.756.8087

Date: December 21, 2005

WDC99 1173131-1.071971.0012

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/995,283	11/24/2004	Mizuki Segawa	71971-012	5361

7590 10/05/2005

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER
POTTER, ROY KARL

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/995,283	SEGAWA ET AL.	
	Examiner	Art Unit	
	Roy K. Potter	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39 and 43* is/are rejected.

7)☒ Claim(s) *40-42 and 44-52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 39 – 52 are pending. These claims are directed to a semiconductor device

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 39, 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al..

Chang et al., U.S. Patent No. 5,817,562 discloses a method for making improved polysilicon FET gate electrode structures. As shown in Figure 7, a gate insulating film 14 is formed over an active area. A gate electrode 16 is formed over the gate insulating film. L-shaped sidewalls 24 are formed over the side surfaces of the gate electrode. The L-shaped sidewalls 24 are polysilicon oxide. In column 7, line 23 describes a silicide layer being used to contact source/drain areas 23.

Allowable Subject Matter

Claims 40-42 and 44 – 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art does not disclose that L-shaped sidewalls are of silicon nitride. They are disclosed as being silicon oxide.

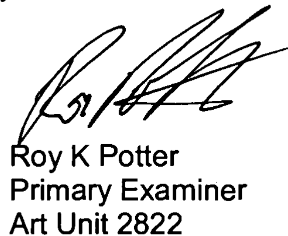
The prior art does not disclose a protection oxide between the gate electrode and the L-shaped sidewall.

The prior art does not disclose a second silicide layer on the gate oxide.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roy K. Potter whose telephone number is 571 272 1842. The examiner can normally be reached on M-F.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Roy K Potter
Primary Examiner
Art Unit 2822

SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 71971-012	SERIAL NO. Divisional of Application No. 10/454,682
	APPLICANT Mizuki SEGAWA, et al.	
	FILING DATE November 24, 2004	GROUP Not yet assigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.		Document Number Number-Kind Code2 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
[initials]			4,578,128	03/1986	Mundt et al.	
[initials]		US	5,177,028	01/1993	Manning	
[initials]		US	5,196,910	03/1993	Moriuchi et al.	
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[initials]		US	5,319,235	06/1994	Kihara et al.	
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[initials]		US	5,397,910	03/1995	Ishimaru	
[initials]		US	5,401,673	03/1995	Urayama	
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[initials]		US	6,022,781	02/2000	Noble, Jr.	
[initials]		US	6,077,344	06/2000	Shoup et al.	
[initials]		US	6,278,138 B1	08/2001	Suzuki	
[initials]		US	6,281,562	08/2001	Segawa et al.	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3 -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	No
[initials]		JP 59181062 A	10/1984				
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[initials]		EPA 0 243 988	11/1987				
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[initials]		JP 09162392 A	06/1997				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	

EXAMINER [signature]	9/15/05 DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Notice of References Cited	Application/Control No. 10/995,283	Applicant(s)/Patent Under Reexamination SEGAWA ET AL.	
	Examiner Roy K. Potter	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,817,562	10-1998	Chang et al.	438/305
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/995,283	SEGAWA ET AL.
	Examiner	Art Unit
	Roy K. Potter	2822

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)	DATE	EXMR
EAST SEARCH	9/15/2005	RP

Index of Claims	Application/Control No. 10/995,283	Applicant(s)/Patent under Reexamination SEGAWA ET AL.
	Examiner Roy K. Potter	**Art Unit** 2822

√	Rejected	—	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	822	interconnect same barrier same seed same metal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/15 16:17
L2	2	(("6709950") or ("6281562")).PN.	USPAT	OR	OFF	2005/09/15 16:17
L3	22	("4578128" | "5177028" | "5196910" | "5286674" | "5319235" | "5397910" | "5401673" | "5413961" | "5433794" | "5497016" | "5521422" | "5561311" | "5777370" | "5804862" | "6022781"). PN. OR ("6281562").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/15 16:23
L4	1466	"L-shaped" with sidewall	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/15 16:23
L5	50	"L-shaped" with sidewall same gate adj electrode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/15 16:28
L6	14	"L-shaped" with sidewall same gate adj electrode same silicide	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/15 16:28

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	822	interconnect same barrier same seed same metal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/15 16:17
L2	2	(("6709950") or ("6281562")).PN.	USPAT	OR	OFF	2005/09/15 16:17
L3	22	("4578128" | "5177028" | "5196910" | "5286674" | "5319235" | "5397910" | "5401673" | "5413961" | "5433794" | "5497016" | "5521422" | "5561311" | "5777370" | "5804862" | "6022781"). PN. OR ("6281562").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/09/15 16:23
L4	1466	"L-shaped" with sidewall	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/15 16:23
L5	50	"L-shaped" with sidewall same gate adj electrode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/15 16:28
L6	14	"L-shaped" with sidewall same gate adj electrode same silicide	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/15 16:28

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2004

Application or Docket Number
10555283

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	14	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	14 minus 20=	* —
INDEPENDENT CLAIMS	1 minus 3 =	* —
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ RATE	FEE	OR	OTHER THAN SMALL ENTITY RATE	FEE
BASIC FEE	395.00	OR	BASIC FEE	790.00
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL		OR	TOTAL	790

CLAIMS AS AMENDED - PART II

11-24-04

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 14	Minus	** —	=
Independent	* 1	Minus	*** —	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 10/04) Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Best Available Copy

Docket No.: 71971-012

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mizuki SEGAWA, et al.	:	Confirmation Number: 5361
Application No.: 10/995,283	:	Group Art Unit: 2812
Filed: November 24, 2004	:	Examiner: Not yet assigned

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

Please be advised that U.S. references 6,077,344 and 6,278,138 B were inadvertently listed on the PTO-1449 filed on November 24, 2004. and need not be considered by the Examiner for this application.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Each non-English language reference was first cited in a corresponding foreign application search report or office action and its relevance discussed therein. A copy of the foreign search report or office action is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ete
Facsimile: 202.756.8087
Date: March 9, 2005

SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 71971-012	SERIAL NO. 10/995,283
	APPLICANT Mizuki SEGAWA, et al.	
	FILING DATE November 24, 2004	GROUP 2812

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	4,966,870	10/30/1990	Barber et al.	
		US	5,384,281	01/24/1995	Kenney et al.	
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	No
		EP 0 706 206 A2	04/10/1996	MOTOROLA, INC.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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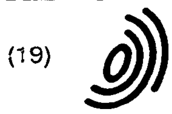


(19) Europäisches Patentamt

European Patent Office

Office européen des brevets

(11) EP 0 706 206 A2

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
10.04.1996 **Bulletin 1996/15**

(51) Int. Cl.[6]: **H01L 21/311**

(21) Application number: **95114230.6**

(22) Date of filing: **11.09.1995**

(84) Designated Contracting States:
DE FR GB IT

(30) Priority: **19.09.1994 US 308224**

(71) Applicant: **MOTOROLA, INC.**
Schaumburg, IL 60196 (US)

(72) Inventors:
- **Lin, Jung-Hui**
Austin, Texas 78750 (US)
- **Koh, Ai**
Austin, Texas 78729 (US)

(74) Representative: **Hirsz, Christopher Stanislaw et al**
Motorola
European Intellectual Property Operations
Midpoint
Alencon Link
Basingstoke, Hampshire RG21 1PL (GB)

(54) **Method for etching silicon nitride**

(57) In accordance with the present invention, a silicon nitride layer (20) in a semiconductor device (10) is anisotropically etched selectively to both silicon dioxide, for example gate oxide layer (16), and to silicon, for example, silicon substrate (12) and polysilicon gate electrode (18). The silicon nitride layer is etched in a plasma etch system using CF_4, O_2, and argon gases. In other applications of the present invention, the etch method is used to remove an ONO dielectric stack and to remove a silicon nitride etch stop layer selectively to both active regions and isolation regions to form contacts or local interconnects across these regions.

EP 0 706 206 A2

Description

Field of the Invention

The present invention relates generally to methods for etching silicon nitride, and more specifically to methods for etching silicon nitride films in semiconductor devices.

Background of the Invention

Silicon nitride is used in semiconductor devices for a variety of reasons, including use as etch stop layers, masking layers, sidewall spacers, gate dielectrics, and the like. Because silicon nitride is used so heavily in the manufacture of semiconductor devices, a variety of etch chemistries are necessary in order to remove the silicon nitride from selective areas of the device. In removing silicon nitride, it is often necessary to etch the silicon nitride away without damaging or etching underlying layers within the semiconductor device. For example, it is often necessary to remove silicon nitride selectively to an underlying layer of silicon dioxide, or to an underlying polysilicon layer, or to the silicon substrate. A variety of dry etch chemistries exist which accomplish these objectives. For example, a common dry etch which is used to etch silicon nitride selectively to silicon dioxide uses SF_6. As another example, a chemistry of CHF_3 and O_2 is used to dry etch silicon nitride selectively to silicon. As is evident from these examples, different dry etch chemistries are often required to etch silicon nitride selectively to silicon dioxide and silicon. To date, no dry etch chemistry has been developed which can etch silicon nitride selectively to both silicon dioxide and to silicon simultaneously with acceptable selectivity values. A dry silicon nitride etch having selectivity to both silicon dioxide and silicon would be a welcome advance in the field of semiconductor manufacturing, particularly in areas such as local interconnect and sidewall spacer technology.

Brief Description of the Drawings

FIGs. 1-3 are cross-sectional illustrations of a portion of a semiconductor device wherein sidewall spacers are formed in accordance with the present invention.

FIGs. 4-6 are cross-sectional illustrations of a portion of a semiconductor device wherein the present invention is used for the manufacture of a device which includes an ONO (oxide-nitride-oxide) gate dielectric stack.

FIGs. 7-9 are cross-sectional illustrations of a portion of a semiconductor device wherein a local interconnect is formed in accordance with the present invention.

Detailed Description of a Preferred Embodiment

In accordance with the present invention silicon nitride can be dry etched selectively to both silicon dioxide and silicon. Etching is accomplished in a plasma etch system and is anisotropic in nature. The selectivity and anisotropic nature of the etch is achieved through the use of CF_4 and O_2 gases with the addition of an inert gas, such as argon. While CF_4, O_2 and argon may be known individually for use in etching materials in semiconductor manufacturing, a combination of these gases in accordance with the present invention can achieve results not accomplished with prior art methods. For example, in prior art methods use of these gases to etch silicon nitride could not be achieved anisotropically, nor could the gases in combination be used to etch silicon nitride selectively to both silicon dioxide and silicon.

A preferred embodiment of the present invention employs a plasma etch system which does not generate a plasma downstream from the material to be etched, rather a plasma is generated within the etch chamber where the device to be etched is located. As an example, a magnetron etcher, such as Applied Materials' AMT5000, is a suitable etch system for practicing the present invention. Specific process parameters may vary depending on the type of plasma etch system used; however, the following process parameters have been demonstrated as providing the foregoing characteristics in the magnetron etch system. A pressure of the etch chamber is held to between 50-300 mTorr, while the RF power is held between 100-300 Watts. A CF_4 gas is introduced into the etch chamber at a rate of 2-8 standard cubic centimeters per minute (sccm). The flow rate of oxygen is 5-35 sccm, while the flow rate of an inert gas is between 40-140 sccm. While in a preferred embodiment argon is used as the inert gas, it is anticipated that other inert gases can be used, for example, xenon, helium, or nitrogen. With the foregoing process parameters, the selectivity of a plasma-enhanced chemical vapor deposited (PECVD) silicon nitride film etched selectively to oxide ranges from 1.5:1 to 9:1, with 33 out of 35 combinations achieving a selectivity greater than 2:1. Also with the foregoing process parameters, the selectivity of etching a PECVD silicon nitride film selectively to polysilicon ranges from 2.3:1 to 17:1, with 34 out of 35 combinations achieving a selectivity greater than 2.5:1.

Within the above process parameter ranges, the mechanism for etching silicon nitride in accordance with the invention involves both a chemical aspect and a physical bombardment or sputtering component, as opposed to being purely chemical mechanism. Thus, the etch may be classified as a reactive ion etch (RIE). The physical etch mechanism can be attributed to the facts that the etch system used is not a downstream etcher, that the pressure is maintained relatively low, that the silicon nitride is etched anisotropically, and that the ion energy within the etch chamber is relatively high (about 200 Volts).

While various combinations within the process parameter ranges provided above can successfully be used to etch silicon nitride selectively to both silicon dioxide and silicon, more preferred process parameter ranges are as follows: etch chamber pressure of 150-300

mTorr; RF Power between 100-300 Watts; CF_4 flow rate of 2-8 sccm; O_2 flow of 20-35 sccm, and inert (argon) flow rate of 40-140 sccm. Selectivity of silicon nitride to oxide within the preferred process parameter ranges is about 6:1 to 10:1, while selectivity of silicon nitride to silicon is about 12:1 to 17:1. A precise set of process parameters as used in the magnetron etch system which achieves a selectivity of silicon nitride to oxide of 8:1 and a selectivity of silicon nitride to polysilicon of 16:1 is as follows: pressure equal to 150 mTorr; RF power equal to 200 Watts; CF_4 flow rate equal to 3 sccm; O_2 flow rate equal to 30 sccm; and inert gas (argon) flow rate equal to 60 sccm. At all times the magnetic field used in the magnetron etch system was held to 30 gauss; however, it is anticipated that an increase or decrease in the magnetic field would only increase or decrease, respectively, the etch rates without adversely affecting the etch selectivities. Accordingly, the present invention may also achieve acceptable selectivity levels in the absence of any magnetic field. Also, it is noted that the etch selectivities resulting from the above processes occurred in etching silicon nitride in the presence of a photoresist mask, and that etch selectivities without a resist mask in place may be lower due to a lower concentration of polymers within the etch chamber.

Although the precise mechanisms for how the present invention as described above achieves selectivity to both silicon dioxide and silicon and achieves an anisotropic etch are not fully understood, experimentation has led to observation of some trends. The selectivity of silicon nitride to both silicon dioxide and polysilicon increases as the oxygen flow rate is increased within the range specified above (without varying any other process parameters). Varying only the RF Power within the range specified above resulted in an initial increase in both the selectivity to oxide and polysilicon, but then both selectivities begin to decrease as the end of this range is approached. Increasing the CF_4 flow rate without varying other process parameters tends to decrease the selectivity to both oxide and polysilicon. Increasing the flow rate of argon likewise decreased the selectivity to both oxide and polysilicon; however, the rate of decrease is less drastic than the trend observed with the CF_4 flow rate. Finally, increasing the pressure through the range specified above tends to increase the selectivity of etching silicon nitride to both oxide and polysilicon. How selectivities are affected by varying more than one process variable at a time have not been analyzed, so that the interaction of the various process variables is not understood. Further, experiments indicate that selectivities to both silicon dioxide and silicon are optimized within the above specified process parameter ranges when the flow rate of O_2 is at least three , and preferably at least four, times as great as the flow rate of CF_4, and when the inert (argon) gas flow rate is at least fifteen, and preferably at least sixteen, times as great as the flow rate of CF_4.

As mentioned earlier, silicon nitride has a variety of uses within the manufacture of semiconductor devices. These applications, and advantages, of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings. FIGs. 1-9 illustrate three examples of applications for use of the present invention in semiconductor manufacturing; however, other applications no doubt exist. It is important to point out that the illustrations may not necessarily be drawn to scale and that there may be other embodiments of the present invention which are not specifically illustrated. Throughout the various views, like reference numerals are used to designate identical or corresponding parts.

FIGs. 1-3 illustrate using the present invention to form silicon nitride sidewall spacers. As shown in FIG. 1, a semiconductor device 10 includes an active region of a semiconductor substrate 12. Within substrate 12 are doped regions 14 which serve as source and drain regions of an MOS (Metal Oxide Semiconductor) transistor. Typically, substrate 12 will be formed of single crystal silicon and doped regions 14 are formed by diffusing or implanting impurity atoms, either P-type or N-type, into the substrate. Overlying substrate 12 is a gate oxide layer 16, which is typically thermally grown to a thickness of less than 300Å. A polysilicon gate electrode 18 is patterned on the gate oxide layer. Gate electrode 18 is aligned such that sides or edges of the gate electrode are closely aligned with doped regions 14, although in actual manufacturing the doped regions are typically formed after the polysilicon gate electrode is patterned and are self-aligned to the gate electrode. After the gate electrode and doped regions have been defined on substrate 12, the polysilicon may be oxidized to form an oxide layer 19 on the gate electrode. A silicon nitride layer 20 is then deposited using conventional chemical vapor deposition (CVD). In accordance with this embodiment of the present invention, silicon nitride layer 20 will be used as a masking layer in a self-aligned silicide process. Silicide is often formed on polysilicon members and doped regions to improve the conductivity between these members and other conductive members within the device, such as contacts. A self-aligned silicide process involves using a mask to protect those regions of the device which are not to be silicided, and wherein the silicidation process can occur without a separate lithography step (i.e. the silicidation is self-aligned).

To achieve the self-aligned silicidation process in device 10 in accordance with the present invention, a resist mask 22, for example a photoresist mask, is formed over the device as illustrated in FIG. 1. Next, silicon nitride layer 20 is anisotropically etched with the resist mask in place using the etch method previously described in accordance with the invention. The resulting structure is illustrated in FIG. 2, wherein portions of silicon nitride layer 20 which were not protected by resist mask 22 in FIG. 1 have been anisotropically etched to form sidewall spacers 24 along sidewalls of polysilicon gate electrode 18 and wherein portions of silicon nitride layer 20 which were protected by resist mask 22 remain intact. Notice that as a result of the etch, gate oxide layer

16 is not attacked, since the etch chemistry used to etch silicon nitride in accordance with the present invention is selective to silicon dioxide. It is desirable to not remove gate oxide layer 16 in order to avoid damaging the underlying substrate when removing the silicon nitride layer by a plasma etch, even though the oxide layer may subsequently be removed.

In prior art methods which have attempted to achieve similar results, a problem known as silicon pitting has arisen. Silicon pitting results from attempting to etch a silicon nitride layer selectively to a thin silicon dioxide layer. Prior art chemistries have the ability to etch silicon nitride selectively to silicon dioxide. An example is the use of SF_6. But many of these chemistries are not selective to silicon, such that if the underlying silicon dioxide layer may be damaged or may include defects, the etch used to etch the silicon nitride selectively to the silicon dioxide will end up etching any underlying silicon or polysilicon members. The present invention overcomes the problem of silicon and polysilicon pitting because even if gate oxide layer 16 or oxide layer 19 is damaged or includes defects, the etch used to etch silicon nitride layer 20 is selective to both silicon dioxide and silicon such that etching silicon nitride layer 20 will not etch any portion of silicon substrate 12 or polysilicon gate electrode 18.

After silicon nitride layer 20 is etched in accordance with the present invention, portions of gate oxide layer 16 and oxide layer 19 which are not protected by either sidewall spacers 24 or remaining portions of silicon nitride layer 20 are then removed with a conventional wet etch to expose portions of doped regions 14 and gate electrode 18, as illustrated in FIG. 3. The exposed portions of doped regions 14, and any exposed polysilicon, undergo a conventional silicidation process. A typical silicidation process involves the deposition of titanium or other refractory metal across the entire device, and thermally reacting the metal with adjacent silicon members to form a refractory metal silicide. An etch is then used to remove unreacted portions of the titanium layer, without removing the reacted titanium silicide. FIG. 3 illustrates silicide regions 26 formed within both doped regions 14 and polysilicon gate electrode 18 in accordance with this embodiment of the present invention.

Another embodiment of the present invention involves the use of ONO (oxide-nitride-oxide) dielectric stacks in a semiconductor device. ONO stacks are sometimes used as gate dielectrics between a floating gate and a control gate of a nonvolatile memory device. An example of this application is illustrated in FIGs. 4-6, which illustrate in cross-section a portion of a semiconductor device 40. Device 40 includes a semiconductor substrate (for example a silicon wafer) having a logic portion 44 and an memory portion 46. The logic portion and memory portion are separated from one another by an isolation region 48, which may be conventional field oxide isolation or trench oxide isolation. As illustrated in FIG. 4, a thin gate oxide layer 50 (about 85Å) is grown over both the memory and logic portions of the substrate. Then, a polysilicon floating gate electrode is formed over the gate oxide layer within memory portion 46. Next, an ONO dielectric stack having a bottom silicon dioxide layer 54, a silicon nitride layer 56, and a top silicon dioxide layer 58 is formed. Bottom silicon dioxide layer 54 is thermally grown by oxidation of silicon and/or polysilicon to a thickness of about 220Å over polysilicon floating gate electrode 52. Due to the presence of gate oxide layer 50 elsewhere in device 40, additional oxidation of these areas will be much less; therefore, bottom oxide layer 54 is only illustrated over the gate electrode. Silicon nitride layer 56 is then deposited using conventional CVD to a thickness of about 150Å across the entire device, as illustrated in FIG. 4. Top silicon dioxide layer 58 is formed by oxidizing the silicon nitride layer to produce a very thin oxide layer of about 30Å.

ONO dielectric stacks, such as that described above, are often used to separate floating gates from control gates in non-volatile memory devices due to a favorable ability of such a dielectric stack to retain charge. However, the stack is not used in logic portions of devices, and therefore is usually removed. To remove the ONO from logic portion 44, a resist mask 60, for instance a photoresist mask, is formed over the memory portion of device 40, and unmasked portions of the ONO (or ON) stack in the logic portion are removed by etching. A problem in removing the ONO (or ON) is the possibility of damaging the underlying substrate. For instance, in reference to FIG. 4, in removing silicon nitride layer 56 over logic portion 44, one could use a dry etch which is selective to silicon dioxide to stop on gate oxide layer 50. However, as discussed above, known dry etches which are selective to silicon dioxide are not selective to silicon, such that damage or defects in gate oxide layer 50 could lead to pitting of the underlying substrate. Such damage to the substrate is undesirable since it adversely affects the integrity of subsequently grown oxide layers. One could instead use a dry etch selective only to silicon so that silicon nitride layer 56 and gate oxide layer 50 are simultaneously removed over logic portion 44; however this too will lead to some degree of damage to the substrate despite the selectivity to silicon since the etch is a dry etch. A known method to overcome this problem is to form a thicker sacrificial oxide layer (e.g. 400Å) in the logic portion of the device than in the memory device so that in removing the ONO (or ON) in the logic areas using a plasma etch selective to silicon, there is a much reduced chance of punching through the thicker sacrificial oxide layer and damaging the silicon. Instead, the plasma etch is terminated about halfway through the sacrificial oxide layer, and a wet etch is used to etch the remaining half of the sacrificial oxide layer without damaging the silicon. A true gate oxide (as opposed to the thick sacrificial oxide) is then grown over the logic portion. As is evident, such a solution to the problem involves the additional steps of having to grow two different initial oxide layers of different thicknesses in the logic and memory portions of the device.

With the present invention, the additional steps discussed above are not necessary. As illustrated in FIG. 4, a thin gate oxide layer 50 of uniform thickness can be formed over both logic and memory portions of the device. In accordance with the present invention, top oxide layer 58 and silicon nitride layer 56 are removed from unmasked portions of the device 40 over logic portion 44 using the inventive etch method described previously. Although the etch is selective to oxide, top oxide layer 58 is thin enough (about 30Å) so that the etch will remove the layer. However, the etch is selective enough so that silicon nitride layer 56 can be removed selectively to gate oxide layer 50, as illustrated in FIG. 5. Furthermore, since the etch is also selective to silicon, there is no threat of damaging underlying substrate 42 in logic portion 44 even though gate oxide layer 50 may be damaged or have defects therein.

FIG. 6 illustrates how processing of device 40 may proceed after the ONO (or ON) stack is removed from the logic portion of the device. A thicker true gate oxide layer is needed in the logic portion of the device than in the memory portion of the device; therefore, a thermal oxidation step is used to grow a gate oxide layer 62 to about 350Å. This is preferably accomplished by first stripping gate oxide layer 50 from above logic portion 44 using a conventional wet etch, and growing a new gate oxide layer 62. A second polysilicon layer is then deposited and patterned to form a gate electrode 64 within logic portion 44 and a control gate electrode 66 overlying floating gate electrode 52 within memory portion 46. The ONO dielectric stack separates floating gate electrode 52 from control gate electrode for enhanced charge storage capability.

Another application in which the present invention is useful is in the formation of local interconnects in semiconductor devices. FIGs. 7-9 illustrate in cross-section a portion of a semiconductor device 70 in which a local interconnect is formed in accordance with the present invention. As illustrated in FIG. 7, device 70 includes a semiconductor substrate 72 having an active region 74 and an isolation region 76. Isolation region 76 is preferably a trench isolation region formed of silicon dioxide in accordance with conventional trench isolation methods, although it may instead be formed as a conventional field oxide. Active region 74 includes an N-well 78 having a P+ doped region 80 formed therein. Alternatively, an N+ doped region may be formed in a P-well in active region 74. Doped region 80 may also include a silicide region 82, for example, a titanium silicide layer, over the doped region.

Formed over isolation region 76 is a polysilicon line 84. Elsewhere in device 70, polysilicon line is likely to be a gate electrode of a transistor; however, it is often necessary to connect such an electrode to other portions of the device, in which case the polysilicon line may be routed across isolation regions. Often, it is desirable to electrically connect the routed polysilicon line to a portion of the active region. One method of achieving this connection is through use of a local interconnect. A known method for forming a local interconnect in this situation involves depositing a dielectric layer, such as PSG (phospho-silicate glass) or BPSG (boron-doped phospho-silicate glass), over the device and etching a hole in the dielectric layer which exposes both the polysilicon line and portions of the active region to be connected. A problem in accomplishing this etch is that it is difficult to etch PSG or BPSG selectively to underlying isolation region 76 since both may be comprised of silicon dioxide. As a result, in removing the dielectric layer, it is likely that isolation region 76 would be overetched or recessed, thereby causing leakage problems in any devices formed within the active region.

The present invention overcomes such leakage problems by employing an etch which is selective to both silicon dioxide and silicon in conjunction with using a silicon nitride etch mask. As illustrated in FIG. 7, and in accordance with the present invention, polysilicon line 84 is routed over isolation region 76. Adjacent sidewalls of polysilicon line 84 are optional sidewall spacers 86. The polysilicon line may optionally include a silicide region 82 as well. A layer of silicon nitride is then deposited over device 70, including over active region 74, isolation region 76, and polysilicon line 84. In a preferred embodiment of the present invention, silicon nitride layer 88 is deposited using a plasma-enhanced chemical vapor deposition (PECVD) process such as those known in the art. Next a dielectric layer 90 is deposited over silicon nitride layer 88. Dielectric layer 90 may be BPSG, PSG, TEOS (tetra-ethyl-ortho-silicate), a SOG (spin-on-glass), or a similar dielectric material. A resist mask 92, for example a photoresist mask, is formed over dielectric layer 90 such that an opening 94 in the resist mask defines the appropriate area where a local interconnect is to be formed. Once a patterned resist mask is in place, dielectric layer 90 is etched selectively to silicon nitride layer 88 within opening 94. This may be accomplished using any of several known methods in the industry to etch silicon dioxide or similar material selectively to silicon nitride, for example by dry etching using CHF_3 and argon. As a result of this etch, dielectric layer 90 within opening 94 is removed, however, silicon nitride layer 88 remains intact within opening 94. At this point, exposed portions of silicon nitride layer 88 within opening 94 are etched by the inventive etch process described above to expose doped region 80 and polysilicon line 84 (or silicide regions 82 if present), as illustrated in FIG. 8. The silicon nitride layer is etched in accordance with the present invention in an anisotropic manner and such that the silicon nitride is etched selectively to both silicon dioxide (isolation region 76) and silicon (doped region 80, polysilicon line 84, silicide regions 82). Because the etch is anisotropic, residual sidewall spacers 96 of silicon nitride may be formed adjacent to sides of polysilicon line 84 or along sidewall spacers 86 if present. In prior art processes used to form local interconnect structures similar to that illustrated in FIG. 7, etches used to remove a silicon nitride layer often resulted in an overetch in either the silicon dioxide material used to form isolation

region 76 or in silicon within the active region 74. However, with the present invention, the silicon nitride layer 88 can be removed selectively to both these regions. thereby minimizing the possibility of junction leakage. Once the active region and polysilicon member overlying the isolation region are exposed, as illustrated in FIG. 8, a glue layer 97 if formed along the sidewalls and bottom of opening 94. Glue layer 97, illustrated in FIG. 9, is used to promote adhesion between dielectric layer 90 and a subsequently deposited conductive material. The conductive material is deposited to fill opening 94, thereby electrically connecting polysilicon line 84 and doped region 80. As an example, a layer of tungsten may be deposited across device 70 and subsequently etched or polished back to form a local interconnect 98, as illustrated in FIG. 9. In the case of using tungsten, a suitable glue layer 97 includes a combination of titanium and titanium nitride to promote adhesion of the tungsten to the adjacent dielectric layer. Rather than using a conductive material to electrically connect a polysilicon line to the active region, the conductive material could instead be used to simply make a contact to the active region. For example, opening 94 may be patterned only over active region 74 and a portion of isolation region 76, without encompassing another conductive member, such as polysilicon line 84.

The foregoing description and illustrations contained herein demonstrate many of the advantages associated with the present invention. A method for etching silicon nitride using CF_4, O_2, and an inert gas, such as argon, etches silicon nitride anisotropically, while at the same time etches selectively to underlying silicon dioxide and silicon materials. As previously described, such an etching method is useful in a variety of applications in manufacturing semiconductor devices, including forming silicon nitride sidewall spacers overlying a thin oxide layer, removing an ONO dielectric stack over a thin oxide to avoid damage to the underlying substrate, and forming a local interconnect or a contact between an active region and a conductive member overlying a dielectric isolation region. While only these three specific applications have been illustrated and described herein, it is anticipated that other applications of the present invention will become apparent given the widespread use of silicon nitride in semiconductor devices. In addition to the many applications of using the present invention, a further advantage is that the present invention is easily implementable in a manufacturing environment since suitable plasma etch systems and gases used are readily available. Moreover, incorporation of a method in accordance with the present invention into a manufacturing process has an advantage of eliminating many existing process steps which are otherwise required to overcome problems that prior art methods have relating to poor selectivity and the isotropic nature of these methods when etching silicon nitride.

Thus, it is apparent that there has been provided in accordance with the invention a method for etching silicon nitride that fully meets the need and advantages set forth above. Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. For example, the present invention is suitable for etching any type of silicon nitride material, including silicon nitride layers which are deposited using standard chemical vapor deposition (CVD) or plasma-enhanced chemical vapor deposition (PECVD). It is also noted that the present invention can be used to etch silicon nitride selectively to a variety of materials comprising silicon, including but not limited to, single crystal silicon, polysilicon, amorphous silicon, silicides, and dielectric materials comprising silicon dioxide which may be formed or deposited in a variety of ways. Also, it is noted that while argon is a preferred inert gas for use in accordance with the present invention that other inert gases such as nitrogen, helium, xenon, or the like may be suitable alternative. Therefore it is intended that this invention encompass all such variations and modifications as fall with the scope of the appended claims.

Claims

1. A method of etching silicon nitride, comprising the steps of:

   providing a material selected from a group of materials consisting of single crystal silicon, polysilicon, amorphous silicon, silicides, and silicon dioxide;

   forming a layer of silicon nitride such that a portion of the layer of silicon nitride is on the material; and

   anisotropically etching the portion of the layer of silicon nitride selectively to the material;

   wherein the step of anisotropically etching is performed using a plasma etch system and using a CF_4 gas, an O_2 gas, and an inert gas.

2. A method of etching silicon nitride in a semiconductor device, comprising the steps of:

   providing a semiconductor substrate comprised of silicon;

   forming a polysilicon member over the semiconductor substrate, the polysilicon member having a sidewall;

   forming a layer of silicon nitride over the semiconductor substrate and the polysilicon member such that the layer of silicon nitride is present along the sidewall of the polysilicon member; and

   anisotropically etching the layer of silicon nitride without etching the semiconductor substrate to form a sidewall spacer adjacent the sidewall of the polysilicon member;

   wherein the step of anisotropically etching is performed using a plasma etch system and a CF_4 gas, an O_2 gas, and an inert gas.

3. The method of claim 2 further comprising the step of forming an oxide layer over the semiconductor substrate, and wherein the step of forming a polysilicon member comprises forming a polysilicon member on the oxide layer, wherein the step of forming a layer of silicon nitride comprises forming a layer of silicon nitride on the oxide layer, and wherein the step of anisotropically etching comprises anisotropically etching the layer of silicon nitride selectively to the oxide layer.

4. A method of etching silicon nitride in a semiconductor device, comprising the steps of:

    providing a semiconductor substrate;

    forming a floating gate electrode over the semiconductor substrate;

    forming a dielectric stack of an oxide layer and a silicon nitride layer over the floating gate electrode and over the semiconductor substrate;

    masking a portion of the dielectric stack over the floating gate electrode with a resist mask to create a masked portion and an unmasked portion of the dielectric stack; and

    removing the dielectric stack in the unmasked portion of the dielectric stack;

    wherein the step of removing comprises anisotropically etching the silicon nitride layer without etching the semiconductor substrate by plasma etching using a CF_4 gas, an O_2 gas, and an inert gas.

5. The method of claim 4 further comprising the step of forming a gate oxide layer over the semiconductor substrate, and wherein the step of forming a dielectric stack comprises forming the silicon nitride layer of the dielectric stack over the gate oxide layer, and wherein the step of removing the dielectric stack comprises anisotropically etching the silicon nitride layer selectively to the gate oxide layer.

6. A method of etching silicon nitride in a semiconductor device, comprising the steps of:

    providing a semiconductor substrate having an active region and an isolation region abutting the active region;

    forming a layer of silicon nitride over the active region and the isolation region;

    forming a dielectric layer over the layer of silicon nitride, the active region, and the isolation region;

    patterning an opening in the dielectric layer, the opening overlying a portion of the active region and a portion of the isolation region and exposing a portion of the layer of silicon nitride; and

    anisotropically etching the portion of the layer of silicon nitride exposed by the opening selectively to the portion of the active region and the portion of the isolation region;

    wherein the step of anisotropically etching comprises plasma etching the layer of silicon nitride using a CF_4 gas, an O_2 gas, and an inert gas.

7. The method of claims 1, 2, 4, or 6 wherein the step of anisotropically etching is performed using argon as the inert gas.

8. The method of claim 1, 2, 4, or 6 wherein the step of anisotropically etching comprises using a plasma etch system having an etch chamber, and wherein a plasma is generated in the etch chamber.

9. The method of claims 1, 2, 4, or 6 wherein the step of anisotropically etching comprises etching in a magnetically enhanced plasma etch system.

10. The method of claims 1, 2, 4, or 6 wherein the step of anisotropically etching is performed with a resist mask in place.

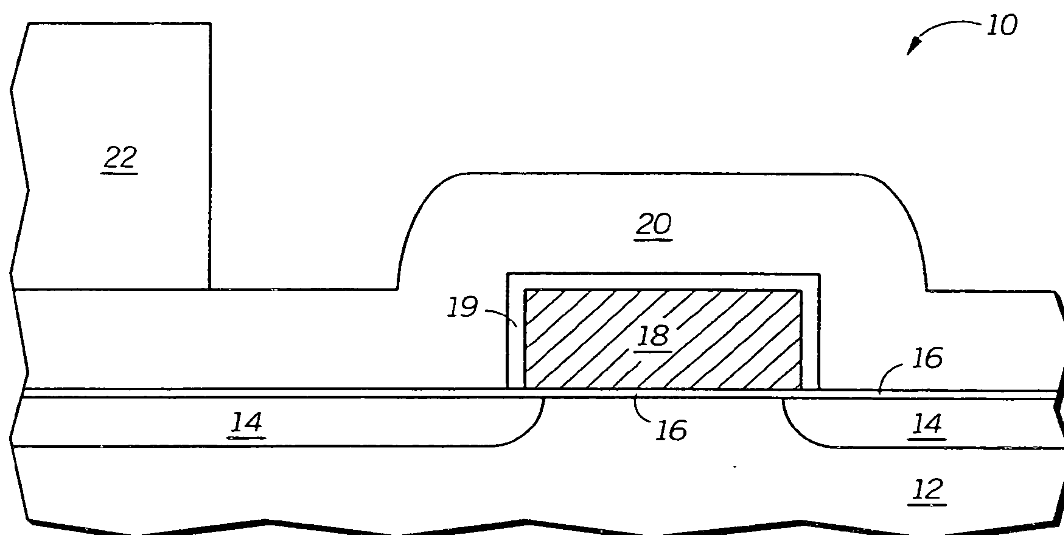


FIG.1

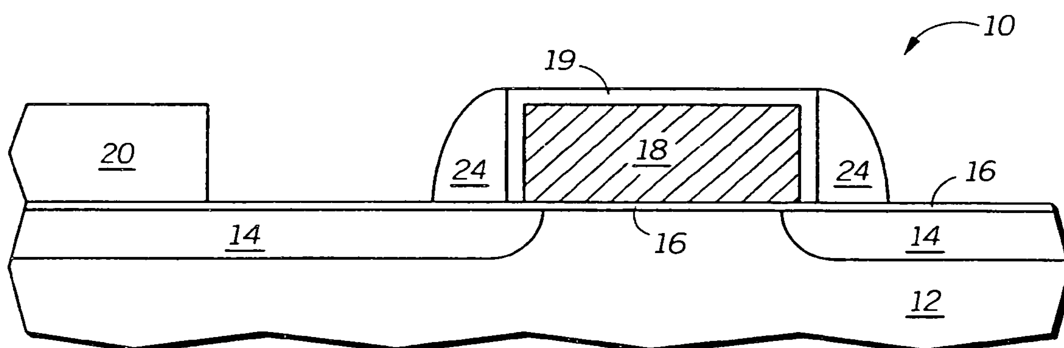


FIG.2

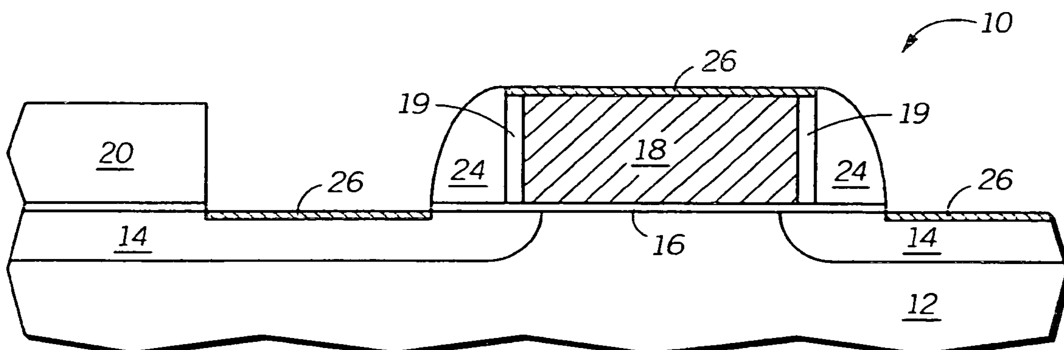


FIG.3

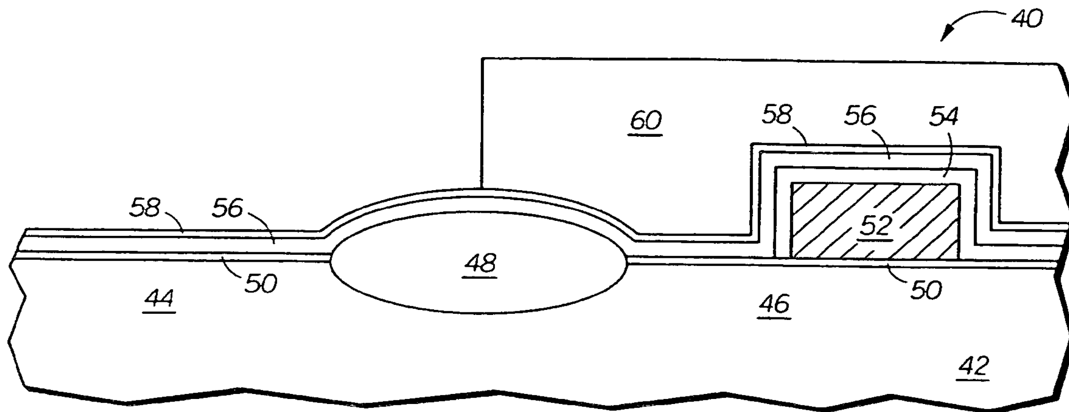


FIG. 4

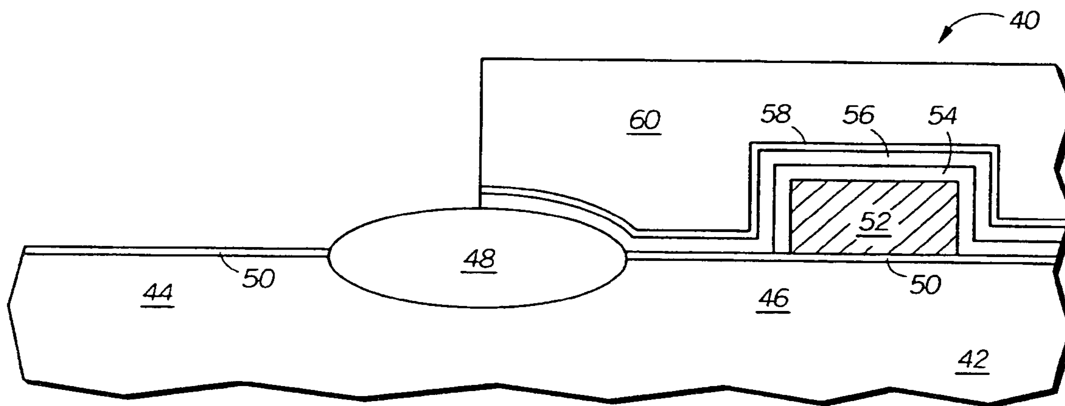


FIG. 5

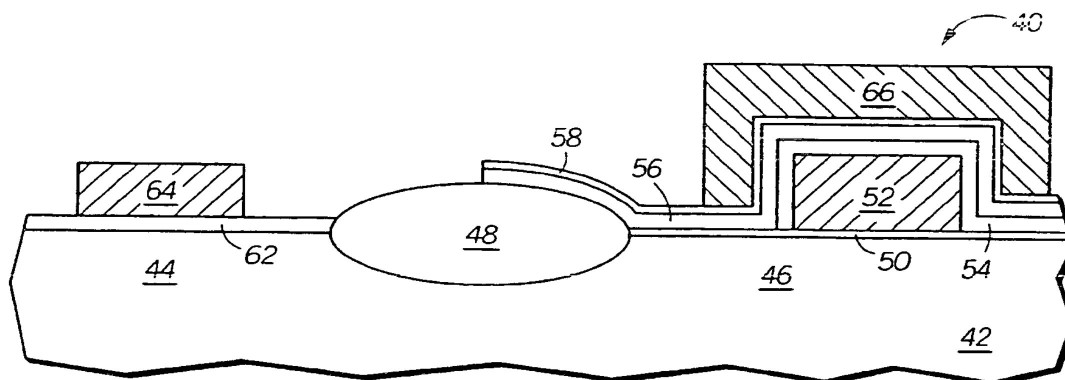


FIG. 6

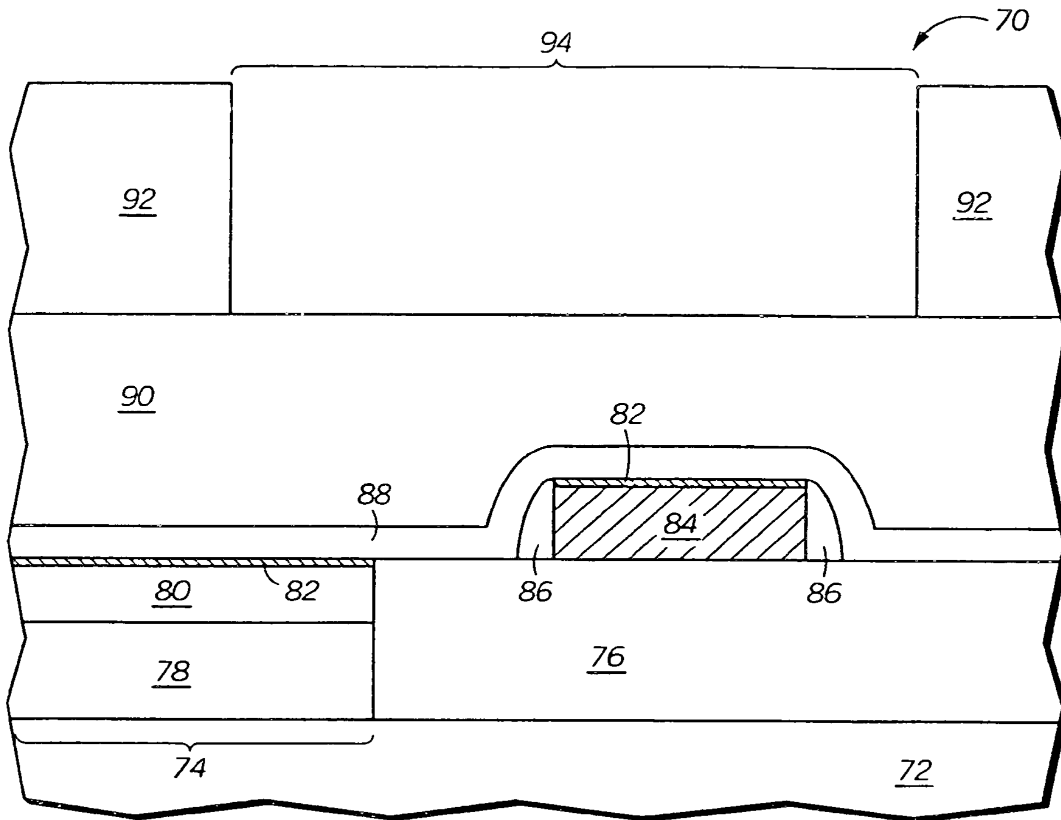


FIG. 7

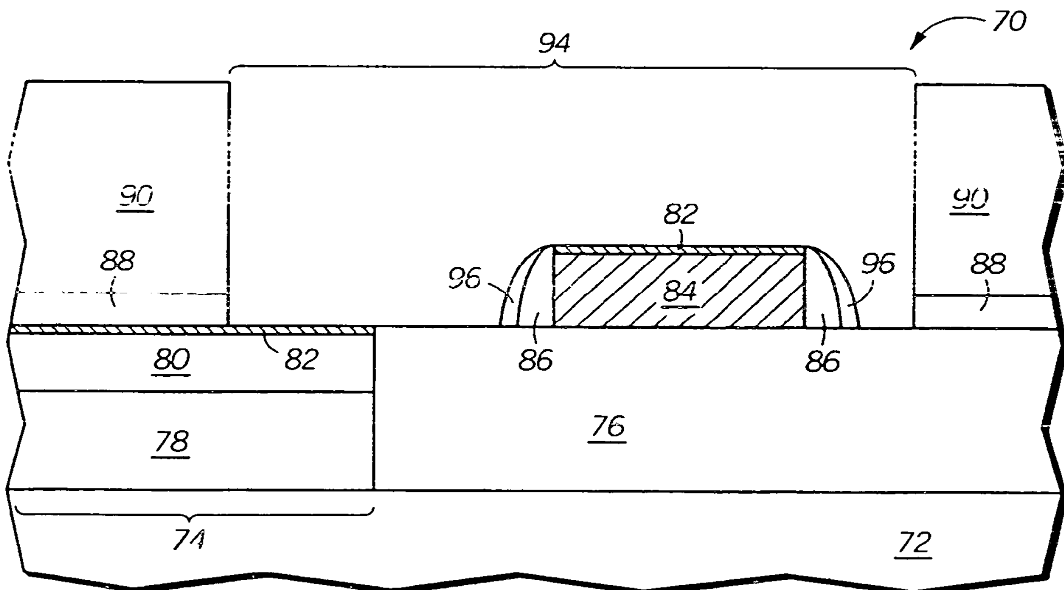


FIG. 8

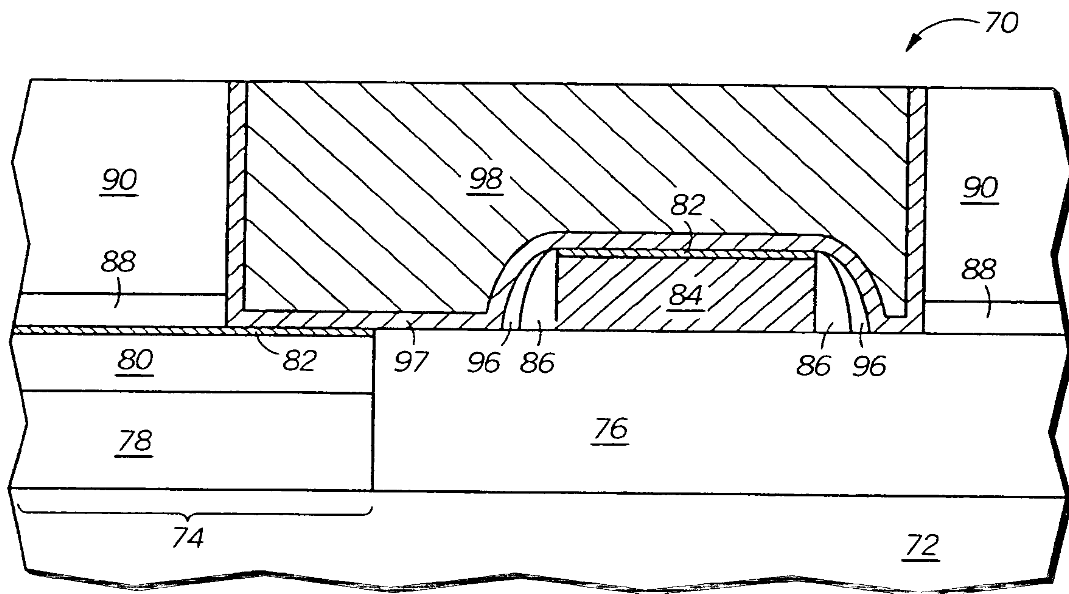
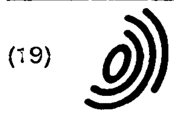


FIG.9

(19) 
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(71) Applicant: MOTOROLA, INC.
Schaumburg, IL 60196 (US)

(72) Inventors:
- **Lin, Jung-Hui**
  Austin, Texas 78750 (US)
- **Koh, Ai**
  Austin, Texas 78729 (US)

(74) Representative: **Hirsz, Christopher Stanislaw et al**
Motorola
European Intellectual Property Operations
Midpoint
Alencon Link
Basingstoke, Hampshire RG21 1PL (GB)

(54) **Method for etching silicon nitride**

(57) In accordance with the present invention, a silicon nitride layer (20) in a semiconductor device (10) is anisotropically etched selectively to both silicon dioxide, for example gate oxide layer (16), and to silicon, for example, silicon substrate (12) and polysilicon gate electrode (18). The silicon nitride layer is etched in a plasma etch system using CF_4, O_2, and argon gases. In other applications of the present invention, the etch method is used to remove an ONO dielectric stack and to remove a silicon nitride etch stop layer selectively to both active regions and isolation regions to form contacts or local interconnects across these regions.

EP 0 706 206 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 95 11 4230

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	EP-A-0 436 387 (HEWLETT-PACKARD) 10 July 1991 * table 1 *	1,7,8,10 2,3,9	H01L21/311 H01L21/28 H01L21/768
X Y	US-A-4 028 155 (LFE CORP) 7 June 1977 * figure 3; table 1 *	1,7,8,10 4-6	
Y	EP-A-0 424 299 (IBM) 24 April 1991 * page 5, line 36 - line 53 *	9	
A	EXTENDED ABSTRACTS, vol. 93, no. 1, May 1993, PRINCETON, NEW JERSEY US, page 415 XP000431754 LOEWENSTEIN ET AL: "Minimizing pad oxide damage and field oxide loss in a remote plasma silicon nitride etch process using an in situ spectral ellipsometer" * left-hand column, paragraph 1-3 *	1,7-10	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
Y	US-A-5 242 532 (VLSI TECHNOLOGY) 7 September 1993 * column 1, line 23 - line 41; figure 3 *	2,3	H01L
A	EXTENDED ABSTRACTS, vol. 93, no. 1, May 1993, PRINCETON, NEW JERSEY US, page 366 XP000430477 POPE ET AL: "A highly selective nitride to oxide etch to reduce single bit failures on memory products" * paragraph 1 *	1,2	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 June 1996	Gori, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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D : document cited in the application
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& : member of the same patent family, corresponding document

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EUROPEAN SEARCH REPORT

Application Number
EP 95 11 4230

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EXTENDED ABSTRACTS, vol. 90, no. 1, May 1990, PRINCETON, NEW JERSEY US, pages 182-183, XP000140771 YANG ET AL: "Selective etching of silicon nitride in a magnetically enhanced plasma reactor" * left-hand column, paragraph 1 *	9	
Y	EP-A-0 430 829 (SGS-THOMSON MICROELECTRONICS) 5 June 1991 * figures *	4,5	
Y	JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART B, vol. 12, no. 1, February 1994, NEW YORK US, pages 427-432, XP000429051 GIVENS ET AL: "Selective dry etching in a high density plasma for 0.5 micrometer complementary metal-oxide-semiconductor technology" * figure 2; table 2 *	6	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	EP-A-0 337 109 (IBM) 18 October 1989 * figures *	6	
A	EP-A-0 395 084 (TOSHIBA) 31 October 1990 * figures *	4	
A	PATENT ABSTRACTS OF JAPAN vol. 17, no. 556 (E-1444), 6 October 1993 & JP-A-05 160077 (SHARP), 25 June 1993, * abstract *	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 June 1996	Gori, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- [ ] All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- [ ] Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.

  namely claims:
- [ ] No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions,
namely:

See Sheet B.

- [x] All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- [ ] Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.

  namely claims:
- [ ] None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

  namely claims:

LACK OF UNITY OF INVENTION

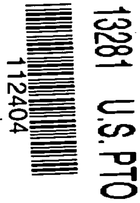
The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1st subject : claims 1, 7-10, searched :
- a method for selectively etching silicon nitride, anticipated.

2nd subject : claims 2, 3, searched :
- application of the method above (1st subject, anticipated) in the formation of nitride sidewall spacers on polysilicon gates.

3rd subject : claims 4,5, not searched :
- application of the method above (1st subject, anticipated) in the formation of a non volatile memory device.

4th subject : claim 6, not searched :
- application of the above method (1st subject, anticipated) in the formation of interconnections structures.



REQUEST FORM FOR APPLICATION UNDER 37 CFR 1.53(b)

DOCKET NUMBER: 71971-012
Prior Application:
Art Unit: 2822
Examiner: Roy Karl Potter

NEW APPLICATIONS
FEE
Mail Stop NEW APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a Request for filing a Divisional application under 37 CFR 1.53(b) of pending prior application Serial No. 10/454,682, filed on June 5, 2003, entitled **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**, by the following named inventors: Mizuki SEGAWA, Isao MIYANAGA, Toshiki YABU, Takashi NAKABAYASHI, Takashi UEHARA, Kyoji YAMASHITA, Takaaki UKEDA, Masatoshi ARAI, Takayuki YAMADA and Michikazu MATSUMOTO.

1. ☒ I hereby state that the enclosed application contains no new matter.

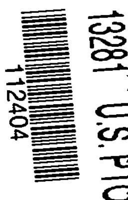
2. Oath or Declaration
   a. ☐ Newly executed (original or copy)
   b. ☒ Copy from a prior application (37 CFR 1.63(d))
      i. ☐ Deletion of inventor(s)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

3. ☒ Incorporation By Reference (useable if Box 2b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 2b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

4. ☒ Preliminary Amendment is enclosed.

5. ☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.

6. ☒ Cancel claims 1-38.



DOCKET NUMBER: 71971-012

7. The filing fee is calculated on the basis of the claims existing in the prior application as amended at 4 and 6 above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	14	-20	0	$18.00 =	$0.00
Independent Claims	1	-3	0	$88.00 =	$0.00
				Basic Application Fee	$790.00
				If multiple dependent claims are presented, add $0.00	$0.00
				Total Application Fee	$790.00
				Subtract ½ if small entity	$0.00
				TOTAL APPLICATION FEE DUE	$790.00
				AMOUNT TO BE CHARGED TO DEPOSIT ACCOUNT NO. 500417	$790.00

7a. ☐ Enclosed is a Verified Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.

7b. ☐ A verified Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 was filed in prior application and such status is still proper and desired.

8a. ☒ **PLEASE CHARGE DEPOSIT ACCOUNT 500417 in the amount of $790.00**

8b. ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees to maintain the pendency of the parent Application No. 10/454,682 or credit any overpayment to Deposit Account No. 500417.

9. ☒ Amend the specification by inserting before the first line the sentence:

--This application is a divisional of Application No. 10/454,682 filed June 5, 2003, which is a divisional of Application No. 09/902,157 filed July 11, 2001, which is a divisional of Application No. 08/685,726 filed on July 24, 1996, which is now U.S. Patent No. 6,281,562.--

10. ☒ Priority of Application No. JP 7-192181 filed on July 27, 1995, in Japan and Application No. 7-330112 filed on December 19, 1995, in Japan is claimed under 35 USC 119. The certified priority documents were filed in Application No. 08/685,726 on July 24, 1996.

11. ☒ The prior application is assigned of record to

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
Kadoma-shi, Osaka, Japan

12. ☒ The power of attorney in the prior application is to:

McDermott, Will & Emery

13. ☒ Also enclosed:

- Supplemental Power of Attorney

DOCKET NUMBER: 71971-012

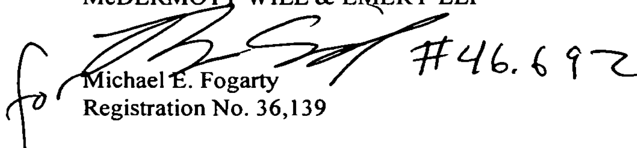
14. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until .

Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, D. C. 20005-3096

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



for Michael E. Fogarty #46,692
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ete
Facsimile: 202.756.8087
Date: November 24, 2004

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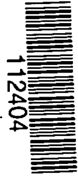

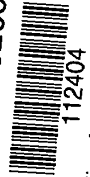

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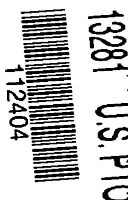

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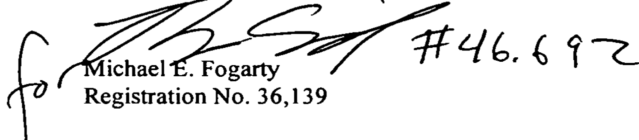

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SEMICONDUCTOR DEVICE AND

METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device including transistors and connection between the transistors for constituting an LSI with high integration and a decreased area.

With the recent development of a semiconductor device with high integration and high performance, there are increasing demands for more refinement of the semiconductor device. The improvement of the conventional techniques cannot follow these demands, and novel techniques are unavoidably introduced in some technical fields. For example, as a method of forming an isolation, the LOCOS isolation method is conventionally adopted in view of its simpleness and low cost. Recently, however, it is considered that a trench buried type isolation (hereinafter referred to as the trench isolation) is more advantageous for manufacturing a refined semiconductor device.

Specifically, in the LOCOS isolation method, since selective oxidation is conducted, the so-called bird's beak occurs in the boundary with a mask for preventing the oxidation. As a result, the dimension of a transistor is changed because an insulating film of the isolation invades a transistor region against the actually designed mask dimension. This dimensional change is unallowable in the refinement of a

semiconductor device after the 0.5 μm generation. Therefore, even in the mass-production techniques, the isolation forming method has started to be changed to the trench isolation method in which the dimensional change is very small. For example,
5 IBM corporation has introduced the trench isolation structure as a 0.5 μm CMOS process for the mass-production of an MPU (IBM Journal of Research and Development, VOL. 39, No. 1/2, 1995, pp. 33 - 42).

Furthermore, in a semiconductor device mounting elements
10 such as a MOSFET in an active area surrounded with an isolation, an insulating film is deposited on the active area, the isolation and a gate electrode, and a contact hole is formed by partly exposing the insulating film for connection between the active area and an interconnection member on a
15 layer above the insulating film. This structure is known as a very common structure for the semiconductor device.

Figure 17 is a sectional view for showing the structure of a conventional semiconductor device. In Figure 17, a reference numeral 1 denotes a silicon substrate, a reference numeral 2b
20 denotes an isolation with a trench isolation structure which is made of a silicon oxide film and whose top surface is flattened so as to be at the same level as the top surface of the silicon substrate 1, a reference numeral 3 denotes a gate oxide film made of a silicon oxide film, a reference numeral 4a denotes a
25 polysilicon electrode working as a gate electrode, a reference numeral 4b denotes a polysilicon interconnection formed

simultaneously with the polysilicon electrode 4a, a reference numeral 6 denotes a low-concentration source/drain region formed by doping the silicon substrate with an n-type impurity at a low concentration, a reference numeral 7a denotes an
5 electrode sidewall, a reference numeral 7b denotes an interconnection sidewall, a reference numeral 8 denotes a high-concentration source/drain region formed by doping the silicon substrate with an n-type impurity at a high concentration, a reference numeral 12 denotes an insulating film made of a
10 silicon oxide film, and a reference numeral 13 denotes a local interconnection made of a polysilicon film formed on the insulating film 12.

The local interconnection 13 is also filled within a connection hole 14 formed in a part of the insulating film 12,
15 so as to be contacted with the source/drain region in the active area through the connection hole 14. In this case, the connection hole 14 is formed apart from the isolation 2b by a predetermined distance. In other words, in the conventional layout rule for such a semiconductor device, there is a rule
20 that the edge of a connection hole is previously located away from the boundary between the active area and the isolation region so as to prevent a part of the connection hole 14 from stretching over the isolation 2b even when a mask alignment shift is caused in photolithography (this distance between the
25 connection hole and the isolation is designated as an alignment margin).

However, in the structure of the semiconductor device as shown in Figure 17, there arise problems in the attempts to further improve the integration for the following reason:

5 A distance La between the polysilicon electrode 4a and the isolation 2b is estimated as an index of the integration. In order to prevent the connection hole 14 from interfering the isolation 2b as described above, the distance La is required to be 1.2 μm, namely, the sum of the diameter of the connection hole 14, that is, 0.5 μm, the width of the electrode sidewall
10 7a, that is, 0.1 μm, the alignment margin from the polysilicon electrode 4a, that is, 0.3 μm, and the alignment margin from the isolation 2b, that is, 0.3 μm. A connection hole has attained a more and more refined diameter with the development of processing techniques, and also a gate length has been
15 decreased as small as 0.3 μm or less. Still, the alignment margin in consideration of the mask alignment shift in the photolithography is required to be approximately 0.3 μm. Accordingly, as the gate length and the connection hole diameter are more refined, the proportion of the alignment
20 margin is increased. This alignment margin has become an obstacle to the high integration.

Therefore, attempts have been made to form the connection hole 14 without considering the alignment margin in view of the alignment shift in the photolithography. Manufacturing
25 procedures adopted in such a case will now be described by exemplifying an n-channel MOSFET referring to Figures 18(a)

through 18(c).

First, as is shown in Figure 18(a), after forming an isolation 2b having the trench structure in a silicon substrate 1 doped with a p-type impurity (or p-type well), etch back or
5 the like is conducted for flattening so as to place the surfaces of the isolation 2b and the silicon substrate 1 at the same level. In an active area surrounded with the isolation 2b, a gate oxide film 3, a polysilicon electrode 4a serving as a gate electrode, an electrode sidewall 7a, a low-concentration
10 source/drain region 6 and a high-concentration source/drain region 8 are formed. On the isolation 2b are disposed a polysilicon interconnection 4b formed simultaneously with the polysilicon electrode 4a and an interconnection sidewall 7b. At this point, the top surface of the high-concentration
15 source/drain region 8 in the active area is placed at the same level as the top surface of the isolation 2b. Then, an insulating film 12 of a silicon oxide film is formed on the entire top surface of the substrate.

Next, as is shown in Figure 18(b), a resist film 25a used
20 as a mask for forming a connection hole is formed on the insulating film 12, and the connection hole 14 is formed by, for example, dry etching.

Then, as is shown in Figure 18(c), the resist film 25a is removed, and a polysilicon film is deposited on the insulating
25 film 12 and within the connection hole 14. The polysilicon film is then made into a desired pattern, thereby forming a

local interconnection 13.

At this point, in the case where the alignment margin in view of the mask alignment shift in the formation of the connection hole 14 is not considered in estimating the distance La between the polysilicon electrode 4a and the isolation 2b, a part of the isolation 2b is included in the connection hole 14 when the exposing area of the resist film 25a is shifted toward the isolation 2b due to the mask alignment shift in the photolithography. Through over-etch in conducting the dry etching of the insulating film 12, although the high-concentration source/drain region 8 made of the silicon substrate is not largely etched because of its small etching rate, the part of the isolation 2b included in the connection hole 14 is selectively removed, resulting in forming a recess 40 in part of the connection hole 14. When the recess 40 in the connection hole 14 has a depth exceeding a given proportion to the depth of the high-concentration source/drain region 8, junction voltage resistance can be decreased and a junction leakage current can be increased because the concentration of the impurity in the high-concentration source/drain region 8 is low at that depth.

In order to prevent these phenomena, it is necessary to provide a predetermined alignment margin as is shown in the structure of Figure 17 so as to prevent the connection hole 14 from interfering the isolation 2b even when the alignment shift is caused in the lithography. In this manner, in the

conventional layout rule for a semiconductor device, an alignment margin in view of the mask alignment shift in the photolithography is unavoidably provided.

Furthermore, a distance between the polysilicon electrode 4a and the connection hole 14 is also required to be provided with an alignment margin. Otherwise, the connection hole 14 can interfere the polysilicon electrode 4a due to the fluctuation caused in the manufacturing procedures, resulting in causing electric short-circuit between an upper layer interconnection buried in the connection hole and the gate electrode.

As described above, it is necessary to provide the connection hole 14 with margins for preventing the interference with other elements around the connection hole, which has become a large obstacle to the high integration of an LSI.

Also in the case where a semiconductor device having the so-called salicide structure is manufactured, the following problems are caused due to a recess formed in the isolation:

Figure 19 is a sectional view for showing an example of a semiconductor device including the conventional trench isolation and a MOSFET having the salicide structure. As is shown in Figure 19, a trench isolation 105a is formed in a silicon substrate 101. In an active area surrounded with the isolation 105a, a gate insulating film 103a, a gate electrode 107a, and electrode sidewalls 108a on both side surfaces of the gate electrode 107a are formed. Also in the active area, a

low-concentration source/drain region 106a and a high-concentration source/drain region 106b are formed on both sides of the gate electrode 107a. A channel stop region 115 is formed below the isolation 105a. Furthermore, in areas of the
5 silicon substrate 101 excluding the isolation 105a and the active area, a gate interconnection 107b made of the same polysilicon film as that for the gate electrode 107a is formed with a gate insulating film 103b sandwiched, and the gate interconnection 107b is provided with interconnection sidewalls
10 108b on its both side surfaces. On the gate electrode 107a, the gate interconnection 107b and the high-concentration source/drain region 106b, an upper gate electrode 109a, an upper gate interconnection 109b and a source/drain electrode 109c each made of silicide are respectively formed.
15 Furthermore, this semiconductor device includes an interlayer insulating film 111 made of a silicon oxide film, a metallic interconnection 112 formed on the interlayer insulating film 111, and a contact member 113 (buried conductive layer) filled in a connection hole formed in the interlayer insulating film
20 111 for connecting the metallic interconnection 112 with the source/drain electrode 109c.

Now, the manufacturing procedures for the semiconductor device including the conventional trench isolation and the MOSFET with the salicide structure shown in Figure 19 will be
25 described referring to Figures 20(a) through 20(e).

First, as is shown in Figure 20(a), a silicon oxide film

116 and a silicon nitride film 117 are successively deposited on a silicon substrate 101, and a resist film 120 for exposing an isolation region and masking a transistor region is formed on the silicon nitride film 117. Then, by using the resist film 120 as a mask, etching is conducted, so as to selectively remove the silicon nitride film 116 and the silicon oxide film 117, and further etch the silicon substrate 101, thereby forming a trench 104. Then, impurity ions are injected into the bottom of the trench 104, thereby forming a channel stop region 115.

Then, as is shown in Figure 20(b), a silicon oxide film (not shown) is deposited, and the entire top surface is flattened until the surface of the silicon nitride film 117 is exposed. Through this procedure, a trench isolation 105a made of the silicon oxide film filled in the trench 104 is formed in the isolation region Reiso.

Next, as is shown in Figure 20(c), after the silicon nitride film 117 and the silicon oxide film 116 are removed, a gate oxide film 103 is formed on the silicon substrate 101, and a polysilicon film 107 is deposited thereon. Then, a photoresist film 121 for exposing areas excluding a region for forming a gate is formed on the polysilicon film 107.

Then, as is shown in Figure 20(d), by using the photoresist film 121 as a mask, dry etching is conducted, thereby selectively removing the polysilicon film 107 and the gate oxide film 103. Thus, a gate electrode 107a of the MOSFET

in the transistor region Refet and a gate interconnection 107b stretching over the isolation 105a and the silicon substrate 101 are formed. After removing the photoresist film 121, impurity ions are injected into the silicon substrate 101 by using the gate electrode 107a as a mask, thereby forming a low-concentration source/drain region 106a. Then, a silicon oxide film 108 is deposited on the entire top surface of the substrate.

Next, as is shown in Figure 20(e), the silicon oxide film 108 is anisotropically dry-etched, thereby forming electrode sidewalls 108a and interconnection sidewalls 108b on both side surfaces of the gate electrode 107a and the gate interconnection 107b, respectively. At this point, the gate oxide film 103 below the silicon oxide film 108 is simultaneously removed, and the gate oxide film 103 below the gate electrode 107a alone remains. Then, impurity ions are diagonally injected by using the gate electrode 107a and the electrode sidewalls 108a as masks, thereby forming a high-concentration source/drain region 106b. Then, after a Ti film is deposited on the entire top surface, high temperature annealing is conducted, thereby causing a reaction between the Ti film and the components made of silicon directly in contact with the Ti film. Thus, an upper gate electrode 109a, an upper gate interconnection 109b and a source/drain electrode 109c made of silicide are formed.

The procedures to be conducted thereafter are omitted, but

the semiconductor device including the MOSFET having the structure as shown in Figure 19 can be ultimately manufactured. In Figure 19, the metallic interconnection 112 is formed on the interlayer insulating film 111, and the metallic
5 interconnection 112 is connected with the source/drain electrode 109c through the contact member 113 including a W plug and the like filled in the contact hole.

When the aforementioned trench isolation structure is adopted, the dimensional change of the source/drain region can
10 be suppressed because the bird's beak, that is, the oxide film invasion of an active area, which is caused in the LOCOS method where a thick silicon oxide film is formed by thermal oxidation, can be avoided. Furthermore, in the procedure shown in Figure 20(c), the surfaces of the isolation 105a and the
15 silicon substrate 101 in the transistor region Refet are placed at the same level.

In such a semiconductor device having the trench type isolation, however, there arise the following problems:

When the procedures proceed from the state shown in Figure
20 20(d) to the state shown in Figure 20(e), the silicon oxide film 108 is anisotropically etched so as to form the sidewalls 108a and 108b. At this point, over-etch is required. Through this over-etch, the surface of the isolation 105a is removed by some depth.

25 Figures 21(a) and 21(b) are enlarged sectional views around the boundary between the high-concentration source/drain

region 106b and the isolation 105a after this over-etch.

As is shown in Figure 21(a), between the procedures shown in Figures 20(d) and 20(e), the impurity ions are diagonally injected so as to form the high-concentration source/drain region 106b. Through this ion injection, the high-concentration source/drain region 106b is formed also below the edge of the isolation 105a because the isolation 105a is previously etched by some depth. Accordingly, the high-concentration source/drain region 106b is brought closer to the channel stop region 115, resulting in causing the problems of degradation of the junction voltage resistance and increase of the junction leakage current.

In addition, as is shown in Figure 21(b), in the case where the Ti film or the like is deposited on the high-concentration source/drain region 106b so as to obtain the silicide layer through the reaction with the silicon below, the thus formed silicide layer can invade the interface between the silicon substrate 101 and the isolation 105a with ease. As a result, a short-circuit current can be caused between the source/drain electrode 109c made of silicide and the channel stop region 115.

SUMMARY OF THE INVENTION

The object of the present invention is improving the structure of an isolation, so as to prevent the problems caused because the edge of the isolation is trenched in etching for

the formation of a connection hole or sidewalls.

In order to achieve the object, the invention proposes first and second semiconductor devices and first through third methods of manufacturing a semiconductor device as described below.

The first semiconductor device of this invention in which a semiconductor element is disposed in each of plural active areas in a semiconductor substrate comprises an isolation for surrounding and isolating each active area, the isolation having a top surface at a higher level than a surface of the active area and having a step portion in a boundary with the active area; an insulating film formed so as to stretch over each active area and the isolation; plural holes each formed by removing a portion of the insulating film disposed at least on the active area; plural buried conductive layers filled in the respective holes; and plural interconnection members formed on the insulating film so as to be connected with the respective active areas through the respective buried conductive layers.

Owing to this structure, in the case where a part of or all the holes are formed so as to stretch over the active areas and the isolation due to mask alignment shift in photolithography, a part of the isolation is removed by over-etch for ensuring the formation of the holes. In such a case, even when the top surface of the isolation is trenched to be lower than the surface of the active area, the depth of the holes formed in the isolation is small in the boundary with the

active area because of the level difference between the top surface of the isolation and the surface of the active area. Accordingly, degradation of the junction voltage resistance and increase of the junction leakage current can be suppressed. Therefore, there is no need to provide a portion of the active area where each hole is formed with an alignment margin for avoiding the interference with the isolation caused by the mask alignment shift in the lithography. Thus, the area of the active area can be decreased, resulting in improving the integration of the semiconductor device.

In the first semiconductor device, at least a part of the plural holes can be formed so as to stretch over the active area and the isolation due to fluctuation in manufacturing procedures.

In other words, even when no margin for the mask alignment in the lithography is provided, the problems caused in the formation of the holes can be avoided.

Furthermore, the angle between a side surface of the step portion and the surface of the active area is preferably 70 degrees or more.

As a result, when the hole interferes the isolation, the part of the isolation included in the hole is definitely prevented from being etched through over-etch in the formation of the holes down to a depth where the impurity concentration is low in the active area.

The isolation is preferably a trench isolation made of an

insulating material filled in a trench formed by trenching the semiconductor substrate by a predetermined depth.

This is because no bird's beak is caused in the trench isolation differently from a LOCOS film as described above, and
5 hence, the trench isolation is suitable particularly for the high integration and refinement of the semiconductor device.

In the first semiconductor device, when the semiconductor element is a MISFET including a gate insulating film and a gate electrode formed on the active area; and source/drain regions
10 formed in the active area on both sides of the gate electrode, the following preferred embodiments can be adopted:

The semiconductor device can further comprise a gate interconnection made of the same material as that for the gate electrode and formed on the isolation, each of the holes can be
15 formed on an area including the source/drain region, the isolation and the gate interconnection, and the plural interconnection members can be connected with the gate interconnection on the isolation.

Owing to this configuration, in the case where the
20 interconnection members work as local interconnections for connecting a gate interconnection on the isolation with the active area, there is no need to separately form holes in the insulating film on the gate interconnection and the insulating film on the active area. In addition, there is no need to
25 provide the separate holes with alignment margins from the boundary between the active area and the isolation.

Accordingly, the area of the isolation can also be decreased, resulting in largely improving the integration of the semiconductor device.

The semiconductor device can further comprise electrode sidewalls made of an insulating material and formed on both side surfaces of the gate electrode; and a step sidewall made of the same material as the insulating material for the electrode sidewalls and formed on the side surface of the step portion. In this semiconductor device, at least a part of the holes can be formed by also removing a portion of the insulating film disposed on the step sidewall.

Owing to this structure, the abrupt level difference between the surfaces of the isolation and the active area can be released by the step sidewall. Therefore, a residue is scarcely generated in patterning the interconnection members, and an upper interconnection is prevented from being disconnected and increasing in its resistance.

The semiconductor device can further comprise a gate protection film formed on the gate electrode, and at least a part of the holes can be formed so as to stretch over the source/drain region and at least a part of the gate protection film.

Owing to this structure, a part of the gate protection film included in the hole is removed by the over-etch in the formation of the holes. However, the gate electrode is protected by the gate protection film, and hence, electrical

short circuit between the gate electrode and the interconnection member can be prevented. Accordingly, there is no need to provide an alignment margin from the gate electrode in the area where each hole is formed, resulting in further
5 improving the integration.

The interconnection members can be first layer metallic interconnections, and the insulating film can be an interlayer insulating film disposed between the semiconductor substrate, and the first layer metallic interconnections. In this case,
10 the semiconductor device preferably further comprises, between the interlayer insulating film and the semiconductor substrate an underlying film made of an insulating material having high etching selectivity against the interlayer insulating film.

The second semiconductor device of this invention in which
15 a semiconductor element is disposed in each of plural active areas in a semiconductor substrate comprises a trench isolation for isolating and surrounding each active area, the trench isolation having a top surface at a higher level than a surface of the active area and having a step portion in a boundary with
20 the active area; and a step sidewall formed on the side surface of the step portion of the trench isolation.

Owing to this structure, in the impurity ion injection for the formation of an impurity diffused layer of the semiconductor device, the step sidewall disposed at the edge of
25 the trench isolation can prevent the impurity ions from being implanted below the edge of the isolation. Furthermore, also

in adopting the structure including a source/drain electrode made of silicide, the step sidewall can prevent the silicide layer from being formed at a deep portion. Therefore, a short circuit current can be prevented from occurring between the source/drain electrode and a substrate region such as the channel stop region. In this manner, the function of the trench isolation to isolate each semiconductor element can be prevented from degrading.

In the second semiconductor device, the step sidewall is preferably made of an insulating material.

Also in the second semiconductor device, the semiconductor element can be a MISFET including a gate insulating film and a gate electrode formed on the active area; and source/drain regions formed in the active area on both sides of the gate electrode. This semiconductor device can be further provided with electrode sidewalls formed on both side surfaces of the gate electrode, and the step sidewall can be formed simultaneously with the electrode sidewalls.

Owing to this structure, the semiconductor elements can be a MISFET having the LDD structure suitable for the refinement. Because of this structure together with the trench isolation structure, the semiconductor device can attain a structure particularly suitable for the refinement and the high integration.

The first method of manufacturing a semiconductor device in which a semiconductor element is disposed in each of plural

active areas in a semiconductor substrate comprises a first step of forming an isolation in a part of the semiconductor substrate, the isolation having a top surface at a higher level than a surface of the semiconductor substrate and having a step
5 portion in a boundary with the surface of the semiconductor substrate; a second step of introducing an impurity at a high concentration into each active area of the semiconductor substrate surrounded by the isolation; a third step of forming an insulating film on the active area and the isolation; a
10 fourth step of forming, on the insulating film, a masking member having an exposing area above an area at least including a portion of the active area where the impurity at the high concentration is introduced; a fifth step of conducting etching by using the masking member so as to selectively remove the
15 insulating film and form holes; and a sixth step of forming a buried conductive layer by filling the holes with a conductive material and forming, on the insulating film, interconnection members to be connected with the buried conductive layer. In this method, in the fourth step, an alignment margin is not
20 provided for preventing the exposing area of the masking member from including a portion above the isolation when mask shift is caused in photolithography.

In adopting this method, even when a part of the isolation is removed by over-etch in the fifth step so that the top
25 surface of the isolation is etched to be lower than the surface of the active area, the depth of the holes formed in the

isolation is small because of the level difference between the isolation and the active area. Accordingly, the decrease of the junction voltage resistance and the increase of the junction leakage current can be suppressed in the manufactured semiconductor device. In addition, the area of the active area can be decreased because no alignment margin from the isolation is provided, resulting in improving the integration of the manufactured semiconductor device.

In the first method of manufacturing a semiconductor device, the following preferred embodiments can be adopted:

The fifth step is preferably performed so as to satisfy the following inequality:

$$OE \times a \times (ER2 / ER1) \le b + D \times (2 / 10)$$

wherein "a" indicates a thickness of the insulating film, "b" indicates a level difference between the surface of the active area and the top surface of the isolation, "ER1" indicates an etching rate of the insulating film, "ER2" indicates an etching rate of the isolation, "D" indicates a depth of an impurity diffused layer in the active area, and "OE" indicates an over-etch ratio of the insulating film.

In adopting this method, even when a part of the isolation included in the hole is removed by over-etch in the formation of the holes, the bottom of the etched portion does not reach a portion where the impurity concentration is low in the active area. In other words, the top surface of the isolation is never placed at a lower level than the surface of the active

area. Accordingly, the degradation of the junction voltage resistance and the increase of the junction leakage current can be definitely prevented in the manufactured semiconductor device.

5 When the semiconductor element is a MISFET, the method can further include, before the second step, a step of forming a gate insulating film on the active area, a step of depositing a conductive film on the gate insulating film and a step of forming a gate electrode by patterning the conducive film, and
10 in the second step, the impurity at the high concentration is introduced so as to form a source/drain region. In such a case, the following preferred embodiments can be adopted.

The method can further comprise, after the step of depositing the conductive film, a step of depositing a
15 protection insulating film on the conductive film, and in the step of forming the gate electrode, the conductive film as well as the protection insulating film are patterned, so as to form a gate protection film on the gate electrode. The fifth step can be performed so as to satisfy the following inequality:

20 $$OE \times a \times (ER3 / ER1) < c$$

wherein "a" indicates a thickness of the insulating film, "c" indicates a thickness of the gate protection film, "ER1" indicates an etching rate of the insulating film, "ER3" indicates an etching rate of the gate protection film and "OE"
25 indicates an over-etch ratio of the insulating film.

When this method is adopted, while the area of the active

area is decreased by not providing an alignment margin for avoiding the interference between the connection hole and the gate electrode, the hole is prevented from reaching the gate electrode below the gate protection film.

5 In the fourth step, the masking member can be formed to be positioned without providing a margin for preventing the exposing area thereof from including a portion above the gate protection film even when the mask shift is caused in the photolithography.

10 Alternatively, in the fourth step, the masking member can be formed to be positioned with the exposing area thereof including at least a part of a portion above the gate protection film when the mask shift is not caused in the photolithography.

15 In the third step, an interlayer insulating film can be formed as the insulating film, and in the sixth step, first layer metallic interconnections can be formed as the interconnection members. In such a case, it is preferred that the interlayer insulating film is formed in the third step 20 after an underlying film made of an insulating material having high etching selectivity against the interlayer insulating film is formed below the interlayer insulating film.

The second method of manufacturing a semiconductor device of this invention comprises a first step of forming an 25 underlying insulating film on a semiconductor substrate; a second step of depositing an etching stopper film on the

underlying insulating film; a third step of forming a trench by exposing a portion of the etching stopper film and the underlying insulating film where an isolation is to be formed and etching the semiconductor substrate in the exposed portion;
5 a fourth step of depositing an insulating film for isolation on an entire top surface of the substrate, flattening the substrate until at least a surface of the etching stopper film is exposed, and forming a trench isolation in the trench so as to surround a transistor region; a fifth step of removing, by
10 etching, at least the etching stopper film and the underlying insulating film, so as to expose a step portion between the transistor region and the trench isolation; a sixth step of depositing a gate oxide film and a conductive film on the substrate and making the conductive film into a pattern of at
15 least a gate electrode; a seventh step of depositing an insulating film for sidewalls on the entire top surface of the substrate and anisotropically etching the insulating film for the sidewalls, so as to form electrode sidewalls and a step sidewall on side surfaces of the gate electrode and the step
20 portion, respectively; and an eighth step of introducing an impurity into the semiconductor substrate in the transistor region on both sides of the gate electrode, so as to form source/drain regions.

When this method is adopted, since the step sidewall is
25 formed between the semiconductor substrate in the transistor region and the trench isolation after completing the fifth

step, the impurity ions are prevented from being implanted below the edge of the trench isolation in the impurity ion injection in the eighth step. Furthermore, also when an area in the vicinity of the surface of the source/drain region is
5 subsequently silicified, the step sidewall made of the insulating film can prevent the silicide layer from being formed at a deep portion. Accordingly, not only the degradation of the junction voltage resistance and the current leakage but also the occurrence of a short circuit current
10 between the source/drain electrode and the substrate region such as the channel stop region can be prevented.

In the second method of manufacturing a semiconductor device, the following preferred embodiments can be adopted:

In the second step, the thickness of the etching stopper
15 film is preferably determined in consideration of an amount of over-etch in the seventh step, so that the step portion having a level difference with a predetermined size or more is exposed in the fifth step.

The method can further comprise, after completing the
20 eighth step, a step of silicifying at least an area in the vicinity of the surface of the source/drain region.

The third method of manufacturing a semiconductor device of this invention comprises a first step of forming a gate insulating film on a semiconductor substrate; a second step of
25 depositing a first conductive film to be formed into a gate electrode on the gate insulating film; a third step of forming

a trench by exposing a portion of the first conductive film where a trench isolation is to be formed and etching the semiconductor substrate in the exposed portion; a fourth step of depositing an insulating film for isolation on an entire top surface of the substrate, flattening the substrate at least until a surface of the first conductive film is exposed, and forming the trench isolation in the trench so as to surround a transistor region; a fifth step of depositing a second conductive film to be formed into at least an upper gate electrode on the entire top surface of the flattened substrate; a sixth step of making the first and second conductive films into a pattern at least of the gate electrode and exposing a step portion between the transistor region and the trench isolation; a seventh step of depositing an insulating film for sidewalls on the entire top surface of the substrate and anisotropically etching the insulating film for the sidewalls, so as to form electrode sidewalls and a step sidewall on side surfaces of the gate electrode and the step portion, respectively; and an eighth step of introducing an impurity into the semiconductor substrate in the transistor region on both sides of the gate electrode, so as to form source/drain regions.

When this method is adopted, the same effects as those attained by the second method of manufacturing a semiconductor device can be attained. In addition, in the patterning process for the gate electrode, the top surface of the substrate is

completely flat, and hence, the patterning accuracy for the gate electrode can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a) through 1(d) are sectional views for showing manufacturing procedures of Embodiment 1 up to the formation of an isolation;

Figures 2(a) through 2(e) are sectional views for showing the manufacturing procedures of Embodiment 1 after the formation of the isolation;

Figures 3(a) through 3(f) are sectional views for showing manufacturing procedures of Embodiment 2 after the formation of an isolation;

Figures 4(a) through 4(c) are sectional views for showing manufacturing procedures of Embodiment 3;

Figures 5(a) through 5(c) are sectional views for showing manufacturing procedures of Embodiment 4;

Figures 6(a) through 6(f) are sectional views for showing manufacturing procedures of Embodiment 5;

Figures 7(a) through 7(c) are sectional views for showing manufacturing procedures of Embodiment 6;

Figures 8(a) through 8(c) are sectional views for showing manufacturing procedures of Embodiment 7 in which a comparatively thin insulating film of Embodiment 1 is replaced with a layered film and an interlayer insulating film;

Figures 9(a) through 9(c) are sectional views for showing

the manufacturing procedures of Embodiment 7 in which a comparatively thin insulating film of Embodiment 2 is replaced with a layered film and an interlayer insulating film;

5 Figures 10(a) through 10(c) are sectional views for showing the manufacturing procedures of Embodiment 7 in which a comparatively thin insulating film of Embodiment 4 is replaced with a layered film and an interlayer insulating film;

10 Figures 11(a) through 11(c) are sectional views for showing the manufacturing procedures of Embodiment 7 in which a comparatively thin insulating film of Embodiment 5 is replaced with a layered film and an interlayer insulating film;

Figure 12 is a sectional view for showing the structure of a semiconductor device of Embodiment 8;

15 Figures 13(a) through 13(e) are sectional views for showing manufacturing procedures for the semiconductor device of Embodiment 8;

Figures 14(a) through 14(e) are sectional views for showing manufacturing procedures for a semiconductor device of Embodiment 9;

20 Figures 15(a) through 15(f) are sectional views for showing manufacturing procedures for a semiconductor device of Embodiment 10;

25 Figures 16(a) through 16(e) are sectional views for showing manufacturing procedures for a semiconductor device of Embodiment 11;

Figure 17 is a sectional view of a conventional

semiconductor device in which the surfaces of an active area and a trench isolation are placed at the same level;

Figures 18(a) through 18(c) are sectional views for showing manufacturing procedures for the conventional semiconductor device of Figure 17;

Figure 19 is a sectional view of a conventional semiconductor device having a salicide structure and a trench isolation structure;

Figures 20(a) through 20(e) are sectional views for showing manufacturing procedures for the conventional semiconductor device of Figure 19; and

Figures 21(a) and 21(b) are partial sectional views for showing problems, in a conventional semiconductor device having a trench isolation, occurring in an impurity ion injection process and a silicifying process, respectively.

DETAILED DESCRIPTION OF THE INVENTION

(Embodiment 1)

Embodiment 1 of the invention will now be described referring to Figures 1(a) through 1(d) and 2(a) through 2(e). In the manufacturing procedures of this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is designed to stretch over an active area and an isolation when alignment shift is not caused in photolithography.

In this embodiment, the isolation is formed as a trench

isolation. Furthermore, interconnection to be formed above is assumed to be local interconnection in which an insulating film can be comparatively thin, but the embodiment is applicable also to general global interconnection formed on a thick interlayer insulating film.

First, as is shown in Figure 1(a), a resist film 50a having a predetermined pattern is formed on a p-type silicon substrate 1 (or a p-type well). The silicon substrate 1 is dry-etched by using the resist film 50a as a mask, thereby forming a trench 51 with a depth of 1 μm.

Then, as is shown in Figure 1(b), the resist film 50a is removed, and then a silicon oxide film 2x is deposited on the entire top surface of the silicon substrate 1. Through this procedure, the previously formed trench 51 is filled with the silicon oxide film 2x.

Next, as is shown in Figure 1(c), the silicon oxide film 2x on the silicon substrate 1 is removed by, for example, a CMP (chemical mechanical polishing) method or etch-back through dry etching using a resist film, and at the same time, a trench isolation 2b is formed. At this point, the top surface of the silicon substrate 1 and the top surface of the isolation 2b are flattened with no level difference therebetween.

Then, as is shown in Figure 1(d), dry etching with high etch selectivity is conducted so as to etch the silicon substrate 1 alone by a thickness of 0.2 μm. Thus, a step portion which is higher in a stepwise manner than the top

surface of the silicon substrate 1 by 0.2 μm is formed in the isolation 2b. The level difference caused by the step portion is required to be sufficiently large in consideration of an amount of over-etch in etching a subsequently formed insulating film 12, and hence, the level difference is preferably equal to or larger than the thickness of the insulating film 12.

It is noted that the method of causing the level difference between the top surface of the isolation 2b and the surface of the active area is not limited to that described above. For example, the level difference can be caused as follows: After an etching stopper film having a thickness corresponding to the level difference is previously deposited on the silicon substrate, a trench is formed and an insulating film for the trench isolation is deposited. Then, the entire top surface of the substrate is flattened by the CMP method or the like, and the etching stopper film is subsequently removed.

Next, As is shown in Figure 2(a), after forming a gate oxide film 3 on the silicon substrate 1, a polysilicon film 4x is deposited on the entire top surface of the substrate.

Then, as is shown in Figure 2(b), after forming a resist film (not shown) having a predetermined pattern on the polysilicon film 4x, dry etching is conducted so as to form a polysilicon electrode 4a on the active area and a polysilicon interconnection 4b on the isolation 2b. Then, by using the gate electrode 4a as a mask, n-type impurity ions are injected at a high concentration, thereby forming high-concentration

source/drain regions 8 in the silicon substrate 1 on both sides of the polysilicon electrode 4a.

After this, as is shown in Figure 2(c), the insulating film 12 having a thickness of, for example, 0.15 μm is deposited, so that an interconnection subsequently formed above the insulating film (i.e., the local interconnection in this embodiment) can be electrically insulated from the polysilicon electrode, the polysilicon interconnection and the active area.

Next, as is shown in Figure 2(d), a resist film 25a having a pattern for forming a connection hole is formed on the insulating film 12. At this point, the exposing area of the resist film 25a is positioned without an alignment margin for preventing interference with the isolation 2b. In this embodiment, after the resist film 25a is formed so that the exposing area stretches over the source/drain region 8, that is, the active area of a transistor, and the isolation 2b, dry etching is conducted by using the resist film 25a as a mask, thereby forming a connection hole 14 by removing the insulating film 12 in the exposing area of the resist film 25a. At this point, when the insulating film 12 is, for example, 40% over-etched than its thickness of 0.15 μm in order to ensure the formation of the connection hole 14, the isolation 2b in the exposing area of the resist film 25a is etched by a thickness of approximately 0.06 μm. However, in this embodiment, the step portion has a height of 0.2 μm, which is sufficiently larger than this etched amount, and hence, a recess where the

top surface of the isolation 2b is lower than the top surface of the silicon substrate 1 is never formed in any part of the connection hole 14.

5 Next, as is shown in Figure 2(e), a polysilicon film is deposited on the entire top surface and is patterned, thereby forming the local interconnection 13. At this point, the local interconnection 13 is also formed within the connection hole 14, so as to be electrically connected with the source/drain region 8 serving as the active area.

10 In a semiconductor device formed in the aforementioned procedures, the top surface of the isolation 2b is higher in a stepwise manner than the surface of the active area. Therefore, even when the isolation 2b is removed by some amount by the over-etch in dry etching the insulating film 12, the 15 isolation 2b is prevented from being etched by a thickness exceeding the level difference caused by the step portion. Accordingly, when mask alignment is shifted in the photolithography, a recess with a depth reaching a certain depth of the source/drain region 8 is prevented from being 20 formed in the connection hole 14. As a result, the conventional problems, that is, the degradation of the junction voltage resistance and the increase of the junction leakage current caused because of the low impurity concentration at a lower part of the active area of the silicon substrate 25 corresponding to the sidewall of the recess, can be effectively prevented.

However, the level difference between the top surface of the isolation 2b and the surface of the active area is not necessarily required to be larger than the thickness of the insulating film 12. The dimensions and materials of the respective components can be determined so as to satisfy the following inequality (1), wherein "a" denotes the thickness of the insulating film 12; "b" denotes the level difference between the top surface of the isolation 2b and the surface of the active area; "ER1" denotes the etching rate of the insulating film 12; "ER2" denotes the etching rate of the isolation 2b; "D" denotes the depth of an impurity diffused layer in the active area; and "OE" denotes the over-etch ratio of the insulating film 12 in the formation of the connection hole 14.

$$OE \times a \times (ER2 / ER1) \geq b + D \times (2 / 10) \quad \ldots (1)$$

As far as the inequality (1) is satisfied, even when a part of the isolation 2b is removed to be at a lower level than the surface of the silicon substrate in the active area through the formation of the connection hole 14, so that the recess 40 as is shown in Figure 18(c) is formed in a part of the connection hole 14, the bottom of the recess 40 is prevented from reaching the depth where the impurity concentration is low.

Since the alignment margin in view of the mask shift in the photolithography can be omitted, the following effects can be attained: When a distance Lb between the polysilicon electrode 4a serving as the gate electrode and the isolation 2b

is estimated as an index of the integration, the distance Lb is 0.8 μm, namely, the sum of the diameter of the connection hole, 0.5 μm, and the alignment margin from the gate electrode, 0.3 μm. Thus, the distance Lb can be decreased by 0.4 μm as compared with the conventional distance La of 1.2 μm (shown in Figure 17).

(Embodiment 2)

Embodiment 2 will now be described referring to Figures 3(a) through 3(f). In this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is formed so as to stretch over an active area and an isolation in the same manner as in Embodiment 1, and a step portion between the isolation and the active area is provided with a sidewall.

First, as is shown in Figures 3(a) and 3(b), an isolation 2b whose top surface is higher in a stepwise manner than the surface of an active area by a predetermined level difference and a gate oxide film 3 are formed on a silicon substrate 1 in the same manner as described in Embodiment 1. Then, a polysilicon film 4x is deposited on the entire top surface.

Next, the polysilicon film 4x is patterned, thereby forming a polysilicon electrode 4a and a polysilicon interconnection 4b. The procedures conducted so far are identical to those adopted in Embodiment 1. Then, a silicon oxide film is deposited on the entire top surface and is subjected to anisotropic etching, thereby forming electrode sidewalls 7a on both side surfaces of the polysilicon electrode

4a and interconnection sidewalls 7b on both side surfaces of the polysilicon interconnection 4b. At the same time, a step sidewall 7c is formed on the side surface of the step portion between the isolation 2b and the active area. Each of the
5 sidewalls has a width of, for example, approximately 0.1 μm. After forming the polysilicon electrode 4a, an n-type impurity with a low concentration is ion-injected into the active area, so as to form a low-concentration source/drain region 6. After forming the electrode sidewalls 7a, an n-type impurity with a
10 high concentration is ion-injected into the active area, so as to form a high-concentration source/drain region 8. This is a generally adopted method of manufacturing a MOSFET having the so-called LDD structure.

Then, as is shown in Figures 3(d) through 3(f), the
15 procedures as described in Embodiment 1 referring to Figures 2(c) through 2(e) are conducted, thereby forming an insulating film 12 and a local interconnection 13 thereon.

This embodiment can achieve the effect to improve the integration similarly to Embodiment 1. In addition, owing to
20 the step sidewall 7c, the abrupt level difference between the isolation 2b and the active area can be released. As a result, the amount of residue generated in the formation of the local interconnection 13 by patterning the polysilicon film can be advantageously decreased, and disconnection of the local
25 interconnection 13 and resistance increase thereof can also be prevented.

At this point, a distance Lc between the polysilicon electrode 4a serving as a gate electrode and the isolation 2b is estimated as an index of the integration. The distance Lc is 1.0 μm, namely, the sum of the diameter of the connection hole, 0.5 μm, the width of the electrode sidewall 7a, 0.1 μm, the alignment margin from the polysilicon electrode 4a, 0.3 μm, and the width of the step sidewall 7c, 0.1 μm. Thus, the distance Lc can be decreased by 0.2 μm as compared with the conventional distance La of 1.2 μm (shown in Figure 17).

(Embodiment 3)

Embodiment 3 will now be described referring to Figures 4(a) through 4(c).

In manufacturing procedures described in this embodiment, a connection hole is formed so as to stretch over an active area and an isolation only when mask alignment shift is caused in the photolithography.

Figure 4(a) shows a state where the procedures described in Embodiment 2 referring to Figures 3(a) through 3(d) have been completed. Specifically, as is shown in Figure 4(a), after an isolation 2b with a top surface higher in a stepwise manner than the surface of an active area, a step sidewall 7c on the side surface of the step portion of the isolation 2b, a gate oxide film 3, a polysilicon electrode 4a serving as a gate electrode, electrode sidewalls 7a on both side surfaces of the polysilicon electrode 4a, a low-concentration source/drain region 6, a high-concentration source/drain region 8, a

polysilicon interconnection 4b on the isolation 2b, and interconnection sidewalls 7b on both side surfaces of the polysilicon interconnection 4b are formed, an insulating film 12 with a thickness of approximately 0.15 μm is formed on the
5 entire top surface.

Next, as is shown in Figure 4(b), a resist film 25b for forming a connection hole is formed. At this point, in this embodiment, the resist film 25b is formed so that the connection hole stretches over the active area (i.e., the high-
10 concentration source/drain region 8) and the step sidewall 7c when the mask alignment shift is not caused in the lithography. Then, the insulating film 12 is etched, thereby forming the connection hole 14 stretching over the active area and the step sidewall 7c.

15 Then, as is shown in Figure 4(c), a local interconnection 13 to be connected with the high-concentration source/drain region 8 is formed on the insulating film 12.

In the state shown in Figure 4(b), the edge of the connection hole 14 can be shifted toward the isolation 2b by a
20 maximum of 0.3 μm due to the mask alignment shift in the lithography. In such a case, the resultant structure becomes that described in Embodiment 2 (shown in Figure 3(e)). However, no recess is formed in the isolation 2b within the connection hole 14 as described in Embodiments 1 and 2 even in
25 such a case. Alternatively, even if a recess is formed, the problems of the degradation of the junction voltage resistance

and the increase of the junction leakage current can be avoided as far as the dimensions and the like of the respective components are determined so as to satisfy the inequality (1).

5 Also in this embodiment, a distance Lc between the polysilicon electrode 4a and the isolation 2b is estimated as an index of the integration. Similarly to Embodiment 2, the distance Lc is 1.0 μm, namely, the sum of the diameter of the connection hole, 0.5 μm, the width of the electrode sidewall 7a, 0.1 μm, the alignment margin from the polysilicon electrode

10 4a, 0.3 μm, and the width of the step sidewall 7c, 0.1 μm. Thus, the distance Lc can be decreased by 0.2 μm as compared with the conventional distance La of 1.2 μm.

(Embodiment 4)

Embodiment 4 will now be described referring to Figures

15 5(a) through 5(c). In manufacturing procedures described in this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is formed so as to stretch over an active area and a polysilicon interconnection on an isolation.

20 Figure 5(a) shows the state where the procedures described in Embodiment 2 referring to Figures 3(a) through 3(d) have been completed. Specifically, as is shown in Figure 5(a), after an isolation 2b with a top surface higher in a stepwise manner than the surface of the active area, a step sidewall 7c

25 on the side surface of the step portion of the isolation 2b, a gate oxide film 3, a polysilicon electrode 4a serving as a gate

electrode, electrode sidewalls 7a on both side surfaces of the polysilicon electrode 4a, a low-concentration source/drain region 6, a high-concentration source/drain region 8, a polysilicon interconnection 4b on the isolation 2b, and interconnection sidewalls 7b on both side surfaces of the polysilicon interconnection 4b are formed, an insulating film 12 with a thickness of approximately 0.15 μm is formed on the entire top surface.

Next, as is shown in Figure 5(b), a resist film 25c for forming a connection hole is formed. In this embodiment, the resist film 25c is formed with its exposing area stretching over the active area (i.e., the high-concentration source/drain region 8) and the polysilicon interconnection 4b on the isolation 2b when the mask alignment shift is not caused in the lithography. Then, the insulating film 12 is etched, thereby forming the connection hole 14 stretching over the high-concentration source/drain region 8, the isolation 2b and the polysilicon interconnection 4b.

Then, as is shown in Figure 5(c), a local interconnection 13 to be connected with the high-concentration source/drain region 8 and the polysilicon interconnection 4b is formed on the insulating film 12.

When the high-concentration source/drain region 8 is to be electrically connected with the polysilicon interconnection 4b serving as a gate interconnection formed on the isolation 2b in the conventional manufacturing procedures, a connection hole

formed on the high-concentration source/drain region 8 and another connection hole formed on the polysilicon interconnection 4b are required to be positioned in consideration of alignment margins from the boundaries with the high-concentration source/drain region 8 and the isolation 2b, respectively. In contrast, in this embodiment, the interconnection member can be connected with the high-concentration source/drain region 8 and the polysilicon electrode 4b through one connection hole 14 without consideration of the alignment margins. In addition, as described in Embodiments 1 through 3, the problems of the degradation of the junction voltage resistance and the increase of the junction leakage current can be prevented from being caused through the over-etch in etching the insulating film 12.

In this embodiment, the interconnection on the isolation 2b is made of a polysilicon film, but another conductive material or an interconnection on a layer different from the polysilicon electrode can be used instead.

(Embodiment 5)

Embodiment 5 will now be described referring to Figures 6(a) through 6(f). In manufacturing procedures described in this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is formed so as to stretch over an active area, a gate electrode and an isolation.

First, as is shown in Figure 6(a), an isolation 2b with a

top surface higher in a stepwise manner than the surface of a p-type silicon substrate 1 is formed.

Next, as is shown in Figure 6(b), a polysilicon film 4x with a thickness of 0.2 μm is deposited on the entire top surface, and a silicon oxide film 15x for gate protection with a thickness of approximately 0.15 μm is deposited on the polysilicon film 4x. At this point, the thickness of the silicon oxide film 15x for gate protection is required to be sufficiently large in consideration of an amount of over-etch to be removed in etching a subsequently formed insulating film 12. In this embodiment, the thickness of the silicon oxide film 15x is substantially the same as that of the insulating film 12.

Then, as is shown in Figures 6(c) and 6(d), the procedures as described in Embodiment 2 referring to Figures 3(c) and 3(d) are conducted. Thus, after a polysilicon electrode 4a and a gate protection film 15a together serving as a gate electrode, electrode sidewalls 7a on both side surfaces of the polysilicon electrode 4a and the gate protection film 15a, a low-concentration source/drain region 6, a high-concentration source/drain region 8, a polysilicon interconnection 4b and an interconnection protection film 15b on the isolation 2b, interconnection sidewalls 7b on both side surfaces of the polysilicon interconnection 4b and the interconnection protection film 15b and a step sidewall 7c are formed, the insulating film 12 with a thickness of approximately 0.15 μm is

formed on the entire top surface.

Next, as is shown in Figure 6(e), a resist film 25d for forming a connection hole is formed. At this point, in this embodiment, the resist film 25d is formed so that the connection hole stretches over the polysilicon electrode 4a, the high-concentration source/drain region 8 serving as the active area and the isolation 2b when the mask alignment shift is not caused in the lithography. Accordingly, when the alignment shift is not caused, the exposing area of the resist film 25d stretches also over a part of the polysilicon electrode 4a. Then, the insulating film 12 is patterned by dry etching. At this point, a part of the isolation 2b and the gate protection film 15a in the exposing area of the resist film 25d are also removed by some amount by the over-etch in the dry etching of the insulating film 12. However, the connection hole 14 never reaches the polysilicon electrode 4a.

Then, as is shown in Figure 6(f), a polysilicon film is deposited on the entire top surface and then patterned, thereby forming a local interconnection 13 to be connected with the high-concentration source/drain region 8.

In this embodiment, the problems of the degradation of the junction voltage resistance and the increase of the junction leakage current can be avoided as in the aforementioned embodiments even when the insulating film 12 is 40% over-etched than its thickness of 0.15 μm in order to form the connection hole 14.

In particular in this embodiment, the connection hole 14 stretches also over the polysilicon electrode 4a when the alignment shift is not caused in the lithography. Therefore, when the insulating film 12 is, for example, 40% over-etched than its thickness of 0.15 μm in the dry etching thereof, although a part of the gate protection film 15a is etched by a thickness of approximately 0.06 μm. However, the conventional problem of the electric short circuit with an interconnection on an upper layer through the connection hole can be avoided since the thickness of the gate protection film 15a is 0.15 μm, which is sufficiently larger than 0.06 μm.

It is noted that the thickness of the gate protection film 15a can be determined as follows: The dimensions and materials of the respective components are determined so as to satisfy the following inequality (2), wherein "a" denotes the thickness of the insulating film 12; "c" denotes the thickness of the gate protection film 4a, "ER1" denotes the etching rate of the insulating film 12; "ER3" denotes the etching rate of the gate protection film 4a; and "OE" denotes the over-etch ratio of the insulating film 12 in the formation of the connection hole 14:

$$OE \times a \times (ER3 / ER1) < c \quad \ldots \quad (2)$$

At this point, a distance Ld between the polysilicon electrode 4a serving as the gate electrode and the isolation 2b is estimated as an index of the integration. The distance Ld is 0.7 μm, namely, the sum of the diameter of the connection hole, 0.5 μm, the width of the electrode sidewall 7a, 0.1 μm,

and the width of the step sidewall 7c, 0.1 μm. Thus, the distance Ld can be decreased by 0.5 μm as compared with the conventional distance of 1.2 μm.

(Embodiment 6)

5 Embodiment 6 will now be described referring to Figures 7(a) through 7(c). In manufacturing procedures described in this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is formed so as to stretch over an active area, an electrode sidewall and an 10 isolation when the alignment shift is not caused, and is formed so as to stretch also over a polysilicon electrode only when the alignment shift is caused.

Figure 7(a) shows the state where the procedures described in Embodiment 5 referring to Figures 6(a) through 6(d) have 15 been completed. Specifically in Figure 7(a), after an isolation 2b having a top surface higher in a stepwise manner than the surface of the active area, a step sidewall 7c on the side surface of the step portion of the isolation 2b, a gate oxide film 3, a polysilicon electrode 4a serving as a gate 20 electrode, a gate protection film 15a on the polysilicon electrode 4a, electrode sidewalls 7a on both side surfaces of the polysilicon electrode 4a and the gate protection film 15a, a low-concentration source/drain region 6, a high-concentration source/drain region 8, a polysilicon interconnection 4b on the 25 isolation 2b, an interconnection protection film 15b on the polysilicon interconnection 4b, and interconnection sidewalls

7b on both side surfaces of the polysilicon interconnection 4b and the interconnection protection film 15b are formed, an insulating film 12 having a thickness of approximately 0.15 μm is formed on the entire top surface.

5 Next, as is shown in Figure 7(b), a resist film 25e having a pattern for forming a connection hole is formed. At this point, in this embodiment, the resist film 25e is formed so that its exposing area can expose at least the step sidewall 7c and the high-concentration source/drain region 8 serving as the

10 active area and stretches also over the electrode sidewall 7a.

Then, a polysilicon film is deposited on the entire top surface and patterned, thereby forming a local interconnection 13 to be connected with the high-concentration source/drain region 8.

15 In the procedure shown in Figure 7(b) of this embodiment, when the exposing area of the resist film 25e is shifted by, for example, a maximum of 0.3 μm due to the alignment shift in the lithography, the connection hole 14 is formed so as to stretch also over a part of the polysilicon electrode 4a. When

20 the exposing area of the resist film 25e is shifted in the reverse direction, the connection hole 14 is formed so as to stretch also over a part of the isolation 2b. However, in either case, the junction voltage at the edge of the isolation 2b is prevented from degrading and the junction leakage current

25 is prevented from increasing as far as the dimensions and the like of the respective components are determined so as to

satisfy the inequalities (1) and (2). In addition, an electrical short circuit between an interconnection member such as the local interconnection and the polysilicon electrode 4a can be avoided.

5 At this point, a distance Le between the polysilicon electrode 4a serving as the gate electrode and the isolation 2b is estimated as an index of the integration. Similarly to Embodiment 5, the distance Le is 0.7 µm, namely, the sum of the diameter of the connection hole, 0.5 µm, the width of the 10 electrode sidewall 7a, 0.1 µm, and the width of the step sidewall 7c, 0.1 µm. Thus, the distance Le can be decreased by 0.5 µm as compared with the conventional distance of 1.2 µm.

In each of the aforementioned embodiments, the local interconnection is adopted as the interconnection member so as 15 to make the insulating film 12 comparatively thin. However, each embodiment can be applied to an interconnection member using a general global interconnection formed with an interlayer insulating film sandwiched. When the global interconnection is adopted, the interlayer insulating film is 20 comparatively thick. Therefore, the effects of the embodiments can be similarly attained by decreasing the over-etch ratio of the interlayer insulating film in the formation of the connection hole or by increasing the level difference between the top surface of the isolation and the surface of the active 25 area. This will be described in more detail in Embodiment 7 below.

Furthermore, when the isolation 2b and the gate protection film 15a used in Embodiment 5 or 6 are made of a material having a smaller etching rate than the material for the insulating film 12 against the etching for forming the connection hole, the semiconductor device can be manufactured with more ease.

In addition, when the insulating film 12 in each of the aforementioned embodiments has a multilayered structure including at least one lower layer made of a material having a smaller etching rate against the etching for forming the connection hole, the semiconductor device can be manufactured with more ease.

(Embodiment 7)

Embodiment 7 will now be described in which an interconnection layer formed on a thick interlayer insulating film is connected with an active area of a semiconductor substrate through a contact hole formed on the interlayer insulating film.

Figures 8(a) through 8(c) are sectional views for showing procedures for forming a layered film 10 and an interlayer insulating film 11 instead of the comparatively thin insulating film 12 of Embodiment 1. As is shown in Figure 8(a), after conducting the procedures shown in Figures 1(a) through 1(d) and 2(a) through 2(c), a layered film 10 including a silicon oxide film 10a with a thickness of approximately 70 nm and a silicon nitride film 10b with a thickness of approximately 80

nm is formed on the entire top surface of the substrate. Then, an interlayer insulating film 11 of a silicon oxide film with a thickness of approximately 600 nm is deposited thereon. Next, a resist film 25a having a pattern for forming a contact hole is formed on the interlayer insulating film 11. At this point, the exposing area of the resist film 25a is positioned without an alignment margin for avoiding interference with an isolation 2b. In Figure 8(a), the resist film 25a is formed so that the exposing area stretches over a source/drain region 8 serving as the active area of a transistor and the isolation 2b.

Next, as is shown in Figure 8(b), etching is conducted by using the resist film 25a as a mask, thereby selectively removing the interlayer insulating 25a and the layered film 10. Thus, a contact hole 20 stretching over the isolation 2b and the active area is formed.

Then, as is shown in Figure 8(c), a plug underlying film 21 made of a TiN/Ti film and a W plug 22 are deposited within the contact hole 20 by selective CVD. Furthermore, an aluminum alloy film is deposited on the entire top surface of the substrate and the aluminum alloy film is patterned, thereby forming a first layer metallic interconnection 23. At this point, the first layer metallic interconnection 23 is electrically connected with the source/drain region 8 serving as the active area through the W plug 22 and the plug underlying film 23 filled in the contact hole 20.

Figures 9(a) through 9(c) are sectional views for showing procedures for forming a layered film 10 and an interlayer insulating film 11 instead of the comparatively thin insulating film 12 of Embodiment 2. In these manufacturing procedures, a procedure for forming sidewalls 7a through 7c is added to the manufacturing procedures shown in Figures 8(a) through 8(c), so as to manufacture a transistor having the LDD structure.

Figures 10(a) through 10(c) are sectional views for showing procedures for forming a layered film 10 and an interlayer insulating film 11 instead of the comparatively thin insulating film 12 of Embodiment 4. In the procedure shown in Figure 10(a), a resist film 25c having its exposing area stretching over the active area and the gate interconnection 4b is formed on the interlayer insulating film 11. Thereafter, the same procedures as those shown in Figures 8(b) and 8(c) are conducted.

Figures 11(a) through 11(c) are sectional views for showing procedures for forming a layered film 10 and an interlayer insulating film 11 instead of the comparatively thin insulating film 12 of Embodiment 5. In the procedure shown in Figure 11(a), a gate protection silicon oxide film 15a is formed on a gate electrode 4a, and the layered film 10 and the interlayer insulating film 11 are formed thereon. Then, a resist film 25d having its exposing area stretching over the isolation, the active area and the gate electrode 4a is formed on the interlayer insulating film 11. Thereafter, the same

procedures as those shown in Figures 8(b) and 8(c) are conducted.

In each of the procedures shown in Figures 8(b), 9(b), 10(b) and 11(b), the silicon nitride film 10b having high etching selectivity against the silicon oxide film is formed below the interlayer insulating film 11. Therefore, the silicon nitride film 10b is prevented from being completely removed by the over-etch in etching the interlayer insulating film 11. When the silicon nitride film 10b is to be removed from the layered film 10, the silicon oxide film 10a is prevented from being completely removed since the etching selectivity between the silicon nitride film 10b and the silicon oxide film 10a below is high. Furthermore, since the silicon oxide film 10a has a thickness of approximately 70 nm, which is smaller than the level difference of 0.2 μm between the isolation and the active area, the isolation 2b is prevented from being etched to be lower than the surface of the active area by the over-etch in etching the silicon oxide film 10a. In other words, a recess where the top surface of the isolation 2b is lower than the surface of the silicon substrate is never formed in any part of the contact hole 20. Accordingly, in the formation of the contact hole for electrically connecting the interconnection layer formed on the interlayer insulating film and the active area of the semiconductor substrate, the same effects as those described in the aforementioned embodiments can be attained.

However, the underlying film below the interlayer insulating film can be omitted in this embodiment. Even when it is omitted, since the step portion is formed between the top surface of the isolation and the surface of the active area, the isolation cannot be etched to be lower than the surface of the active area in the formation of the contact hole. Thus, the degradation of the junction voltage resistance the increase of the junction leakage current can be prevented as much as possible.

(Embodiment 8)

Embodiment 8 will now be described referring to Figures 12 and 13(a) through 13(e). Figure 12 is a sectional view showing the structure of a semiconductor device of this embodiment, and Figures 13(a) through 13(e) are sectional views for showing manufacturing procedures for the semiconductor device having the structure shown in Figure 12.

As is shown in Figure 12, in a silicon substrate (or well) 1 of one conductivity type, a trench isolation 2b is formed in an isolation region Reiso for partitioning an area in the vicinity of the surface of the silicon substrate 1 into a plurality of transistor regions Refet. The top surface of the isolation 2b is sufficiently higher than the surface of the silicon substrate 1 in each transistor region Refet, and a step portion with a predetermined level difference is formed between the isolation 2b and the transistor region Refet. This isolation 2b is formed by filling a trench formed in the

silicon substrate 1 with an insulating material as described below. Furthermore, a channel stop region 60 of the same conductivity type as that of the silicon substrate 1 is formed at least below the isolation 2b.

5 In each transistor region Refet partitioned by the isolation 2b is formed a MOS transistor including a gate electrode 4a, a gate oxide film 3, electrode sidewalls 7a, a low-concentration source/drain region 6 and a high-concentration source/drain region 8. Also, on the silicon
10 substrate 1 excluding the transistor regions Refet and on the isolation 2b, a gate interconnection 4b formed simultaneously with the gate electrode 4a and interconnection sidewalls 7b are formed. Furthermore, an upper gate electrode 9a, an upper gate interconnection 9b and a source/drain electrode 9c each made of
15 titanium silicide ($TiSi_2$) are formed on the gate electrode 4a, the gate interconnection 4b and the high-concentration source/drain region 8, respectively.

This embodiment is characterized by a step sidewall 7c formed on the side surface of the step portion of the isolation
20 2b simultaneously with the electrode sidewalls 7a and the interconnection sidewalls 7b. A part of the step sidewall 7c is communicated with the electrode sidewalls 7a and the interconnection sidewalls 7b.

Furthermore, on the entire top surface of the substrate
25 bearing the isolation 2b, the gate electrode 4a and the like, an interlayer insulating film 11 and a first layer metallic

interconnection 23 are formed. The first layer metallic interconnection 23 is connected with the upper gate electrode 9a and the source/drain electrode 9c in the transistor region through a W plug 22.

5 Now, the manufacturing procedures for realizing the structure shown in Figure 12 will be described referring to Figures 13(a) through 13(e).

First, as is shown in Figure 13(a), a silicon oxide film 52 and a silicon nitride film 53 are deposited on a silicon 10 substrate 1. Then, a resist film 50a for exposing the isolation regions Reiso and masking the transistor regions Refet is formed on the silicon nitride film 53. After this, etching is conducted by using the resist film 50a as a mask, so as to selectively remove the silicon nitride film 53 and the 15 silicon oxide film 52 and further etch the silicon substrate 1, thereby forming a trench 51. At this point, differently from the conventional method of forming a trench, the silicon nitride film 53 has a thickness as large as approximately 150 through 200 nm. However, the silicon oxide film 52 has a 20 thickness of 10 through 20 nm as in the conventional method. The depth of the trench 51 can be approximately 500 nm also as in the conventional method. Then, impurity ions of a conductivity type different from that of an impurity to be injected into a subsequently formed source/drain region are 25 injected, thereby forming a channel stop region 60.

Next, as is shown in Figure 13(b), after removing the

resist film 50a, a silicon oxide film (not shown) is deposited so as to have a sufficient thickness larger than the sum of the depth of the trench 51 and the thickness of the remaining silicon nitride film 53, namely, the height from the bottom of
5 the trench 51 to the top surface of the silicon nitride film 53. Then, the silicon oxide film is removed by the CMP method so as to expose the surface of the silicon nitride film 53, thereby flattening the entire top surface of the substrate. Through this procedure, a trench isolation 2b made of the
10 silicon oxide film is formed in the isolation region Reiso. The flattening method to be adopted is not limited to that described above but the surface can be flattened by etch-back using a resist film having a reverse pattern to the pattern of the transistor region Refet.

15 Then, the silicon nitride film 53 is removed by using a phosphoric acid boiling solution or the like and the silicon oxide film 52 is removed by using a hydrofluoric acid type wet etching solution or the like, so as to expose the surface of the silicon substrate 1 in the transistor region Refet, which
20 procedures are not shown in the drawing. At this point, a step portion having a sufficient level difference between the surface of the silicon substrate 1 in the transistor region Refet and the top surface of the isolation 2b is exposed characteristically in this embodiment. The level difference is
25 set at approximately 50 through 100 nm in consideration of the amount of over-etch in a procedure for forming sidewalls

described below. However, in order to effectively achieve the effects of this embodiment, the thickness of an insulating film for the sidewall and the amount of over-etch are required to be appropriately determined in the subsequent procedure for
5 forming the sidewalls.

Then, as is shown in Figure 13(c), a polysilicon film 4 is deposited on the silicon substrate 1 and the isolation 2b, and the resist film 50b for exposing an area excluding the areas for a gate electrode and a gate interconnection is formed
10 thereon. Then, the dry etching is conducted by using the resist film 50b as a mask, thereby forming the gate electrode 4a and the gate interconnection 4b, which procedure is not shown in the drawing.

Next, as is shown in Figure 13(d), by using the gate
15 electrode 4a as a mask, impurity ions at a low concentration are injected, thereby forming a low-concentration source/drain region 6. Then, an insulating film 7 (a silicon oxide film) is deposited on the entire top surface of the substrate.

Then, as is shown in Figure 13(e), the insulating film 7
20 is anisotropically etched, thereby forming the electrode sidewalls 7a on the both side surfaces of the gate electrode 4a and interconnection sidewalls 7b on the both side surfaces of the gate interconnection 4b. At the same time, a step sidewall 7c is formed on the side surface of the step portion between
25 the silicon substrate 1 in the transistor region Refet and the isolation 2b. After forming these sidewalls, impurity ions are

injected, thereby forming the high-concentration source/drain region 8. Also at this point, the step portion between the silicon substrate 1 in the transistor region Refet and the isolation 2b has the sufficient level difference.

5 Although the procedures thereafter are not shown in the drawing, an upper gate electrode 9a, an upper gate interconnection 9b and a source/drain electrode 9c are formed by a silicifying procedure, an interlayer insulating film 11 is deposited and a contact hole is formed, and then the contact 10 hole is filled with a metal, and a first layer metallic interconnection 12 is formed. In this manner, the MOS transistor having the trench isolation structure as shown in Figure 12 is manufactured.

In the aforementioned procedures, the electrode sidewalls 15 7a and the like are formed in order to manufacture a transistor with the LDD structure. However, the electrode sidewalls 7a and the like can be formed in a transistor having the so-called pocket injection structure, in which a punch-through stopper is formed by injecting an impurity of a different conductivity 20 type into an area between the source/drain region and the channel region. Therefore, this embodiment is applicable to such a transistor having the pocket injection structure.

In manufacturing a MOS transistor having a gate length of 1 µm or less as in this embodiment, it is necessary to form the 25 electrode sidewalls 7a on the side surfaces of the gate electrode 4a in order to provide the transistor with the LDD

structure or the pocket injection structure in which the short channel effect can be suppressed and the reliability of the transistor can be ensured. The thickness of the electrode sidewall 7a depends upon the characteristics of a device to be manufactured. Since the sidewall is formed by dry etching with high anisotropy, its thickness can be controlled substantially only by controlling the thickness of the film to be deposited. However, 10% through 30% over-etch is generally conducted in consideration of the fluctuation in the etching rate in the wafer and the fluctuation in the thickness of the deposited film. For example, when the electrode sidewall 7a is formed out of an insulating film with a thickness of 100 nm, the etching is conducted for a time period corresponding to time required for removing an insulating film with a thickness of 110 through 130 nm.

At this point, the isolation 2b made of an oxide film is etched at higher selectivity than the silicon substrate 1 in the transistor region Refet, and hence, the isolation 2b is removed by a thickness of, for example, 10 through 30 nm. Therefore, in the conventional structure, the surface of the isolation 105a becomes lower than the surface of the silicon substrate 101 as is shown in Figures 21(a) and 21(b), resulting in causing the aforementioned problems. In contrast, in the state of this embodiment shown in Figure 13(d), the isolation 2b has the step portion whose surface is higher than the surface of the silicon substrate in the transistor region

Refet, resulting in effectively preventing the problems. In other words, even when the impurity ions are diagonally injected for the formation of the high-concentration source/drain region 8, the impurity ions are prevented from
5 being implanted below the edge of the isolation 2b because the step portion of the isolation 2b has a sufficient level difference. Accordingly, a distance between the high-concentration source/drain region 8 and the channel stop region 60 can be made substantially constant, thereby preventing the
10 degradation of the junction voltage resistance and the increase of the junction leakage. Furthermore, in the formation of the source/drain electrode 9c of silicide on the high-concentration source/drain region 8, the step sidewall 7c effectively prevents the silicide layer from being formed in the boundary
15 between the silicon substrate 1 and the isolation 2b. Therefore, it is possible to effectively prevent a short circuit current from occurring between the source/drain electrode 9c and the channel stop region 60.

In order to effectively achieve the aforementioned effects
20 in this embodiment, however, the level difference caused by the step portion is preferably larger than the amount of over-etch in the formation of the sidewalls, that is, 10 through 30 nm. Furthermore, in practical use, after the formation of the isolation 2b, other procedures are conducted in which the
25 thickness of the silicon oxide film used as the isolation 2b is decreased, such as a procedure for removing the silicon oxide

film 52. Therefore, it is preferred that the step portion is previously formed so as to have a sufficiently large level difference also in consideration of the afterward decreased amount. Accordingly, the lower limit of the thickness of the
5 silicon nitride film 53 deposited in the procedure shown in Figure 13(a) is determined on the basis of the amount of over-etch and the etched amount in the procedure for removing the silicon oxide film 52.

In this embodiment, the silicon nitride film 53 is used as
10 an etching mask for forming the trench 51. This film can be made of any material which has large etching selectivity against the silicon oxide film, and can be, for example, a polysilicon film or the like.

This embodiment exemplifies the so-called salicide
15 structure in which the upper gate electrode 9a and the source/drain electrode 9c are simultaneously silicified in a self-aligned manner for attaining low resistance. It goes without saying that the embodiment is applicable to a structure in which a gate electrode is previously formed as a polycide
20 electrode and a source/drain electrode alone is silicified afterward.

(Embodiment 9)

Embodiment 9 will now be described referring to Figures 14(a) through 14(e). This embodiment is different from
25 Embodiment 8 in that a gate oxide film and a polysilicon film serving as a gate electrode are deposited before forming a

trench isolation.

First, as is shown in Figure 14(a), a gate oxide film 3 and a polysilicon film 4 serving as a gate electrode of a MOS transistor are successively deposited on a silicon substrate 1. A resist film 50a for exposing an isolation region Reiso and masking a transistor region Refet is patterned. By using the resist film 50a as a mask, the polysilicon film 4 and the gate oxide film 3 are selectively removed, and further the silicon substrate 1 is etched, thereby forming a trench 51 serving as the isolation region. At this point, differently from the conventional method of forming a trench, the thickness of the polysilicon film 4 is set at 150 through 200 nm, that is, substantially the same thickness as that of the silicon nitride film used in Embodiment 8. The gate oxide film 3 has a thickness of 10 through 20 nm. The depth of the trench 51 is approximately 500 nm. Then, impurity ions of a different conductivity type from that of an impurity to be injected into a source/drain region formed afterward are injected, thereby forming a channel stop region 60.

Then, after removing the resist film 50a, a silicon oxide film 2 (not shown) is deposited so as to have a sufficient thickness larger than the sum of the depth of the trench 51 and the thickness of the remaining polysilicon film 4, namely, the height from the bottom of the trench 51 to the top surface of the polysilicon film 4. The silicon oxide film 2 is removed by the CMP method until the surface of the polysilicon film 4 is

exposed, thereby flattening the top surface of the substrate. Through this procedure, a trench isolation 2b made of the silicon oxide film is formed in the isolation region Reiso. The flattening method to be adopted is not limited to that described above but the surface can be flattened by etch-back using a resist film having a reverse pattern to the pattern of the transistor region Refet.

Next, as is shown in Figure 14(b), a conductive film 18 serving as a gate interconnection layer (which can be made of a conductive polysilicon film; a silicide film of WSi, TiSi or the like; or a metal with a high melting point such as W with a sandwiched barrier metal such as TiN for achieving low resistance) and a protection film 19 made of an insulating film are deposited on the flattened substrate. Then, a resist film 50b for exposing an area excluding the areas for a gate electrode and a gate interconnection is formed. By using the resist film 50b as a mask, dry etching is conducted, thereby forming a gate electrode 4a, an upper gate electrode 18a and a protection film 19a, a gate interconnection 4b, an upper gate interconnection 18b and a protection film 19b, which procedures are not shown in the drawing. At this point, a step portion having a sufficient level difference between the surfaces of the silicon substrate 1 in the transistor region Refet and the isolation 2b is exposed characteristically in this embodiment. The level difference is approximately 50 through 100 nm in consideration of the amount of over-etch in the subsequent

procedure for forming sidewalls and the like. However, in order to effectively achieve the effects of this embodiment, the thickness of an insulating film for the sidewall and the amount of over-etch are required to be appropriately determined
5 in the subsequent procedure for forming the sidewalls.

Then, as is shown in Figure 14(c), similarly to Embodiment 8, after forming a low-concentration source/drain region 6 on either side of the gate electrode 4a in the active area, an insulating film 7 (silicon oxide film) is deposited on the
10 entire top surface of the substrate.

Next, as is shown in Figure 14(d), the insulating film 7 is anisotropically etched, thereby forming electrode sidewalls 7a on both side surfaces of the gate electrode 4a and the like and interconnection sidewalls 7b on both side surfaces of the
15 gate interconnection 4b and the like. At the same time, a step sidewall 7c is formed on the side surface of the step portion between the silicon substrate 1 in the transistor region Refet and the isolation 2b. After forming these sidewalls, impurity ions are injected, thereby forming a high-concentration
20 source/drain region 8. Also at this point, the step portion between the silicon substrate 1 in the transistor region Refet and the isolation 2b has a sufficient level difference.

Next, as is shown in Figure 14(e), a source/drain electrode 9c is formed out of silicide only on the high-
25 concentration source/drain region 8.

Although the procedures thereafter are not shown in the

drawing, an interlayer insulating film 11 is deposited, a contact hole is formed, and the contact hole is filled with a metal (such as tungsten), and a first layer metallic interconnection 12 is formed. Thus, a MOS transistor having a trench isolation similar to that shown in Figure 12 is manufactured. In this embodiment, however, on the gate electrode 4a and the gate interconnection 4b are formed the upper gate electrode 18a and the upper gate interconnection 18b made of conductive polysilicon, silicide or the like as well as the protection films 19a and 19b made of the insulating film, respectively. The source/drain electrode 9c of silicide is formed in the procedure different from that for forming the upper gate electrode 18a and the upper gate interconnection 18b.

In this manner, the step portion which is higher at the side closer to the isolation 2b is formed between the silicon substrate1 in the transistor region Refet and the isolation 2b, and the step portion is provided with the step sidewall 7c on its side surface in this embodiment. Therefore, the same effects as those of Embodiment 8 can be exhibited with a reduced number of manufacturing procedures.

In addition, the procedure for forming the gate electrode 4a and the gate interconnection 4b after the procedure shown in Figure 14(b) can be conducted on the completely flat top surface of the substrate without being affected by the step portion at the edge of the isolation 2b in this embodiment.

Therefore, a refined pattern can be advantageously stably formed.

(Embodiment 10)

Embodiment 10 will now be described referring to Figures 15(a) through 15(f), which are sectional views for showing manufacturing procedures for a semiconductor device of this embodiment.

Before achieving the state shown in Figure 15(a), a trench isolation 2b, a channel stop region 60, a low-concentration source/drain region 6, a gate insulating film 3, a gate electrode 4a, a gate interconnection 4b and the like are formed through the same procedures as those described in Embodiment 8. Then, a protection oxide film 31, a silicon nitride film 32 for sidewalls and a polysilicon film 33 for a mask are deposited on the substrate by the CVD method. At this point, the thickness of a polysilicon film to be used as the gate electrode 4a and the gate interconnection 4b is 330 nm, and the minimum line width is 0.35 μm. The protection oxide film 31 has a thickness of approximately 20 nm, the silicon nitride film 32 has a thickness of approximately 30 nm, and the polysilicon film 33 has a thickness of approximately 100 nm.

Then, as is shown in Figure 15(b), the polysilicon film 33 is etched back by RIE (reactive ion etching), thereby forming electrode polysilicon masks 33a, interconnection polysilicon masks 33b and a step polysilicon mask 33c on side surfaces of the gate electrode 4a, the gate interconnection 4b and a step

portion of the isolation 2b, respectively. At this point, the etching selectivity between the polysilicon film 33 and the silicon nitride film 32 is large.

5 Next, as is shown in Figure 15(c), by using the remaining polysilicon masks 33a, 33b and 33c as masks, wet etching using heated phosphoric acid (H_3PO_4) at 150°C is conducted, so as to have portions of the silicon nitride film 32 covered with the polysilicon masks 33a, 33b and 33c remained and remove the other portions thereof. At this point, the etching selectivity
10 between the silicon nitride film 32 and the polysilicon masks 33a, 33b and 33c can be approximately 30:1. Through this procedure, electrode sidewalls 32a, interconnection sidewalls 32b and a step sidewall 32c each having an L-shape remain on the sides of the gate electrode 4a, the gate interconnection 4b
15 and the step portion, respectively.

Then, as is shown in Figure 15(d), by using the gate electrode 4a, the protection oxide film 31, the electrode polysilicon mask 33a, the electrode sidewall 32a, the step polysilicon mask 33c and the step sidewall 32c as masks,
20 impurity ions are injected at a high concentration into the active area of the silicon substrate 1, thereby forming a high-concentration source/drain region 8.

Then, as is shown in Figure 15(e), the polysilicon masks 33a, 33b and 33c are removed by dry or wet etching.

25 Next, as is shown in Figure 15(f), exposed portions of the protection oxide film 31 on the substrate are removed by using

a HF type etching solution. Then, a titanium film is deposited and a first RTA treatment is conducted, thereby forming a silicide layer of a $TiSi_2$ film through the reaction between titanium and silicon. The titanium film is then removed, and a second RTA treatment is conducted, so that an upper electrode 9a, an upper interconnection 9b and a source/drain electrode 9c each of a silicide layer with a low resistance are formed on the gate electrode 4a, the gate interconnection 4b and the source/drain region 8, respectively. Thereafter, an interlayer insulating film is deposited, the top surface of the substrate is flattened, a contact hole is formed, a metallic interconnection film is deposited, and a metallic interconnection is formed. Thus, an LSI is manufactured.

Since the protection oxide film 31 and the L-shaped step sidewall 32c are formed on the side surface of the step portion in the procedure shown in Figure 15(f) in this embodiment, the silicide layer is effectively prevented from being formed in the boundary between the active area of the silicon substrate 1 and the isolation 2b.

Furthermore, since the protection oxide film 31 is formed on the isolation 2b and the active area of the silicon substrate 1 in the procedures shown in Figures 15(c) and 15(d), the thickness of the isolation 2b is never decreased through the formation of the L-shaped sidewalls 32a, 32b and 32c. Accordingly, it is possible to decrease the level difference between the isolation 2b and the silicon substrate 1, resulting

in improving the patterning accuracy for the gate.

In the formation of the gate electrode, first and second conductive films can be used similarly to Embodiment 2. Also in this case, the same effects as those of this embodiment can be exhibited.

(Embodiment 11)

In each of the aforementioned embodiments, each sidewall is made of an insulating material such as a silicon oxide film and a silicon nitride film. The sidewall can be made of a conductive material such as a polysilicon film. Figure 16(a) through 16(e) are sectional views for showing manufacturing procedures for a semiconductor device including conductive sidewalls.

Before attaining the state shown in Figure 16(a), a trench isolation 2b, a channel stop region 60, a low-concentration source/drain region 6, a gate insulating film 3, a gate electrode 4a, a gate interconnection 4b and the like are formed through the same procedures as those described in Embodiment 8. Then, a protection oxide film 31 and a polysilicon film 34 for sidewalls are deposited on the top surface by the CVD method. In this embodiment, on the gate electrode 4a and the gate interconnection 4b are formed protection silicon oxide films 15a and 15b, respectively. At this point, a polysilicon film to be used as the gate electrode 4a and the gate interconnection 4b has a thickness of 330 nm, and the minimum line width is 0.35 μm. The protection oxide film 31 has a

thickness of approximately 20 nm and the polysilicon film 34 has a thickness of approximately 100 nm.

Next, as is shown in Figure 16(b), the polysilicon film 34 is etched back by the RIE, thereby forming electrode sidewalls 34a, interconnection sidewalls 34b and a step sidewall 34c each made of the polysilicon film on sides of the gate electrode 4a, the gate interconnection 4b and a step portion of the isolation 2b, respectively.

Next, as is shown in Figure 16(c), by using the gate electrode 4a, the protection oxide film 31, the electrode sidewalls 34a and the step sidewall 34c as masks, impurity ions are injected at a high concentration into an active area of the silicon substrate 1, thereby forming a high-concentration source/drain region 8.

Then, as is shown in Figure 16(d), exposed portions of the protection oxide film 31 on the substrate are removed by using the HF type etching solution. Then, as is shown in Figure 16(e), a titanium film is deposited and a first RTA treatment is conducted, thereby forming a silicide layer made of a $TiSi_2$ film through the reaction between titanium and silicon. The titanium film is then removed and a second RTA treatment is conducted, thereby forming a source/drain electrode 9d made of a silicide layer stretching over the electrode sidewall 34a, the high-concentration source/drain region 8 and the step sidewall 34c. Since the silicide layer is formed also on the interconnection sidewall 34b, this silicide layer can be

connected with the source/drain electrode. Therefore, in this embodiment, etching is conducted on the isolation 2b by using a resist film or the like, so as to selectively remove the interconnection sidewalls 34b on the sides of the gate
5 interconnection 4b as well as the silicide layer thereon. Thus, the source/drain electrodes 9d in the respective active areas are prevented from being mutually connected. It is possible to selectively remove merely the interconnection sidewalls 34b on the sides of the gate interconnection 4b
10 immediately after forming the sidewalls 34a, 34b and 34c of the polysilicon film.

Thereafter, an interlayer insulating film is deposited, the top surface of the substrate is flattened, a contact hole is formed, a metallic interconnection film is deposited, and a
15 metallic interconnection is formed. Thus, an LSI is manufactured.

In this embodiment, the source/drain electrode 9d is ultimately formed so as to stretch over a large area including the electrode sidewall 34a, the high-concentration source/drain
20 region 8 and the step sidewall 34c. Accordingly, the level difference between the transistor region Refet and the isolation 2b can effectively prevent the high-concentration source/drain region 8 from being brought close to the channel stop region 60 in the impurity ion injection. Furthermore, in
25 the formation of the source/drain electrode 9d of silicide on the high-concentration source/drain region 8, also the step

sidewall 34c is silicified by a certain thickness. However, since the silicide layer is prevented from being formed in a further thickness, a short circuit current between the source/drain electrode 9d and the channel stop region 60 is
5 effectively prevented from being caused by the formation of the silicide layer in the interface between the isolation and the silicon substrate. Moreover, since the large area stretching over the electrode sidewall 34a, the high-concentration source/drain region 8 and the step sidewall 34c is silicified
10 in this embodiment, it is very easy to form a contact member to be connected with an upper first layer interconnection. As a result, the area of the transistor region Refet can be decreased, namely, the integration of the semiconductor device can be advantageously improved. Although the electrode
15 sidewalls 34a and the interconnection sidewalls 34b are made of a conductive polysilicon film, there is no possibility of a short circuit between the sidewall and the gate because the respective sidewalls 34a and 34b are insulated from the gate electrode 4a and the gate interconnection 4b by the protection
20 oxide film 31.

In the formation of the gate electrode, first and second conductive films can be used similarly to Embodiment 9, and also in this case, the same effects as those of this embodiment can be attained.

25 The sidewalls are made of a polysilicon film in this embodiment, and the polysilicon film can be replaced with an

amorphous silicon film. Furthermore, the sidewalls can be made not only of a silicon film but also of another conductive material such as a metal, and it is not necessarily required to silicify the sidewalls.

5 In each of the aforementioned embodiments, the description is made on the case where the semiconductor element formed in the active area is a field effect transistor. However, the invention is not limited to these embodiments, and is applicable when the semiconductor element is a bipolar 10 transistor and the active area is an emitter diffused layer, a collector diffused layer or a base diffused layer of the bipolar transistor.

In each embodiment, setting of an angle of the side surface of the step portion to be equal to or more than 70° 15 ensures a large level difference between the active area and the side surface of the step portion around the boundary of the active area, thereby preventing formation of a deep recess on the isolation.

WHAT IS CLAIMED IS:

1. A semiconductor device in which a semiconductor element is disposed in each of plural active areas in a semiconductor substrate comprising:

5 an isolation for surrounding and isolating each active area, the isolation having a top surface at a higher level than a surface of the active area and having a step portion in a boundary with the active area;

an insulating film formed so as to stretch over each 10 active area and the isolation;

plural holes each formed by removing a portion of the insulating film disposed at least on the active area;

plural buried conductive layers filled in the respective holes; and

15 plural interconnection members formed on the insulating film so as to be connected with the respective active areas through the respective buried conductive layers.

2. The semiconductor device of Claim 1,

wherein at least a part of the plural holes are formed by 20 also removing another portion of the insulating film disposed on the isolation due to fluctuation in manufacturing procedures.

3. The semiconductor device of Claim 1,

wherein dimensions and materials of respective components 25 are determined so as to satisfy the following inequality:

$OE \times a \times (ER2 / ER1) \leq b + D \times (2 / 10)$

wherein "a" indicates a thickness of the insulating film, "b" indicates a level difference between the surface of the active area and the top surface of the isolation, "ER1" indicates an etching rate of the insulating film in forming the holes, "ER2" indicates an etching rate of the isolation in forming the holes, "D" indicates a depth of an impurity diffused layer in the active area, and "OE" indicates an over-etch ratio of the insulating film in forming the holes.

4. The semiconductor device of Claim 1,

wherein an angle between a side surface of the step portion and the surface of the active area is 70 degrees or more.

5. The semiconductor device of Claim 1,

wherein the isolation is a trench isolation made of an insulating material filled in a trench formed by trenching the semiconductor substrate by a predetermined depth.

6. The semiconductor device of Claim 1,

wherein the semiconductor element is a MISFET including:

a gate insulating film and a gate electrode formed on the active area; and

source/drain regions formed in the active area on both sides of the gate electrode.

7. The semiconductor device of Claim 6 further comprising a gate interconnection made of a material the same as a material for the gate electrode and formed on the isolation,

wherein each of the holes is formed on an area including

the source/drain region, the isolation and the gate interconnection, and

the plural interconnection members are connected with the gate interconnection on the isolation.

5 8. The semiconductor device of Claim 6 further comprising:

electrode sidewalls made of an insulating material and formed on both side surfaces of the gate electrode; and

a step sidewall made of a material the same as the insulating material for the electrode sidewalls and formed on

10 a side surface of the step portion,

wherein at least a part of the holes are formed by also removing a portion of the insulating film disposed on the step sidewall.

9. The semiconductor device of Claim 6 further comprising

15 a gate protection film formed on the gate electrode,

wherein at least a part of the holes are formed so as to stretch over the source/drain region and at least a part of the gate protection film.

10. The semiconductor device of Claim 9,

20 wherein dimensions and materials of respective components are determined so as to satisfy the following inequality:

$OE \times a \times (ER3 / ER1) < c$

wherein "a" indicates a thickness of the insulating film, "c" indicates a thickness of the gate protection film, "ER1"

25 indicates an etching rate of the insulating film in forming the holes, "ER3" indicates an etching rate of the gate protection

film in forming the holes, and "OE" indicates an over-etch ratio of the insulating film in forming the holes.

11. The semiconductor device of Claim 6,

wherein the interconnection members are local
5 interconnections.

12. The semiconductor device of Claim 6,

wherein the interconnection members are first layer metallic interconnections, and

the insulating film is an interlayer insulating film
10 disposed between the semiconductor substrate and the first layer metallic interconnections.

13. The semiconductor device of Claim 12 further comprising, between the interlayer insulating film and the semiconductor substrate, an underlying film made of an
15 insulating material having high etching selectivity against the interlayer insulating film.

14. A semiconductor device in which a semiconductor element is disposed in each of plural active areas in a semiconductor substrate comprising:

20 a trench isolation for isolating and surrounding each active area, the trench isolation having a top surface at a higher level than a surface of the active area and having a step portion in a boundary with the active area; and

a step sidewall formed on a side surface of the step
25 portion of the trench isolation.

15. The semiconductor device of Claim 14,

wherein the step sidewall is made of an insulating material.

16. The semiconductor device of Claim 14,

wherein the semiconductor element is a MISFET including:

5 a gate insulating film and a gate electrode formed on the active area; and

source/drain regions formed in the active area on both sides of the gate electrode,

the semiconductor device is further provided with 10 electrode sidewalls formed on both side surfaces of the gate electrode, and

the step sidewall is formed simultaneously with the electrode sidewalls.

17. The semiconductor device of Claim 16 further 15 comprising an electrode formed by silicifying at least a portion in the vicinity of the surface of the active area.

18. A method of manufacturing a semiconductor device in which a semiconductor element is disposed in each of plural active areas in a semiconductor substrate comprising:

20 a first step of forming an isolation in a part of the semiconductor substrate, the isolation having a top surface at a higher level than a surface of the semiconductor substrate and having a step portion in a boundary with the surface of the semiconductor substrate;

25 a second step of introducing an impurity at a high concentration into each active area of the semiconductor

substrate surrounded by the isolation;

a third step of forming an insulating film on the active area and the isolation;

a fourth step of forming, on the insulating film, a masking member having an exposing area above an area at least including a portion of the active area where the impurity at the high concentration is introduced;

a fifth step of conducting etching by using the masking member so as to selectively remove the insulating film and form holes; and

a sixth step of forming a buried conductive layer by filling the holes with a conductive material and forming, on the insulating film, interconnection members to be connected with the buried conductive layer,

wherein, in the fourth step, an alignment margin is not provided for preventing the exposing area of the masking member from including a portion above the isolation when mask shift is caused in photolithography.

19. The method of manufacturing a semiconductor device of Claim 18,

wherein, the fifth step is performed so as to satisfy the following inequality:

$$OE \times a \times (ER2 / ER1) \leq b + D \times (2 / 10)$$

wherein "a" indicates a thickness of the insulating film, "b" indicates a level difference between the surface of the active area and the top surface of the isolation, "ER1" indicates an

etching rate of the insulating film, "ER2" indicates an etching rate of the isolation, "D" indicates a depth of an impurity diffused layer in the active area, and "OE" indicates an over-etch ratio of the insulating film.

5 20. The method of manufacturing a semiconductor device of Claim 18,

wherein, in the fourth step, the masking member is formed to be positioned with the exposing area thereof including a portion above the isolation when the mask shift is not caused

10 in the photolithography.

21. The method of manufacturing a semiconductor device of Claim 18,

wherein, in the first step, a trench isolation is formed.

22. The method of manufacturing a semiconductor device of

15 Claim 18,

wherein the semiconductor element is a MISFET,

the method further includes, before the second step, a step of forming a gate insulating film on the active area, a step of depositing a conductive film on the gate insulating

20 film and a step of forming a gate electrode by patterning the conducive film, and

in the second step, the impurity at the high concentration is introduced so as to form a source/drain region.

23. The method of manufacturing a semiconductor device of

25 Claim 22,

wherein, in the step of forming the gate electrode, a gate

interconnection is simultaneously formed so as to stretch over the conductive film and the isolation, and

in the fourth step, the masking member is formed so that the exposing area thereof includes portions above the source/drain region and above the gate interconnection.

24. The method of manufacturing a semiconductor device of Claim 22 further comprising, after the step of forming the gate electrode, a step of depositing an insulating film for sidewalls on the gate electrode, the active area and the isolation, and anisotropically etching the insulating film for the sidewalls, so as to form electrode sidewalls on both side surfaces of the gate electrode and form a step sidewall on a side surface of the step portion in the boundary between the isolation and the active area.

25. The method of manufacturing a semiconductor device of Claim 24 further comprising, after the step of depositing the conductive film, a step of depositing a protection insulating film on the conductive film,

wherein, in the step of forming the gate electrode, the conductive film as well as the protection insulating film are patterned, so as to form a gate protection film on the gate electrode, and

the fifth step is performed so as to satisfy the following inequality:

$$OE \times a \times (ER3 / ER1) < c$$

wherein "a" indicates a thickness of the insulating film, "c"

indicates a thickness of the gate protection film, "ER1" indicates an etching rate of the insulating film, "ER3" indicates an etching rate of the gate protection film and "OE" indicates an over-etch ratio of the insulating film.

5 26. The method of manufacturing a semiconductor device of Claim 25,

wherein, in the fourth step, the masking member is formed to be positioned without providing a margin for preventing the exposing area thereof from including a portion above the gate 10 protection film even when the mask shift is caused in the photolithography.

27. The method of manufacturing a semiconductor device of Claim 25,

wherein, in the fourth step, the masking member is formed 15 to be positioned with the exposing area thereof including at least a part of a portion above the gate protection film when the mask shift is not caused in the photolithography.

28. The method of manufacturing a semiconductor device of Claim 22,

20 wherein, in the sixth step, local interconnections are formed as the interconnection members.

29. The method of manufacturing a semiconductor device of Claim 22,

wherein, in the third step, an interlayer insulating film 25 is formed as the insulating film, and

in the sixth step, first layer metallic interconnections

are formed as the interconnection members.

30. The method of manufacturing a semiconductor device of Claim 29,

wherein, in the third step, after an underlying film made
5 of an insulating material having high etching selectivity against the interlayer insulating film is formed below the interlayer insulating film, the interlayer insulating film is formed.

31. A method of manufacturing a semiconductor device
10 comprising:

a first step of forming an underlying insulating film on a semiconductor substrate;

a second step of depositing an etching stopper film on the underlying insulating film;

15 a third step of forming a trench by exposing a portion of the etching stopper film and the underlying insulating film where an isolation is to be formed and etching the semiconductor substrate in the exposed portion;

a fourth step of depositing an insulating film for
20 isolation on an entire top surface of the substrate, flattening the substrate until at least a surface of the etching stopper film is exposed, and forming a trench isolation in the trench so as to surround a transistor region;

a fifth step of removing, by etching, at least the etching
25 stopper film and the underlying insulating film, so as to expose a step portion between the transistor region and the

trench isolation;

a sixth step of depositing a gate oxide film and a conductive film on the substrate and making the conductive film into a pattern of at least a gate electrode;

5 a seventh step of depositing an insulating film for sidewalls on the entire top surface of the substrate and anisotropically etching the insulating film for the sidewalls, so as to form electrode sidewalls and a step sidewall on side surfaces of the gate electrode and the step portion,

10 respectively; and

an eighth step of introducing an impurity into the semiconductor substrate in the transistor region on both sides of the gate electrode, so as to form source/drain regions.

32. The method of manufacturing a semiconductor device of

15 Claim 31,

wherein, in the second step, a thickness of the etching stopper film is determined in consideration of an amount of over-etch in the seventh step, so that the step portion having a level difference with a predetermined size or more is exposed

20 in the fifth step.

33. The method of manufacturing a semiconductor device of Claim 31 further comprising, after completing the eighth step, a step of silicifying at least an area in the vicinity of the surface of the source/drain region.

25 34. The method of manufacturing a semiconductor device of Claim 31,

wherein, in the sixth step, a first protection insulating film is deposited on the conductive film, and the first protection insulating film as well as the gate electrode are made into the pattern,

5 the method further includes, after the sixth step and before the seventh step, a step of depositing a second protection insulating film on the entire top surface of the substrate,

in the seventh step, a silicon film is deposited as the

10 insulating film for the sidewalls, and

the method further includes, after the eighth step, a step of silicifying an area stretching over the electrode sidewall, the active area and the step sidewall.

35. A method of manufacturing a semiconductor device

15 comprising:

a first step of forming a gate insulating film on a semiconductor substrate;

a second step of depositing a first conductive film to be formed into a gate electrode on the gate insulating film;

20 a third step of forming a trench by exposing a portion of the first conductive film where a trench isolation is to be formed and etching the semiconductor substrate in the exposed portion;

a fourth step of depositing an insulating film for

25 isolation on an entire top surface of the substrate, flattening the substrate at least until a surface of the first conductive

film is exposed, and forming the trench isolation in the trench so as to surround a transistor region;

a fifth step of depositing a second conductive film to be formed into at least an upper gate electrode on the entire top surface of the flattened substrate;

a sixth step of making the first and second conductive films into a pattern at least of the gate electrode and exposing a step portion between the transistor region and the trench isolation;

a seventh step of depositing an insulating film for sidewalls on the entire top surface of the substrate and anisotropically etching the insulating film for the sidewalls, so as to form electrode sidewalls and a step sidewall on side surfaces of the gate electrode and the step portion, respectively; and

an eighth step of introducing an impurity into the semiconductor substrate in the transistor region on both sides of the gate electrode, so as to form source/drain regions.

36. The method of manufacturing a semiconductor device of Claim 35,

wherein, in the second step, a thickness of the first conductive film is determined in consideration of at least an amount of over-etch in the seventh step, so that the step portion having a level difference with a predetermined size or more is exposed in the sixth step.

37. The method of manufacturing a semiconductor device of

Claim 35 further comprising, after completing the eighth step, a step of silicifying at least a portion in the vicinity of the surface of the active area.

38. The method of manufacturing a semiconductor device of Claim 35,

wherein, in the sixth step, a first protection insulating film is deposited on the conductive film and the first protection insulating film as well as the gate electrode are made into the pattern,

the method further includes, after the sixth step and before the seventh step, a step of depositing a second protection insulating film on the entire top surface of the substrate,

in the seventh step, a silicon film is deposited as the insulating film for the sidewalls, and

the method further includes, after the eighth step, a step of silicifying an area stretching over the electrode sidewall, the source/drain region and the step sidewall.

ABSTRACT OF THE DISCLOSURE

An isolation which is higher in a stepwise manner than an active area of a silicon substrate is formed. On the active area, an FET including a gate oxide film, a gate electrode, a gate protection film, sidewalls and the like is formed. An insulating film is deposited on the entire top surface of the substrate, and a resist film for exposing an area stretching over the active area, a part of the isolation and the gate protection film is formed on the insulating film. There is no need to provide an alignment margin for avoiding interference with the isolation and the like to a region where a connection hole is formed. Since the isolation is higher in a stepwise manner than the active area, the isolation is prevented from being removed by over-etch in the formation of a connection hole to come in contact with a portion where an impurity concentration is low in the active area. In this manner, the integration of a semiconductor device can be improved and an area occupied by the semiconductor device can be decreased without causing degradation of junction voltage resistance and increase of a junction leakage current in the semiconductor device.

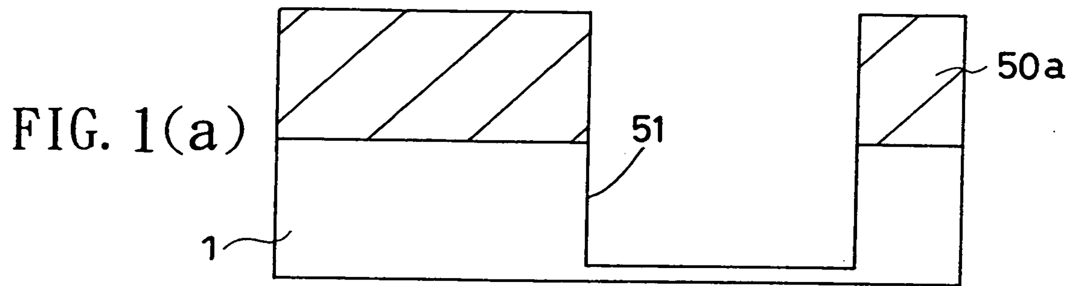


FIG. 1(a)

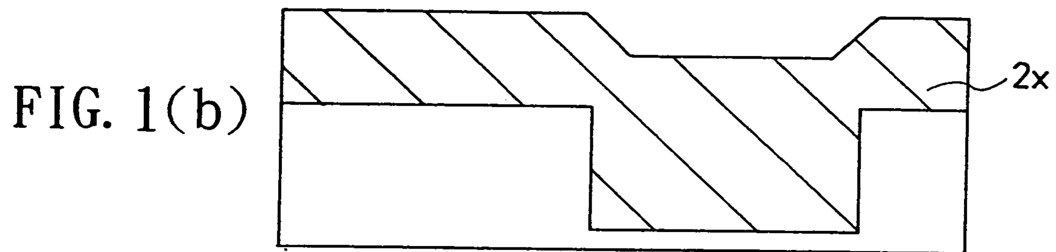


FIG. 1(b)

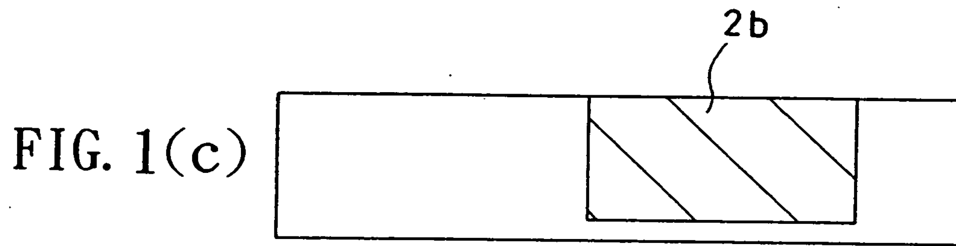


FIG. 1(c)

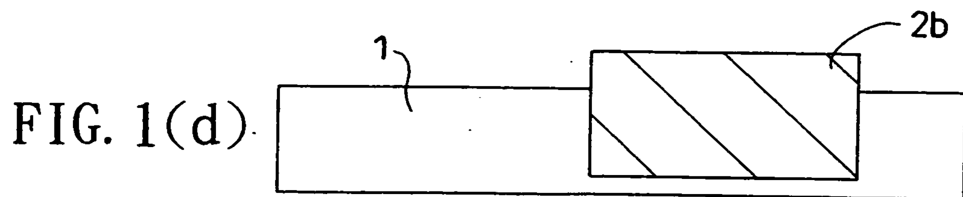


FIG. 1(d)

FIG. 2(a)

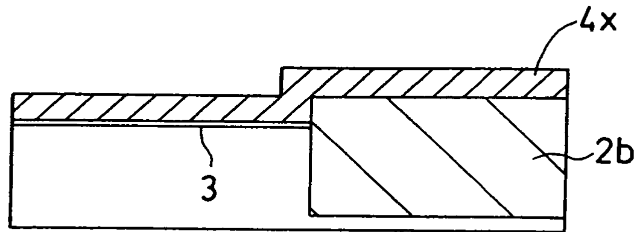


FIG. 2(b)

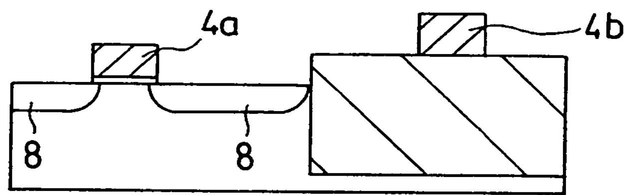


FIG. 2(c)

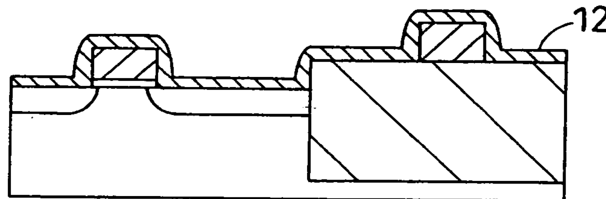


FIG. 2(d)

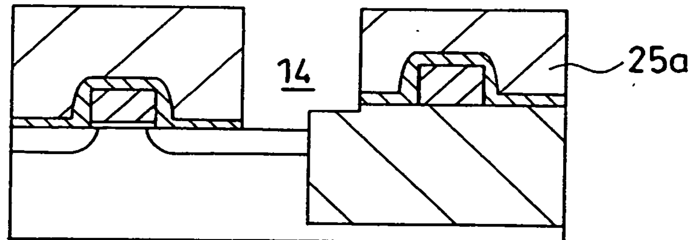
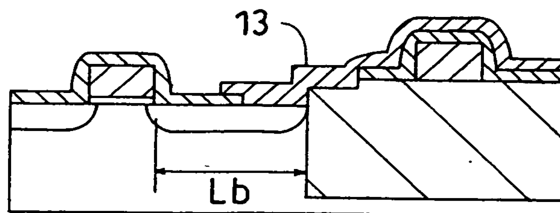


FIG. 2(e)



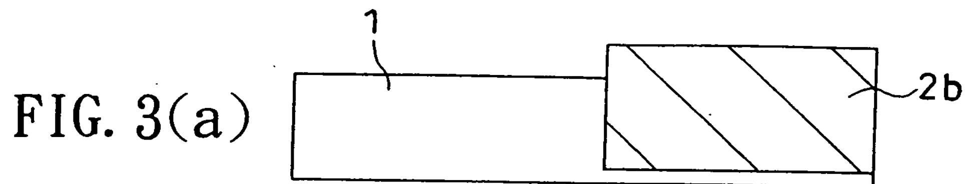


FIG. 3(a)

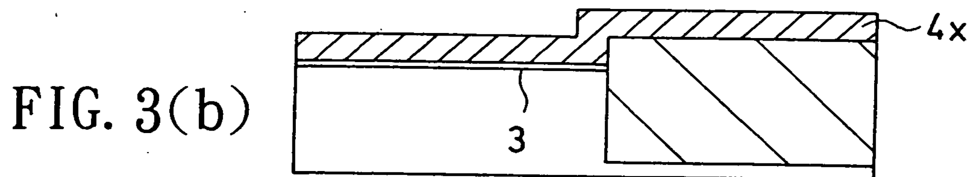


FIG. 3(b)

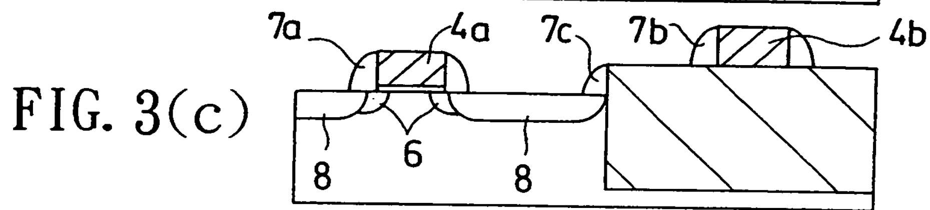


FIG. 3(c)

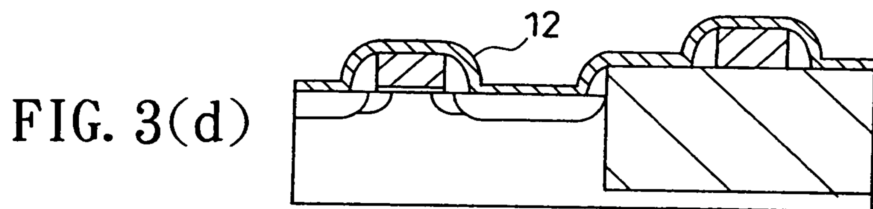


FIG. 3(d)

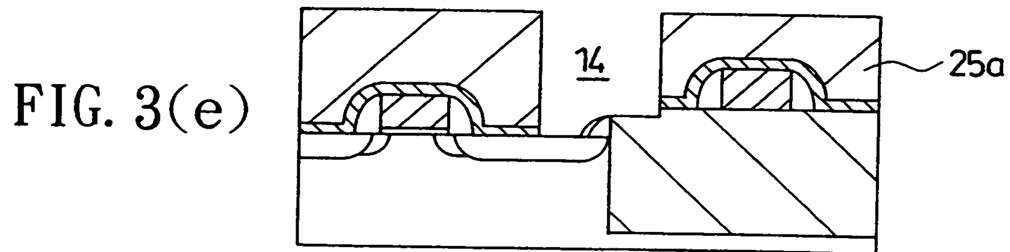


FIG. 3(e)

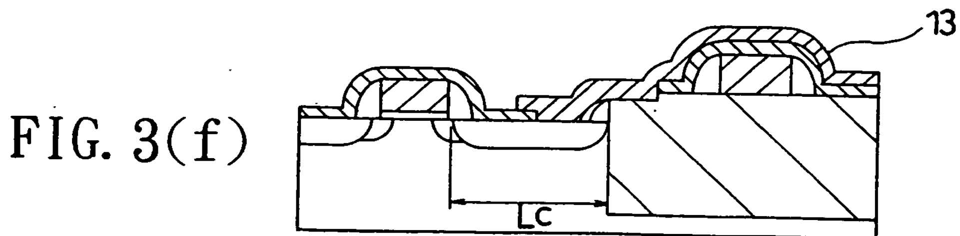


FIG. 3(f)

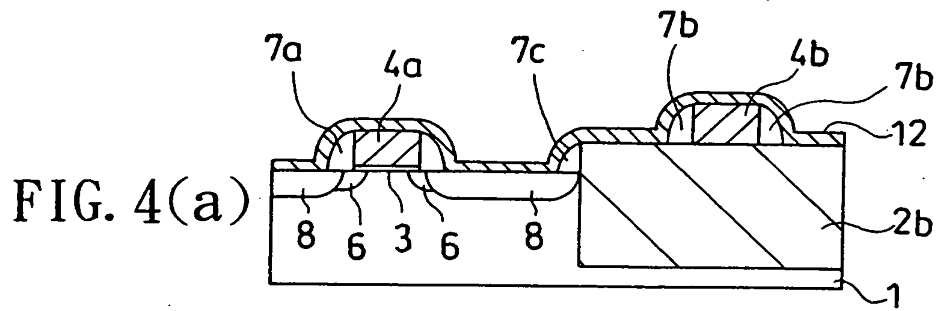


FIG. 4(a)

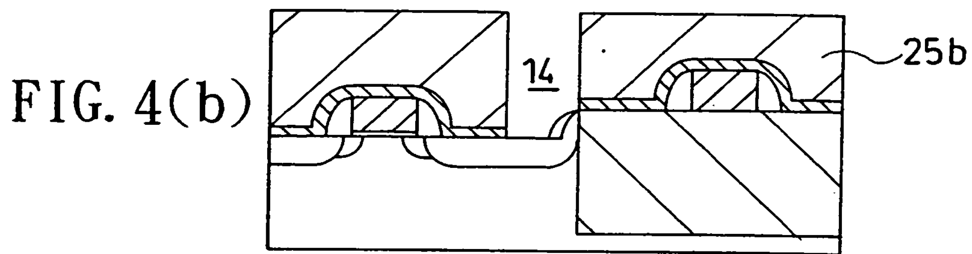


FIG. 4(b)

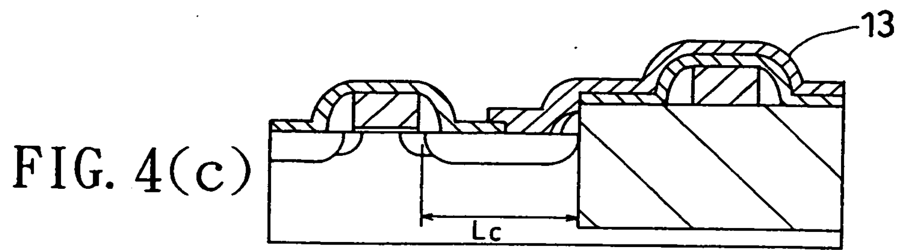


FIG. 4(c)

FIG. 5(a)

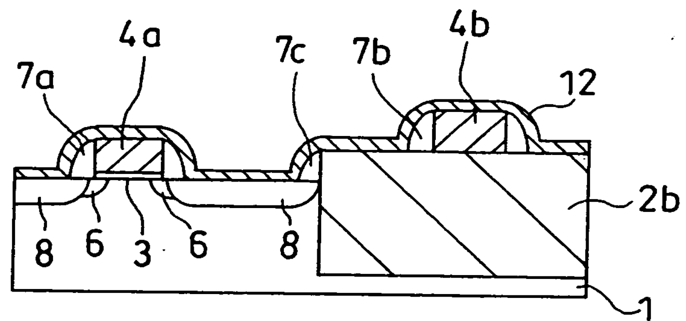


FIG. 5(b)

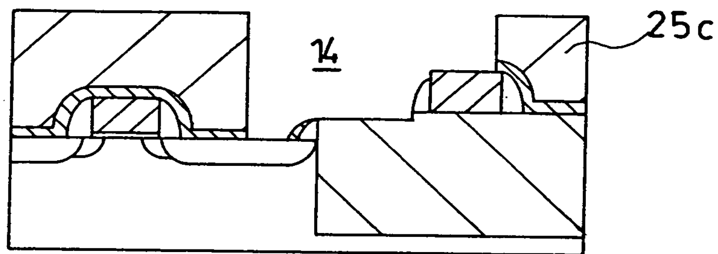
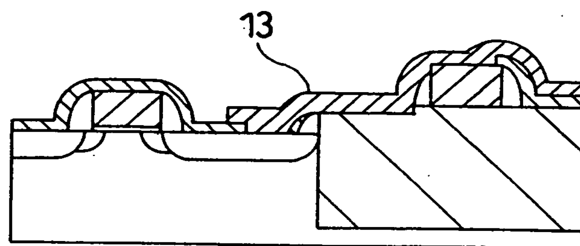


FIG. 5(c)



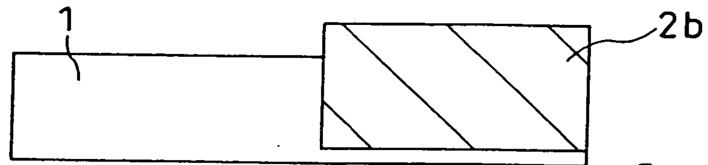


FIG. 6(a)

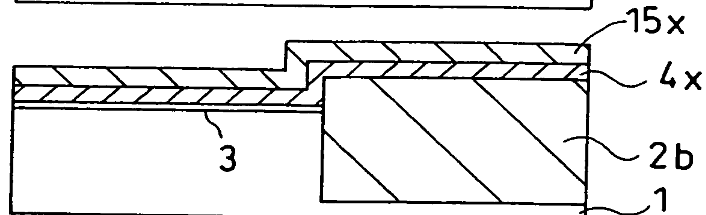


FIG. 6(b)

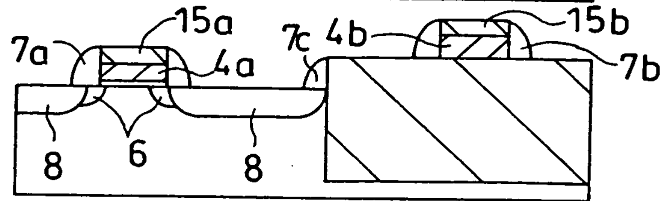


FIG. 6(c)

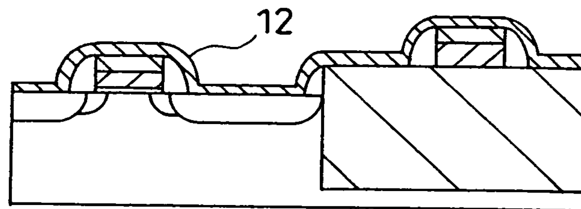


FIG. 6(d)

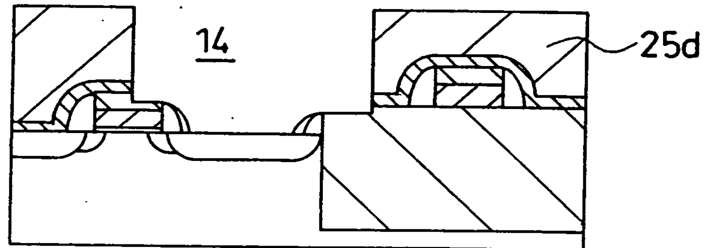


FIG. 6(e)

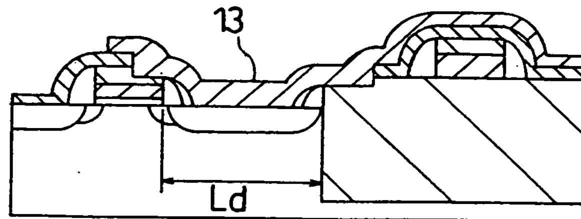


FIG. 6(F)

FIG. 7(a)

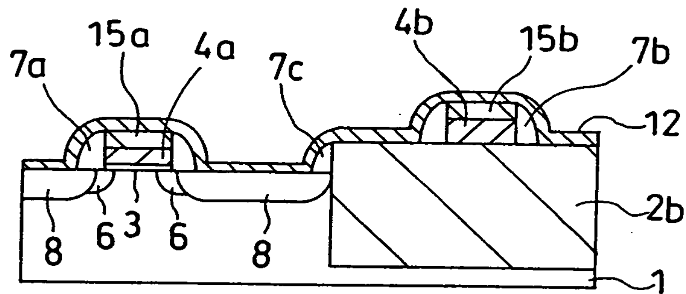


FIG. 7(b)

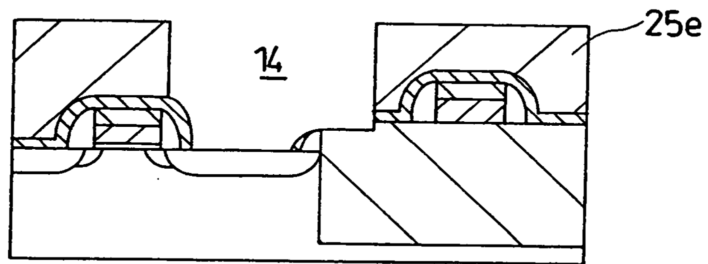


FIG. 7(c)

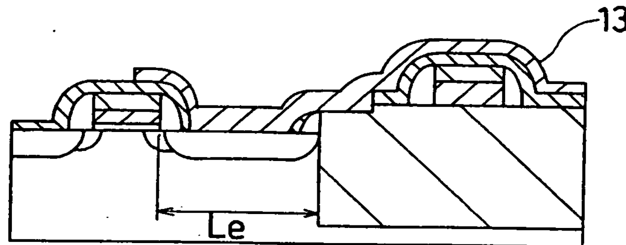


FIG. 8(a)

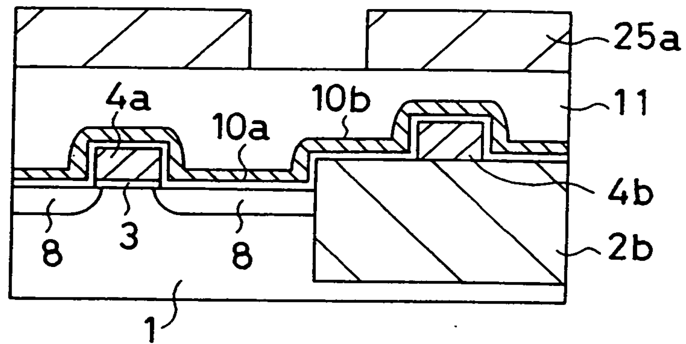


FIG. 8(b)

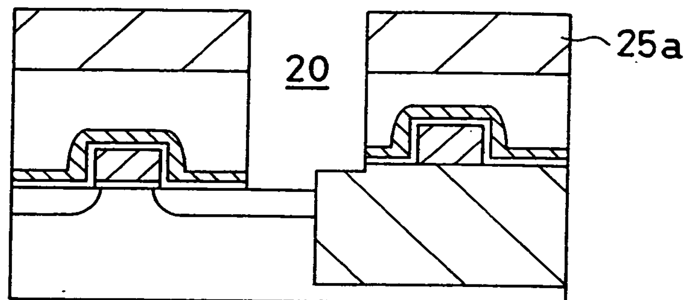


FIG. 8(c)

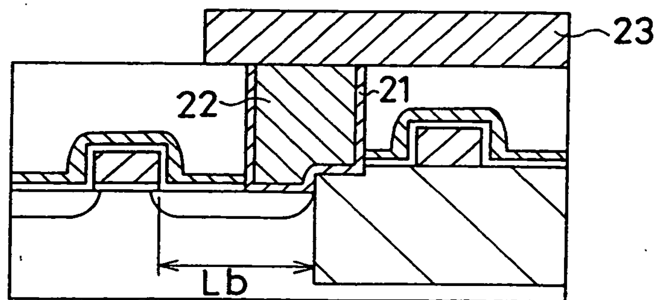


FIG. 9(a)

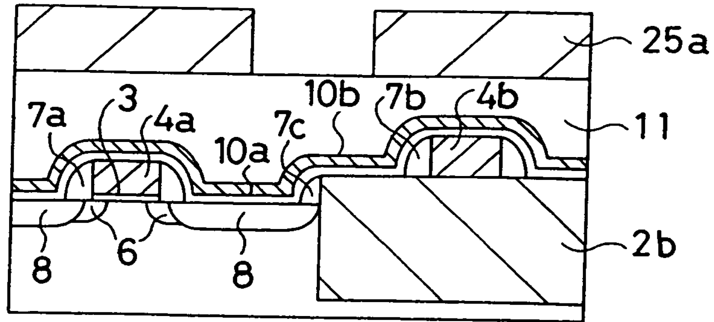


FIG. 9(b)

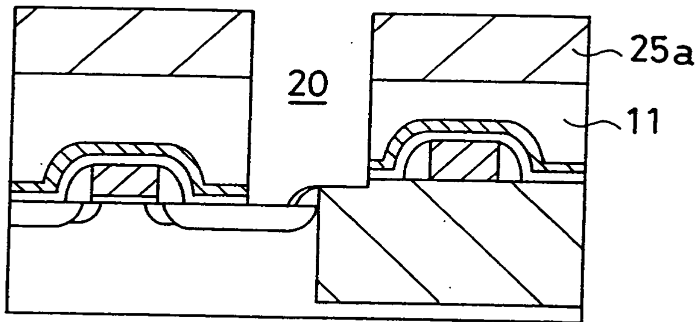


FIG. 9(c)

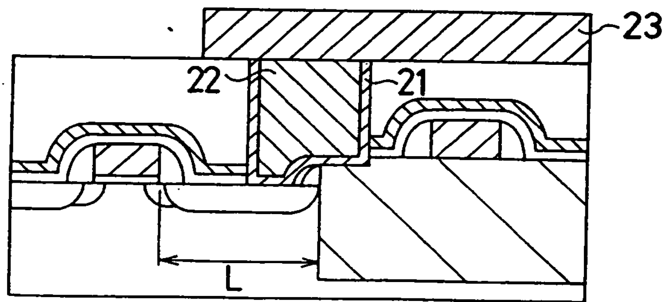


FIG. 10(a)

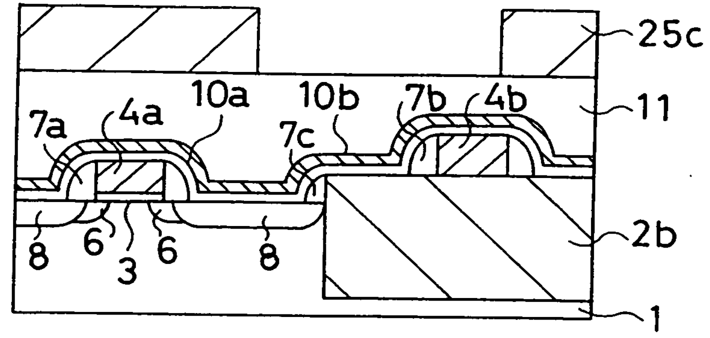


FIG. 10(b)

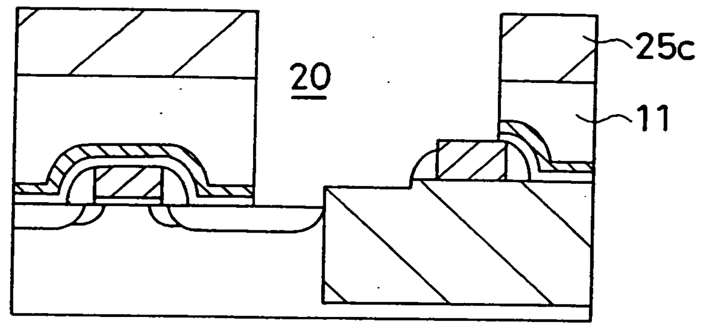


FIG. 10(c)

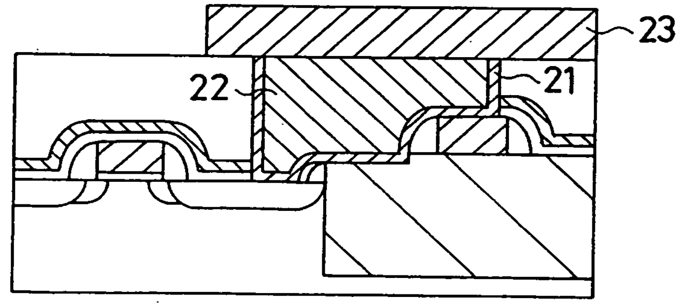


FIG. 11(a)

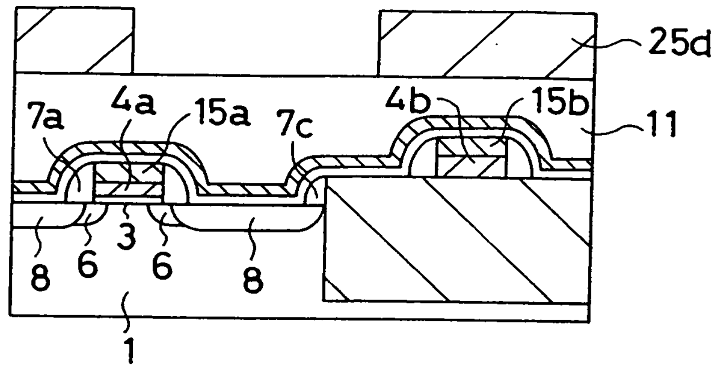


FIG. 11(b)

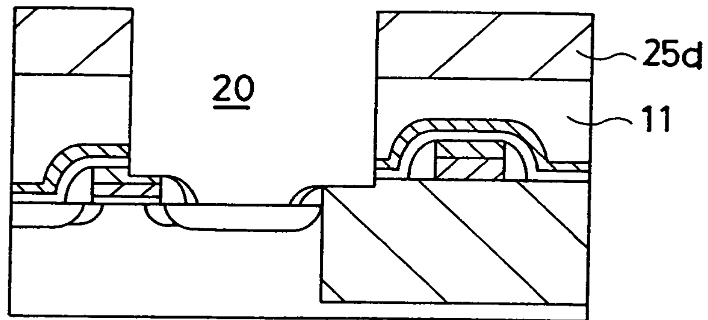


FIG. 11(c)

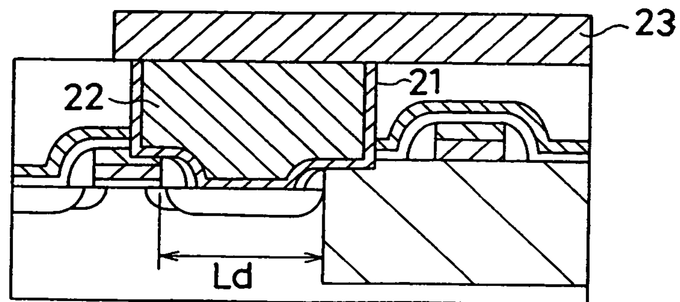
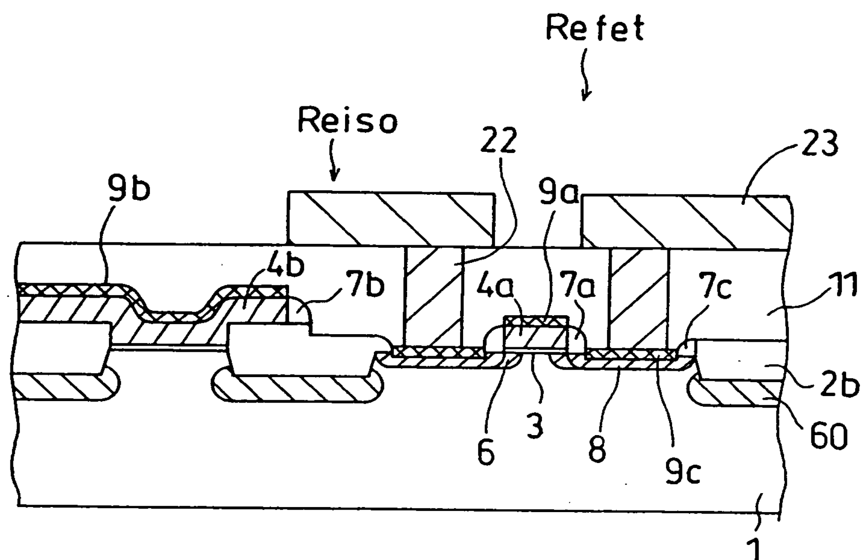


FIG. 12



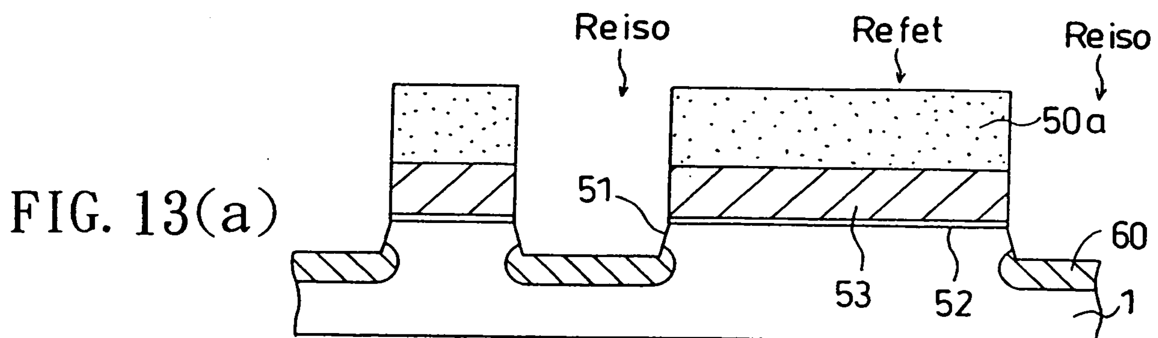


FIG. 13(a)

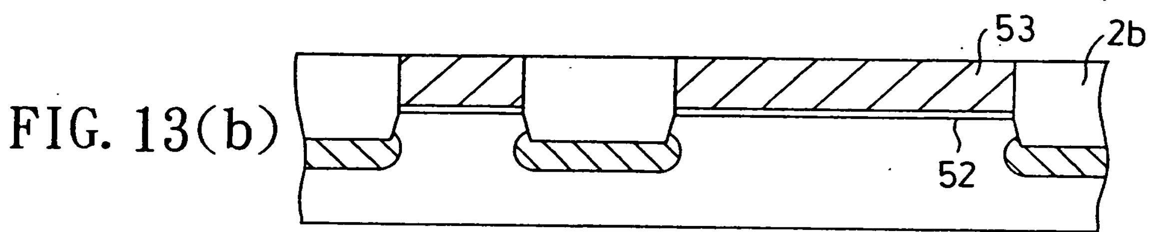


FIG. 13(b)

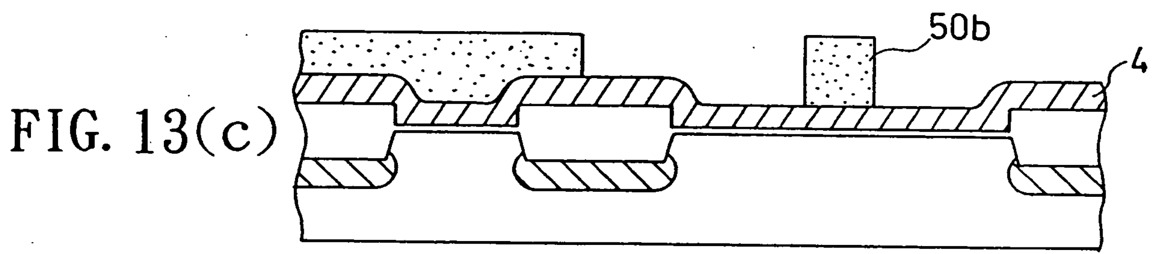


FIG. 13(c)

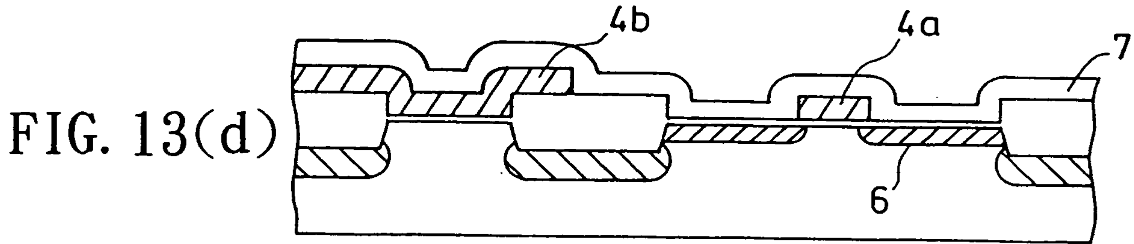


FIG. 13(d)

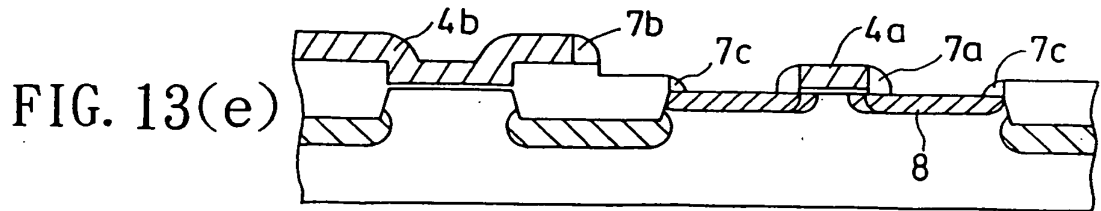


FIG. 13(e)

FIG. 14(a)

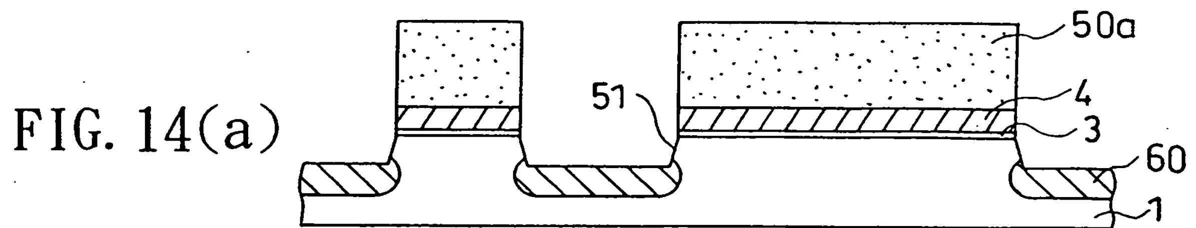


FIG. 14(b)

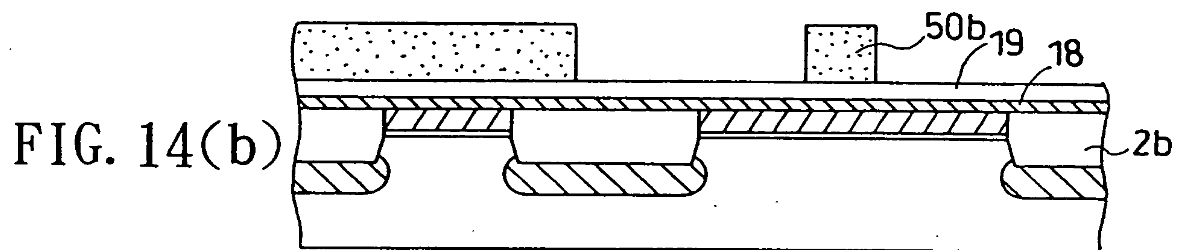


FIG. 14(c)

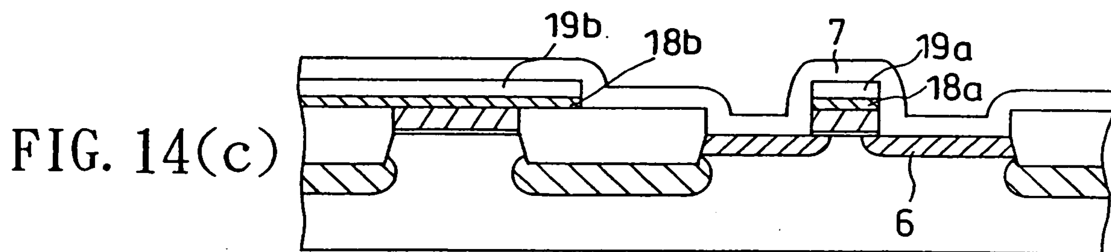


FIG. 14(d)

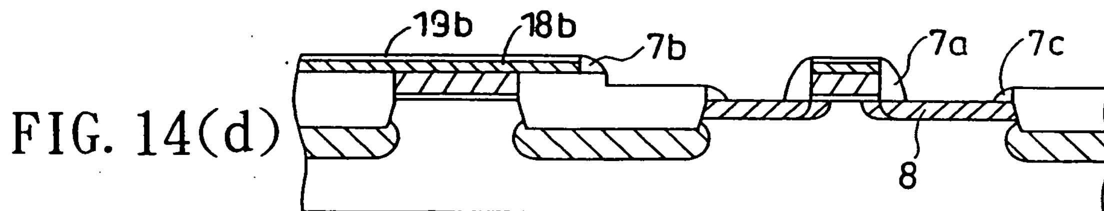
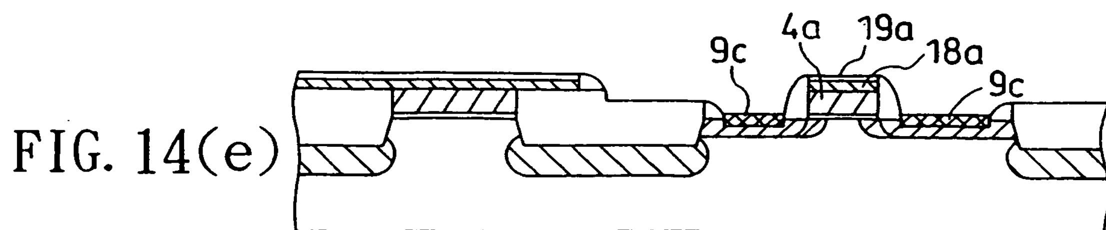


FIG. 14(e)



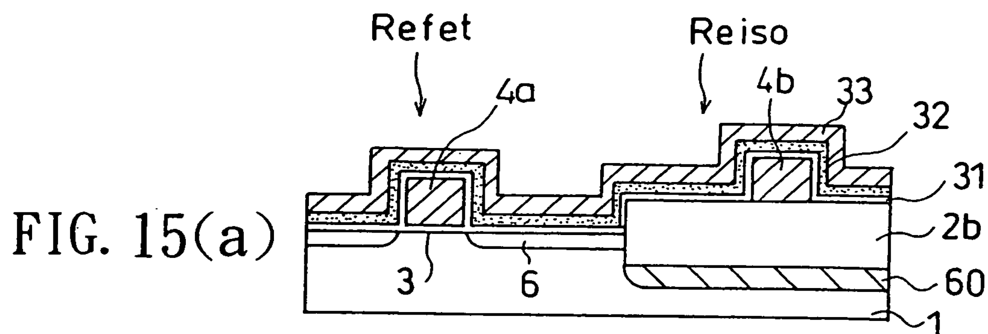


FIG. 15(a)

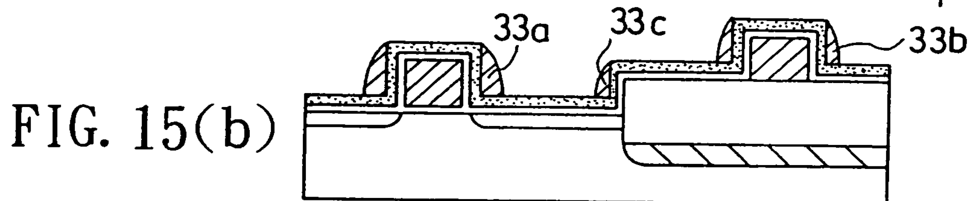


FIG. 15(b)

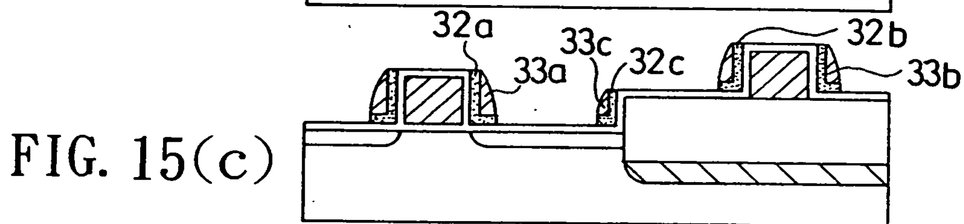


FIG. 15(c)

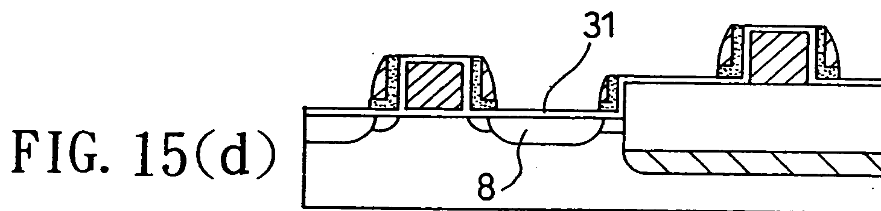


FIG. 15(d)

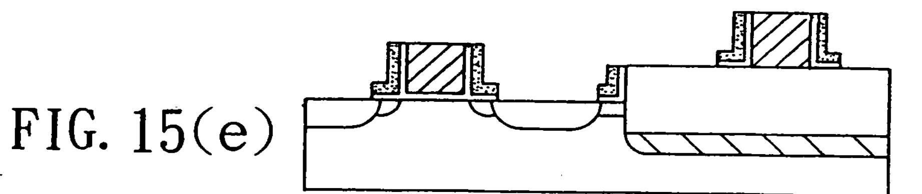


FIG. 15(e)

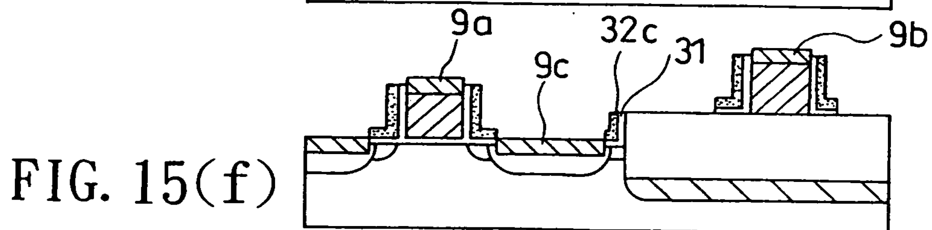


FIG. 15(f)

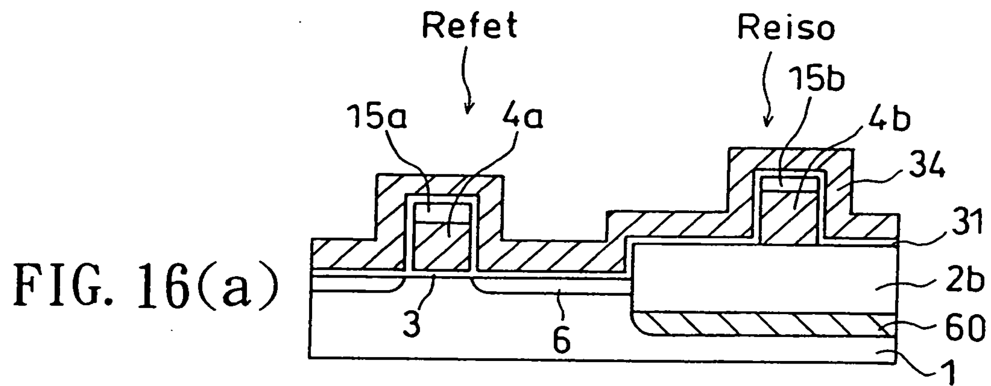


FIG. 16(a)

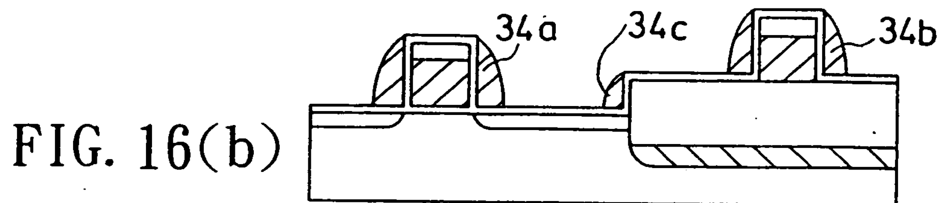


FIG. 16(b)

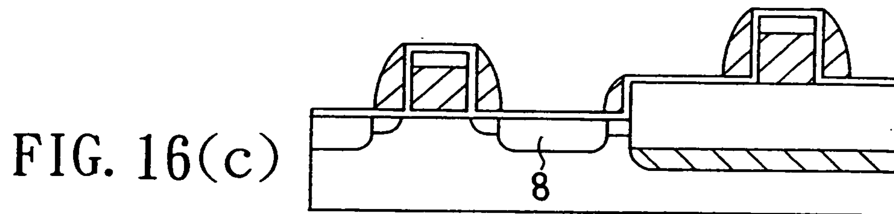


FIG. 16(c)

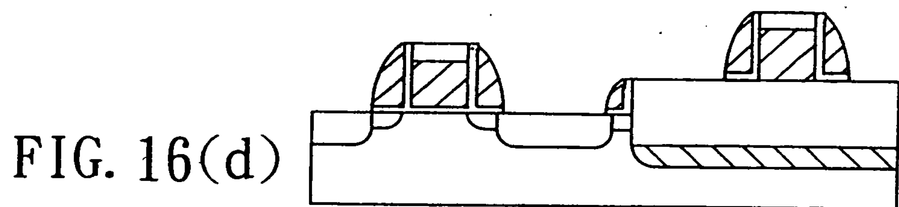


FIG. 16(d)

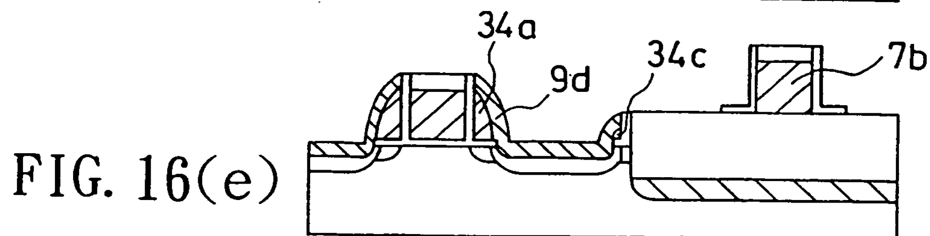


FIG. 16(e)

FIG. 17
PRIOR ART

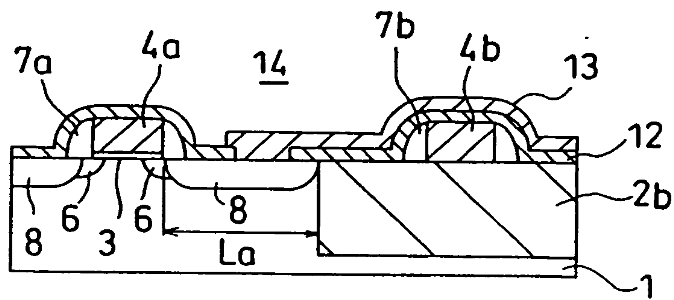


FIG. 18(a)
PRIOR ART

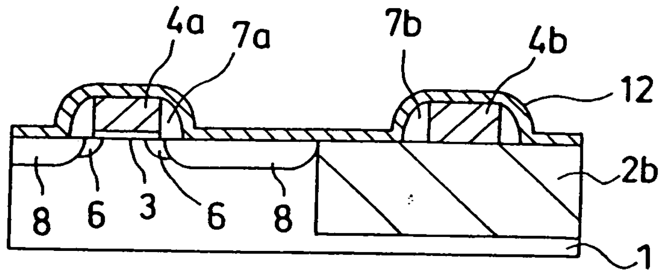


FIG. 18(b)
PRIOR ART

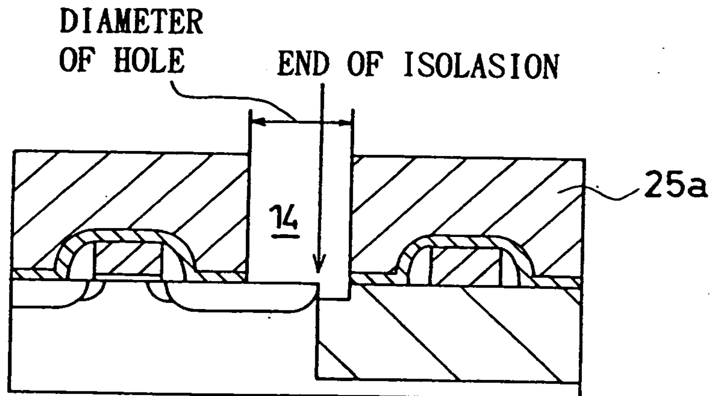


FIG. 18(c)
PRIOR ART

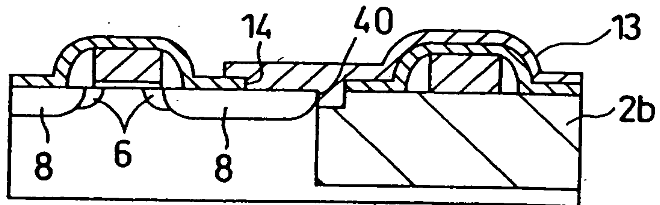
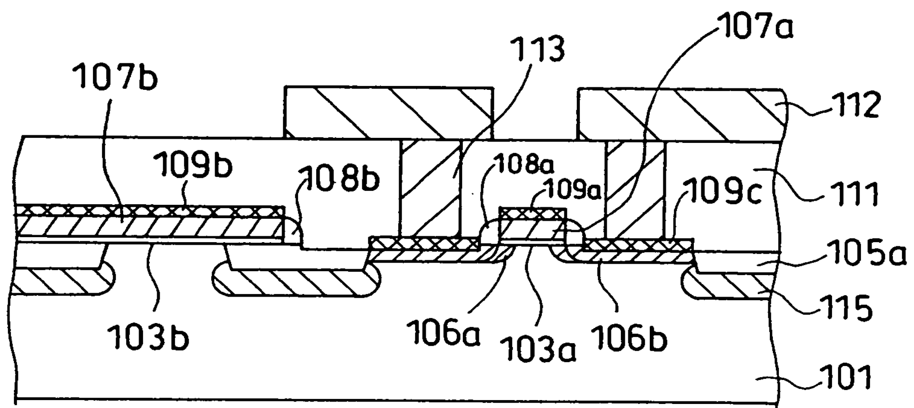


FIG. 19
PRIOR ART



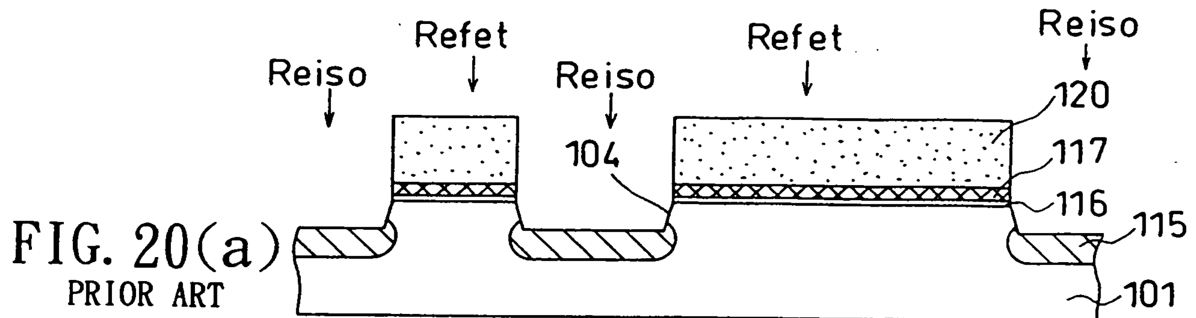


FIG. 20(a)
PRIOR ART

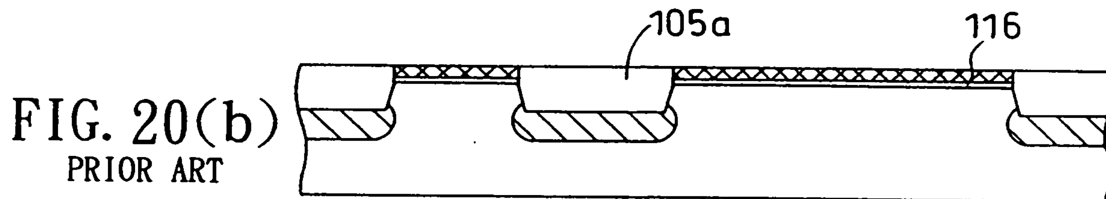


FIG. 20(b)
PRIOR ART

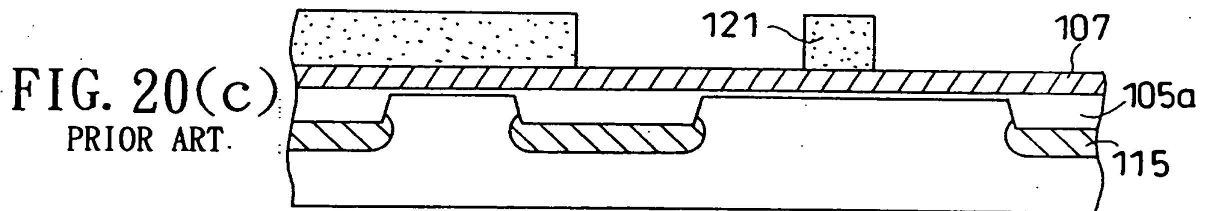


FIG. 20(c)
PRIOR ART

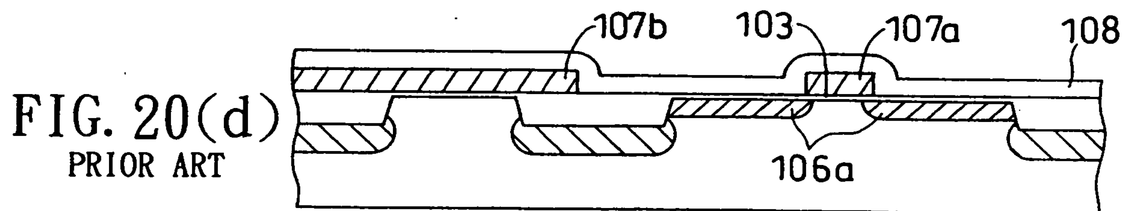


FIG. 20(d)
PRIOR ART

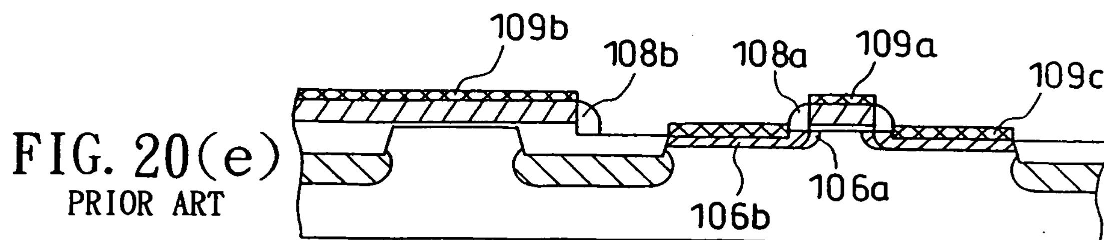


FIG. 20(e)
PRIOR ART

FIG. 21(a)
PRIOR ART

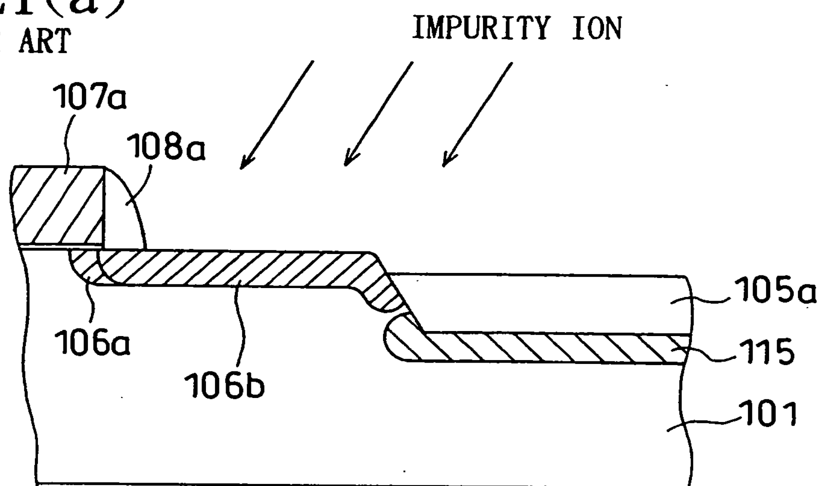
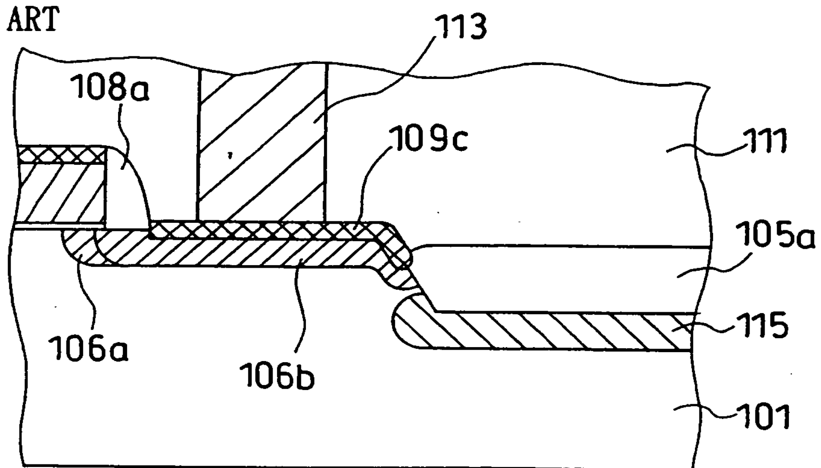


FIG. 21(b)
PRIOR ART



Docket No. ________

COMBINED DECLARATION/POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME ______________________, the specification of which

(check one) X is attached hereto.

__ was filed on ______________ as Application Serial No. ______________.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
7-192181 (Number)	JAPAN (Country)	27/07/1995 (Day/Month/Year Filed)	X Yes __ No
7-330112 (Number)	JAPAN (Country)	19/12/1995 (Day/Month/Year Filed)	X Yes __ No
(Number)	(Country)	(Day/Month/Year Filed)	__ Yes __ No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.) (Filing Date) (Status-patented, pending, abandoned)

(Appln. Serial No.) (Filing Date) (Status-patented, pending, abandoned)

I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Paul Devinsky (Reg. No. 28,553); Edward E. Kubasiewicz (Reg. No. 30,020), Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); and Wilhlem F. Gadiano (Reg. No. 37,136).

Please address all correspondence and telephone calls to:

Kenneth L. Cage, Esquire
McDERMOTT, WILL & EMERY
1850 K STREET, N.W., SUITE 500
WASHINGTON, D.C. 20006
(202) 778-8300

The undersigned hereby authorizes the U.S. attorneys named herein to accept and follow instructions from Maeda Patent Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by the undersigned.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Mizuki SEGAWA

Inventor's signature Mizuki Segawa Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 7-11-64, Nagao-motomachi, Hirakata-shi, Osaka 573-01, Japan

Full name of second inventor Isao MIYANAGA

Inventor's signature [signature] Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 996-3, Kido-cho, Kawachinagano-shi, Osaka 576, Japan

Full name of third inventor Toshiki YABU

Inventor's signature [signature] Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 4-14-1, Nagaodai, Hirakata-shi, Osaka 573-01, Japan

Full name of fourth inventor Takashi NAKABAYASHI

Inventor's signature [signature] Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 3-13-1-306, Oogaichi-cho, Hirakata-shi, Osaka 573, Japan

Full name of fifth inventor Takashi UEHARA

Inventor's signature [signature] Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 6-Nishi 1-1506, Sotoshima-cho, Moriguchi-shi, Osaka 570, Japan

Full name of sixth inventor Kyoji YAMASHITA

Inventor's signature [signature] Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 1-4-40-554, Nonaka-minami, Yodogawa-ku, Osaka-shi, Osaka 532, Japan

Full name of seventh inventor Takaaki UKEDA

Inventor's signature [signature] Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 6-2-205, Myokenzaka, Katano-shi, Osaka 576, Japan

Full name of eighth inventor Masatoshi ARAI

Inventor's signature *Masatoshi Arai* Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 1-4-40-741, Nonaka-minami, Yodogawa-ku, Osaka-shi, Osaka 532, Japan

Full name of ninth inventor Takayuki YAMADA

Inventor's signature *Takayuki Yamada* Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 4-2-6, Yamashiro-cho, Yao-shi, Osaka 581, Japan

Full name of tenth inventor Michikazu MATSUMOTO

Inventor's signature *Michikazu Matsumoto* Date July 22, 1996
Residence* Osaka, Japan Citizenship Japan
Post Office Address 5-26-6, Fujita-cho, Moriguchi-shi, Osaka 570, Japan

* City and State, or City and Country for foreign inventors

Docket No.: 71971-012 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mizuki SEGAWA et al.	:	Confirmation Number: Not yet assigned
Application No.: Divisional of Application No. 10/454,682	:	Group Art Unit: Not yet assigned
Filed: November 24, 2004	:	Examiner: Not yet assigned

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

SUPPLEMENTAL POWER OF ATTORNEY AND CUSTOMER NUMBER

Mail Stop OIPE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

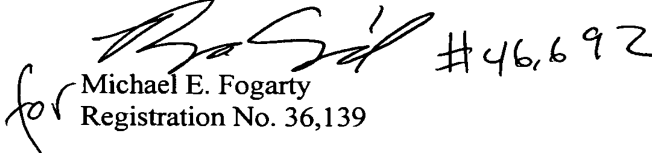
Here is a listing of ten registered attorneys to be made of record in this application. All are registered practitioners of McDermott Will & Emery (Customer Number 20277).

Stephen A. Becker, Reg. No. 26,527; Bernard P. Codd, Reg. No. 46,429; Ramyar M. Farid, Reg. No. 46,692; Michael E. Fogarty, Reg. No. 36,139; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Michael A. Messina, Reg. No. 33,424; Gene Z. Rubinson, Reg. No. 33,351, Arthur J. Steiner, Reg. No. 26,106; and Tomoki Tanida, admitted under 37 CFR 10.9(b).

Please recognize our Customer No. 20277 as our correspondence address.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ete
Facsimile: 202.756.8087
Date: November 24, 2004

PATENT APPLICATION SERIAL NO. ____________________

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

11/29/2004 HMARZI1 00000018 500417 10995283
01 FC:1001 790.00 DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2004

Application or Docket Number: 10555283

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	14	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	14 minus 20=	* —
INDEPENDENT CLAIMS	1 minus 3 =	* —
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	395.00	OR	BASIC FEE	790.00
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL		OR	TOTAL	790

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 10/04) Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Docket No.: 71971-012 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mizuki SEGAWA et al.	:	Confirmation Number: Not yet assigned
Application No.: Divisional of Application No. 10/454,682	:	Group Art Unit: Not yet assigned
Filed: November 24, 2004	:	Examiner: Not yet assigned

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

PRELIMINARY AMENDMENT

Mail Stop NEW APPLICATIONS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1 – 38 *(Cancelled)*

39. (New) A semiconductor device, comprising:

an isolation insulating area surrounding an active area of a semiconductor substrate;

a gate insulating film formed over the active area;

a gate electrode formed over the gate insulating film;

first L-shaped sidewalls formed over the side surfaces of the gate electrode; and first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area.

40. (New) The semiconductor device of Claim 39, wherein the first L-shaped sidewalls are made of a silicon nitride film.

41. (New) The semiconductor device of Claim 39, further comprising first protection oxide films formed between the gate electrode and the first L-shaped sidewalls.

42. (New) The semiconductor device of Claim 39, further comprising a second silicide layer formed on the gate electrode.

43. (New) The semiconductor device of Claim 39, further comprising source/drain regions formed on both sides of the gate electrode within the active area,

wherein the first silicide layers are formed on the source/drain regions.

44. (New) The semiconductor device of Claim 39, further comprising an interconnection formed over the isolation insulating area; and

second L-shaped sidewalls formed over the side surfaces of the interconnection.

45. (New) The semiconductor device of Claim 44, the second L-shaped sidewalls are made of a silicon nitride film.

46. (New) The semiconductor device of Claim 44, further comprising second protection oxide films formed between the interconnection and the second L-shaped sidewalls.

47. (New) The semiconductor device of Claim 44, further comprising a third silicide layer formed on the interconnection.

48. (New) The semiconductor device of Claim 39, wherein the isolation insulating area is a trench isolation.

49. (New) The semiconductor device of Claim 48, the trench isolation has an upper surface higher than the surface of the active area.

50. (New) The semiconductor device of Claim 48, wherein a lower portion of the interconnection provided on the upper surface of the trench isolation is located higher than the surface of the active area.

51. (New) The semiconductor device of Claim 44, wherein the interconnection is composed of the same material as the gate electrode.

52. (New) The semiconductor device of Claim 51, wherein the gate electrode and the interconnection has at least a polysilicon film.

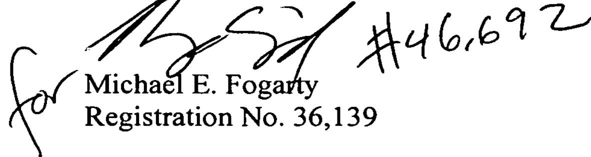
REMARKS

Please cancel claims 1 – 38 without prejudice or disclaimer. New claims 39 – 52 have been added.

No new matter has been introduced. Entry of this amendment is respectfully solicited.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



for Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ete
Facsimile: 202.756.8087
Date: November 24, 2004

Please recognize our Customer No. 20277 as our correspondence address.

Docket No.: 71971-012 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mizuki SEGAWA et al.	:	Confirmation Number: Not yet assigned
Application No.: Divisional of Application No. 10/454,682	:	Group Art Unit: Not yet assigned
Filed: November 24, 2004	:	Examiner: Not yet assigned

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

INFORMATION DISCLOSURE STATEMENT

Mail Stop NEW APPLICATIONS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

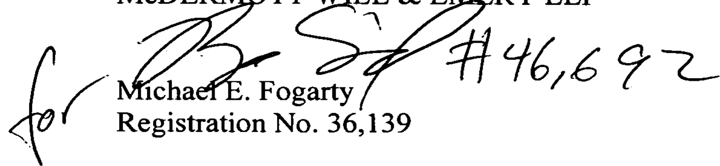
The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 10/454,682, filed June 5, 2003, which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Application No.: Divisional of Application No. 10/454,682

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ete
Facsimile: 202.756.8087
Date: November 24, 2004

Please recognize our Customer No. 20277 as our correspondence address.

SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **71971-012**	SERIAL NO. **Divisional of Application No. 10/454,682**
	APPLICANT **Mizuki SEGAWA, et al.**	
	FILING DATE **November 24, 2004**	GROUP **Not yet assigned**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
			4,578,128	03/1986	Mundt et al.	
		US	5,177,028	01/1993	Manning	
		US	5,196,910	03/1993	Moriuchi et al.	
		US	5,286,674	02/1994	Roth et al.	
		US	5,319,235	06/1994	Kihara et al.	
		US	5,393,708	02/1995	Hsia et al.	
		US	5,397,910	03/1995	Ishimaru	
		US	5,401,673	03/1995	Urayama	
		US	5,413,961	05/1995	Kim	
		US	5,433,794	07/1995	Fazan et al.	
		US	5,497,016	03/1996	Koh	
		US	5,521,422	05/1996	Mandelman et al.	
		US	5,561,311	10/1996	Hamamoto et al.	
		US	5,777,370	07/1998	Omid-Zohoor et al.	
			5,804,862	09/1998	Matumoto	
		US	6,022,781	02/2000	Noble, Jr.	
		US	6,077,344	06/2000	Shoup et al.	
		US	6,278,138 B1	08/2001	Suzuki	
		US	6,281,562	08/2001	Segawa et al.	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3 -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	No
		JP 59181062 A	10/1984				
		JP 62-85461	04/1987				
		EP 0234988-A1	04/1987				
		EPA 0 243 988	11/1987				
		JP 03079033 A	04/1991				
		JP 4-48647	02/1992				
		JP 4-68564	03/1992				
		JP 4-305922	10/1992				
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		JP 6-163843	06/1994				
		JP 7-273330	10/1995				
		JP 09162392 A	06/1997				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.