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I am well acquainted with the English and Japanese languages and have in the past translated numerous English/Japanese documents of legal and/or technical content.

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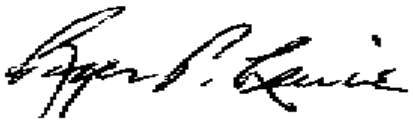

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[Document Name] Specification
[Title of Invention] Semiconductor device and method of manufacturing the same
[Scope of Claims]
[Claim 1]
A semiconductor device comprising:
a semiconductor substrate;
an isolation formed such that the top surface is higher in a stepwise manner than the surface of the semiconductor substrate;
a plurality of active areas formed by introducing impurities in the semiconductor substrate surrounded by the isolation;
an insulating film formed so as to stretch over the active areas and the isolation;
contact holes formed so as to expose a part of the insulating film, at least a portion of the contact holes reaching to the surface of the active areas; and
an upper interconnection formed above the insulating film and in the contact hole, the upper interconnection connecting to the active areas.

[Claim 2]
The semiconductor device according to Claim 1, wherein through dispersion in manufacturing procedures of the semiconductor device, at least some of the contact holes out of the plurality of contact holes are formed so as to stretch from the surface of the active areas to the isolation.

[Claim 3]
The semiconductor device according to Claim 1, further comprising:
an interconnection member formed such that at least a portion thereof is positioned on the isolation;
wherein the contact holes are formed so as to stretch from the surface of the active areas to the interconnection member near the active areas; and
the upper interconnection is also connected to an interconnection member on the isolation.

[Claim 4]
The semiconductor device according to any one of Claims 1 to 3, further comprising:
an isolation sidewall made of an insulating material and formed on a side surface of a step portion from the surface of the active areas reaching to the top surface of the isolation;
wherein the contact holes are formed so as to stretch over the isolation sidewall.

[Claim 5]
The semiconductor device according to Claim 1, wherein the dimensions and materials of the respective components can be determined so as to satisfy the inequality:
$OE \times a \times (ER2/ER1) \geq b + D \times (2/10)$,
wherein "a" denotes the thickness of the insulating film; "b" denotes the level difference between the surface of the field oxide film and the surface of the active area; "ER1" denotes the etching rate of the insulating film; "ER2" denotes the etching rate of the field oxide film; "D" denotes the depth of an impurity diffused layer in the active area; and "OE" denotes the over-etch ratio of the insulating film in the formation of the contact hole.

[Claim 6]

The semiconductor device according to Claim 1, further comprising:

a FET having a gate electrode formed on top of the active area, a source/drain region formed in the active area positioned on both side surfaces of the gate electrode, and a gate protection film formed on top of the gate electrode;

wherein the contact holes are formed so as to stretch from the source/drain region to at least a portion of the gate protection film.

[Claim 7]

The semiconductor device according to Claim 4, further comprising:

a FET having a gate electrode formed on the active area, a source/drain region formed in the semiconductor substrate positioned to the side of the gate electrode, a gate protection film formed on top of the gate electrode, and an electrode sidewall formed on both side surfaces of the gate electrode;

wherein the isolation sidewall is formed at the same time as the electrode sidewall.

[Claim 8]

The semiconductor device according to Claim 6 or Claim 7, wherein the dimensions and materials of the respective components are determined so as to satisfy the inequality:

$OE \times a \times (ER3/ER1) < c$,

wherein "a" denotes the thickness of the insulating film; "c" denotes the thickness of the gate protection film; "ER1" denotes the etching rate of the insulating film; "ER3" denotes the etching rate of the gate protection film; and "OE" denotes the over-etch ratio of the insulating film in the formation of the contact hole.

[Claim 9]

The semiconductor device according to Claim 1, wherein the angle of inclination of the side surface of the step portion from the surface of the active area to the surface of the isolation to the semiconductor substrate surface is at least 70 degrees.

[Claim 10]

A manufacturing method for a semiconductor device, the method including:

a procedure for forming, on a semiconductor substrate, an isolation having a top surface that is higher in a stepwise manner than the surface of the semiconductor substrate;

a procedure for introducing impurities in a plurality of active areas surrounded by the isolation in the semiconductor substrate;

a procedure for depositing an insulating film on the active areas and the isolation;

a procedure for forming a mask member having an exposing area for forming contact holes to the active areas, on the insulating film;

a procedure for removing the insulating film in the exposing area of the mask member through etching, and furthermore accomplished a prescribed over-etch, thereby forming a contact hole; and

a procedure for forming an upper interconnection connecting to the active areas above the insulating film and in the contact hole;

wherein in the procedure for forming the mask member, a margin is not provided for ensuring that the exposing area of the mask member does not include the isolation when a mask

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