## United States Patent [19]

## Lowrey et al.

### [54] SPLIT-POLYSILICON CMOS PROCESS INCORPORATING SELF-ALIGNED SILICIDATION OF CONDUCTIVE REGIONS

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- [52]
   U.S. Cl.
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   [58]
   Field of Search
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357/23.3, 23.4, 40, 41, 42, 44

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#### ABSTRACT

[57]

An improved CMOS fabrication process which uses separate masking steps to pattern N-channel and Pchannel transistor gates from a single layer of conductively-doped polycrystalline silicon (poly) and incorporates self-aligned salicidation of conductive regions. The object of the improved process is to reduce the cost and improve the reliability, performance and manufacturability of CMOS devices by a process which features a dramatically reduced number of photomasking steps and which further allows self-aligned salicidation of transistor conductive regions. By processing N-channel and P-channel devices separately, the number of photomasking steps required to fabricate complete CMOS circuitry in a single-polysilicon-layer or single-metal layer process can be reduced from eleven to eight. Starting with a substrate of P-type material, N-channel devices are formed first, with unetched poly left in the future P-channel regions until N-channel processing is complete. The improved CMOS process provides the following advantages over conventional process technology: Use of a masked high-energy punch-through implant for N-channel devices is not required; individual optimization of N-channel and P-channel transistors is made possible; a lightly-doped drain (LDD) design for both N-channel and P-channel transistors is readily implemented; source/drain-to-gate offset may be changed independently for N-channel and P-channel devices; and N-channel and P-channel transistors can be independently controlled and optimized for best LDD performance and reliability.

### 5 Claims, 13 Drawing Sheets







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