Some problems of MOS technology

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Introduction

Scientists and engineers working in MOS transistor technology are charged with the production of MOS transistors and integrated circuits that possess certain specified characteristics, are stable in behaviour, and give high production yields. The specified requirements determine the various steps in the production process: from the design geometry to the choice and techniques of oxidation, etching, diffusion and other processes in the manufacture of a MOS transistor [1]. Some of the problems which this involves are described in this article; the structure and operation of the MOS transistor, which are dealt with elsewhere in this issue [2], are assumed to be generally familiar to the reader.

A typical example of a quantity that is determined by design geometry and technological processes is the transconductance of the MOS transistor. In the article just noted [2] it is shown that the transconductance — and hence the current that the transistor can carry at the maximum permissible gate voltage — is proportional to

$$\beta = \mu C_{ox} w/l. \quad \ldots\ldots \quad (1)$$

Here μ is the mobility of the charge carriers in the channel, C_{ox} the capacitance of the gate per unit area, w is the width and l the length of the channel (*fig. 1*).

The mobility μ depends on the semiconductor material of which the MOS transistor is made. For practical reasons this is almost invariably silicon. One of these reasons is that it is relatively simple to apply effective isolating layers to silicon by oxidation. Although impurity centres or defects may be present at the Si/SiO_2 interface, the nature and concentrations of these impurities can now be controlled, and they can in fact be used to alter the behaviour of a MOS transistor in a desired direction. Much of this article will be concerned with the Si/SiO_2 interface.

In the bulk of the silicon the mobility μ may be regarded as a constant of the material. At the surface the mobility is usually appreciably lower than in the bulk. Not only may it be affected here by the impurities or defects, but it is also found that μ decreases with increasing gate voltage, and therefore depends on the magnitude of the charge induced in the channel. A theoretical analysis based on detailed physical considerations has shown that this is to be expected [3].

It has also been found that the surface mobility is dependent on the crystal orientation at the surface. For electrons the mobility is greatest for the (100) plane of silicon; the surface mobility in this plane can even approach the value of μ in the bulk. For the holes the mobility is greatest for the (111) orientation, but hole mobility is substantially less than electron mobility. To achieve the maximum carrier mobility, and hence the maximum transconductance, the best choice is an N-channel transistor on a silicon chip whose surface is oriented in the (100) plane.

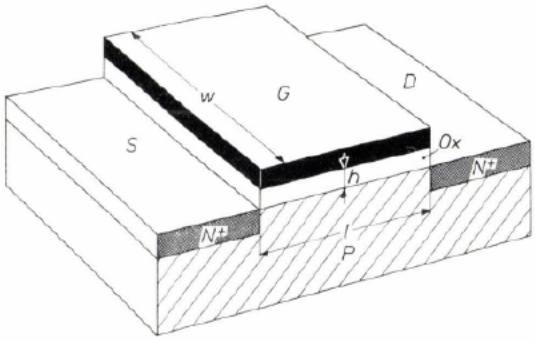

Fig. 1. Schematic diagram of a MOS transistor, made on a P-type silicon substrate. Two diffused zones of N^+ silicon constitute the source S and the drain D. Between them, isolated by an oxide layer Ox, is a metal control electrode, the gate G. If G is sufficiently positive, a concentration of free electrons occurs under the gate, forming an N-type conducting channel between source and drain. The length l and width w of the channel, and the thickness h of the oxide are the chief factors that determine the characteristics of the MOS transistor.

If a high value of β is desired it is also necessary to have a high C_{ox} (see equation 1), and for this purpose the oxide layer under the gate is made as thin as possible. The minimum thickness is mainly determined by

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[1] A description of the photo-etching and diffusion processes is given in: A. Schmitz, Solid circuits, Philips tech. Rev. **27**, 192-199, 1966.

[2] J. A. van Nielen, Operation and d.c. behaviour of MOS transistors; this issue, page 209.

[3] N. St. J. Murphy, F. Berz and I. Flinn, Carrier mobility in MOS transistors; this issue, page 237.

the breakdown field-strength (about 10^3 V/μm); practical values frequently lie between 0.05 and 0.25 μm.

The dimensions of the silicon chips set an upper limit to the width w of the channel, and of course the chance of a defect increases with increasing w. A width of a few millimetres is fairly easy to achieve, and special techniques can be applied to give a channel with a width of a few centimetres [4].

The length l of the channel cannot be made very small without running the risk of "punch-through", i.e. a flow of current between source and drain outside the channel. The length l is usually a few microns, but special methods can be used to bring it down to about 1 micron. A very short channel is particularly important in MOS transistors for the UHF band [5].

In addition to the transconductance β, the parasitic capacitances play an important part in fast transistors. The most detrimental one is usually the feedback capacitance between drain and gate [6]. This capacitance depends on the amount of overlap between drain and gate: it can be reduced by bringing the gate into accurate register with the channel region. Various useful methods that we have developed for this will be discussed in this article.

The speed of integrated circuits made with MOS transistors is mainly limited by the parasitic capacitance between wiring and substrate. MOS transistors are therefore made with thick oxide layers under the wiring but with thin oxide layers at the active regions. This approach also tends to prevent the formation of parasitic MOS transistors; these can be formed when a voltage applied to a conductor induces a conducting channel in the substrate underneath the conductor. In the transition from the thick oxide to the thin oxide there has to be a step in the metallization; this has often proved to be a weak spot. We have therefore developed a process in which the thicker oxide is embedded deeper in the silicon substrate, so that any steps above the surface are smaller. This is known as the LOCOS process (local oxidation of silicon), and will also be described in this article.

First of all we shall take a closer look at the silicon/silicon-dioxide interface. The surface defects present there and the contact potential of the gate metal and the substrate doping all have an important effect on the threshold voltage, i.e. the minimum gate voltage needed to form a channel [2]. In fact these defects can have a much greater influence than the contact potential and substrate doping. They can change the threshold voltage by tens of volts, whereas the changes due to differences in contact potential between dissimilar metals and the variation of substrate doping that occurs in practice amount to only a few volts. The in the threshold voltage. Control of the threshold voltage and making sure that it is stable are the main factors that decide which technology should be followed.

The silicon/silicon-dioxide interface

The theoretical treatment given here of the silicon/silicon-dioxide interface makes no pretence at being complete, but is a simple model that is nevertheless capable of explaining many experimental results, and one that has also been found useful for qualitatively predicting the behaviour of the Si/SiO_2 system from the processing conditions that were used when it was made. In this model we distinguish between defects of two kinds:

a) Surface states — states that can exchange charge with the silicon, and which can be described in physical terms as quantum states with an energy level between the valence and conduction band;
b) Oxide charge — fixed positive charges (ionized donors) near the interface and presumably in the oxide.

We shall now consider both types of defect in turn.

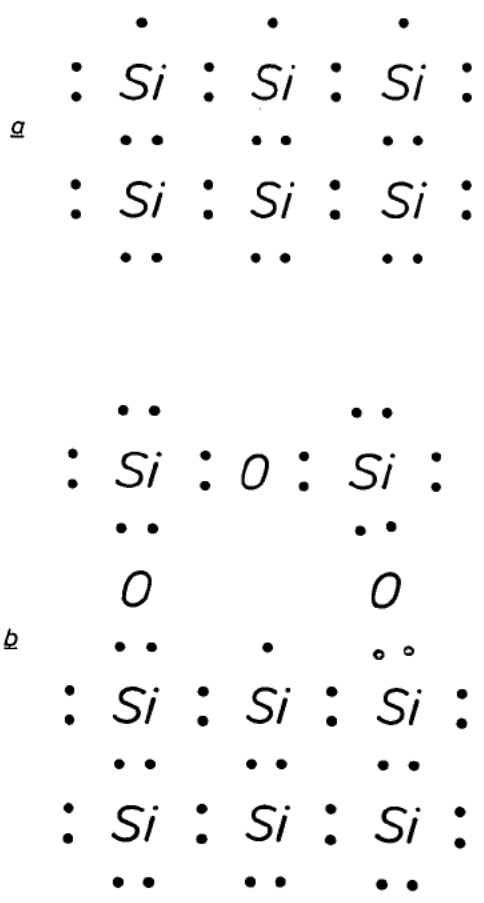

Fig. 2. *a*) Crystal lattice of silicon. At the surface of the crystal (top of the figure) each atom has an unpaired electron. *b*) Where the surface of the silicon crystal is covered with silicon dioxide,

Surface states

If the crystal lattice terminates abruptly at the surface of a silicon chip, then a large number of unsaturated silicon bonds are to be expected, i.e. each atom in the outside layer of silicon atoms should have an unpaired electron (*fig. 2a*). Since there are about 10^{15} Si atoms per cm^2 at the surface, one would expect about the same number of unsaturated bonds on a "clean" surface. If the silicon is oxidized, as it is in the case under consideration, then the number of unsaturated bonds is of course lower, but it is not equal to zero because there will probably not be an exact fit between the Si and SiO_2 networks (fig. 2*b*). We shall now consider what electrical effects can result from the unsaturated silicon bonds.

It is very probable that it will take less energy to raise an unpaired electron into the conduction band than to raise a paired valence electron; in other words, the unpaired electron possesses an energy level that lies in the forbidden band. A silicon atom to which such an electron is bound may give up this electron or take up a hole, but in both cases the atom itself becomes positively charged (*fig. 3*):

$$:\dot{\underset{\cdot\cdot}{\text{Si}}}: \rightleftarrows :\overset{+}{\underset{\cdot\cdot}{\text{Si}}}: + e^-, \quad \ldots\ldots \quad (2)$$

$$e^+ + :\dot{\underset{\cdot\cdot}{\text{Si}}}: \rightleftarrows :\overset{+}{\underset{\cdot\cdot}{\text{Si}}}: \quad \ldots\ldots\ldots \quad (3)$$

If we are dealing, for example, with *P*-type silicon, then there are many holes and the equilibria (2) and (3) shift to the right. If moreover the energy gap $E_{ss} - E_v$ is small, a number of holes from the silicon may be trapped, and therefore the hole conduction near the surface of the crystal is not so good as in the bulk of the material.

bonds may act not only as electron donors or traps for holes, but also as traps for electrons, since trapping an electron changes a silicon atom with an unpaired electron into an atom with eight electrons in its outer shell. This is the inert-gas configuration:

$$:\dot{\underset{\cdot\cdot}{\text{Si}}}: + e^- \rightleftarrows :\overset{-}{\underset{\cdot\cdot}{\text{Si}}}: \quad \ldots\ldots \quad (4)$$

The effect may also be seen as the giving-up of a hole:

$$:\dot{\underset{\cdot\cdot}{\text{Si}}}: \rightleftarrows :\overset{-}{\underset{\cdot\cdot}{\text{Si}}}: + e^+, \quad \ldots\ldots \quad (5)$$

and we may then conclude that the relevant energy level must lie in the forbidden band.

From a wide variety of measurements [7] it has been found that energy levels do in fact occur in the forbidden band, and that broadly two groups may be distinguished: a group near the conduction band

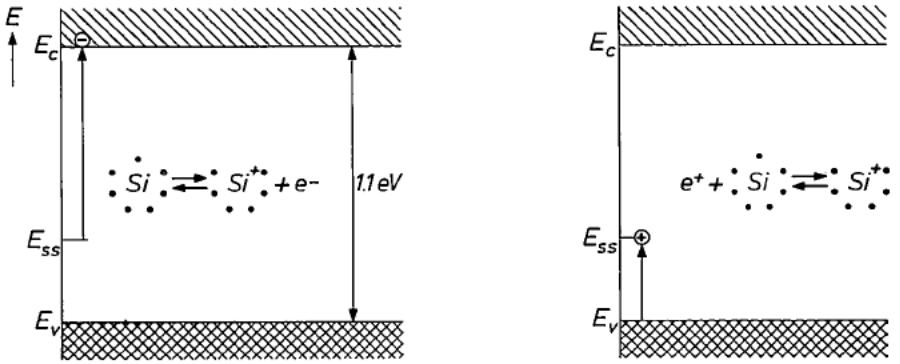

Fig. 3. The unpaired electron of a silicon atom with an unsaturated bond has an energy E_{ss} which lies in the forbidden band between valence band (energy E_v) and conduction band (energy E_c). The atom may occur as a donor; by giving up an electron (*on the left*) or taking up a hole (*on the right*) it then acquires a positive charge. If there is a high electron concentration the atom may also occur as an acceptor and acquire a negative charge.

— these are probably acceptor levels — and a group near the valence band — probably donor levels. Depending on the voltages applied in the measurements, there is a tendency for electrons or holes to concentrate at the Si/SiO_2 interface; if there is a high electron concentration the defects act mainly as acceptor levels, but at a high hole concentration mainly as donor levels. On the same sample the number of acceptor levels found in one measurement is invariably almost equal

[4] R. D. Josephy, MOS transistors for power amplification in the HF band; this issue, page 251.
[5] R. J. Nienhuis, A MOS tetrode for the UHF band with a channel 1.5 μm long; this issue, page 259.
[6] P. A. H. Hart and F. M. Klaassen, The MOS transistor as a small-signal amplifier; this issue, page 216.
[7] E. Kooi, The surface properties of oxidized silicon, Thesis, Eindhoven 1967.
M. V. Whelan, Influence of charge interactions on capacitance versus voltage curves in MOS structures, Philips Res.

to the number of donor levels found in another measurement; this lends plausibility to our assumption that the same trapping centres are involved in both cases.

The assumption that the centres are related to unsaturated silicon bonds explains why the number of surface states depends on the crystal orientation of the silicon surface. If this is a (111) plane, then there are usually 3 to 5 times as many surface states as on a (100) plane. This suggests that the oxide network fits better on a (100) crystal plane than on a (111) plane. Other crystal orientations give various numbers of surface states that lie between those of the (100) and (111) planes.

The way in which the surface states can affect the characteristics of a MOS transistor will be demonstrated by means of a number of experimental transistors on a *P*-type silicon substrate, i.e. with an *N*-type channel. This channel would have to be induced by applying a positive voltage to the gate. Since the effect of this is a decrease in the concentration of holes near the silicon surface and an increase in the electron concentration, the equilibria (2) and (3) shift to the left and the equilibria (4) and (5) to the right. This means that the donor states tend to become neutral (if they were not neutral already) and the acceptor states negative. The build-up of negative charge in the surface states means that the mobile charge entering the bulk of the silicon is less than the total induced charge. Consequently the threshold voltage, required for inversion, is higher than expected, and on increasing the gate voltage the subsequent increase in the inversion charge (and hence in the current through the transistor) is lower, and the transconductance is therefore affected.

The effect of the surface states is illustrated in *fig. 4*, which shows the I_d-V_{gs} curves for the experimental MOS transistors that all have the same dimensions but were annealed in different gas atmospheres after forming the gate oxide in an extremely dry atmosphere at about 1100 °C. During the anneal, the temperature was kept low (450 °C) compared with the normal growth temperature of SiO_2 on Si (1000 °C or higher), so that the processing steps could cause no difference in oxide thickness. They did, however, give rise to differences in the numbers of surface states, as may be shown from the threshold voltages and transconductances. In fact a hydrogen atmosphere and water vapour in an atmosphere of wet nitrogen even lead to negative threshold voltages and thus appear to remove the surface states for the most part. Water vapour in an oxygen atmosphere has considerably less effect. This suggests that a reduction of water

that the treatment in wet nitrogen is most effective when the chip is heated to a high temperature in an inert gas immediately after the silicon is oxidized. This treatment reduces the oxygen content of the SiO_2 through the influence of the silicon beneath it.

The simplest explanation for the disappearance of the surface states is a chemical reaction of hydrogen with the centres involved, i.e. the formation of SiH groups in our model. This explanation has been confirmed by infra-red absorption measurements [8]. With the aid of a sensitive method of measurement it has been shown that the SiO_2 almost invariably contains a certain number of SiH groups, whose concentration is particularly high when the oxidized surface is subjected to operations which reduce the number of surface states.

Often very little water vapour is sufficient to reduce the number of surface states; a heat treatment in an inert gas (e.g. nitrogen or helium) which is not extremely dry (containing a few ppm of water) may be effective. It is also found that treatment in a fairly dry environment may also be highly effective if there is a base-metal electrode (e.g. of aluminium) on the silicon surface. Here again the surface states under the electrode disappear upon heating. It is assumed that in this case a reaction of the metal with traces of water produces sufficient hydrogen.

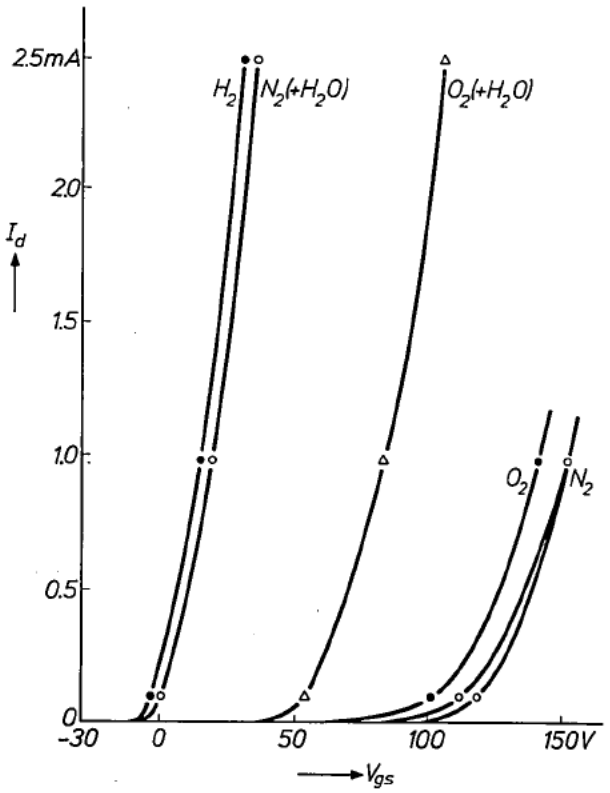

Fig. 4. The I_d-V_{gs} characteristics of a number of geometrically

We may therefore conclude that the structure of the interface is generally very dependent on the crystal orientation of the silicon, on the method of growing the oxide and on the subsequent treatments. Many experiments can be explained on the assumption that the silicon bonds are or are not saturated with hydrogen. We can be certain, however, that this does not give a complete description of the interface. A more exact theory would have to take into account, for example, the occurrence of SiOH groups and particularly the influence of other impurities (whether deliberately introduced or not) on the interface structure. We shall return to this in the next section.

Positive charge at the oxide|silicon interface

Anyone assuming that all the difficulties are resolved by a suitable after-treatment that reduces the number of surface states to a negligible value will be surprised by the result that, although the I_d-V_{gs} curve has approximately the theoretically expected shape after such a treatment, the threshold voltage often has a value less positive (or more negative) than was expected.

Indeed, the *N*-channel MOS transistors of fig. 4 have a negative threshold voltage after treatment in hydrogen or wet nitrogen; in other words, they already have an inversion channel when the gate voltage is zero. This effect cannot be explained in terms of the surface states, since they have the very effect of opposing the inversion.

We must therefore assume that there are other centres present in addition to the ones we have mentioned. It is usually supposed that the effect is caused by the presence of positively charged centres in the oxide immediately adjacent to the silicon surface, although these are difficult to distinguish experimentally from ionized donor centres in the silicon near the surface. The amount of oxide charge, like the number of surface states described above, is connected with the interface structure. Again, with identical processing, the oxidized (100) plane is found to give the lowest oxide charge, and the (111) plane the highest. Impurities have an important effect, particularly sodium. It has been clearly demonstrated [7] that the presence of sodium during oxidation can have a marked effect on the amount of charge, although the crystal orientation still remains important. It has been shown by neutron-activation analysis that the sodium has a distribution in the oxide like that illustrated in *fig. 5*. Most of the sodium can be seen to lie in the top layer of the oxide, but there is also an accumulation at the interface with the silicon. The position of sodium in the oxide structure may perhaps best be represented as in *fig. 6a*. This structure may be regarded as a somewhat reduced oxide structure, the oxide layer. The sodium atom breaks the bond between an oxygen and a silicon atom, and itself forms a bond with the oxygen atom. As a result, one of the valence electrons of the silicon loses its bond, and as this electron is easily released, a positively charged centre is formed.

The sodium at the interface may conceivably be replaced by other alkali metals and even by hydrogen. This may perhaps explain why, even under fairly clean conditions, oxidation in steam gives rise to more oxide charge than oxidation in dry oxygen. On the other hand, it has also been observed that heating in hydro-

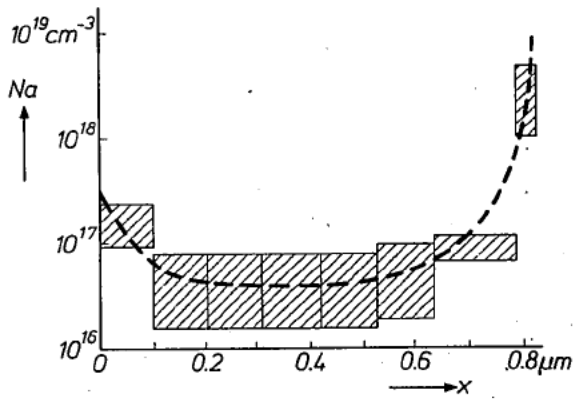

Fig. 5. Distribution of the concentration of Na atoms in the oxide as a function of the distance x from the silicon; the hatched area indicates the scatter of the measuring results.

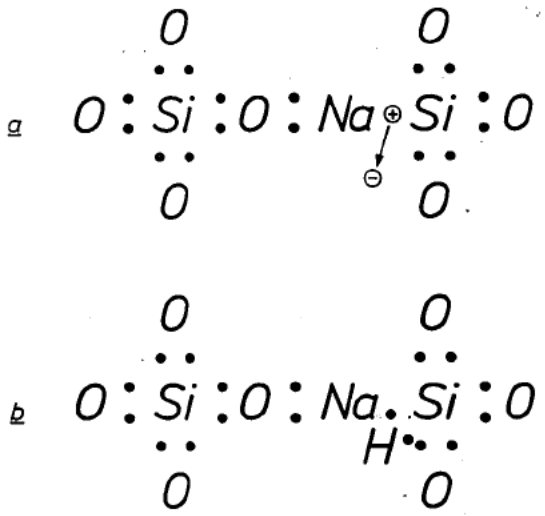

Fig. 6. *a*) The location of a sodium atom in SiO_2. The sodium atom breaks the bond between a silicon and an oxygen atom, and as a result one of the valence electrons of the silicon loses its bond; this electron is easily released and leaves behind a positive charge. *b*) A hydrogen atom can introduce an SiH group in SiO_2. In this group the hydrogen atom forms a homopolar bond with the silicon and there is no longer an unpaired electron.

[8] These measurements were carried out by Dr. K. H. Beckmann and T. Tempelmann of the Philips Hamburg laboratories:

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