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Paper 9
Entered: January 4, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

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Cases IPR2016-01246 and IPR2016-01247
Patent 7,126,174 B2

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Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
*37 C.F.R. § 42.108*

Petitioner Taiwan Semiconductor Manufacturing Company, Ltd. filed two Petitions requesting *inter partes* review of claims 1–12 and 14–18 of U.S. Patent No. 7,126,174 B2 (Ex. 1001, "the '174 patent")[1] pursuant to 35 U.S.C. § 311(a). Patent Owner Godo Kaisha IP Bridge 1 filed a Preliminary Response and Motion for District Court-Type Claim Construction in each proceeding, as listed in the following chart.

| Case Number | Challenged Claims | Petition | Preliminary Response | Motion |
|---|---|---|---|---|
| IPR2016-01246 | 1–3, 5–7, 9–12, and 14–18 | Paper 2 ("Pet.") | Paper 7 ("Prelim. Resp.") | Paper 6 ("Mot.") |
| IPR2016-01247 | 1, 4, 5, 8–12, 14, and 16 | Paper 2 ("-1247 Pet.") | Paper 7 ("-1247 Prelim. Resp.") | Paper 6 ("-1247 Mot.") |

Pursuant to 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons that follow, we institute an *inter partes* review as to claims 1–12 and 14–18 of the '174 patent on certain grounds of unpatentability. We also exercise our authority under 35 U.S.C. § 315(d) to consolidate the two proceedings and conduct the proceedings as one trial.

[1] Unless otherwise specified with the "-1247" prefix, references to exhibits herein are to those filed in Case IPR2016-01246.

# I. BACKGROUND

## *A. The '174 Patent*[2]

The '174 patent discloses a "semiconductor device including transistors and connection[s] between the transistors for constituting [a large-scale integration (LSI) integrated circuit (IC)] with high integration and a decreased area." Ex. 1001, col. 1, ll. 13–16. At the time of the '174 patent, various improvements had been made in semiconductor manufacturing due to "increasing demands for more refinement of the semiconductor device." *Id.* at col. 1, ll. 17–22. The '174 patent describes one known method of forming an isolation structure (for shielding devices from each other on a substrate) known as Local Oxidation of Silicon (LOCOS), which was "conventionally adopted in view of its simpleness and low cost." *Id.* at col. 1, ll. 22–25. The LOCOS isolation method involves selective oxidation of a silicon substrate, but has a disadvantage in that it results in a "bird's beak" overhanging area of silicon dioxide. *Id.* at col. 1, ll. 29–31. "As a result, the dimension of a transistor is changed because an insulating film of the isolation invades [the] transistor region against the actually designed mask dimension." *Id.* at col. 1, ll. 31–34. According to the '174 patent, compared to LOCOS, "trench buried type isolation" (or "trench isolation") was determined to be "more advantageous for manufacturing a refined semiconductor device." *Id.* at col. 1, ll. 25–28.

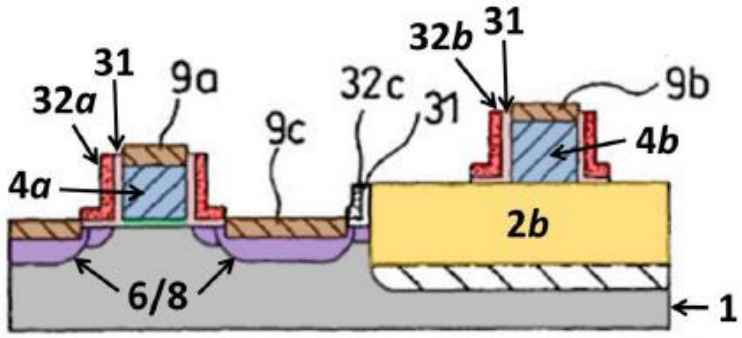
The '174 patent describes a "conventional semiconductor device" with a trench isolation structure "whose top surface is flattened so as to be at the same level as the top surface of the silicon substrate" (as shown in

[2] The '174 patent is a division of a series of U.S. applications ultimately descending from a U.S. application filed on July 24, 1996, and claims the benefit of foreign applications filed on July 27 and December 19, 1995.

Figure 17) or whose top surface is higher than the surface of the silicon substrate (as shown in Figure 20(e)). *Id.* at col. 1, l. 52–col. 2, l. 6 (structure 2b), col. 4, l. 16–col. 5, l. 11 (trench isolation 105a). By using the "conventional trench isolation" structure, "the dimensional change of the source/drain region can be suppressed because the bird's beak" created using LOCOS is avoided. *Id.* at col. 4, ll. 16–19, col. 5, ll. 12–17. According to the '174 patent, using the trench isolation method caused various problems of its own due to the etching required. *Id.* at col. 5, ll. 21–58.

The '174 patent describes various embodiments of semiconductor devices and methods of manufacturing the same. The manufacturing process for Embodiment 10 is depicted in the sequence of Figures 12, 13(a)–(e), and 15(a)–(f). *Id.* at col. 21, ll. 33–34, col. 26, ll. 36–45 (referring to the previously described process of Embodiment 8). Petitioner provides on page 13 of the Petition a colored and annotated version of Figure 15(f) of the '174 patent, reproduced below, which is consistent with the '174 patent's disclosure.

FIG. 15(f)




1—Substrate (Si)
2—Trench Isolation ($SiO_2$)
3—Gate Insulating Film ($SiO_2$)
4—Gate Electrode/Interconnect (poly-Si)
31—Protection Oxide Film ($SiO_2$)
32—Sidewall (SiN)
6/8—Source/Drain Region
9—Silicide

The figure above depicts a device including isolation 2b, which is the result of forming a trench in silicon substrate 1 and filling it with insulating

material. *Id.* at col. 21, ll. 39–50, col. 22, ll. 34–44. "[E]lectrode sidewalls 32a, interconnection sidewalls 32b and a step sidewall 32c each having an L-shape remain on the sides of the gate electrode 4a, the gate interconnection 4b and the step portion, respectively." *Id.* at col. 27, ll. 4–8. The '174 patent describes various advantages of forming "L-shaped sidewalls" in the manner disclosed. *Id.* at col. 27, ll. 34–47.

### *B. Illustrative Claim*

Claim 1 of the '174 patent recites:

> 1. A semiconductor device, comprising:
>
> a trench isolation surrounding an active area of a semiconductor substrate;
>
> a gate insulating film formed over the active area;
>
> a gate electrode formed over the gate insulating film;
>
> first L-shaped sidewalls formed over the side surfaces of the gate electrode;
>
> first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area
>
> an interconnection formed on the trench isolation; and
>
> second L-shaped sidewalls formed over the side surfaces of the interconnection.

### *C. The Prior Art*

Petitioner relies on the following prior art:

> U.S. Patent No. 4,506,434, issued Mar. 26, 1985 (Ex. 1010, "Ogawa");
>
> U.S. Patent No. 5,021,353, issued June 4, 1991 (Ex. 1017, "Lowrey");

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