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Paper 10
Entered: January 3, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
and GLOBALFOUNDRIES U.S. INC.,
Petitioners,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01246[1]
Patent 7,126,174 B2

Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a)

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[1] Case IPR2016-01247 has been consolidated with this proceeding. GlobalFoundries U.S. Inc.'s motions for joinder in Cases IPR2017-00925 and IPR2017-00926 were granted.

I. BACKGROUND

Petitioner Taiwan Semiconductor Manufacturing Company, Ltd. filed two Petitions requesting *inter partes* review of claims 1–12 and 14–18 of U.S. Patent No. 7,126,174 B2 (Ex. 1001, "the '174 patent") pursuant to 35 U.S.C. § 311(a), as listed in the following chart.

Case Number	Challenged Claims	Petition
IPR2016-01246	1–3, 5–7, 9–12, and 14–18	Paper 2 ("Pet.")
IPR2016-01247	1, 4, 5, 8–12, 14, and 16	Paper 2 ("-1247 Pet.")

On January 4, 2017, we instituted an *inter partes* review of claims 1–12 and 14–18 on four grounds of unpatentability and consolidated Case IPR2016-01247 with Case IPR2016-01246 (Paper 8, "Dec. on Inst.").[2] Patent Owner Godo Kaisha IP Bridge 1 filed a Patent Owner Response (Paper 14, "PO Resp."), Petitioner filed a Reply (Paper 21, "Reply"), and Patent Owner filed a Sur-Reply (Paper 37, "Sur-Reply"), pursuant to our authorization (Paper 28). Petitioner filed a Motion to Exclude (Paper 29, "Pet. Mot.") certain evidence submitted by Patent Owner. Patent Owner filed an Opposition (Paper 39, "PO Mot. Opp.") and Petitioner filed a Reply (Paper 42, "Pet. Mot. Reply"). Patent Owner filed a Motion to Exclude (Paper 32, "PO Mot.") certain evidence submitted by Petitioner. Petitioner

[2] On June 9, 2017, we granted motions for joinder filed by GlobalFoundries U.S. Inc. ("GlobalFoundries") in Cases IPR2017-00925 and IPR2017-00926, and authorized GlobalFoundries to participate in this proceeding only on a limited basis. *See* Paper 20; IPR2017-00925, Paper 13; IPR2017-00926, Paper 12. Although the papers referenced herein were filed by Taiwan Semiconductor Manufacturing Company, Ltd., we refer to both entities as "Petitioner" throughout this Decision.

filed an Opposition (Paper 40, "Pet. Mot. Opp.") and Patent Owner filed a Reply (Paper 41, "PO Mot. Reply"). An oral hearing was held on August 7, 2017, and a transcript of the hearing is included in the record (Paper 46, "Tr.").[3]

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–12 and 14–18 are unpatentable.

A. The '174 Patent

The '174 patent discloses a "semiconductor device including transistors and connection[s] between the transistors for constituting [a large-scale integration (LSI) integrated circuit (IC)] with high integration and a decreased area." Ex. 1001, col. 1, ll. 13–16. At the time of the '174 patent, various improvements had been made in semiconductor manufacturing due to "increasing demands for more refinement of the semiconductor device." *Id.* at col. 1, ll. 17–22. The '174 patent describes one known method of forming an isolation structure (for shielding devices from each other on a substrate) known as Local Oxidation of Silicon (LOCOS), which was "conventionally adopted in view of its simpleness and low cost." *Id.* at col. 1, ll. 22–25. The LOCOS isolation method involves selective oxidation of a silicon substrate, but has a disadvantage in that it results in a "bird's beak" overhanging area of silicon dioxide. *Id.* at col. 1, ll. 29–31. "As a result, the dimension of a transistor is changed because an

[3] Pursuant to our authorization provided to the parties by email, the parties filed a joint errata to the hearing transcript (Paper 47).

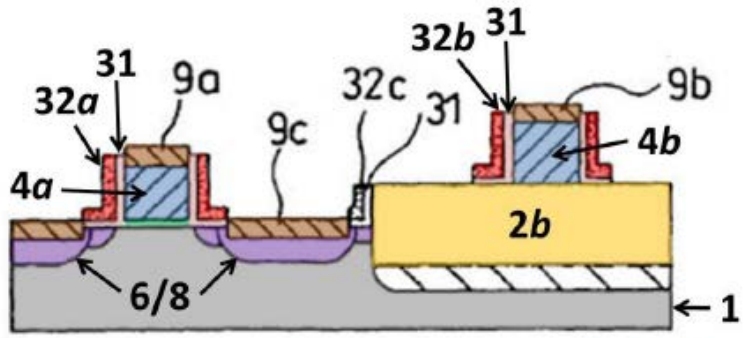
insulating film of the isolation invades [the] transistor region against the actually designed mask dimension." *Id.* at col. 1, ll. 31–34. According to the '174 patent, compared to LOCOS, "trench buried type isolation" (or "trench isolation") was determined to be "more advantageous for manufacturing a refined semiconductor device." *Id.* at col. 1, ll. 25–28.

The '174 patent describes a "conventional semiconductor device" with a trench isolation structure "whose top surface is flattened so as to be at the same level as the top surface of the silicon substrate" (as shown in Figure 17) or whose top surface is higher than the surface of the silicon substrate (as shown in Figure 20(e)). *Id.* at col. 1, l. 52–col. 2, l. 6 (structure 2b), col. 4, l. 16–col. 5, l. 11 (trench isolation 105a). By using the "conventional trench isolation" structure, "the dimensional change of the source/drain region can be suppressed because the bird's beak" created using LOCOS is avoided. *Id.* at col. 4, ll. 16–19, col. 5, ll. 12–17. According to the '174 patent, using the trench isolation method caused various problems of its own due to the etching required. *Id.* at col. 5, ll. 21–58.

The '174 patent describes various embodiments of semiconductor devices and methods of manufacturing the same. The manufacturing process for Embodiment 10 is depicted in the sequence of Figures 12, 13(a)–(e), and 15(a)–(f). *Id.* at col. 21, ll. 33–34, col. 26, ll. 36–45 (referring to the previously described process of Embodiment 8).

Petitioner provides on page 13 of the Petition a colored and annotated version of Figure 15(f) of the '174 patent, reproduced below, which is consistent with the '174 patent's disclosure.

FIG. 15(f)



1—Substrate (Si)
2—Trench Isolation (SiO_2)
3—Gate Insulating Film (SiO_2)
4—Gate Electrode/Interconnect (poly-Si)
31—Protection Oxide Film (SiO_2)
32—Sidewall (SiN)
6/8—Source/Drain Region
9—Silicide

The figure above depicts a device including isolation 2b, which is the result of forming a trench in silicon substrate 1 and filling it with insulating material. *Id.* at col. 21, ll. 39–50, col. 22, ll. 34–44. "[E]lectrode sidewalls 32a, interconnection sidewalls 32b and a step sidewall 32c each having an L-shape remain on the sides of the gate electrode 4a, the gate interconnection 4b and the step portion, respectively." *Id.* at col. 27, ll. 4–8. The '174 patent describes various advantages of forming "L-shaped sidewalls" in the manner disclosed. *Id.* at col. 27, ll. 34–47.

B. Illustrative Claim

Claim 1 of the '174 patent recites:

> 1. A semiconductor device, comprising:
>
> a trench isolation surrounding an active area of a semiconductor substrate;
>
> a gate insulating film formed over the active area;
>
> a gate electrode formed over the gate insulating film;

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