Petitioner's Demonstratives

Taiwan Semiconductor Manufacturing Co.
v.
Godo Kaisha IP Bridge 1

Case Nos. IPR2016-01246, -01247
U.S. Patent No. 7,126,174

TSMC Exhibit 1060
TSMC v. IP Bridge
IPR2016-01246

BACKGROUND

References and Instituted Grounds

REFERENCES*

Inventor	Application Date	Publication No.
Lee et al.	October 17, 1989	U.S. Patent No. 5,153,145
Lowrey et al.	February 26, 1990	U.S. Patent No. 5,021,353
Noble et al.	September 3, 1982	U.S. Patent No. 4,506,434
Ogawa et al.	December 28, 1994	U.S. Patent No. 5,539,229

*IP Bridge does not contest status of these references as prior art.

GROUNDS

IPR Number	Prior Art	Claims
IPR2016-01246	Lee, Noble	1–3, 5–7, 9–12, and 14–18
IPR2016-01246	Lee, Ogawa	1–3, 5–7, 9–12, and 14–18
IPR2016-01247	Lowrey, Noble	1, 4, 5, 8–12, 14, and 16
IPR2016-01247	Lowrey, Ogawa	1, 4, 5, 8–12, 14, and 16

Institution Decision (Paper 8) at 5–6

Claim 1 of the '174 Patent

[1.1] 1. A semiconductor device, comprising:

[1.2] a trench isolation surrounding an active area of a semiconductor substrate;

[1.3] a gate insulating film formed over the active area;

[1.4] a gate electrode formed over the gate insulating film;

[1.5] first L-shaped sidewalls formed over the side surfaces of the gate electrode;

[1.6] first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area

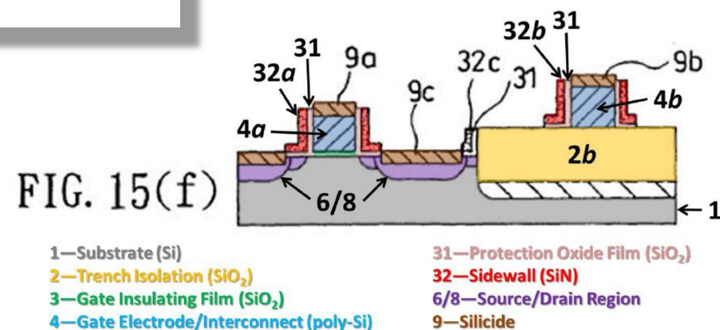
[1.7] an interconnection formed on the trench isolation; and

[1.8] second L-shaped sidewalls formed over the side surfaces of the interconnection.

EX1001 at 29:39–50.

Claim 1 of the ’174 Patent

[1.1] 1. A semiconductor device, comprising:
[1.2] a trench isolation surrounding an active area of a semiconductor substrate;
[1.3] a gate insulating film formed over the active area;
[1.4] a gate electrode formed over the gate insulating film;
[1.5] first L-shaped sidewalls formed over the side surfaces of the gate electrode;
[1.6] first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area
[1.7] an interconnection formed on the trench isolation; and
[1.8] second L-shaped sidewalls formed over the side surfaces of the interconnection.

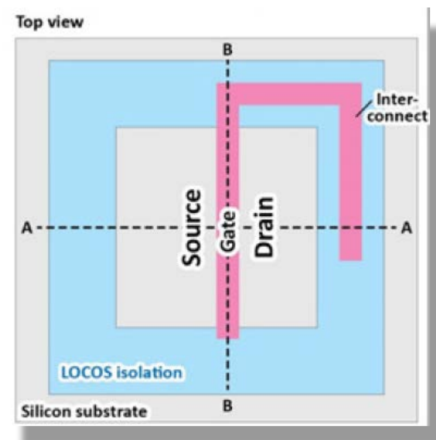


’174 Patent, FIG. 15(f)

EX1001 at 29:39–50, FIG. 15(f); 1246 Petition (Paper 2) at 13; 1247 Petition (Paper 2) at 13.

Device Isolation

- **Isolation**
  - "In silicon integrated circuit fabrication it is necessary to isolate devices from one another which are built into the same silicon matrix. They are subsequently interconnected to create the desired circuit configuration." Schuegraf, EX1009, at 1:11–15.
  - "[B]uried insulating layers each . . . surrounds a portion of a semiconductor substrate in which elements are fabricated, the buried insulating layers functioning to isolate from one another, each element fabricated in a chip." Ogawa, EX1010, at 1:11–15.



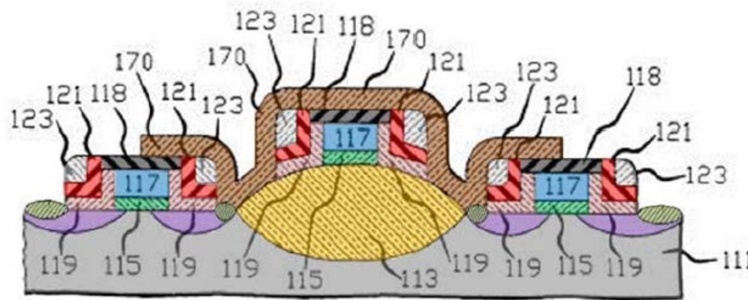
E.g., EX1009 at 1:11–15; EX1010 at 1:11–15; EX1056 at 79:17–80:5; Response (Paper 14) at 54, 111.

OBVIOUSNESS

COMBINATIONS

Lee Teaches Everything Except Trench Isolation

FIG. 15



111—Substrate (Si)
113—LOCOS Field Oxide (SiO_2)
115—Gate Oxide (SiO_2)
117—Gate Electrode/Interconnect (poly-Si)
118—Protective Nitride (SiN or SiON)
(Appended)—Optional Silicide
119—Spacer (SiO_2)
121—Spacer (SiN or SiON)
123—Spacer (TEOS or BPTEOS SiO_2)
170—Conductor (poly-Si, Al, Au, W, silicide, etc.)
300/301/302 (not labeled)—Source/Drain

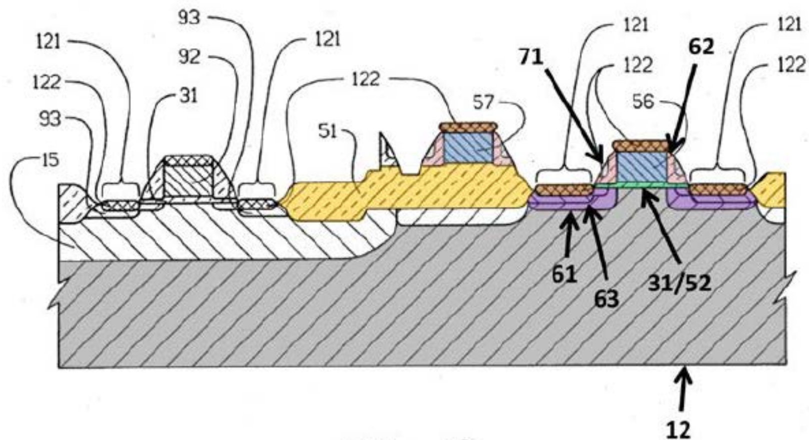
Lee, FIG. 15 (silicide appended)

1. A semiconductor device, comprising:
a trench isolation surrounding an active area of a semi-conductor substrate;
a gate insulating film formed over the active area;
a gate electrode formed over the gate insulating film;
first L-shaped sidewalls formed over the side surfaces of the gate electrode;
first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area
an interconnection formed on the trench isolation; and
second L-shaped sidewalls formed over the side surfaces of the interconnection.

- Lee uses LOCOS isolation instead of trench isolation

EX1001 at 29:39–50; 1246 Petition (Paper 2) at 13, 17–18; EX1002 at FIG. 15.

Lowrey Teaches Everything Except Trench Isolation



12—Substrate (Si)
51—LOCOS Field Oxide (SiO_2)
31/52—Gate Oxide (SiO_2)
56/57—Gate Electrode/Interconnect (poly-Si)
62—Mini-Spacer Oxide (SiO_2)
71—First Spacer Oxide Layer (SiO_2)
61/63/121—Source/Drain
122—Silicide ($TiSi_2$)

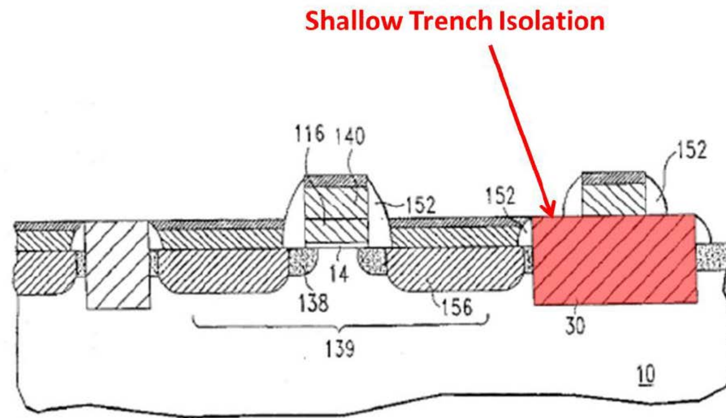
Lowrey, FIG. 12

1. A semiconductor device, comprising:
a trench isolation surrounding an active area of a semiconductor substrate;
a gate insulating film formed over the active area;
a gate electrode formed over the gate insulating film;
first L-shaped sidewalls formed over the side surfaces of the gate electrode;
first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area
an interconnection formed on the trench isolation; and
second L-shaped sidewalls formed over the side surfaces of the interconnection.

- Lowrey uses LOCOS isolation instead of trench isolation

EX1001 at 29:39–50; 1247 Petition (Paper 2) at 13, 17–18; EX1017 at FIG. 12.

Noble: Trench Isolation in a Semiconductor Device

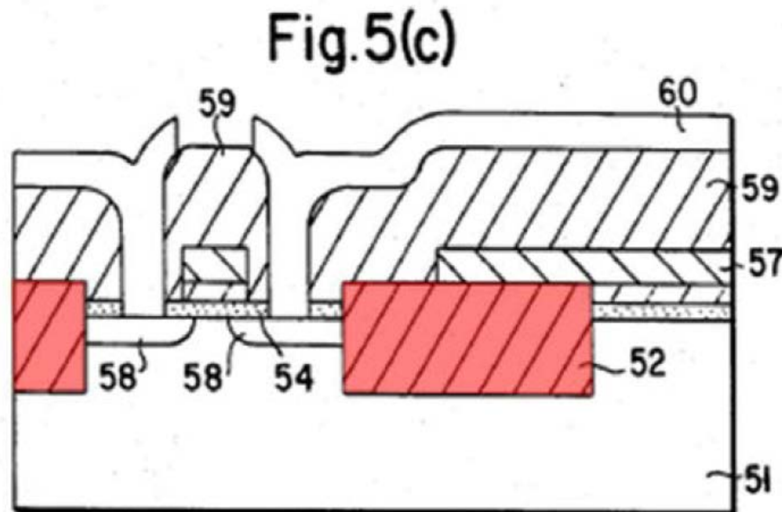


Noble, FIG. 13

1. A semiconductor device, comprising:
a trench isolation surrounding an active area of a semiconductor substrate;
a gate insulating film formed over the active area;
a gate electrode formed over the gate insulating film;
first L-shaped sidewalls formed over the side surfaces of the gate electrode;
first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area
an interconnection formed on the trench isolation; and
second L-shaped sidewalls formed over the side surfaces of the interconnection.

1246 Petition (Paper 2) at 32; 1247 Petition (Paper 2) at 31; EX1015 at FIG. 13.

Ogawa Trench Isolation in a Semiconductor Device



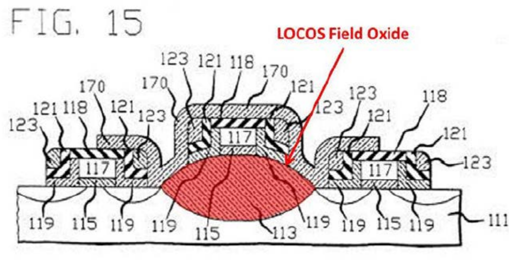
Ogawa, Fig. 5(c)

1. A semiconductor device, comprising:
a trench isolation surrounding an active area of a semi-conductor substrate;
a gate insulating film formed over the active area;
a gate electrode formed over the gate insulating film;
first L-shaped sidewalls formed over the side surfaces of the gate electrode;
first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area
an interconnection formed on the trench isolation; and
second L-shaped sidewalls formed over the side surfaces of the interconnection.

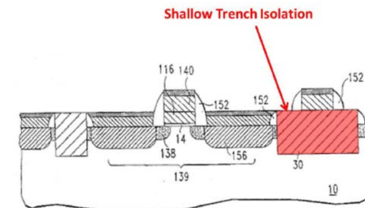
1246 Petition (Paper 2) at 77; 1247 Petition (Paper 2) at 69; EX1010 at Fig. 5(c).

The Asserted Obviousness Grounds

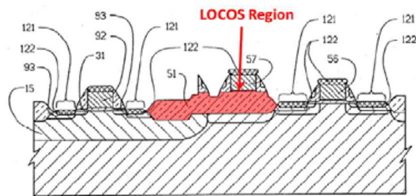
- "[Lee/Lowrey] teaches every limitation of the challenged claims except trench isolation. A POSITA would have understood that [Noble's/Ogawa's] STI was a known substitute for [Lee's/Lowrey's] LOCOS isolation. The combined teachings discussed in this section refer to **the teachings of [Lee/Lowrey], with its LOCOS isolation replaced by [Noble's/Ogawa's] STI**."



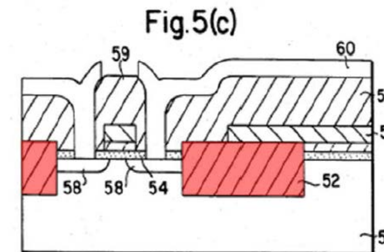
Lee, FIG. 15



Noble, FIG. 13



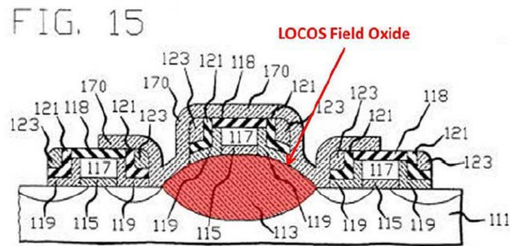
Lowrey, FIG. 12



Ogawa, FIG. 13

1246 Petition (Paper 2) at 21, 32, 33, 70, 77; 1247 Petition (Paper 2) at 21, 31, 32, 62, 69.

The Resulting Combinations (i.e., “How”)



Lee, FIG. 15

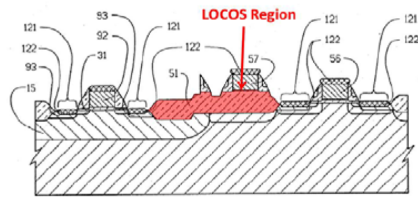
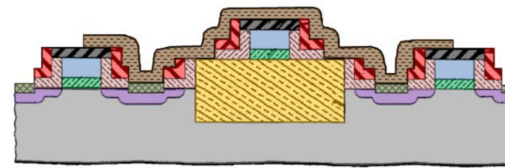


FIG. 12

Lowrey, FIG. 12

FIG. 15′



Substrate (Si)
Trench Isolation (SiO_2)
Conductor (poly-Si, Al, Au, W, silicide, etc.)
Gate Electrode/Interconnection (poly-Si)
Protective Nitride (Si_3N_4 or SiON)
Spacer (SiO_2)
Spacer (Si_3N_4 or SiON)
Gate Oxide (SiO_2)
Optional Silicide
Optional LDD Source/Drain

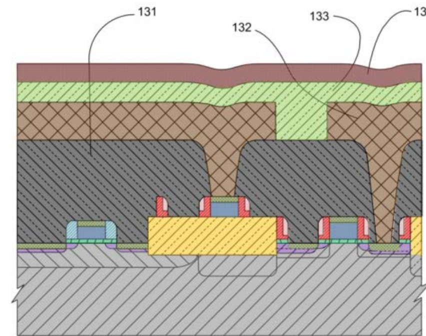


FIG. 13′

Substrate (Si)
Trench Isolation (SiO_2)
Metal Layer (Al)
Gate Electrodes/Interconnections (poly-Si)
Gate Oxide (SiO_2)
Oxide Isolation Layer
Nitride Passivation Layer
Mini-Spacer Oxide (SiO_2)
First Spacer Oxide (SiO_2)
Second Spacer Oxide (SiO_2)
Silicide ($TiSi_2$)
LDD Source/Drain
Oxide Passivation Layer

1246 Petition (Paper 2) at 33; 1247 Petition (Paper 2) at 32; Reply (Paper 21) at 20, 25; EX1057 at 57, 87.

MOTIVATION

The LOCOS Bird's Beak Was a Well-Known Issue for Scaling

In spite of its success, several limitations of LOCOS technology have driven the development of alternative isolation structures. A well-known limitation in LOCOS isolation is that of oxide undergrowth at the edge of the mask which defines the active regions of the substrate. This so-called bird's beak (as it appears) poses a limitation to device density, since that portion of the oxide adversely influences device performance while not significantly contributing to device isolation. Another problem associated

Schuegraf, EX1009, at 1:29–43

Evolution of isolation with DRAM generations

The IBM 4Mb DRAM contained many innovative process features, but elected to employ the conventional LOCOS process for device isolation. It has the lowest cost and is a well-understood "industry standard" process, but it has two major disadvantages. One is area loss to the "bird's-beak" phenomenon at the isolation boundary, which remains at approximately 0.10–0.15 μm per edge and thus becomes an ever-increasing fraction of the total lithographically limited isolation pitch. A second drawback is isolation oxide thinning in very narrow isolation areas due to multidimensional oxidation effects [18].

Adler, EX1025, at 8

1246 Petition (Paper 2) at 4–7, 10, 21–30, 70–76; 1247 Petition (Paper 2) at 4–7, 10, 21–30, 62–68; Reply (Paper 21) at 2, 8, 38; EX1009 at 1:30–2:22; EX1025 at 8–10.

The LOCOS Bird's Beak Was a Well-Known Issue for Scaling

EX1034, 1:60-64; EX1046, 557; EX1053, 636; Paper 14, at 8, 69. Even IPB's declarant agrees with the premises underlying the combinations of references. EX1056, 78:9-17 ("[B]oth structures are isolation structures."), 76:8-9 ("[Y]es, there is a concern that LOCOS uses up too much real estate."), 76:11-78:2 ("Trench isolation was considered at that time, and was one of the candidates [for replacing LOCOS].").

Reply (Paper 21) at 2

Reply (Paper 21) at 2; EX1056 at 76:5–78:17.

LOCOS Isolation Was Becoming Obsolete

- **LOCOS was** “**unallowable** in the refinement of a semiconductor device **after the 0.5 µm generation**,” and “**IBM** corporation has introduced the trench isolation structure as a 0.5 µm CMOS process for the mass-production of an MPU.” ’174 Patent, EX1001 at 1:29–43.

area. As a result, STI became the complete answer for both storage-trench capping and standard device isolation beginning with the 16Mb generation.

Adler, EX1025, at 9, (Jan./Mar. 1995)

The extendability of the basic STI process has been demonstrated in the 64Mb and 256Mb DRAM processes being developed by IBM and its alliance partners. While

Adler, EX1025, at 10, (Jan./Mar. 1995)

	1995 0.35 µm	1998 0.25 µm	2001 0.18 µm	2004 0.13 µm	2007 0.10 µm	2010 0.07 µm
Isolation	LOCOS/STI†/SOI	STI†/SOI				

1994 NTRS, EX1054, at 60 Tbl. 6

Table 3 Comparison of last generation of LOCOS isolation with first generation of STI isolation in IBM DRAMs.

Parameter	*4 Mb (LOCOS)*	*16 Mb (STI)*
Process complexity	Low	High (50% increase in number of steps)
Minimum isolation width, drawn dimension	0.5 µm	0.55 µm
Minimum active area width, drawn dimension	1.3 µm	0.60 µm
Nominal isolation oxide thickness	240 nm	570 nm
Surface topography (step height)	90 nm	50 nm
Active area width reduction (drawn wafer)	0.45–0.75 µm	0.10–0.25 µm
Depth of isolation oxide (position of bottom below silicon surface)	0.25 µm	0.55 µm

Adler, EX1025, at 9 Tbl. 3

1246 Petition (Paper 2) at 4–7, 21–30, 70–76; 1247 Petition (Paper 2) at 4–7, 21–30, 62–68; EX1001 at 1:29–43; EX1025 at 8–10, Tbl. 3; EX1054 at 60, Tbl. 6.

LOCOS/STI Were Interchangeable Functional Equivalents

Shallow-trench isolation (STI), an alternative to LOCOS, offers the possibility of true lithographically limited pitch and feature size, low thermal cycle, and improved surface planarity. It is accomplished by etching isolation trenches into the silicon wafer, depositing oxide to fill them, and planarizing the surface. Its major

Adler, EX1025, at 9

wide). Shallow Trench Isolation (STI) is used primarily for isolating devices of the same type and is often considered an alternative to LOCOS isolation. Shallow trench isolation has

Schuegraf, EX1009, at 2:20–22

Although the isolation is composed of the LOCOS film in the above embodiments, the present invention is not limited thereto. The present invention is also applicable to an isolation of trench structure or the like.

Ueda, EX1014, at 22:48–52

Field oxide **12**, preferably silicon dioxide (SiO_2), is grown or deposited in selected portions of the surface of the substrate **10** for isolation of active regions from one another according to the well known local oxidation (LOCOS) isolation technique; of course, other isolation techniques such as trench isolation may alternatively be used. The active transistors of the integrated circuit

Douglas, EX1011, at 4:10–16

The n and p well of FIG. **1** are isolated from one another by a recessed isolation region specifically, trench **10**. Additionally, within the n well **21** there are other isolation trenches **12** for isolating from one another p-channel transistors formed within the n well. Likewise, there are isolation trenches **13** formed within the p well to isolate n-channel transistors formed in the p well from one another. The isolation trenches may be formed using well-known technology. Other isolation technologies such as local oxidation of silicon (LOCOS) may be used instead of trenches

Thompson, EX1012, at 3:1–10

E.g., 1246 Petition (Paper 2) at 4–7, 21–30, 70–76; 1247 Petition (Paper 2) at 4–7, 21–30, 62–68; Reply (Paper 21) at 2–17; EX1009 at 2:20–22; EX1010 at 1:24–66; EX1011 at 4:10–16; EX1012 at 3:8–10; EX1014 at 22:49–52; EX1015 at 3:35–37; EX1025 at 8–10.

Patent Owner Admits Using STI was not New to the '174 Patent

The '174 patent contains 21 figures. Figures 17-21 are identified as prior art, and are contrasted with Figures 1-16 which illustrate various embodiments of the invention. Trench isolation appears both in the prior art Figures and the Figures of the invention such that it is apparent that the inclusion of trench isolation *per se* was never portrayed as being something new or unique to the '174 patent.

Preliminary Response (Paper 7) at 16.

Board Decision

Petitioner provides a detailed explanation for why a person of ordinary skill in the art would have been motivated to replace Lee's LOCOS with trench isolation, as taught by Noble, with supporting testimony from Dr. Banerjee. *Id.* at 21–30 (citing Ex. 1004 ¶¶ 82–97). For example,

[5] Patent Owner notes the additional cited references, but states that its arguments only address the prior art references that make up each asserted ground. Prelim. Resp. 20. We have reviewed Petitioner's citations to the other references and are persuaded, based on the current record, that they appropriately show the background knowledge that a person of ordinary skill in the art would have had in reading Lee and Noble, and why a person of ordinary skill in the art would have been motivated to make the asserted combination. *See Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015); *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362–63 (Fed. Cir. 2013). We also agree with Petitioner, based on the current record, that the references are prior art because the challenged claims are not entitled to the July 27, 1995 filing date of Japanese Patent Application No. 7-192181, such that the earliest potential effective filing date would be December 19, 1995. *See* Pet. 14–15 (citing Exs. 1019, 1020); Prelim. Resp. 20 (not disputing Petitioner's assertion for purposes of the Preliminary Response, but reserving the right to contest the effective filing date during trial).

Institution Decision (Paper 8) at 12, 13 n.5.

POSITA'S REASONABLE EXPECTATION OF SUCCESS

Petition Shows a Reasonable Expectation of Success

Ueda also teaches, "Although the isolation is composed of the LOCOS film in the above embodiments, . . . [t]he present invention is also applicable to an isolation of trench structure or the like." (*Id.*, 22:49–52.) *Ueda* even discloses how to form trench isolation. (*See id.*, 13:14–63.) Figures 12(a) through 12(f) of *Ueda*

1246 Petition at 25

the claims. LOCOS and STI are both methods for forming insulating materials in the same locations of the substrate to perform the same function. They are both performed near the very beginning in device processing, and how the isolation regions are formed would not affect *Lee*'s processes or the resultant device structures. It is therefore my opinion that the combined teachings of *Lee* and *Noble*

EX1004 at ¶ 82

E.g., 1246 Petition (Paper 2) at 25; 1247 Petition (Paper 2) at 25; EX1004 at ¶¶ 82, 198; EX1024 at ¶¶ 93, 173; EX1014 at 13:14–63.

A POSITA Knew How to Make STI

- IPB's declarant admitted, "The person of ordinary skill in the art would know that there are multiple ways how to form a LOCOS isolation. The person of ordinary skill in the art would also know that there are multiple [ways] to form a trench isolation." **EX1056 at 145:11–15**; *see also* **EX1059 at 2**.
- Thompson shows a POSITA knows how to form STI, and how it is an alternative to LOCOS isolation. **EX1012 at 3:1–10** (discussing FIG. 1).
  - "The isolation trenches may be formed using well-known technology. Other isolation technologies such as local oxidation of silicon (LOCOS) may be used instead of trenches." **EX1012 at 3:8–10**.

EX1012 at 3:1–10; EX1056 at 145:11–15; EX1059 at 2.

A POSITA Knew STI Could Substitute for LOCOS Isolation in 1996

- In early 1995, **IBM** announced it had been replacing LOCOS isolation with STI in commercial devices for several years.
- Numerous references mention the substitutability of STI for LOCOS. *See ,e.g*., **EX1057 at 33–34**.
- "Although the isolation is composed of the LOCOS film in the above embodiments, the present invention is not limited thereto. The present invention is also applicable to an isolation of trench structure or the like." **Ueda, EX1014 at 22:49–52**.
- "Shallow Trench Isolation (STI) is used primarily for isolating devices of the same type and is often considered an alternative to LOCOS isolation." **Schuegraf, EX1009 at 2:20–22**.

1246 Petition (Paper 2) at 4–7, 21–30, 70–76; 1247 Petition (Paper 2) at 4–7, 21–30, 62–68; Reply (Paper 21) at 2–17; EX1001 at 1:29–43; EX1009 at 2:20–22, EX1014 at 22:49–52; EX1057 at 33–34.

A POSITA Knew STI Could Substitute for LOCOS Isolation in 1996

- "Field oxide 12, preferably silicon dioxide (SiO_2), is grown or deposited in selected portions of the surface of the substrate 10 for isolation of active regions from one another according to the well known local oxidation (LOCOS) isolation technique; of course, other isolation techniques such as trench isolation may alternatively be used." **Douglas, EX1011 at 4:10–16**.
- "To overcome the foregoing drawbacks [with LOCOS], a method wherein each element is isolated from one another by buried insulating layers which are grown to fill grooves produced along the surface of a silicon (Si) substrate to surround each element, has been developed and is presently being used." **Ogawa, EX1010 at 1:24–66**.

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1246 Petition (Paper 2) at 4–7, 10, 21–30, 70–76 ; 1247 Petition (Paper 2) at 4–7, 10, 21–30, 62–68; EX1011 at 4:10–16; EX1010 at 1:24–66.

A POSITA Knew STI Could Substitute for LOCOS Isolation in 1996

- "This technology can be scaled to the 1 Gbit DRAM generation with minor modifications, such as replacing LOCOS with trench isolation . . . ." **Kang, et al., EX1053 at 2, Fig. 1**.
- "As the miniaturizing and integration densities of semiconductor integrated circuits increase, the conventional selectively oxidized film (LOCOS) method used for isolating circuit elements has been replaced by the shallow trench method." **Sato, EX1034 at 1:60–64**.
- "Trench isolation will also be incorporated into more BiCMOS structures. Such trench-isolated BiCMOS processes have already been reported . . . ." **S. Wolf, EX1046 at 30**.

Reply (Paper 21) at 2–17; EX1034 at 1:60–64; EX1046 at 30; EX1053 at 2, Fig. 1; EX1057 at 26–50.

A POSITA Knew STI Could Substitute for LOCOS Isolation in 1996

- "The purpose of this paper is to present the newly developed field isolation technology which overcomes these difficulties [of LOCOS]." **Kurosawa, EX1052, at 1**.
- "LOCOS is not expected to scale significantly beyond 1 μm pitch due to its intrinsic limitations such as field oxide thinning, bird's beak encroachment, lack of planarity, and punchthrough. As a result, trench isolation is required to meet the demands of ULSI." **Poon, EX1048, at 1**.
- "LOCOS-based isolation is used almost exclusively in the fabrication of ICs due to its simplicity. However, it is widely recognized that LOCOS-based technology cannot be extended to deep submicrometer dimensions because of lateral oxide encroachment and field oxide thinning in narrow isolation regions. Trench isolation has been proposed as a potential LOCOS replacement in scaled and high-performance ULSI." **Fry, EX1047, at 8–10**.

Reply (Paper 21) at 2–17; EX1047 at 8–10; EX1048 at 1; EX1052 at 1; EX1057 at 26–50.

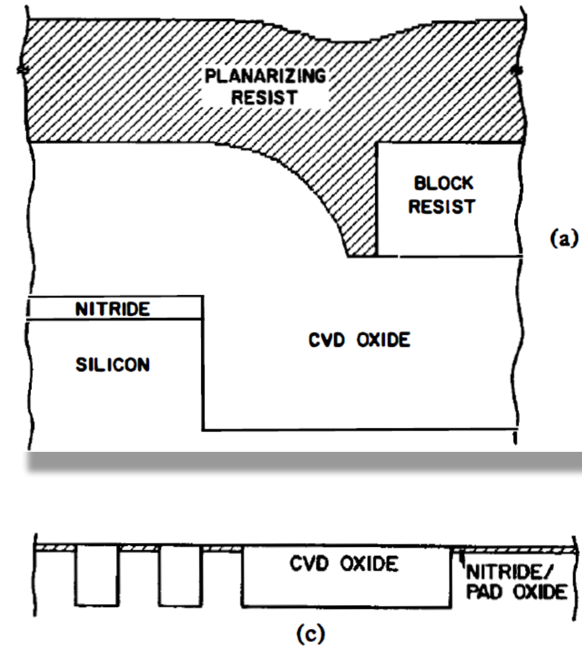
A POSITA Knew STI Could Substitute for LOCOS Isolation in 1996

Shallow-trench isolation (STI), an alternative to LOCOS, offers the possibility of true lithographically limited pitch and feature size, low thermal cycle, and improved surface planarity. It is accomplished by etching isolation trenches into the silicon wafer, depositing oxide to fill them, and planarizing the surface. Its major

application of planarization polymer. Reactive ion etch (RIE) of the oxide–polymer stack and chemical-mechanical polishing (CMP) to remove deposited oxide from the active areas complete the planarization process [19]. **Figures 10**

Adler (IBM), EX1025 at 9 (citing Davari, EX1055)

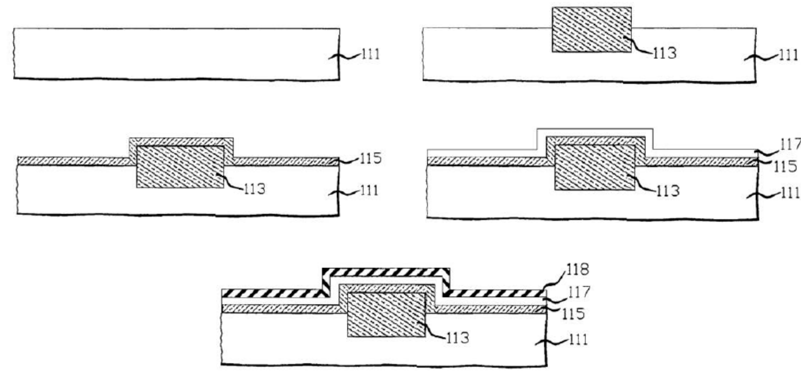
19. B. Davari, C. W. Koburger, R. Schulz, J. D. Warnock, T. Furukawa, M. Jost, Y. Taur, W. G. Schwittek, J. K. DeBrosse, M. L. Kerbaugh, and J. L. Mauer, "A New Planarization Technique, Using a Combination of RIE and Chemical Mechanical Polish (CMP)," *IEDM Tech. Digest*, p. 861 (1989).



Davari, EX1055, at FIGS. 2(a), 1(c)

EX1025 at 9, 20; EX1055 at 1–3.

A POSITA Knew How to Integrate the STI into Lee's Device



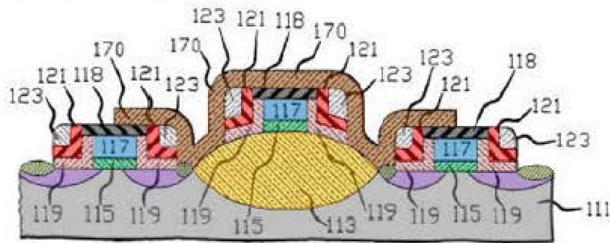
Trivial Substitute Process Sequence

polish/etch-stop and pad oxide, and formed the gate stack. EX1057, ¶¶79-83. IPB provides no basis for asserting a POSITA would have retained the polish/etch-stop and pad oxide as the gate stack. That assertion makes no sense because, as the following figures illustrate, removing those features makes trivial the substitution, TSMC described in its Petitions. EX1057, ¶¶80-83; Paper 2, at 21, 70.

Reply (Paper 21) at 18–20; EX1057 at 50–57.

The Result of the Combination of Lee and Noble/Ogawa

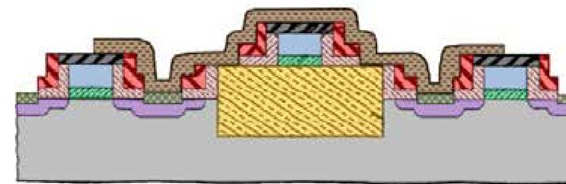
FIG. 15



111—Substrate (Si)
113—LOCOS Field Oxide (SiO_2)
115—Gate Oxide (SiO_2)
117—Gate Electrode/Interconnect (poly-Si)
118—Protective Nitride (SiN or SiON)
(Appended)—Optional Silicide

119—Spacer (SiO_2)
121—Spacer (SiN or SiON)
123—Spacer (TEOS or BPTEOS SiO_2)
170—Conductor (poly-Si, Al, Au, W, silicide, etc.)
300/301/302 (not labeled)—Source/Drain

FIG. 15'



Substrate (Si)
Trench Isolation (SiO_2)
Conductor (poly-Si, Al, Au, W, silicide, etc.)
Gate Electrode/Interconnection (poly-Si)
Protective Nitride (Si_3N_4 or SiON)

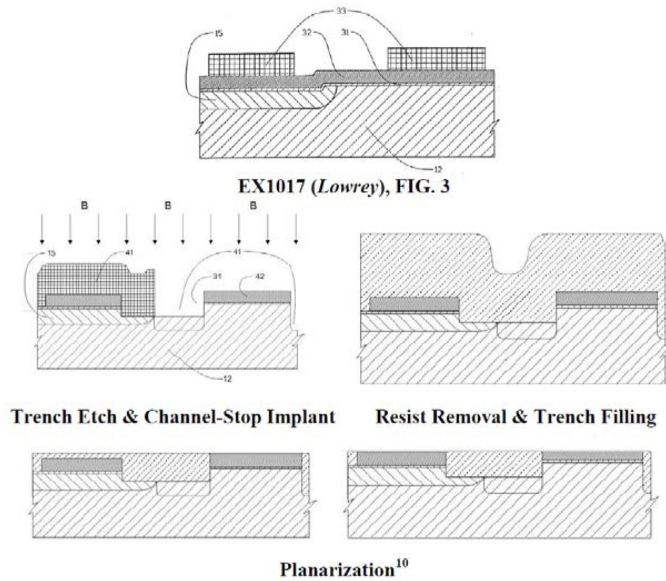
Spacer (SiO_2)
Spacer (Si_3N_4 or SiON)
Gate Oxide (SiO_2)
Optional Silicide
Optional LDD Source/Drain

EX1057 at 57

Reply (Paper 21) at 20; EX1057 at 57.

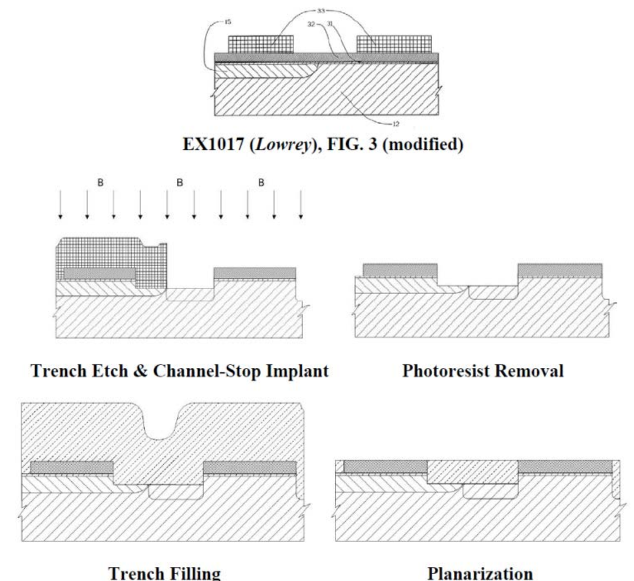
Integrating the STI Process into Lowrey's Device

- **Non-Planar Process**



Reply (Paper 21) at 21

- **Planar Processes**

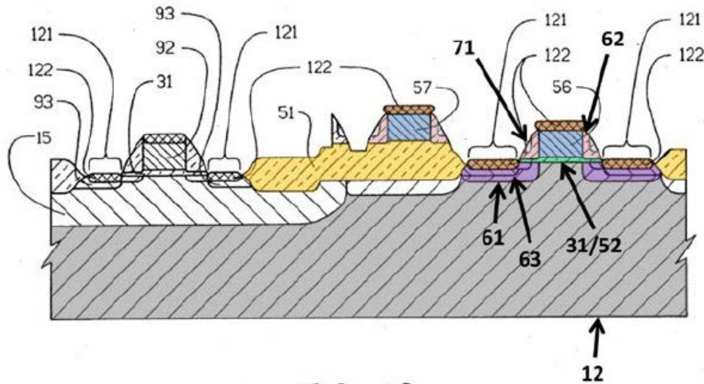


Reply (Paper 21) at 23

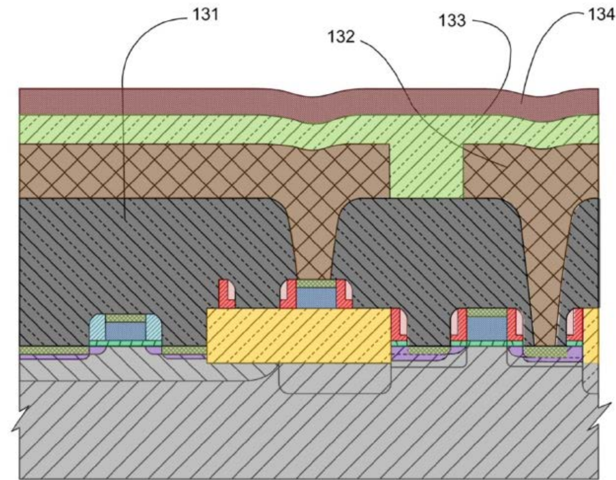
***There should be a "slight jog" under the trenches on the left above, such that the left-hand side of the STI structure is slightly lower than the right-hand side of the STI structure. Reply (Paper 21) at 24 n.12; EX2078 at 194:12–17.**

Reply (Paper 21) at 20–25 & n.12; EX1057 at 57–87 & n.11; EX2078 at 194:12–17.

The Result of the Combination of Lee and Noble/Ogawa



1247 Petition(Paper 2) at 18



Reply (Paper 21) at 25

***The non-planar example would have a "slight jog" under the trench, such that the left-hand side of the STI structure is slightly lower than the right-hand side of the STI structure. Reply (Paper 21) at 24 n.12; EX2078 at 194:12–17**

1247 Petition (Paper 2) at 18; Reply (Paper 21) at 22–25 & n.12; EX1057 at 87; EX2078 at 194:15–17.

Similarity of the LOCOS and STI Processes

You start off with similarly, which is you protect the active regions with silicon nitride, PAD oxide in the case of LOCOS. And that could be used by your etch stop layer, if you want to do in the case of STI.

Then in STI you will have to etch a shallow trench in the silicon, which you don't have to do with LOCOS. And then you refill the thing with CVD oxide, unlike growing a thermal oxide in the case of LOCOS. I am not sure if it is particularly more complicated.

And then you use CMP or maybe resist etch back for planarizing and polishing it down to the etch stop layer, in this case, for example, the silicon nitride layer.

THE WITNESS: I simply wanted to point out there are many ways to skin a cat. So the issue at hand is how does one make a raised STI structure.

And even in Noble and Ogawa, they use an etch stop layer to do so, as do some of the other patents that I listed. And in some cases you etch off -- you remove that etch stop layer prior to continuing the fabrication of the transistor.

In Ogawa and Noble, they chose to retain the etch stop layer to make --

BY MR. GREENBLUM:

Q. Okay.

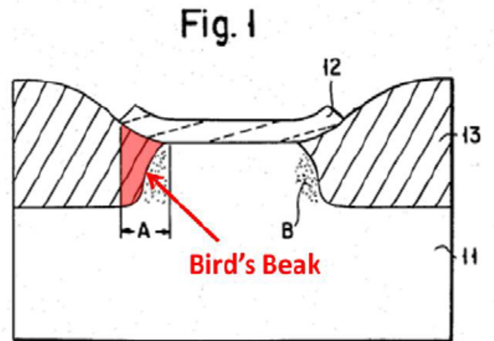
A. -- to make the gates.

Q. So Noble and Ogawa --

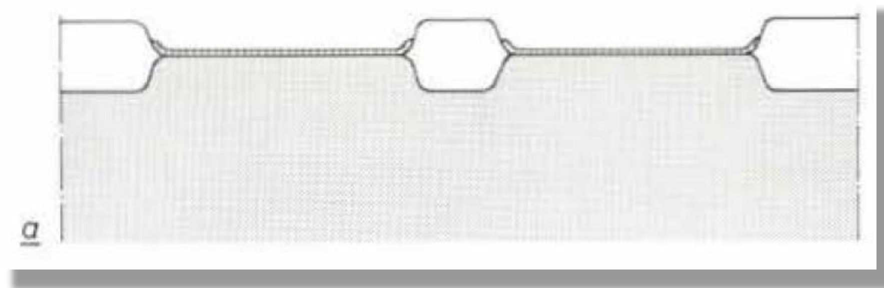
MR. YOCHES: You interrupted him again.

EX2078 at 218:5–22, 243:5–19.

The LOCOS Process



Ogawa, Fig. 1

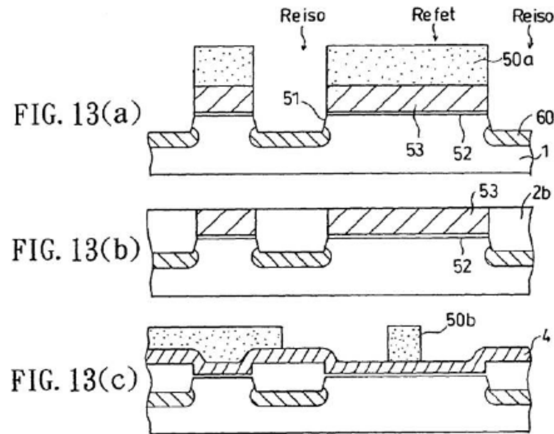


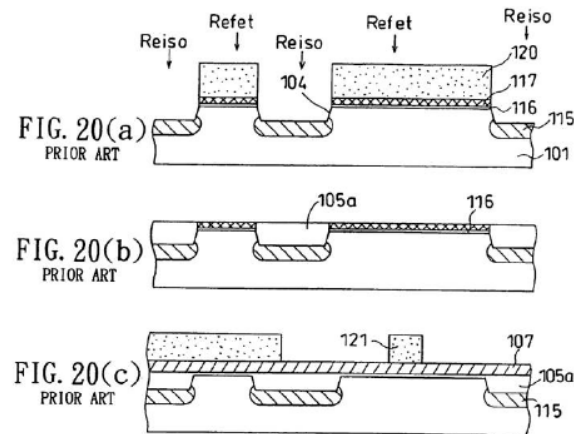
EX1008 at Fig. 2a

- **The LOCOS Process (*see, e.g.*, EX1005 at 10; EX1008 at 3, Fig. 2; EX1017 at 7:57–8:16, FIGS. 1–2):**
  - Deposit optional pad oxide
  - Deposit silicon nitride
  - Define isolation region (by etching nitride only)
  - Form isolation (by thermal oxidation)
  - Remove nitride
  - Remove pad oxide

EX1005 at 10; EX1008 at 3, Fig. 2; EX1010 at 1:33–42; Fig. 1; EX1017 at 7:57–8:16, FIGS. 1–2; EX2078 at 218:5–22.

The STI Process—Admitted Prior Art



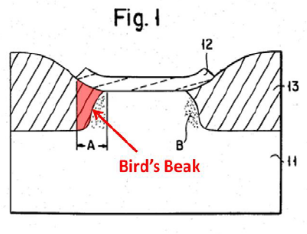


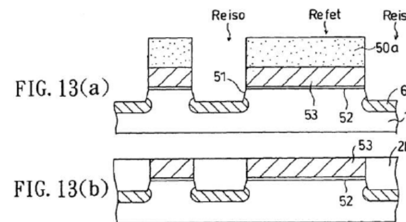
’174 Patent, FIGS. 13(a)–13(b), 20(a)–20(b)

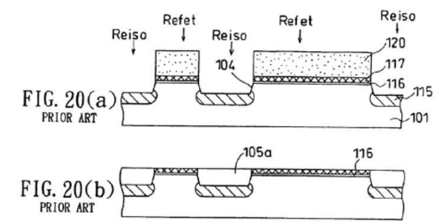
- **The STI Process (*see, e.g.*, EX1001 at 4:16–41 (admitted prior art)):**
  - Deposit optional pad oxide
  - Deposit polish/etch-stop (e.g., silicon nitride) (IBM calls it a planarization block mask (PBM))
  - Define isolation region (by etching polish/etch-stop, pad oxide, and substrate)
  - Form isolation (by CVD oxidation + planarization)
  - Remove polish/etch-stop (e.g., nitride)
  - Remove pad oxide

EX1001 at 4:16–41, 21:33–23:6, 26:36–45; EX1057 at 26–50; EX2078 at 218:5–22, 243:5–19.

Similarity of the LOCOS and STI Processes







The LOCOS Process

- Deposit optional pad oxide
- Deposit silicon nitride
- Define isolation region
  (by etching nitride)
- Form isolation
  (by thermal oxidation)
- Remove nitride
- Remove pad oxide

The STI Process

- Deposit optional pad oxide
- Deposit stopper (e.g., silicon nitride)
- Define isolation region
  (by etching stopper, pad, and substrate)
- Form isolation
  (by CVD oxidation + planarization)
- Remove stopper (e.g., nitride)
- Remove pad oxide

EX1001 at 4:16–41, 21:33–23:6, 26:36–45; EX1005 at 10; EX1008 at 3, Fig. 2; EX1010 at 1:33–42; Fig. 1; EX1017 at 7:57–8:16, FIGS. 1–2; EX1057 at 26–50; EX2078 at 218:5–22, 243:5–19.

Board Decision

Dr. Banerjee elaborates as to why an ordinarily skilled artisan would have been able to make the combination, opining that "LOCOS and STI are both methods for forming insulating materials in the same locations of the substrate to perform the same function," and "[t]hey are both performed near the very beginning in device processing, and how the isolation regions are formed would not affect *Lee*'s processes or the resultant device structures." Ex. 1004 ¶ 82.

Institution Decision (Paper 8) at 14.

OTHER CLAIM LIMITATIONS

PATENT OWNER MISCONSTRUES LOWREY'S L-SHAPED SIDEWALLS

Meaning of "L-Shaped Sidewalls"

- TSMC and the Board felt the plain and ordinary meaning sufficed

which it appears" (37 C.F.R. §42.100(b)), the '174 patent will expire on July 24, 2016, so the *Phillips* standard for claim construction should govern this petition, *see id.* The plain and ordinary meaning as understood by a POSITA should be applied to all claim terms of the '174 patent.

Petitions (Paper 2) at 16

court case involving the '174 patent. Prelim. Resp. 18–20. We also have considered the district court's Order interpreting various claim terms of the '174 patent, dated November 9, 2016. *See* Ex. 3001, 7–11, App'x A. However, for purposes of this Decision, we conclude that no claim terms require interpretation at this time.

Institution Decision (Paper 8) at 7

- IP Bridge advocates the construction the district court adopted, but that appears to be the plain and ordinary meaning

U.S. Patent No. 7,126,174	
Term	Parties' Agreement
"L-shaped sidewalls" (Claims 1, 14)	"sidewalls that substantially resemble a capital letter 'L' or its mirror image"

Response (Paper 14) at 42

41

Petitions (Paper 2) at 16; Institution Decision (Paper 8) at 7; Response (Paper 14) at 42.

IP Bridge Implicitly Adds Another Requirement

- IP Bridge suggests "L-shaped" sidewalls must be "distinguishable" by a specific experimental technique (SEM).

A necessary condition for a sidewall to appear L-shaped is that it is distinguishable from other components of the sidewall. Given that layer **62** is chemically indistinguishable from layer **71**, its physical appearance is indistinguishable from layer **71** as well, and so the sidewall does not substantially resemble an L-shaped component. Exhibit 2012, ¶¶383-386; Exhibits 2026-2030.

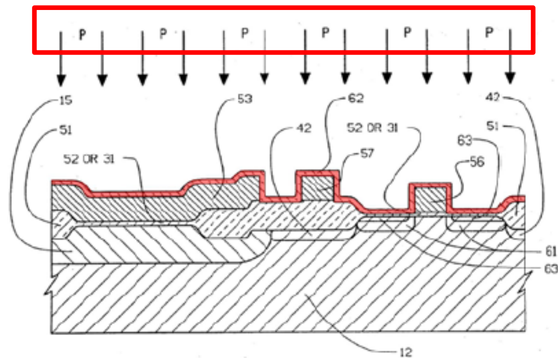
Response (Paper 14) at 104

The shape of the mini spacer oxide layer **62** may have an L-shape when it is initially deposited, but since both layers **62** and **71** are made of the same oxide material, they will ultimately be indistinguishable once layer **62** is applied. That is, a commonly used microscopic assessment technique such as scanning electron microscopy (SEM) of the sidewall structure in 1995 would show the two layers as an indistinguishable entity (Exhibit 2012, ¶¶383-386, 410; Exhibits 2026 - 2030)[16]

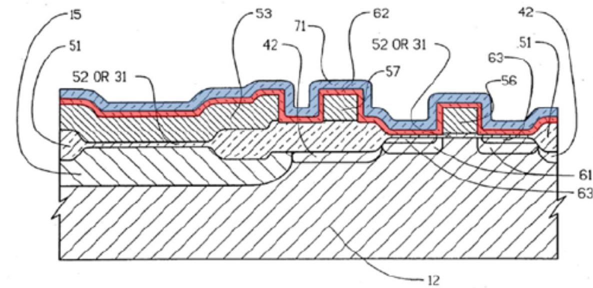
Response (Paper 14) at 103

Response (Paper 14) at 42, 102–04.

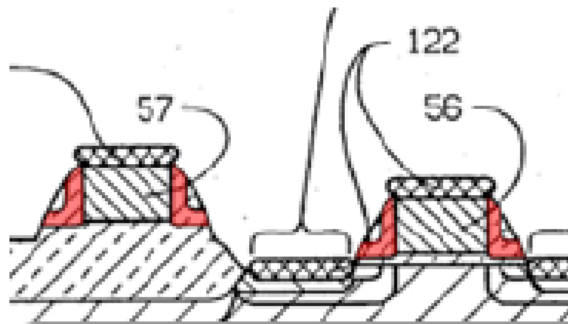
Lowrey Discloses L-Shaped Sidewalls



1247 Petition (Paper 2) at 59



1247 Petition (Paper 2) at 37



1247 Petition (Paper 2) at 59

sidewall made from layer 62 and a wedge-shaped sidewall made from layer 71. Layers 62 and 71 are different layers, formed at different times, with intervening steps between their formation, and the drawings show them as separate layers throughout the process description.

Reply (Paper 21) at 40

1247 Petition (Paper 2) at 35–38, 42–44, 58–59; Reply (Paper 21) at 40–42; EX1017 at 8:58–9:12, FIGS. 6–8, 12; EX1057 at 87–92.

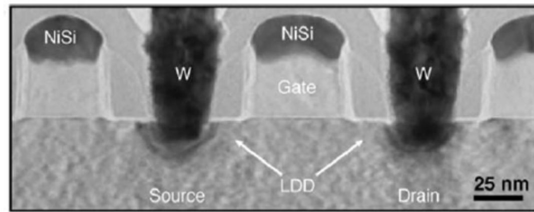
Lowrey's L-Shaped Sidewalls Are Separate

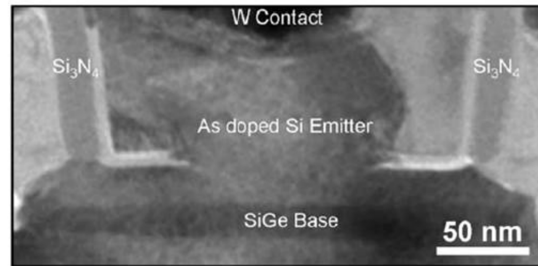
IPB provides no reason an interface would not exist between these two layers. Instead, an interface would likely exist because layer 71 can be formed using CVD which takes place well below the glass transition temperature of SiO_2 in layer 62. EX1057, ¶146.

Reply (Paper 21) at 40

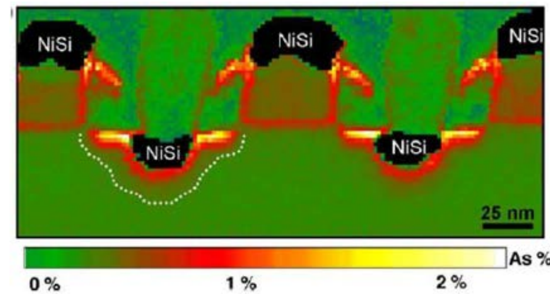
formed, and layer 71 does not contain phosphorous because it is never exposed to a phosphorous treatment. EX1017 at 8:61-9:2, FIG. 6. A POSITA would have understood *Lowrey* includes one L-shaped spacer layer with phosphorous and another without. EX1057, ¶147.

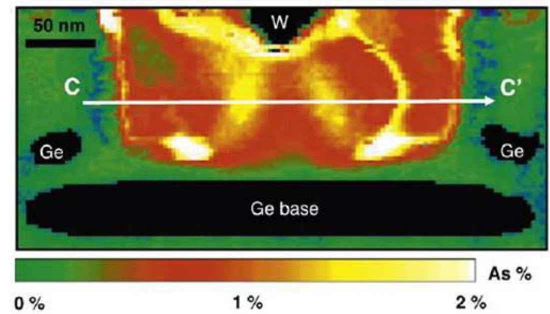
Reply (Paper 21) at 41





Reply (Paper 21)at 42





44

1247 Petition (Paper 2) at 35–38, 42–44, 58–59; Reply (Paper 21) at 40–42; EX1051 at 3–4, Figs. 1, 5; EX1057 at 87–92.

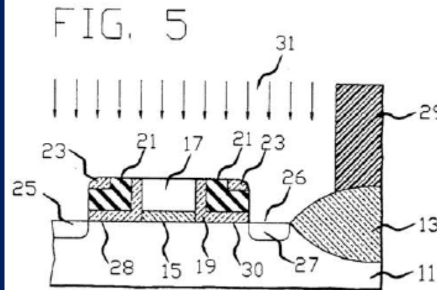
PATENT OWNER'S CRITICISM OF LEE IGNORES LEE'S DISCLOSURE

Lee Discloses Silicide Regions and LDD Doping

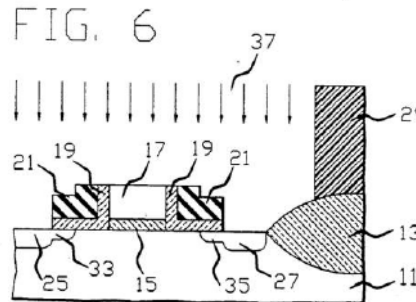
Next, in a manner analogous to that depicted in FIGS. **4-10**, layers **123**, **121**, and (optionally) **119** are anisotropically etched to create spacer layers **119**, **121**, and **123** illustrated in FIG. **14**. Source/drain regions **300**, **301**, and **302** may be formed in a manner similar to that discussed before. Although FIG. **14** shows the shapes of junctions **300**, **301**, and **302** to have standard profiles, lightly doped drain (LDD) profiles may be created, if desired, by the process discussed in connection with FIGS. **5-7**. Should salicidation be desired over source/drain regions **300**, **301**, and **302** it may also be performed in a manner analogous to that depicted in FIG. **9**. Therefore it should be apparent that although FIG. **14** depicts spacer layer **123** adjacent gates **201** and **205** and runner **203**, layer **123** would be removed if a lightly doped drain structure were created. Furthermore, examination of FIG. **14** shows that gates **201** and **205**, unlike the gates of FIGS. **3-10**, has an overlying protective nitride layer **118**. Furthermore, gate runner **203** has a similar overlying protective nitride layer **118'**. Thus it can be seen that the structures depicted in FIG. **14** have at least two protective layers flanking the gate and have an overlying protective nitride layer.

EX1002 at 7:13–35

LDD Doping

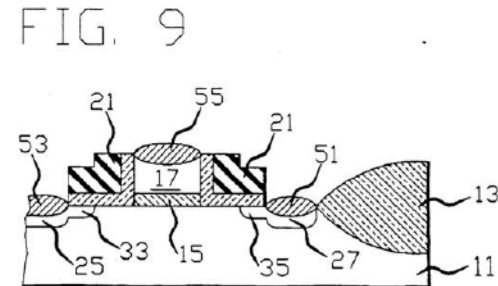


Lee, FIG. 5



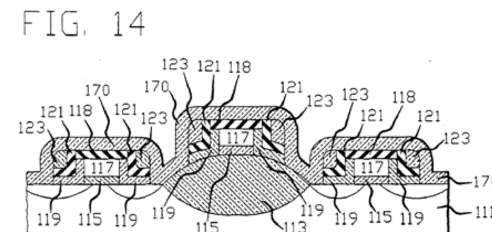
Lee, FIG. 6

Self-Aligned Silicide



Lee, FIG. 9

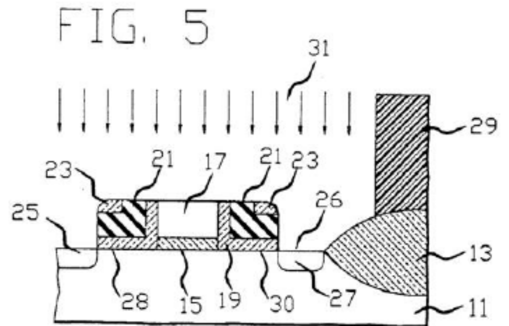
Reference Figure (see text)



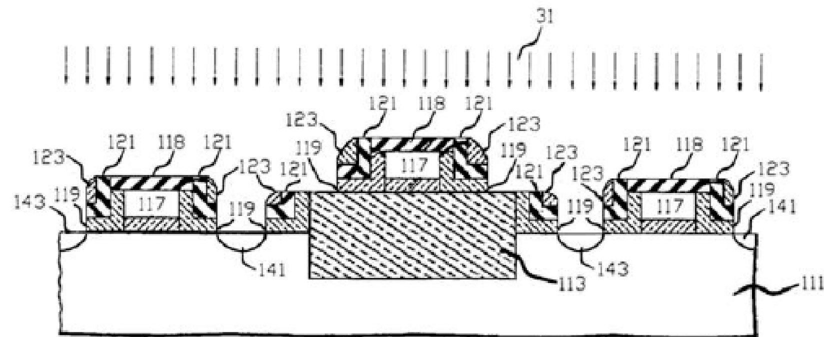
Lee, FIG. 14

1246 Petition (Paper 2) at 37–40; Reply (Paper 21) at 20, 42–44; EX1002 at 3:49–4:3, 4:53–6:30, 7:13–35, FIGS. 5–6, 9, 15; EX1057 at 56–57, 92–94.

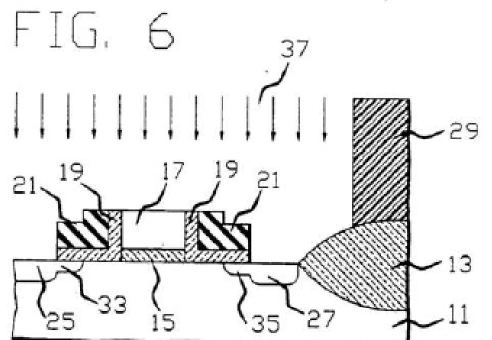
Lee Discloses LDD Doping Using L-Shaped Sidewalls



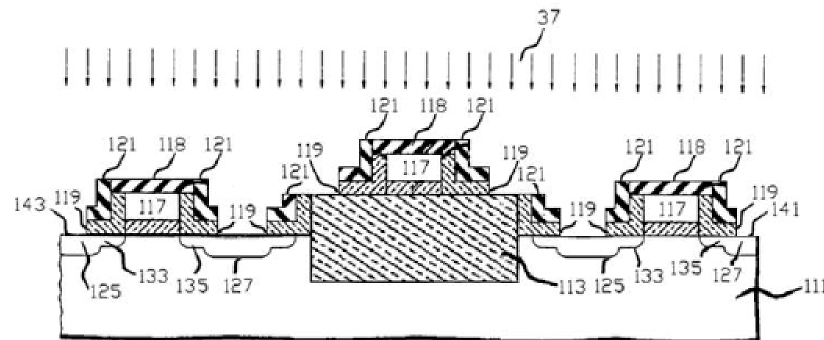
Lee, FIG. 5



EX1057 at 56



Lee, FIG. 6

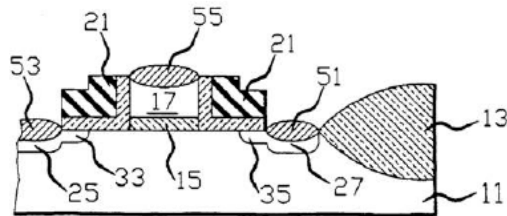


EX1057 at 56

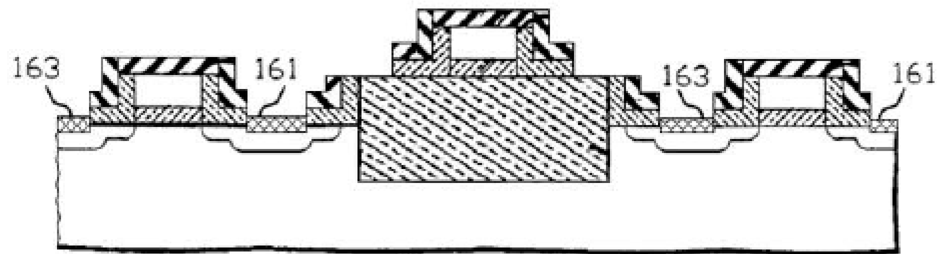
47

1246 Petition (Paper 2) at 37; Reply (Paper 21) at 20; EX1002 at 3:49–4:3, 4:53–6:30, 7:16–22, FIGS. 5–6, 15; EX1057 at 56.

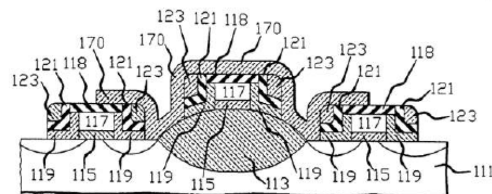
Lee Discloses Self-Aligned Silicide Regions



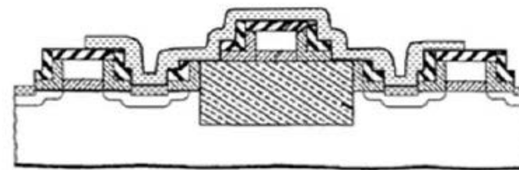
Lee, FIG. 9



EX1057 at 56



Lee, FIG. 15



EX1057 at 57

1246 Petition (Paper 2) at 38–40; Reply (Paper 21) at 20, 42–44; EX1002 at 4:53–6:30, 7:22–28, FIGS. 9, 15; EX1057 at 56–57, 92–94.

RAISED SHALLOW TRENCH ISOLATION (STI)

Noble Discloses Raised STI (Claims 9 and 10)

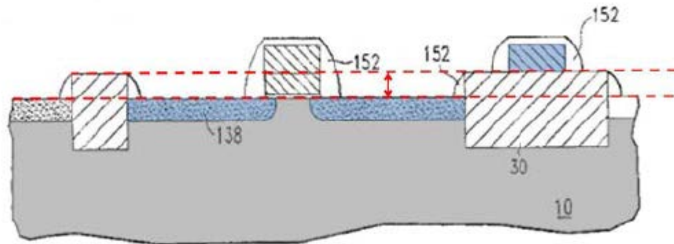


FIG. 12

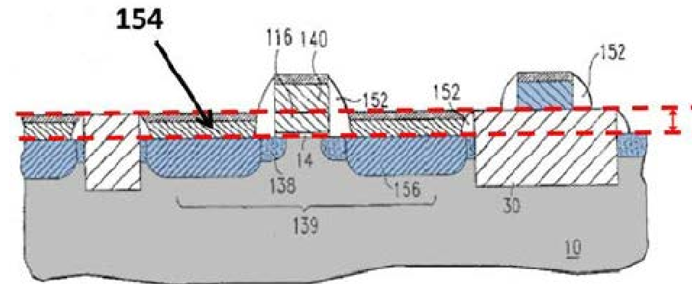


FIG. 13

1246 Petition (Paper 2) at 56

exposed gate dielectric **14**. Finally, the etch is extended into silicon substrate **10** to form raised deep trench **20** for a capacitor, as shown in FIG. **2**, or raised shallow trench **30** for STI, as illustrated in FIG. **4**. The term "raised trench" refers to the fact that the trench extends beyond the surface of substrate **10** to the top of the gate stack. In this process, a

Noble at 4:14–19

In a similar process to that described above for the raised deep trench, raised shallow trench isolation (raised STI) **30** is formed. Referring to FIG. **4**, after the photomasking and gate stack etching steps as described above, a silicon etch is used in silicon substrate **10** to form shallow trenches for raised STI **30**. Then a passivation oxide is thermally grown along surfaces of the silicon thereby exposed. TEOS is then deposited to fill the shallow trenches (and the top of deep trench **20**). Next, a planarization step is implemented stopping on the nitfide cap of the gate stack. Thus, raised STI is provided adjacent a sidewall of the gate stack. Of course,

Noble at 4:39–50

50

1246 Petition (Paper 2) at 52–57; Response (Paper 14) at 86–88; Reply (Paper 21) at 49–50; EX1015 at 3:49–54, 4:14–19, 4:39–50, 5:49–52, 6:13–24, FIGS. 4–5, 9–13.

RESPONSE TO PATENT OWNER ARGUMENTS

PATENT OWNER HAS NOT CHANGED POSITIONS

Petitions

Lee teaches every limitation of the challenged claims except trench isolation. A POSITA would have understood that *Noble*'s STI was a known substitute for *Lee*'s LOCOS isolation.

As demonstrated above in Section V.B., *Lee* teaches every limitation of the challenged claims except trench isolation. A POSITA would have understood that *Ogawa*'s trench isolation was a known substitute for *Lee*'s LOCOS isolation.

1246 Petition (Paper 2) at 21, 62.

Petitions

Lowrey teaches every limitation of the challenged claims except trench isolation. A POSITA would have understood that *Noble*'s trench isolation was a known substitute for *Lowrey*'s LOCOS isolation.

As explained in Section V.B, *Lowrey* teaches every limitation of the challenged claims except trench isolation. A POSITA would have understood that *Ogawa*'s trench isolation was a known substitute for *Lowrey*'s LOCOS isolation.

1247 Petition (Paper 2) at 21, 62.

Institution Decision

Petitioner relies on Noble as allegedly teaching a "trench isolation," citing Noble's description of STI 30. *Id.* at 32. Petitioner provides on page 19 of the Petition the following colored and annotated version of Figure 13 of Noble, which we find, based on the current record, is consistent with Noble's disclosure.

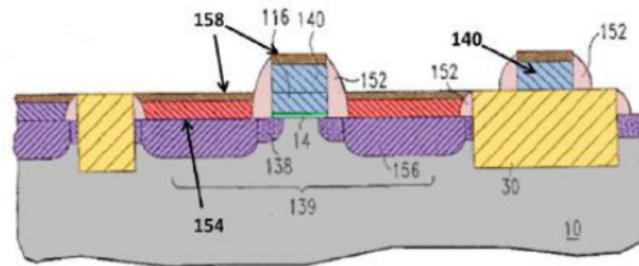


FIG. 13

10—Substrate (Si)
30—Raised STI
14—Gate Dielectric
116/140—Gate Electrode
154—Raised Source/Drain
152—Dielectric Spacers
138/156—Substrate Source/Drain
158—Silicide Regions (silicide)
140—Interconnection

Institution Decision (Paper 8) at 12.

Institution Decision

Petitioner's arguments regarding the combination of Lee and Ogawa are similar to those made with respect to Lee and Noble. Petitioner relies on Lee as allegedly teaching the majority of the limitations of claim 1, and relies on Ogawa for the "trench isolation" limitation, citing portion 52 in

Institution Decision (Paper 8) at 20

Institution Decision

Petitioner relies on Lowrey as allegedly teaching all limitations of claim 1 other than a "trench isolation."

Petitioner relies on Noble as allegedly teaching a "trench isolation," citing Noble's

Petitioner relies on Lowrey as allegedly teaching the majority of the limitations of claim 1, and relies on Ogawa for the "trench isolation" limitation, citing portion 52 in Ogawa. *Id.* at 62, 68–71.

Institution Decision (Paper 8) at 23, 24, 27.

Reply

In its Petitions, TSMC explained how *Lee* and *Lowrey* teach every limitation of the challenged claims, and why a POSITA would have wanted to substitute *Noble*'s and *Ogawa*'s functionally equivalent shallow-trench isolation ("STI") structures for *Lee*'s and *Lowrey*'s LOCOS isolation. One reason was such substitutions allow increased device density. TSMC even showed several examples how a POSITA would have known to make the STI structures in *Noble* and *Ogawa*.

IPB does not challenge this evidence.

Reply (Paper 21) at 1.

PATENT OWNER ATTACKS COMBINATIONS PETITIONER NEVER ASSERTED

The Asserted Combinations Do not Use Noble or Ogawa Gates

- Patent Owner did not argue a distinction between "embedded STI" and "non-embedded STI" until the Sur-Reply.
  - No reference refers to an embedded gate or a non-embedded gate.
- Petitioner never suggested using the gate stack of Noble or Ogawa in any combination. **1246 Petition** (Paper 2) at 21, 70; **1247 Petition** (Paper 2) at 21, 62; **Institution Decision** (Paper 8) at 12, 21, 24, 27.
- Noble and Ogawa use a standard process for forming STI. **Reply** (Paper 21) at 15–17.
- How the gate stack is made does not affect the STI. **EX1004** at ¶¶ 82, 198; **EX1024** at ¶¶ 93, 173.

1246 Petition (Paper 2) at 21, 70; 1247 Petition (Paper 2) at 21, 62; Institution Decision (Paper 8) at 12, 21, 24, 27; Reply (Paper 21) at 15–17; Sur-Reply (Paper 37) at 3–4, 6, 10–11, 23–24, 26; EX1004 at ¶¶ 82, 198; EX1024 at ¶¶ 93, 173.

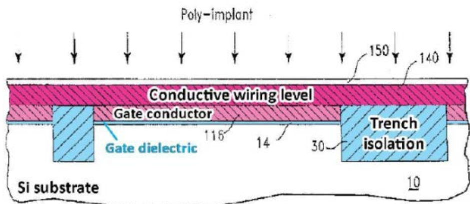
The Asserted Combinations Do not Use Noble or Ogawa Gates

- To show likelihood of success, Petitioner referred to prior art that did not use the gate as a polish-stop or etch-stop.
  - Ueda (E.g., EX1014 at 13:14–63)
  - Mandelman (E.g., EX1016 at 3:55–65)
  - Admitted Prior Art in ’174 Patent (E.g., EX1001 at 4:16–39)

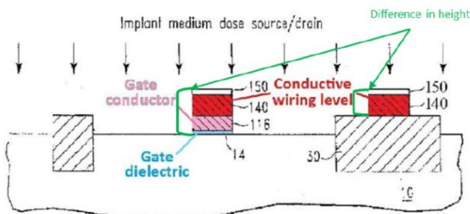
E.g., 1246 Petition (Paper 2) at 5–7, 10–11, 21–26, 31, 70–71; 1247 Petition (Paper 2) at 5–7, 10–11, 21–26, 30–31, 62–63; EX1001 at 4:16–39; EX1014 at 13:14–63; EX1016 at 3:55–65.

IPB Never addressed TSMC's Combination; It Attacked Different One

- IP Bridge **included Noble's/Ogawa's gate stack and interconnection**, with the trench isolation, and only attacked that combination.

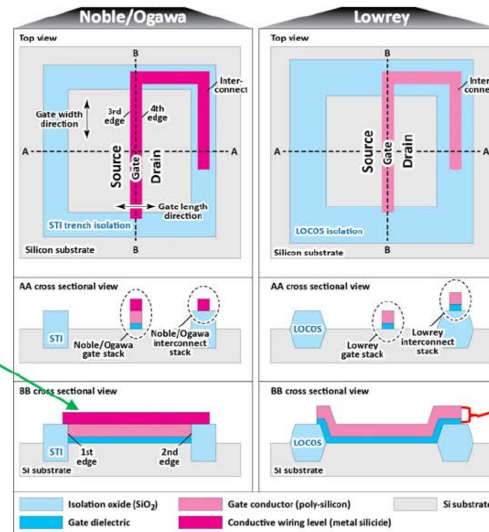


Response (Paper 14) at 55



Response (Paper 14) at 65

Only the wiring layer goes across



Gate electrode and gate dielectric extend across

Response (Paper 14) at 111

- But TSMC never proposed this combination.

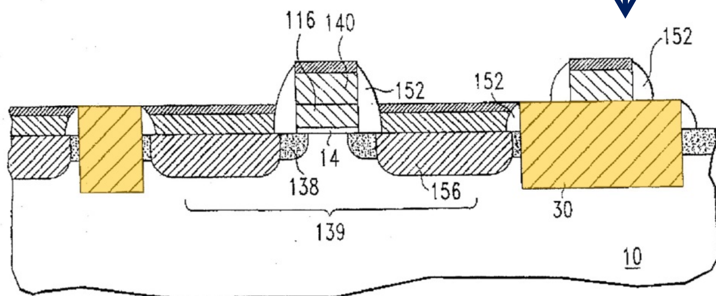
62

Response (Paper 14) at 55; 65, 111.

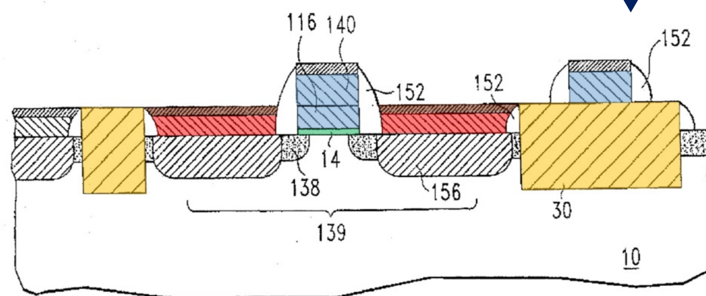
Petitioner Only Used the Noble STI

Noble

Portion in Petitioner's combination



Portion in Patent Owner's combination



Response (Paper 14) at 55; 65, 111; EX1015 at FIG. 13.

Patent Owner Admits it Uses a Different Combination

- IP Bridge seeks to incorporate features not part of the alleged obviousness combination (i.e., raised source/drains).

> 1015, 6:26-29. Thus, if a POSITA were to implement *Noble*'s STI in *Lee* (and they would not, as discussed above), the POSITA would also use the raised source/drain regions disclosed in *Noble*, and thus, would have the heightened active area (under the understanding of "active area" that would be necessary for the silicide layers in *Noble* to be formed within the active area). Thus, the trench isolation would not

Response (Paper 14) at 87

- This is inconsistent with the claim language.

> 1. A semiconductor device, comprising:
> a trench isolation surrounding an active area of a semi-conductor substrate;

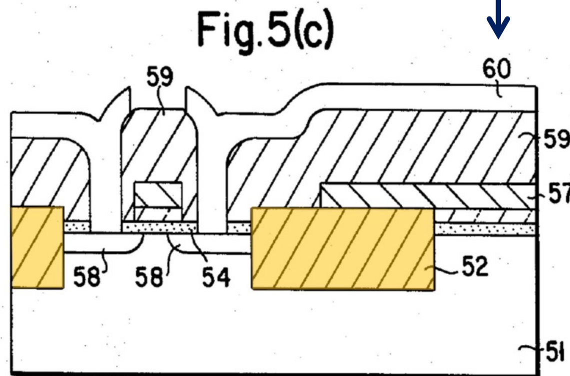
Claim 1

1246 Petition (Paper 2) at 52–57; Response (Paper 14) at 86–88; Reply (Paper 21) at 49–50.

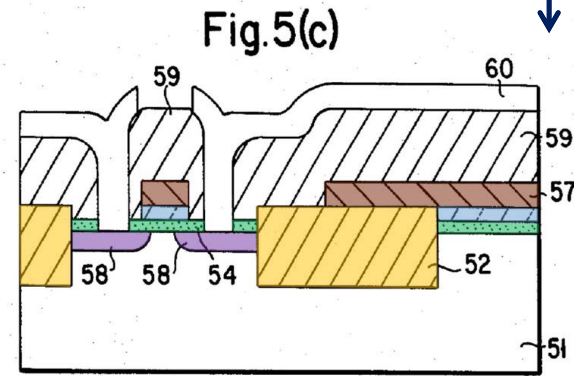
Petitioner Only Used the Ogawa STI

Ogawa

Portion in Petitioner's combination



Portion in Patent Owner's combination



Response (Paper 14) at 55; 65, 111; EX1010 at Fig. 5(c).

PATENT OWNER ARGUMENTS BASED ON MISREPRESENTATION OF PROPOSED COMBINATIONS

Patent Owner Arguments Based on Faulty Combination

Response

Patent Owner Argument	Source
Lee and Noble/Ogawa Are Not Combinable To Arrive At The Claimed Invention	POR at 50, et seq.
Lee And Ogawa Are Not Combinable To Arrive At the Claimed Invention	POR at 59, et seq.
Substituting The Trench Isolation of Noble/Ogawa Into Lee Conflates Two Contradictory Designs	POR at 63, et seq.
Substituting The Trench Isolation Of Noble/Ogawa Into Lowrey Conflates Two Contradictory Device Designs	POR at 111, et seq.

NO NEED TO DISCLOSE PROCESS

Process Not Required to Invalidate a Structure Claim

- The law treats structure claims (all of those in issue) differently from process claims
  - IPB cited no law in its papers requiring disclosure of the actual process sequence of making the combination.

69

Reply (Paper 21) at 26–29; Institution Decision (Paper 8) at 17.

Process Not Required to Invalidate a Structure Claim

- "The patentability of a product does not depend on its method of production." ***In re Thorpe***, 777 F.2d 695, 697 (Fed. Cir. 1985).
- "The method of manufacture, even when cited as advantageous, does not of itself convert product claims into claims limited to a particular process." ***Vanguard Prods. Corp. v. Parker Hannifin Corp.***, 234 F.3d 1370, 1372-73 (Fed. Cir. 2000).
- "Courts must generally take care to avoid reading process limitations into an apparatus claim." ***Baldwin Graphics Sys., Inc. v. Siebert, Inc.***, 512 F.3d 1338, 1344 (Fed. Cir 2008).
- "Appellants claim a gene sequence. Accordingly, the obviousness inquiry requires this court to review the Board's decision that the claimed sequence, not appellants' unclaimed cloning technique, is obvious in light of the abundant prior art." ***In re Kubin***, 561 F.3d 1351, 1356 (Fed. Cir. 2009).

Reply (Paper 21) at 18 n.9, 26–30.

Process Not Required to Invalidate a Structure Claim

- IPB cases involve process claims, not structure claims
- IPB cases discussing "how or why" an obviousness combination would be made do not require a process for making a claimed structure
  - ***Kinetic Concepts***—rev'd JMOL because "[t]he record [wa]s devoid of any reason someone would combine the[] references"
  - ***Innogenetics***—aff'd exclusion of expert testimony that had only a "stock phrase" concluding the claims were obvious
  - ***Personal Web***—"how" described the Board's failure to explain how combination satisfied claims; not a reference to failure to show a process for making a claimed structure

Reply (Paper 21) at 26–29.

Board Decision

We have reviewed Patent Owner's arguments and the testimony of Dr. Schubert, but do not find them persuasive based on the current record and stage of the proceeding. Claim 1 is an apparatus claim, not a method claim. It recites a "semiconductor device" comprising various physical components, including a "trench isolation," but does not recite anything about how those components are formed. Thus, Petitioner's contentions appropriately are directed to how the cited prior art teaches each component of the claimed device. *See* Pet. 21–44. Indeed, Patent Owner does not collectively, teach all of the recited components.[6] The record further indicates, as explained above, that there were known ways to fabricate a semiconductor device with a LOCOS isolation structure and known ways to fabricate a semiconductor device with a trench isolation, both of which were within the skill level of an ordinarily skilled artisan. *See id.* at 4–7, 22–23,

Institution Decision (Paper 8) at 16–17.

Board Decision

[6] Patent Owner argues that "Petitioner has failed to provide the actual process sequence it is contemplating [for the combined device of Lee and Noble]. To properly establish obviousness, disclosure of the sequence is necessary." Prelim. Resp. 36–37. Patent Owner does not cite any authority for this proposition, and we are aware of none.

Institution Decision (Paper 8) at 17 n.6.

PROCESS DETAILS UNNECESSARY BECAUSE A POSITA KNEW HOW TO MAKE STI

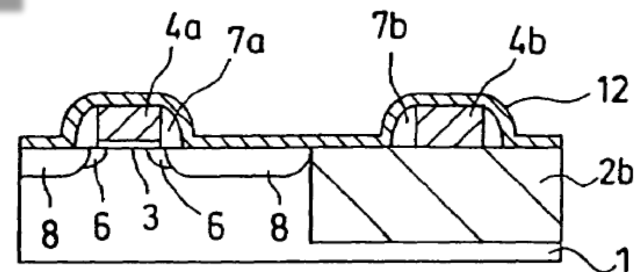
Forming an STI is not Complex

view of the alignment shift in the photolithography. Manufacturing procedures adopted in such a case will now be described by exemplifying an n-channel MOSFET referring to FIGS. **18**(*a*) through **18**(*c*).

First, as is shown in FIG. **18**(*a*), after forming an isolation **2***b* having the trench structure in a silicon substrate **1** doped with a p-type impurity (or p-type well), etch back or the like is conducted for flattening so as to place the surfaces of the isolation **2***b* and the silicon substrate **1** at the same level. In an active area surrounded with the isolation **2***b*, a gate oxide film **3**, a polysilicon electrode **4***a* serving as a gate electrode, an electrode sidewall **7***a*, a low-concentration source/drain region **6** and a high-concentration source/drain region **8** are formed. On the isolation **2***b* are disposed a polysilicon

'174 Patent at 2:47–60

'174 Patent FIG. 18(a)



EX1001 at 2:47–60, FIG. 18(a).

Forming an STI is not Complex

Although the isolation is composed of the LOCOS film in the above embodiments, the present invention is not limited thereto. The present invention is also applicable to an isolation of trench structure or the like.

Ueda, EX1014, at 22:48–52

process.

This technology can be scaled to the 1 Gbit DRAM generation with minor modifications, such as replacing LOCOS with trench isolation and adding hemispherical-grained poly-Si on cylinder capacitors.

Kang, EX1053, at 2

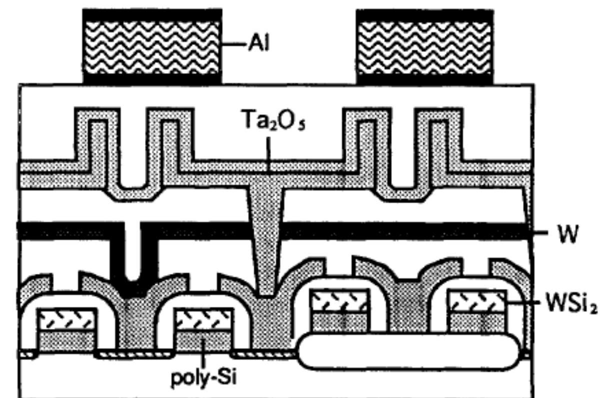
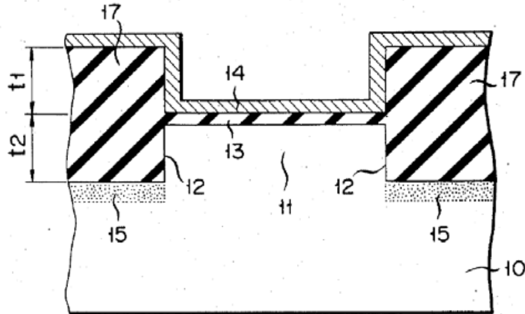


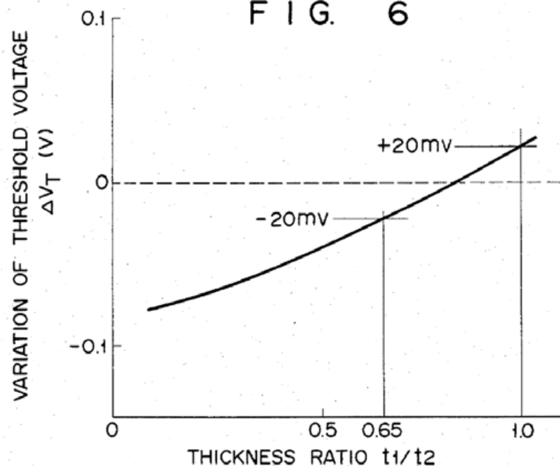
Fig. 1 Schematic cross-section of the DRAM cell.

Kang, EX1053, at Fig. 1

EX1014 at 22:48–52; EX1053 at 2; EX1057 at 33–34.

Forming an STI is not Complex





groove **12**. The above steps are the same as those in the conventional BOX structure method.

As shown in FIG. 7B, an element formation region **11** surrounded by the silicon oxide film **17** is selectively etched so as to define the thickness of the upward projection of the silicon oxide film **17** which must be smaller than that of the embedded portion thereof. As shown in FIG. 7C, a gate oxide film **13** is formed on the element formation region **11**. Furthermore, a polysilicon gate electrode **14** is formed on the gate oxide film **13** and on the silicon oxide film **17**.

The structure of FIG. 7B can be provided without etching the silicon substrate **10**. This may be achieved by obtaining the structure of FIG. 7A without removing the etching mask (e.g. Al film, Si_3N_4 film, photoresist film, etc.) used in cutting the groove **12** and then by removing the etching mask thereafter.

Konaka, EX1032, at 3:65–4:13, FIGS. 5, 6

- **Filed June 17, 1985**
- **Claims priority to an application filed October 27, 1981, which contains FIGS. 5 & 6.**

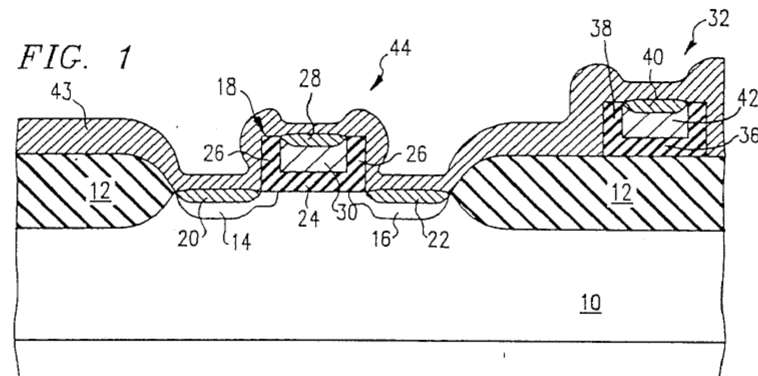
Reply (Paper 21) at 3–5, 17, 38; EX1032 at 3:65–4:13, FIGS. 5, 6; EX1033 at 3; EX1057 at 27–29, 35–36, 41, 45, 47–48, 52.

Forming an STI is not Complex

FIG. 1 shows the first step utilizing the method of the preferred embodiment of the present invention, as directed to an integrated circuit wafer **44**. Wafer **44** contains a semiconducting substrate **10** formed of silicon. Field oxide **12**, preferably silicon dioxide (SiO_2), is grown or deposited in selected portions of the surface of the substrate **10** for isolation of active regions from one another according to the well known local oxidation (LOCOS) isolation technique; of course, other isolation techniques such as trench isolation may alternatively be used. The active transistors of the integrated circuit

Douglas, EX1011, at 4:6–16

Douglas, EX1011, FIG. 1



EX1011 at 4:6–16; EX1057 at 33–34.

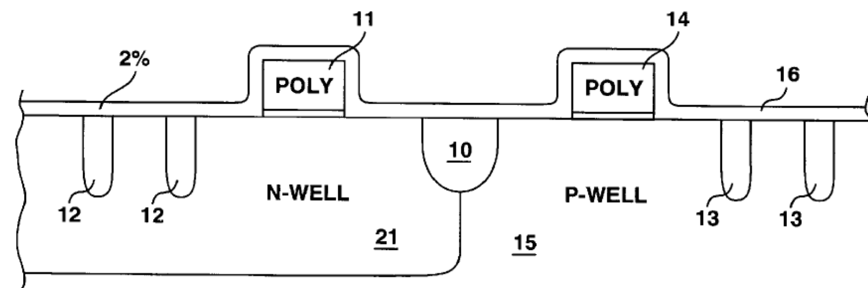
Forming an STI is not Complex

The n and p well of FIG. **1** are isolated from one another by a recessed isolation region specifically, trench **10**. Additionally, within the n well **21** there are other isolation trenches **12** for isolating from one another p-channel transistors formed within the n well. Likewise, there are isolation trenches **13** formed within the p well to isolate n-channel transistors formed in the p well from one another. The isolation trenches may be formed using well-known technology. Other isolation technologies such as local oxidation of silicon (LOCOS) may be used instead of trenches

A gate insulative layer (such as a high quality, thermally

Thompson, EX1012, at 3:1–11

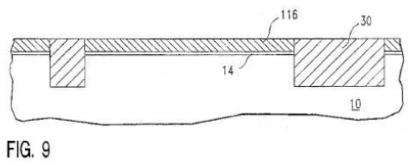
Thompson, EX1012, FIG. 1



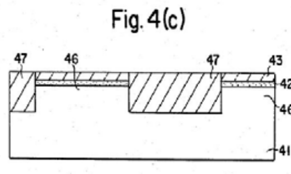
EX1012 at 3:1–10; EX1057 at 33–34.

A POSITA KNEW HOW TO FORM STI WITHOUT THE TRANSISTOR GATE

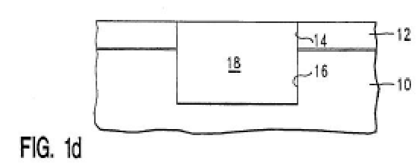
The STI Structure Is Independent of the Gate Process



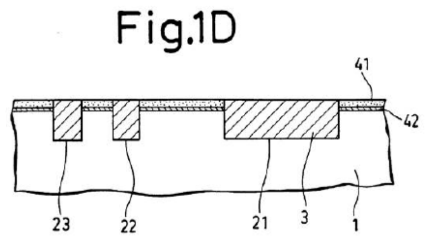
Noble, FIG. 9



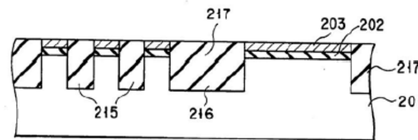
Ogawa, Fig. 4(c)



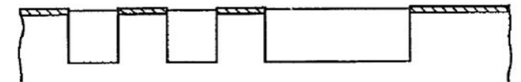
Mandelman, FIG. 1d



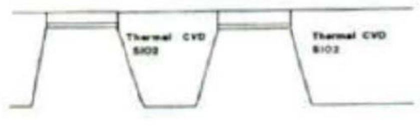
Sato, Fig. 1D



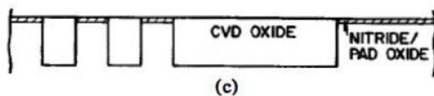
Kodera, Fig. 29C



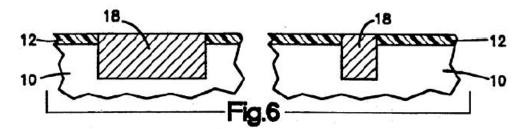
Pierce, Fig. 1



Deleonibus, Fig. 1



Davari, Fig. 1(c)

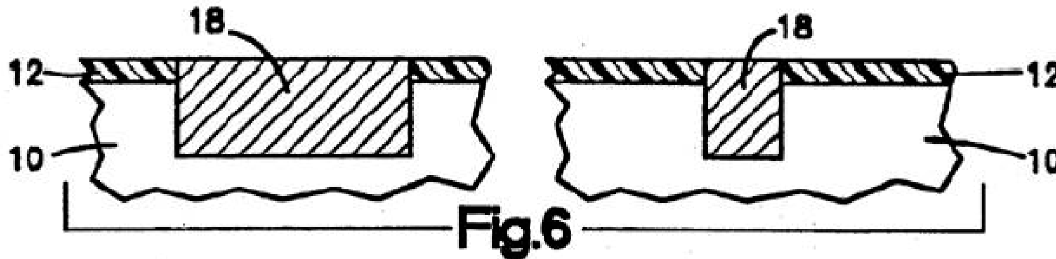


Dash, Fig. 6

81

Reply (Paper 21) at 2–17; EX1010 at 5:57–6:59, Fig. 4(c); EX1015 at 3:64–4:19, 4:40–49, 5:49–57, FIG. 9; EX1016 at 3:27–4:22, Fig. 1d; EX1034 at 4:30–5:49, Fig. 1D; EX1035 at 26:62–28:33, FIG. 29C; EX1042 at 4–5, Fig. 1; EX1043 at 2–3, Fig. 1; EX1055 at 1–3, Fig. 1(c); EX1057 at 26–50; EX1058 at 2:48–4:28, Fig. 6.

Making STI Before the Gate Stack Was Routine



Dash, Fig. 6

STI and processes for forming STI are described in commonly assigned U.S. Pat. No. 5,173,439, by Dash et al., incorporated herein by reference.

Noble at 3:35–37

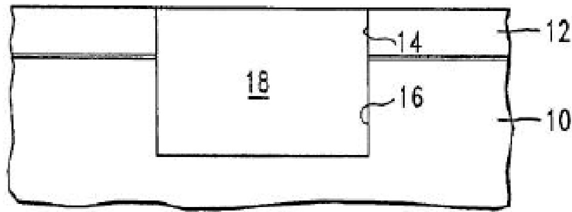
- Noble incorporates Dash by reference.

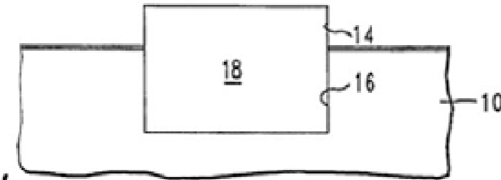
The entire wafer shown in FIG. **5** is then again chemically-mechanically polished using a silica slurry in basic aqueous solution and polished against a rotating polyurethane disk. This polishing step will remove the plugs of material which are above the wide trenches **14** resulting in a final structure shown in FIG. **6**. The silicon nitride **12** acts as the end point for the polishing so that the entire surface of the wafer which includes both wide and narrow trenches filled with silicon dioxide are essentially planarized and hence ready for further processing such as the formation of the conductor patterns on the surface.

Dash at 4:17–28

Reply (Paper 21) at 3–17; EX1015 at 3:35–37; EX1057 at 34–44; EX1058 at 4:17–28, Fig. 6.

Making STI Before the Gate Stack Was Routine





In the process, silicon substrate **10** is provided with a pad oxide **11** and nitride surface coating **12** as illustrated in FIG. **1***a*. Window **13** with nearly vertical sidewall **14** is photolithographically defined in surface coating **12** and oxide **11** as shown in FIG. **1***b*. Then trench **16** is etched, defined by window **13** as illustrated in FIG. **1***c*.

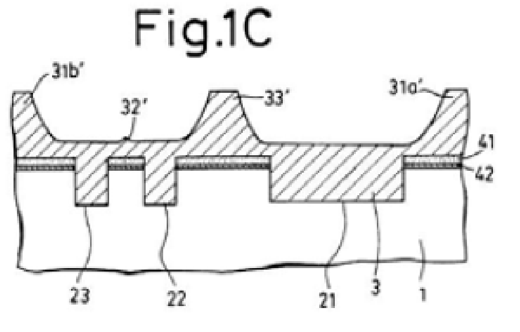
Trench **16** and window **13** are then filled with insulator **18**. Insulator **18** is then polished, stopping on surface coating **12** as illustrated in FIG. **1***d*. Then surface coating **12** is removed, leaving insulator **18** with nearly vertical sidewalls **20** extending above the surface **21** of silicon substrate **10**.

With any of the above embodiments, a MOSFET can then formed bounded by a corner dielectric rather than the corner and sidewall of the STI. As illustrated in FIG. **5**, gate dielectric **38** is formed by conventional processing. Gate conductor **40** is then deposited and photolithographically defined. Gate conductor **40** is spaced from corner **24** by corner dielectric **22**, **22***a*, or **22***c*. Thus, the electric field in the corner region is significantly reduced.

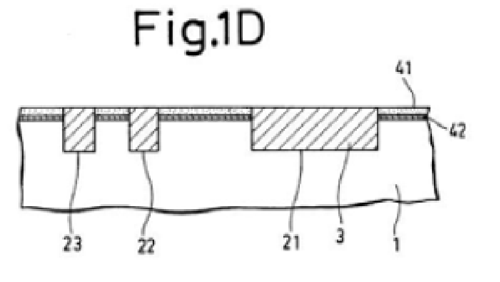
Mandelman at 3:55–65, 5:40–47, FIG. 1d

Reply (Paper 21) at 3–17; EX1016 at 3:55–65, 5:40–47, FIGS. 1d, 5; EX1057 at 34–44.

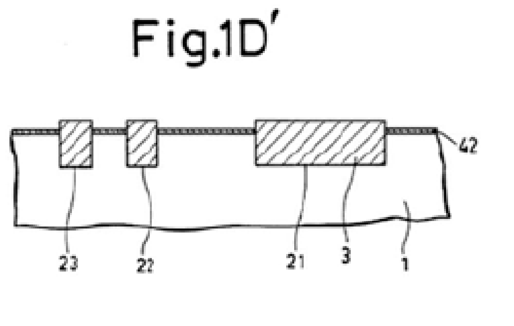
Making STI Before the Gate Stack Was Routine



Sato, Fig. 1C



Sato, Fig. 1D



Reply (Paper 21) at 5

Thereafter, an excessive SiO_2 is removed by polishing, whereby a smoothed structure such as shown in FIG. 1D is obtained. The polishing process used here may be of the conventional type or of the type using the nylon balls described above. For the polishing process, the structure preferably has patterns of the same width which are formed by using a stencil structure as described in Japanese Patent Application No. 3-24041 filed by to the present assignee.

Subsequently, the Si_3N_4 polish-stop layer **41** is etched off as required. In this instance, due to the presence of the SiO_2 etch-stop layer **42**, the base silicon substrate **1** is not affected at all by the etching process. With this etching, the SiO_2 slightly projects from the trenches **21–23**, so that the dielectric breakdown strength of the structure is improved.

Sato at 5:36–49

Reply (Paper 21) at 3–17; EX1034 at 5:36–49, Figs. 1C, 1D; EX1057 at 34–44.

Making STI Before the Gate Stack Was Routine

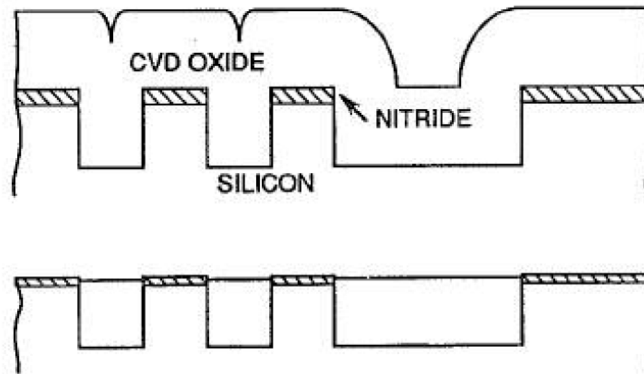


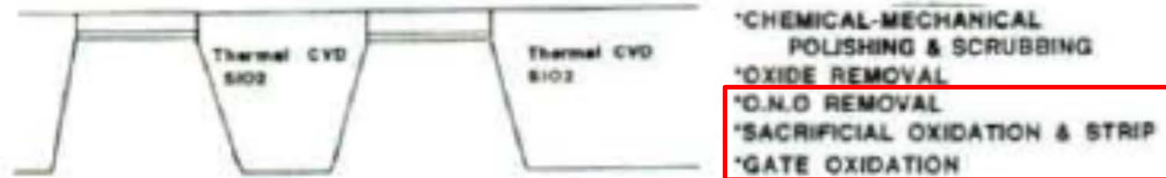
Fig. 1. ISO-P process cross-sections before and after CMP planarization.

CMP planarization was carried out using a glass-impregnated polyurethane polishing pad with fumed colloidal silica slurry. Polishing was terminated when the nitride over the active silicon areas was completely exposed. The pad, slurry and polishing parameters were optimized to produce the leveling results discussed below. After planarization, the nitride/oxide stack was stripped, and the devices were completed using normal process steps.

Pierce, at 2–3, Fig. 1

Reply (Paper 21) at 3–17; EX1043 at 2–3, Fig. 1; EX1057 at 34–44.

Making STI Before the Gate Stack Was Routine



2. PROCESS FLOW

The process flow of this process is given in figure 1. After a masking step using a silicon nitride/silicon dioxide stack (180nm/17.5nm), mask and trench etching are performed in a P5000 equipment, using an HBr,Cl2 chemistry in order to get 70° sloped grooves. After resist removal eliminating also the polymer residues, a sidewall oxidation is performed to control the silicon surface quality and screening of a possible sidewall implantation. The refill material is then deposited in a LPCVD reactor at 900°C using an SiH2Cl2,N2O based mixture. Chlorine is out-diffused using low temperature steam densification to avoid "pancakes shapes"[6] after gate oxidation. The planarization step is achieved by using a 100% chemical-mechanical polishing (CMP) process on a PRESI equipment. Silicon nitride is used as an etch-stopper with an oxide to niride selectivity of 4. Scrubbing is performed after this step to remove the generated particles. The influence of the subsequent HF dip is examined in the following. The active mask stack is removed by using standard a BOE, H3PO4, HF dip sequence before an implant sacrificial oxide growth and strip. The BOx-ON process is thus completed. The following process steps are derived from standard CMOS.

densified material. The damaged areas can be a source of contamination (mobile and metallic ions) that can reach the oxide/silicon interface later in process. The removal of the damaged layer is necessary to achieve a contamination free process.

Deleonibus, at 4–5, Figure 1

86

Reply (Paper 21) at 3–17; EX1042 at 4–5, Figure 1; EX1057 at 34–44.

ADDITIONAL REFERENCES CAN SHOW REASONABLE EXPECTATION OF SUCCESS

No Need to Limit Analysis to References

- The Board recognized other references besides those used for the obviousness combination could be used to show reasonable expectation of success.
  - ***Genzyme Therapeutic Prods. Ltd. v. Biomarin Pharm. Inc.***, 825 F.3d 1360, 1367–68 (Fed. Cir. 2016) (rejecting an argument that references not among the combinations of references on which the Board granted review could not be used to show a reasonable expectation of success).
  - "Art can legitimately serve to document the knowledge that skilled artisans would bring to bear in reading the prior art identified as producing obviousness." ***Ariosa Diagnostics v. Verinata Health, Inc.***, 805 F.3d 1359, 1365 (Fed. Cir. 2015).

Institution Decision (Paper 8) at 13 n.5.

No Need to Limit Analysis to References

- "By narrowly focusing on the four prior-art references cited by the Examiner and ignoring the additional record evidence Randall cited to demonstrate the knowledge and perspective of one of ordinary skill in the art, the Board failed to account for critical background information that could easily explain why an ordinarily skilled artisan would have been motivated to combine or modify the cited references to arrive at the claimed inventions. **As *KSR* established, the knowledge of such an artisan is part of the store of public knowledge that must be consulted when considering whether a claimed invention would have been obvious."** ***Randall Mfg. v. Rea***, 733 F.3d 1355, 1362–63 (Fed. Cir. 2013) .
- "The record shows the well-known and reliable nature of the cloning and sequencing techniques in the prior art, not to mention the readily knowable and obtainable structure of an identified protein. Therefore this court cannot deem irrelevant the ease and predictability of cloning the gene that codes for that protein." ***In re Kubin***, 561 F.3d 1351, 1360 (Fed. Cir. 2009).

Institution Decision (Paper 8) at 13 n.5.

PATENT OWNER IGNORES THE LAW IN LIMITING THE PRIOR ART TO A SPECIFIC EMBODIMENT

A POSITA Must Consider a Reference for All it Teaches

- "A reference must be considered for everything that it teaches, not simply the described invention or a preferred embodiment." ***In re Applied Materials, Inc.***, 692 F.3d 1289, 1298 (Fed. Cir. 2012).
- "A reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect. On the issue of obviousness, the combined teachings of the prior art as a whole must be considered." ***Belden Inc. v. Berk-Tek LLC***, 805 F.3d 1064, 1076 (Fed. Cir. 2015).
- "It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements. . . . Rather, the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art." ***In re Mouttet***, 686 F.3d 1322, 1332–33 (Fed. Cir. 2012).

Reply (Paper 21) at 30–32.

A POSITA Has Ordinary Creativity

- "[O]ne of ordinary skill is also one of 'ordinary creativity' that knows how to combine familiar prior art elements to achieve the same functions." ***Tyco Healthcare Grp. LP v. Ethicon Endo-Surgery, Inc.***, 774 F.3d 968, 978 (Fed. Cir. 2014).
- "[W]e do not ignore the modifications that one skilled in the art would make to a device borrowed from the prior art. One skilled in the art would size the components from Teague appropriately for Icon's application, therefore producing an embodiment meeting Icon's claims." ***In re ICON Health & Fitness, Inc.***, 496 F.3d 1374, 1382 (Fed. Cir. 2007) (citation omitted).

Reply (Paper 21) at 6.

RESPONSE TO SUR-REPLY

PETITIONER'S REPLY DID NOT RAISE NEW ISSUES

TSMC's EX1025 through EX1059 Respond to IPB Arguments

Corroborating Evidence to Show Substitutability of STI for LOCOS Isolation	Evidence Showing That Making STI Without Using the Gate Stack Was Known	Other Rebuttal Evidence(e.g., L-Shaped Sidewalls, SEM)
• EX1025 (Adler) • EX1046 (Wof & Tauber, vol. 2) • EX1047 (Fry) • EX1048 (Poon) • EX1052 (Kurosawa) • EX1053 (Kang) • EX1054 (NTRS)	• EX1026/EX1027 (Sumi)* • EX1028/EX1029 (Horiguchi)* • EX1030/EX1031 (Ueda JP)† • EX1032/EX1033 (Konaka and JP counterpart) • EX1034 (Sato) • EX1035 (Kodera) • EX1037 (Gasner) • EX1042 (Deleonibus) • EX1043 (Pierce) • EX1055 (Davari) • EX1058 (Dash)‡	• EX1036 (Chen) • EX1038 (Ma) • EX1039 (Manukonda) • EX1040 (Hiroki) • EX1041 (Kusunoki) • EX1044 (Chang & Sze) • EX1045 (Wolf & Tauber, vol. 1) • EX1049 (Clement) • EX1050 (Pantel) • EX1051 (Servanton)

* Cited on the face of the '174 patent.

† This is the July 21, 1995, publication of JPH 05-284820, a priority document for Ueda (EX1014), which confirms the portions of Ueda cited in the Petition had been published earlier.

‡ Incorporated by reference by Noble for teaching "STI and processes for forming STI." EX1015 at 3:35–37.

Petitioner's Opposition to Motion to Exclude (Paper 40) at 9.

TSMC's EX1025 through EX1059 Respond to IPB Arguments

First, it is not possible to follow *Lee's* process by simply substituting *Noble* and *Ogawa's* trench isolation for *Lee's* LOCOS isolation. *Lee **starts*** with LOCOS isolation formation ***followed*** by gate dielectric and gate conductor formation, while both *Noble* and *Ogawa **start*** with gate dielectric and gate conductor formation ***followed*** by trench formation. *Noble* and *Ogawa* specifically rely on the pre-existence of gate dielectric and gate conductor when forming the trench isolation.

Second, it is not possible to simply start with *Noble's* or *Ogawa's* trench isolation without first forming the gate dielectric and gate conductor because *Noble/Ogawa's* trench isolation formation depends on the availability of the gate dielectric and gate conductor. Thus, it would undermine the *Noble and Ogawa*

Response (Paper 14) at 64

[9] This evidence in this section "respond[s] to arguments raised in the . . . patent owner response" (37 C.F.R. §42.23(b)), specifically IPB's theory that it would have been impossible to substitute STI for LOCOS isolation. TSMC did not present it in its petitions because there was no need to include process descriptions to prove a device structure claim is obvious. *See Thorpe*, 777 F.2d at 697; *Kubin*, 561 F.3d at 1356.

Reply (Paper 21) at 18 n.9

Response (Paper 14) at 10, 64–65, 114–16; Reply (Paper 21) at 3–18 & nn.8, 9.

TSMC's EX1025 through EX1059 Respond to IPB Arguments

Conversely, if a trench isolation (not taught by *Noble*) is formed in *Lee* without previously-deposited layers on the substrate, and before layers **115**, **117** and **118** of *Lee* are applied, the resulting trench isolation would not be raised above the surface of the substrate. Such a trench is not taught by *Noble* (or *Ogawa*) and would be highly undesirable.[9] Accordingly, a POSITA considering any of the combinations proposed by Petitioner, would not proceed in this manner. Exhibit 2012, ¶182.

Response (Paper 14) at 47–48; Reply (Paper 21) at 3–18 & nn.8, 9.

TSMC's EX1025 through EX1059 Respond to IPB Arguments

A necessary condition for a sidewall to appear L-shaped is that it is distinguishable from other components of the sidewall. Given that layer **62** is chemically indistinguishable from layer **71**, its physical appearance is indistinguishable from layer **71** as well, and so the sidewall does not substantially resemble an L-shaped component. Exhibit 2012, ¶¶383-386; Exhibits 2026-2030.

Response (Paper 14) at 104

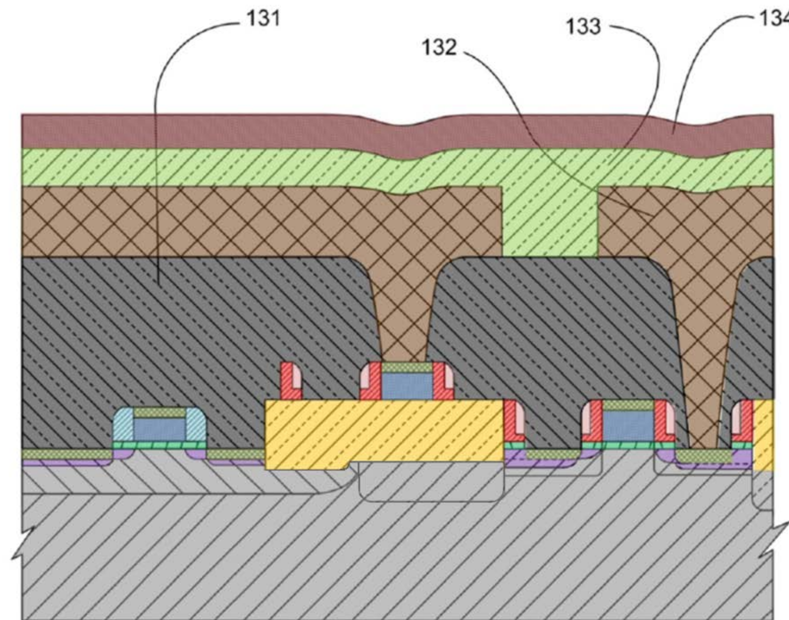
To support its position, IPB arbitrarily chooses SEM—a technique that is not chemically sensitive—as the appropriate metric for determining distinguishability (EX2012, ¶¶136-140), but other chemically sensitive imaging techniques, like EELS, EDS/EDX, and EFTEM can distinguish materials SEM cannot— even doping. EX1051, Figs. 1, 5; EX1049, Figures 2, 5, 6; EX1057, ¶147. The STEM-EELS and STEM-EDX images of MOSFETs below show how even small chemical differences (e.g., doping) are distinguishable where SEM and TEM images appear uniform.[16] *Id.*

Reply (Paper 21) at 41

Response (Paper 14) at 102–04; Reply (Paper 21) at 40–42.

THE BUMP ("JOG") IN LOWREY'S STI DOES NOT HURT DEVICE OPERATION

The Small Bump, or "Jog," Does Not Hurt Isolation



Reply (Paper 21) at 24 n.12, 25; EX1057 at ¶¶ 107 n.11, 143; Sur-Reply (Paper 37) at 29; EX2078 at 194:12–17.

The Small Bump, or "Jog," Does Not Hurt Isolation

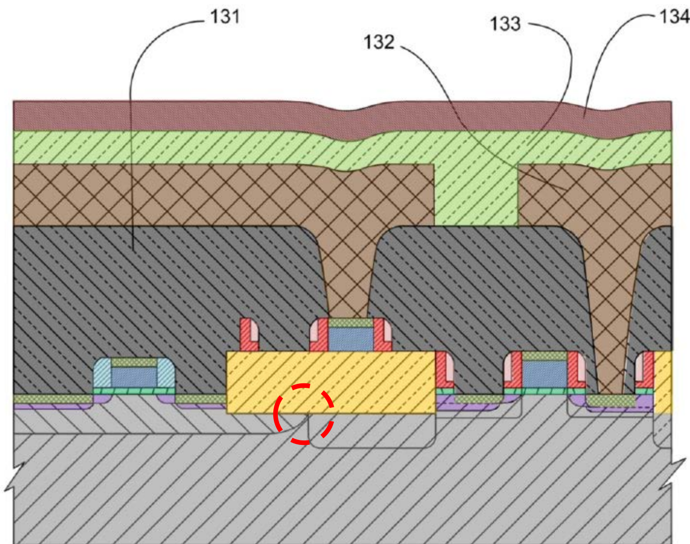
Q. Can you look carefully at that depiction and tell me if there is anything wrong or missing from that depiction?

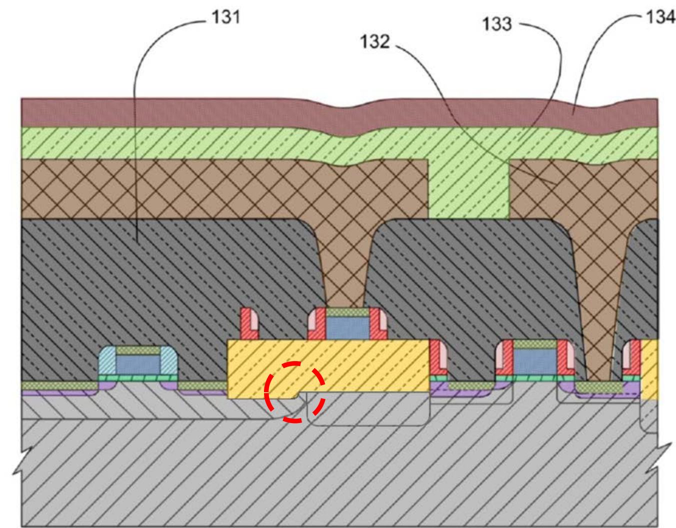
A. Well, I omitted to show a slight jog, if you will, at the bottom of the trench on the left-hand side.

A. No. I mean, once again the draftsman drew it under my direction, and it is slightly sloppy but it doesn't change the conclusions at all.

EX2078 at 194:12–17, 197:3–6.

The Small Bump, or "Jog," Does Not Hurt Isolation





Reply (Paper 21) at 25, Sur-Reply (Paper 37) at 29.

The Small Bump, or "Jog," Does Not Hurt Isolation

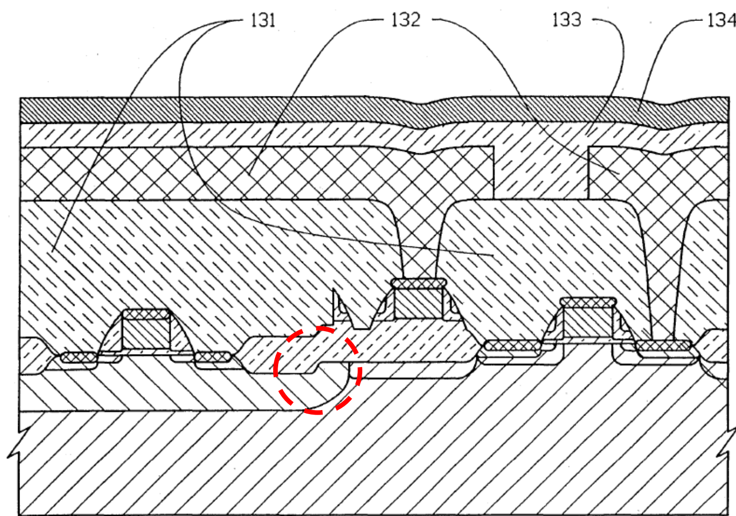


FIG. 13

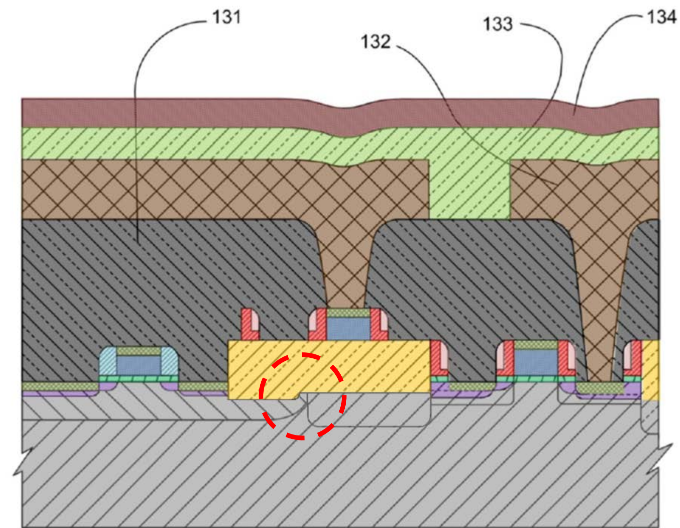


FIG. 13′

EX1017 at FIG. 4; Reply (Paper 21) at 25, Sur-Reply (Paper 37) at 29.

The Small Bump, or "Jog," Does Not Hurt Isolation

[11] I do not agree with Dr. Schubert that non-uniformity at the bottom of the trench would enhance leakage currents. *Lowrey* itself discloses a non-planar LOCOS isolation with non-uniformity at the bottom of the isolation region. Using STI with non-uniformity at the bottom of the trench would be no different and would not have deterred a person of ordinary skill in the art from this solution.

EX1057 at 68 n.11.

The Small Bump, or "Jog," Does Not Hurt Isolation

How wide you make this isolation region, be that LOCOS or STI, ultimately depends on the isolation capabilities between the adjacent transistors, okay, which would depend on the parasitic field transistor action underneath the isolation region, which in turn depends on mostly the thickness of that field oxide because at the end of the day you are looking at parasitic capacitive coupling between interconnects on top of the field oxide.

As long as that field oxide is thick enough and you optimize the process, I see no problems whatsoever.

A. If they are sharp corners, that can enhance electrical fields. It is interesting that you mention that. That, it turns out, is one of the advantages of STI.

It is a well-known effect called the corner effect where the sharp corners of edges of the STI actually enhance electrical isolation compared to LOCOS. So in this case that actually benefits you.

So from that, depending on the structure including this step, you would get the contours and enhanced electrical field in some cases may increase the potential barrier. And, if it does, it will actually help with electrical isolation.

Q. And in some cases it may decrease it, in which case it would hurt?

A. It may not hurt because as long as you make the overall oxide thick enough, and you have adequate electrical barriers between one transistor on one side of the trench and another transistor on the other side, this is a non-issue.

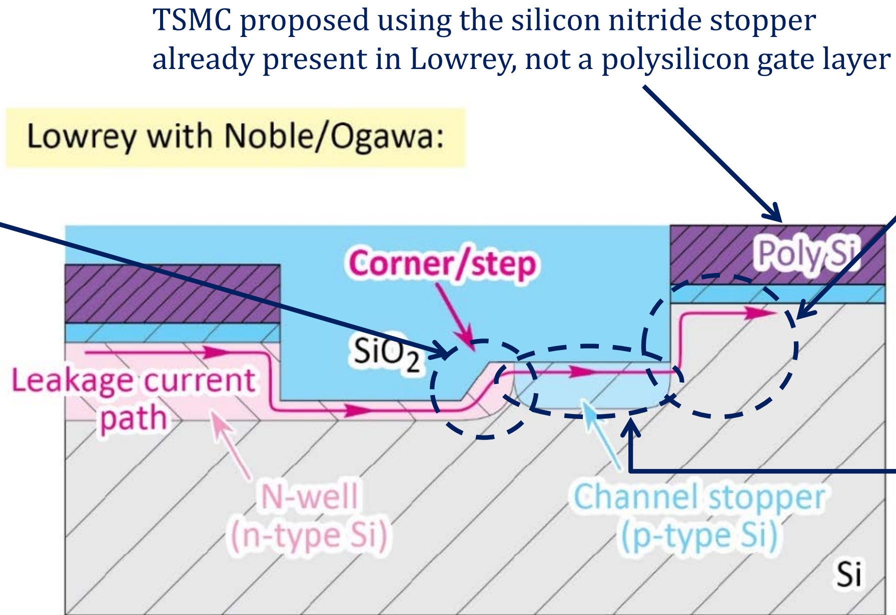
EX2078 at 207:12–215:10.

The Small Bump, or "Jog," Does Not Hurt Isolation

TSMC proposed using the silicon nitride stopper already present in Lowrey, not a polysilicon gate layer

No explanation why field enhancement would forward bias p-n junction, which is necessary to conduct current.

No meaningful current path through lightly-doped substrate, as IPB suggests

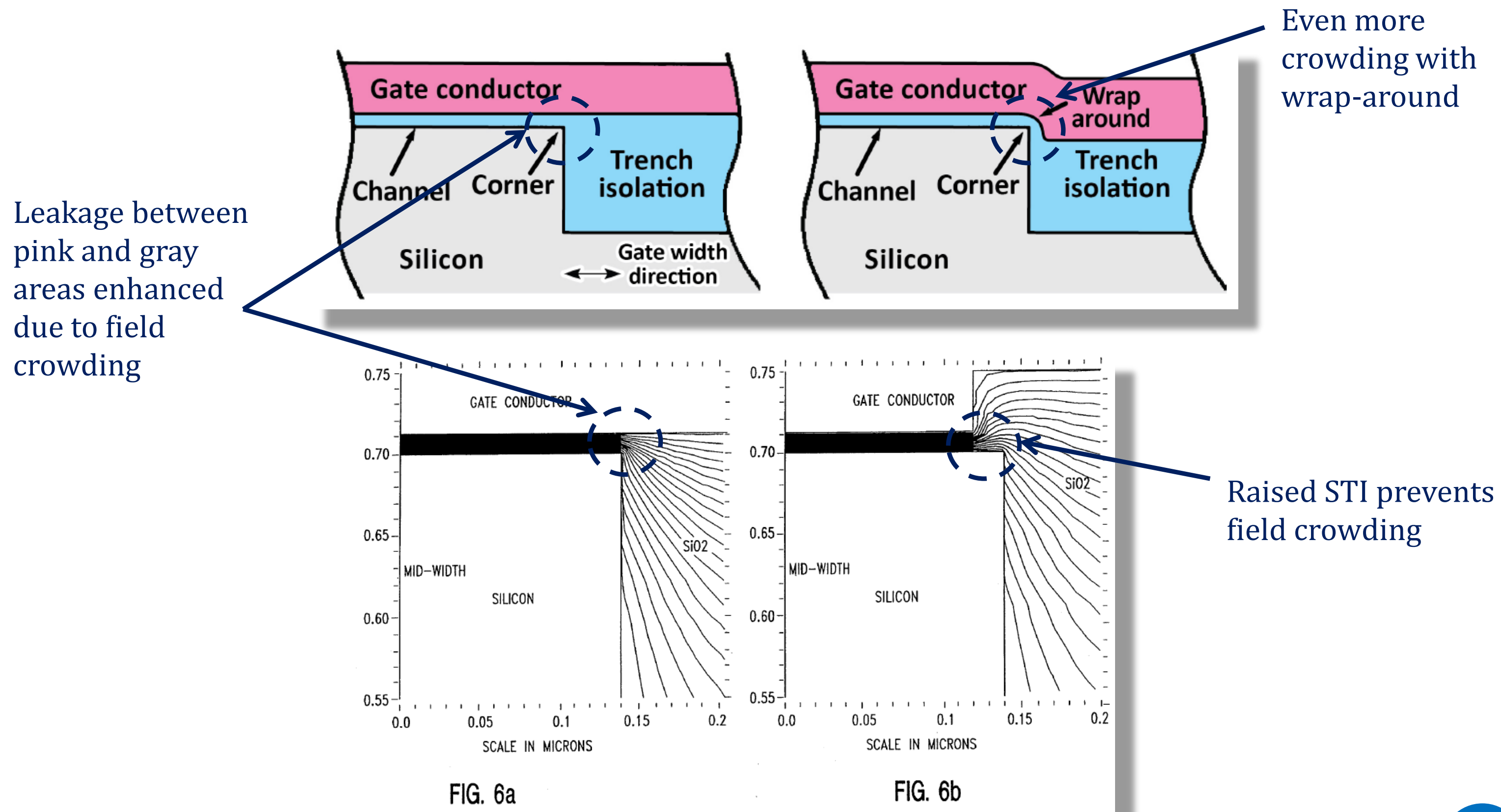


Channel stop is designed to prevent this type of leakage path; no evidence the a small bump would undo that

E.g., Sur-Reply (Paper 37) at 29.

The Small Bump, or "Jog," Does Not Hurt Isolation

- IPB's argument involves gate leakage, not the "jog"



E.g., EX2012 at ¶¶ 195–197, 342, 361–363; EX1016 at FIGS, 6a, 6b.

The Small Bump, or "Jog," Does Not Hurt Isolation

Table 3 Comparison of last generation of LOCOS isolation with first generation of STI isolation in IBM DRAMs.

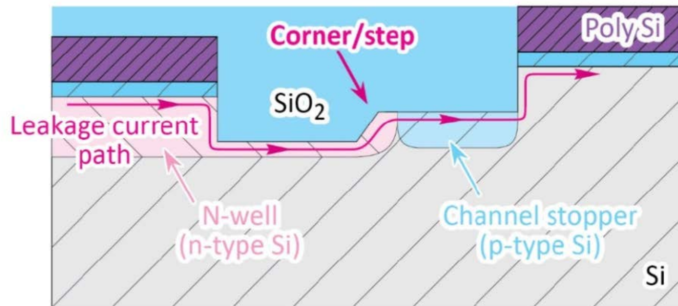
Parameter	*4 Mb (LOCOS)*	*16 Mb (STI)*
Process complexity	Low	High (50% increase in number of steps)
Minimum isolation width, drawn dimension	0.5 μm	0.55 μm
Minimum active area width, drawn dimension	1.3 μm	0.60 μm
Nominal isolation oxide thickness	240 nm	570 nm
Surface topography (step height)	90 nm	50 nm
Active area width reduction (drawn wafer)	0.45–0.75 μm	0.10–0.25 μm
Depth of isolation oxide (position of bottom below silicon surface)	0.25 μm	0.55 μm

Adler, EX1025, at 9 Tbl. 3

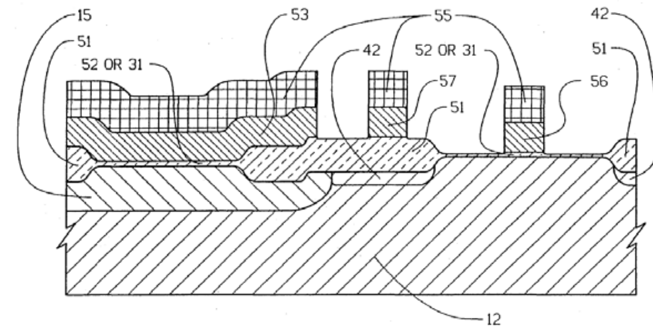
EX1025 at 9.

The Small Bump, or "Jog," Does Not Hurt Isolation

Lowrey with Noble/Ogawa:



Corner/step → Non-uniformity → Higher electric fields → Greater leakage current



- Patent Owner exaggerated height of jog
- Height of jog is less important for STI because STI thickness is more than double LOCOS thickness

Parameter	4 Mb (LOCOS)	16 Mb (STI)
Nominal isolation oxide thickness	240 nm	570 nm

E.g., Sur-Reply (Paper 37) at 29; EX1017, FIG. 5; EX1025 at 9, Tbl. 3.

THE LEE IMPLANT ORDER MAKES NO DIFFERENCE ON THE DEVICE STRUCTURE

Dr. Banerjee Corrected His Testimony on Implant Order

Q. I wanted to confirm something that you said before. When you ran through your explanation of Lee, did you -- did I understand you correctly that in your understanding of Lee, the lightly doped region is formed before the deeply doped region? Or the shallow region is formed before the deep region?

MR. YOCHES: I'm going to object to that question.

THE WITNESS: I misspoke earlier. In this Lee process, you actually do the deep junction first, layer 27, and then the shallow LDD region afterwards.

A. I was thinking of the vast majority of cases that are -- I was thinking off the top of my head in terms of making these LDD structures. Once again, as I said, I misspoke as it pertains to Lee. But it does not change my opinions in terms of the claim elements.

A. I had the doping sequence flipped over here, but it doesn't change my opinion about the claim elements.

EX2078 at 124:18–125:7, 126:2–17, 129:9–17.

Implant Order Is a Distinction Without Difference

Q. But despite that, you sit here as an LDD expert and you said that you couldn't imagine anyone doing it in effect the way Lee does it. Does that make Lee inoperative?

A. No.

Q. Well, you said you couldn't imagine anybody doing it that way?

A. I mean the -- the sequence in which you do the heavy versus the lightly doped implant --

Q. Yeah.

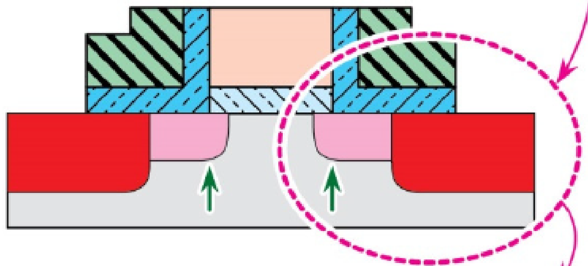
A. -- doesn't ultimately impact the device functionality. What is important is the LDD region should abut the gate electrode and the heavy source drains should be farther away.

EX2078 at 132:5–18.

The Claims Are Satisfied Regardless of Implant Order

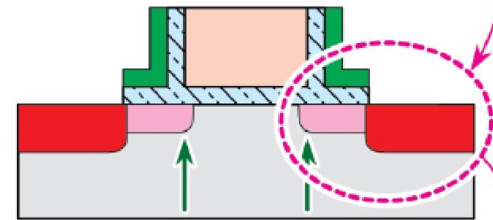
16. The semiconductor device of claim **5**, wherein the source/drain regions include low-concentration source/drain regions and high-concentration source/drain regions, and the first silicide layers are formed on the high-concentration source/drain regions.

Post-implantation annealing:



Problem: (1) Excessive diffusion required, (2) Inherent process variations, (3) Deeper junctions. → Unsuitable for 250-350 nm nodes used with STI.

Post-implantation annealing:

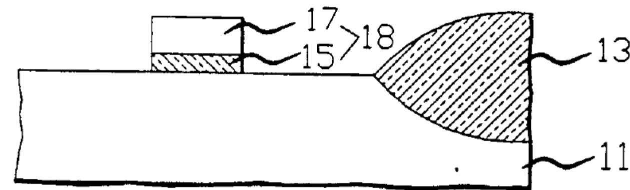


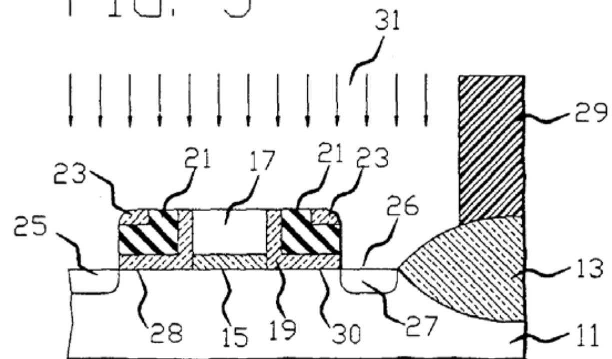
Advantage: (1) Minimal diffusion required, (2) Minimal variations, (3) Shallow junctions. → Suitable for 250-350 nm nodes used with STI.

- Implant order not something either the ’174 patent or the obviating references emphasize

EX1001 at 30:38–42; Sur-Reply (Paper 37) at 18.

Changing Implant Order Does Not Alter Lee Structure

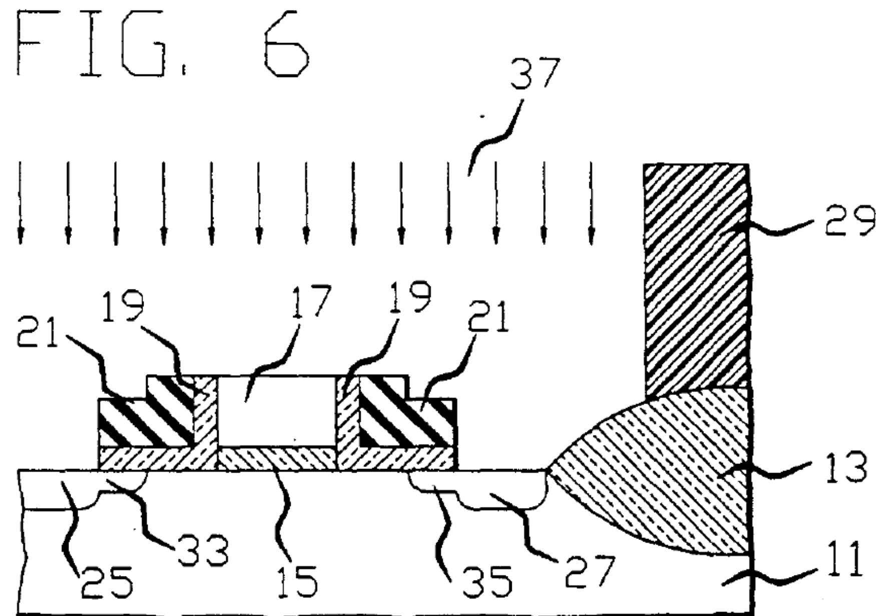




EX1002 at FIGS. 2, 5.

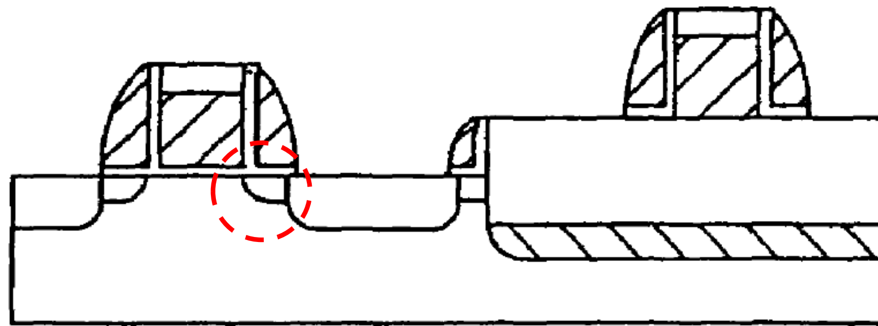
Lee Teaches Thinner Sidewalls Also Affect Profile

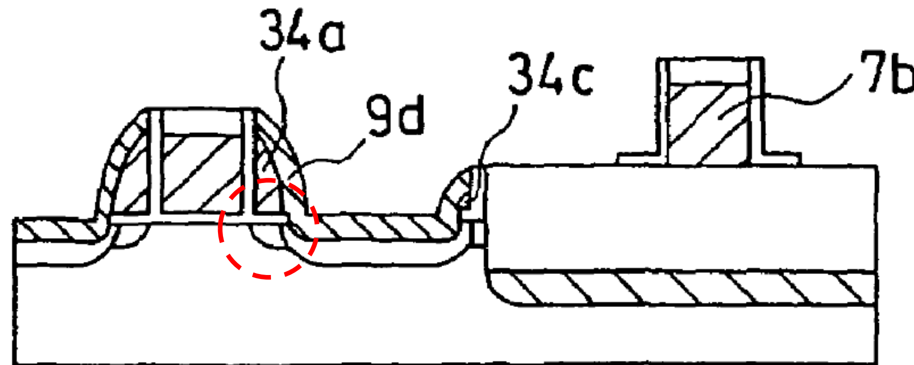
33 and 35 in portions 28 and 30 of substrate 11. Proper tailoring of the implant energy and dosage and the thickness of the feet of layers 21 and 19 permits the achievement of carefully controlled shallow junctions 33 and 35.



EX1002 at 4:24–33, FIG. 6.

The '174 Patent Lacks the Precision IPB Demands of Dr. Banerjee



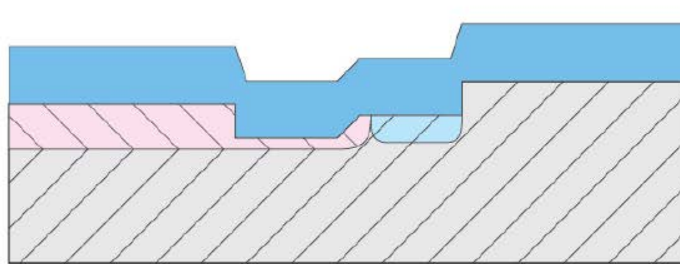


EX1001 at FIGS. 16(d), 16(e).

MISREPRESENTATIONS

IPB Misrepresents TSMC's Argument

(1) Nitride / pad-oxide removal.
(2) CVD oxide re-fill.



- Wrong order

Compare Sur-Reply (Paper 37) at 31, with Reply (Paper 21) at 21–22.

IPB Misrepresents Dr. Banerjee's Testimony

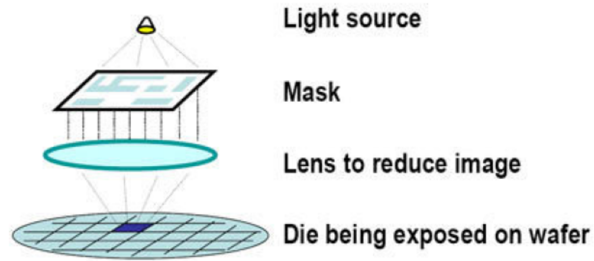
Dr. Banerjee admitted that in an established Si IC fabrication process, the layers in question, particularly the "LOCOS … silicon oxide [masking] layer"[6] would not be optional. Ex.2078, 260:20-22 ("Because when you say optional, I don't mean you do it on some wafers and you don't do it on other wafers." Ex.1056, 164:18-22 ("That's not what *Lowrey* teaches. *Lowrey* teaches the use of layer 31 – 21."). That is, an actual fabrication process would consistently include

```
      A.   Because when you say optional, I don't
mean you do it on some wafers and you don't do it on
other wafers.  You develop a process flow, either
using the boron implant or you develop a process
flow without using the boron implant.
           And if you choose the second route, you
wouldn't have a boron implant on any of the wafers.
```


Sur-Reply (Paper 37) at 39; EX2078 at 260:13–261:4.

ATTORNEY ARGUMENT

Attorney Argument



For an Si wafer with non-planar topology, the "imaging focal plane" could not be made to coincide with the wafer surface plane, so that at least a part of the mask's image on the Si wafer would be out of focus. A POSITA would have known that high-fidelity photo-lithography requires a wafer with a planar surface topology; thus, a POSITA would have avoided designs having non-planar topologies.

- Same step present in *Lowrey* and no problem with lithography.
- Depth of focus was large enough (around 1 μm) that this was not an issue.

Sur-Reply (Paper 37) at 35

A. Same answer, it is a small step of 100 nanometers.

EX2078 at 259:7–8

Sur-Reply (Paper 37) at 35; EX2078 at 259:7–8.

Unsupported Attorney Argument re: Technical Details

- **Unsupported Attorney Argument Regarding Technical Details**
  - Sections III.A.2 and III.A.3 (process nodes)
  - Section III.B (embedded/non-embedded STI)
  - Section III.B (ion implant order)
  - Section III.C.1 ("jog" in the isolation)
  - Section III.C.1 (photolithography)
  - Section III.C.3 (L-shaped sidewalls)
- **Responses to Arguments Not Presented in PO Response**
  - Sections III.A.2 and III.A.3 (process nodes)
  - Section III.B (ion implant order)
  - Section III.C.1 (photolithography)
- **Reiterated Argument From the PO Response**
  - Section III.A.1

See generally Sur-Reply (Paper 37).

OTHER ISSUES

LEVEL OF ORDINARY SKILL

Level of Ordinary Skill in the Art

• TSMC's Proposal

A POSITA would possess (1) the equivalent of a Master of Science degree from an accredited institution in electrical engineering, materials science, physics, or the equivalent; (2) a working knowledge of semiconductor processing technologies for integrated circuits; and (3) at least two years of experience in related semiconductor processing analysis, design, and development. Additional graduate education could substitute for professional experience, and significant work experience could substitute for formal education. (Ex. 1004, ¶72.)

• Board Agreed with TSMC

equipment manufacturing, or semiconductor materials." Based on the current record, including our review of the '174 patent and the types of problems and solutions described in the '174 patent and cited prior art, we agree with Petitioner's assessment of the level of ordinary skill in the art and apply it for purposes of this Decision. *See, e.g.*, Ex. 1001, col. 1, l. 13–col. 11, l. 9 (describing previous designs of semiconductor devices with high integration and high performance, issues with previous designs, and potential solutions).

• IP Bridge's Proposal

Patent Owner contends that a POSITA at the time the application leading to the '174 patent was filed would have at least a Bachelor's degree in Electrical, Materials, Mechanical, or Chemical Engineering, or a related degree, and at least two years of experience working in semiconductor processing and fabrication, semiconductor equipment manufacturing, or semiconductor materials. Exhibit 2012, ¶29.

Petitions (Paper 2) at 16; Institution Decision (Paper 8) at 9–10; Response (Paper 14) at 23–24; Reply (Paper 21) at 33–35.

IP Bridge's Declarant Is Not an Expert in the Field

isolation in Si MOSFETs, the subject of this IPR. Although he has experience with III-V compound semiconductors[2] and light-emitting devices (e.g., LEDs and laser diodes), those devices are very different from the Si MOSFET structures at issue in these proceedings, and they do not involve LOCOS isolation or STI.[3] His

Petitioner's Motion to Exclude (Paper 29) at 4

Q. So just so the record is clear, for publications between the years 1989 through 1996, on pages 232 to 236 of Exhibit 2055, is it your testimony that items 74, 78, 99, and 129 are the references that are most representative of your personal experience working on silicon MOSFET devices?

THE WITNESS: You asked me to limit the number of publications, and so I can have additional publications here that are relevant to the field of silicon technology.

EX1056 at 46:3–14

EX2012 at 232–36

74. H.-J. Gossmann, E. F. Schubert, D. J. Eaglesham, and M. Cerullo "Low temperature Si molecular beam epitaxy: Solution to the doping problem" *Applied Physics Letters*, **57**, 2440 (1990)

78. H.-J. Gossmann, E. F. Schubert, D. J. Eaglesham, and M. Cerullo "Si molecular beam epitaxy at room temperature: Solution to the Si doping problem" *Proceedings of the International Conference on Electronic Materials*, 11541-9008-48TM

99. (**Invited**) H.-J. Gossmann and E. F. Schubert "Delta doping in silicon" *CRC Critical Reviews in Solid State and Materials Sciences* **18**, 1 (1993)

129. (**Book**) E. F. Schubert, Editor "Delta Doping of Semiconductors" 604 pages, Cambridge University Press, Cambridge ISBN 0-521-48288-7 (1996)

Petitioner's Objections (Paper 16) at 3–4; Petitioner's Motion to Exclude (Paper 29) at 3–6; EX2012 at 213–273; EX1056 at 46:3–14, 67:18–68:7.

Declarant's Only Knowledge of Isolation is Some "Awareness"

The focus of this IPR is not doping, and certainly not delta doping, but device isolation—specifically, whether STI could substitute for LOCOS isolation. Nothing in Dr. Schubert's declarations, CV, or deposition testimony suggest he is qualified to opine on LOCOS isolation or STI. He identified no experience designing or fabricating LOCOS isolation or STI, and admitted his only exposure to MOSFET device isolation structures was a general awareness of them. EX1056 at 67:18–71:14.

Petitioner's Motion to Exclude (Paper 29) at 5–6

Q. Did you ever design or perform a process that used shallow trench isolation between 1989 and 1996?

A. I was aware of various ways to isolate devices, but I would say that the focus of my work was more on the doping, more on the device design. And I was aware of, as I indicated earlier, of trenches in silicon, and how they came about with DRAM structures, that there was a desire to reduce the area used up by a capacitor. And trenches, in general, were also -- no. I was aware of trenches that can be formed in silicon technology devices.

EX1056 at 67:18–68:7

Petitioner's Objections (Paper 16) at 3–4; Petitioner's Motion to Exclude (Paper 29) at 3–6; EX2012 at 213–273; EX1056 at 46:3–14, 67:18–68:7.

ATTACK ON UEDA

IP Bridge Did not Preserve its Objections to Ueda

IV. Documents Dated After the Japanese Priority Date

Patent Owner objects to the following exhibits because they have filing dates after the '174 Patent's priority date of July 27, 1995.

Exhibit 1009: filing date of October 24, 1995

Exhibit 1013: filing date of December 29, 1995

Exhibit 1014: filing date of December 12, 1995

PO Objections (Paper 12) at 4

A. Exhibit 1014 ("Ueda") Should Be Excluded As It Is Not Prior Art

Exhibit 1014 ("*Ueda*") is not prior art under 35 U.S.C. §103 against the '174 patent because *Ueda* and the '174 patent were commonly owned by the same person (entity) at the time the claimed invention was made.

PO Motion to Exclude (Paper 32) at 1

(Fed. Cir. 2013). We also agree with Petitioner, based on the current record, that the references are prior art because the challenged claims are not entitled to the July 27, 1995 filing date of Japanese Patent Application No. 7-192181, such that the earliest potential effective filing date would be December 19, 1995. *See* Pet. 14–15 (citing Exs. 1019, 1020); Prelim. Resp. 20 (not disputing Petitioner's assertion for purposes of the Preliminary Response, but reserving the right to contest the effective filing date during trial).

Institution Decision (Paper 8) at 13 n.5

- IP Bridge did not dispute priority or challenge Ueda in its Patent Owner's Response (Paper 14).

Petitioner's Opposition to Motion to Exclude (Paper 40) at 1–3 & n.2; Institution Decision (Paper 8) at 13 n.5; Patent Owner's Objections (Paper 12) at 4; Response (Paper 14) (generally).

Ueda Provides an Example of POSITA Knowledge

- Even if not prior art, Ueda is not irrelevant because it provides evidence of what a POSITA knew about the substitutability of STI.
- A reference does not need to be prior art to show what a POSITA knew. EX1030/EX1031 show the disclosures of Ueda that TSMC cited had been published as of July 21, 1995.

Paper 40, at 1–3 & n.2

A POSITA would have understood that *Noble*'s STI was a known substitute for *Lee*'s LOCOS isolation. (Ex. 1004, ¶82; *see also* Ex. 1009, 1:31–2:24; Ex. 1011, 4:8–16; Ex. 1012, 3:3–10; Ex. 1013, 5:56–67; Ex. 1014, 22:49–52; Ex. 1015, Title,

1246 Petition (Paper 2) at 21

Besides *Schuegraf*, other references demonstrate that replacing *Lee*'s LOCOS with *Noble*'s STI would have constituted a simple substitution of one element for an equivalent element, according to known methods, to achieve predictable results. (Ex. 1011, 4:8–16; Ex. 1012, 3:1–10; Ex. 1013, 5:56–67; Ex. 1014, 22:49–52; *see also* Ex. 1004, ¶¶89–90.) A POSITA would have understood

1246 Petition (Paper 2) at 24–25

Ueda also teaches, "Although the isolation is composed of the LOCOS film in the above embodiments, . . . [t]he present invention is also applicable to an isolation of trench structure or the like." (*Id.*, 22:49–52.) *Ueda* even discloses how to form trench isolation. (*See id.*, 13:14–63.) Figures 12(a) through 12(f) of *Ueda*

1246 Petition (Paper 2) at 25

Petitioner's Opposition to Motion to Exclude (Paper 40) at 1–3 & n.2; 1246 Petition (Paper 2) at 5, 21, 24–26, 70; 1247 Petition (Paper 2) at 5, 21, 24–25, 62; Reply (Paper 21) at 2–4, 9, 16; EX1014 at 13:14–63, Figs. 12(a)–12(f); EX1031 at ¶¶64–72, Figs. 12(a)–12(f).

EVIDENCE TO EXCLUDE

"Cumulative" Exhibits Are Not Irrelevant

- Exhibits 1032, 1034–1035, 1042–1043, 1055, and 1057–1058 establish a history of using the techniques of Ueda, Mandelman, and the admitted prior art.

Reply (Paper 21) at 17

IPB and its declarant do not deny making raised STI structures before forming the gate layers was well-known. EX1056, 136:7-15. They could not because several references demonstrate the techniques in *Ueda*, *Mandelman*, and the admitted prior art had been known and used for over a decade. EX1057, ¶¶49-57; EX1032, 3:57-4:13; EX1034, 4:58-6:44, 7:46-8:33; EX1035, 26:59-28:33; EX1055, 61-62; EX1042, 267-68 & Fig. 1; EX1043, 651-52; EX1058, 2:48-4:46. Although these additional cited references are duplicative of evidence in TSMC's Petitions, and thus not essential to any obviousness findings, they confirm what a POSITA would have known, and contradict IPB's assertions about the need to form the gate layers before the STI.[8] Paper 14, at 64; *see also id.*, 115.

- While not necessary to establish a *prima facie* case of obviousness, this evidence rebuts IPB's argument that "it is not possible to simply start with Noble's or Ogawa's trench isolation without first forming the gate dielectric and gate conductor" (Response (Paper 14) at 64).

Reply (Paper 21) at 17–18 & nn.8, 9; Petitioner's Opposition to Motion to Exclude (Paper 40) at 5–6.

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), this is to certify that I served true and a correct copy of the **PETITIONER'S DEMONSTRATIVES** by electronic mail, on this 3rd day of August, 2017, on counsel of record for the Patent Owner as follows:

Neil F. Greenblum
ngreenblum@gbpatent.com

Michael J. Fink
mfink@gbpatent.com

Arnold Turk
aturk@gbpatent.com

Dated: August 3, 2017

By: */Lauren K. Young/*
Lauren K. Young
Litigation Legal Assistant
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.