PATENT OWNER'S DEMONSTRATIVE EXHIBIT

Case IPR2016-01246

August 7, 2017

IP Bridge Exhibit 2079
TSMC v. IP Bridge
IPR2016-01246

Given this evidence, we conclude that Dr. Schubert's conflicting testimony creates genuine issues of material fact as to whether a person of ordinary skill in the art would have been motivated and able to fabricate the semiconductor device of Lee, replacing its LOCOS with trench isolation as taught by Noble. *Compare* Ex. 1004 ¶¶ 82–96, *with* Ex. 2001 ¶¶ 109–30.

Institution Decision, Paper 8, p. 17-18

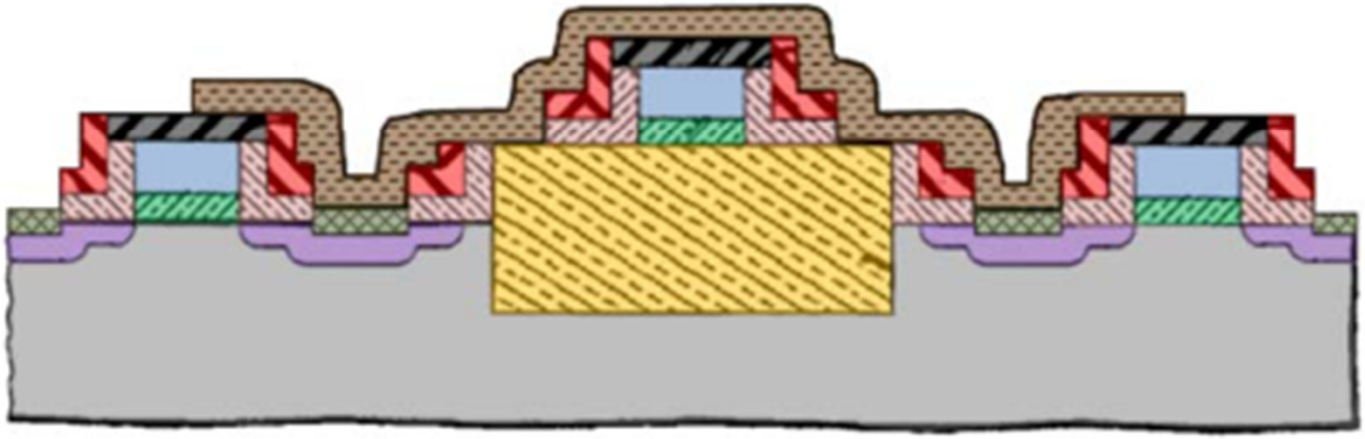
Owner, performing the STI process on Lowrey, including planarization, would result in problems due to the non-uniformity of the trench, as well as leaving unwanted insulation material on the wafer and/or removing wanted material (such as the gate conductor) from the surface of the wafer. *Id.* at 35–40. Patent Owner further argues that performing the STI process on Lowrey would also cause a p-n junction under the STI at the point where Lowrey's p-type and n-type doped regions meet, resulting in "enhanced leakage currents." *Id.* at 40–42.

Institution Decision, Paper 8, pp. 25-26

it in Lowrey instead of LOCOS. *See* -1247 Pet. 21–44. Petitioner's arguments are supported by the prior art of record and Dr. Banerjee's testimony. Dr. Schubert's conflicting testimony creates genuine issues of material fact as to whether a person of ordinary skill in the art would have been motivated and able to fabricate the semiconductor device of Lowrey, replacing its LOCOS with trench isolation as taught by Noble. *Compare* -1247 Ex. 1004 ¶¶ 80–94, *with* -1247 Ex. 2001 ¶¶ 111–35. We view those issues in the light most favorable to Petitioner at this stage of the proceeding. *See* 37 C.F.R. § 42.108(c).

Institution Decision, Paper 8, p. 26

FIG. 15'



Substrate (Si)

Trench Isolation (SiO_2)

Conductor (poly-Si, Al, Au, W, silicide, etc.)

Gate Electrode/Interconnection (poly-Si)

Protective Nitride (Si_3N_4 or SiON)

Spacer (SiO_2)

Spacer (Si_3N_4 or SiON)

Gate Oxide (SiO_2)

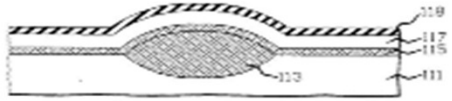
Optional Silicide

Optional LDD Source/Drain

Petitioner's Reply, Paper 21, p. 20

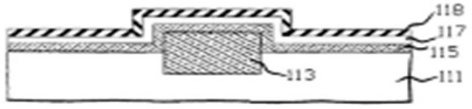
6:46-61, FIG. 11. To substitute *Noble*'s and *Ogawa*'s STI structures for *Lee*'s LOCOS isolation, a POSITA would have first made raised STI, removing the polish/etch-stop and pad oxide, and formed the gate stack. EX1057, ¶¶79-83. IPB provides no basis for asserting a POSITA would have retained the polish/etch-stop and pad oxide as the gate stack. That assertion makes no sense because, as the following figures illustrate, removing those features makes trivial the substitution, TSMC described in its Petitions. EX1057, ¶¶80-83; Paper 2, at 21, 70.

FIG. 11



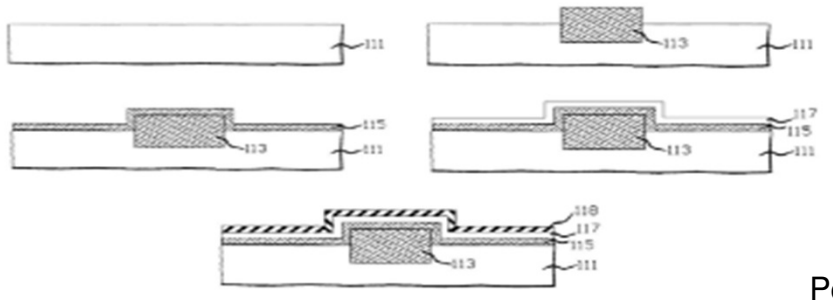
***Lee* FIG. 11**

FIG. 11′



Modified *Lee* FIG. 11

Instead of LOCOS, raised STI 113 is formed by any of the well-known processes discussed above. *Id.* Then, as in *Lee*, gate oxide 115, polysilicon 117, and silicon nitride/silicon oxynitride layer 118 are successively deposited. EX1057, ¶83.



Petitioner's Reply, Paper 21, p. 19

FIG. 4

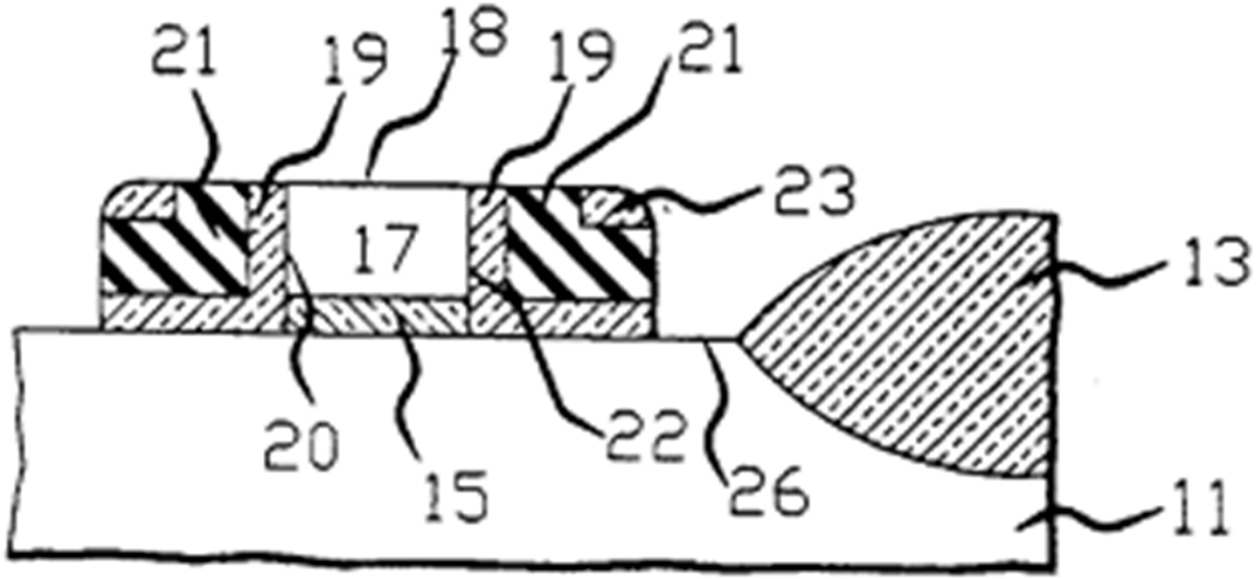
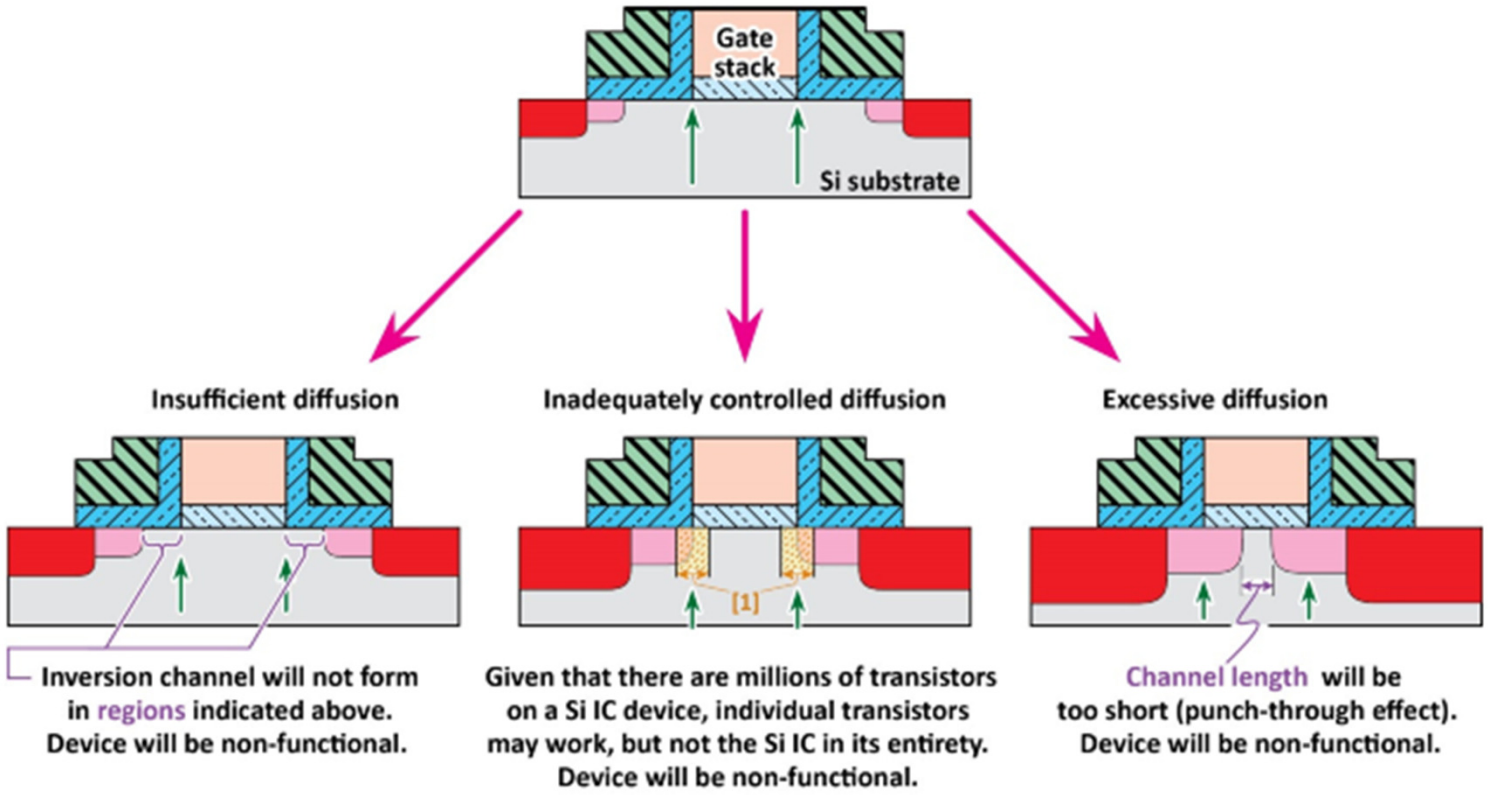
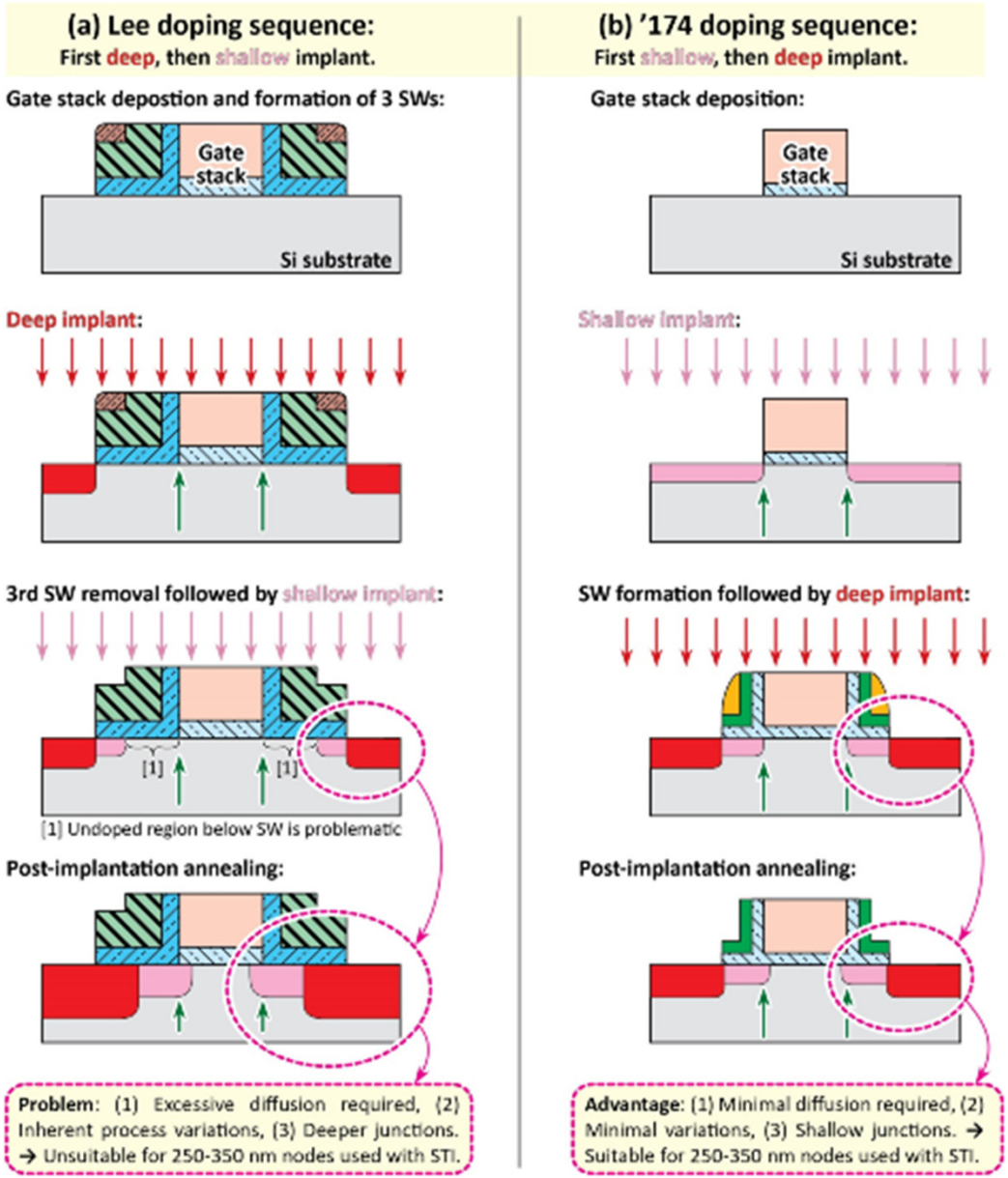


Exhibit 1002, Lee, Fig. 4



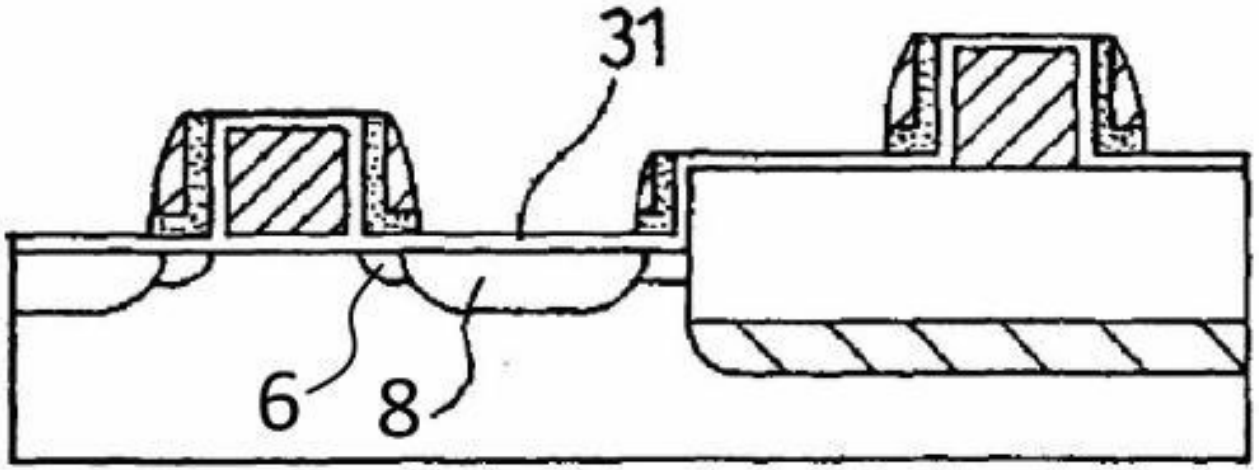
[1] Double arrows represent variation in diffusion, $\Delta L_{Diffusion}$; this quantity is inherently long because $L_{Diffusion}$ is long.



Patent Owner's Sur-Reply, Paper 37, p. 18

Segawa/'174 Patent

FIG. 15(d)



Patent Owner's Response, Paper 14, p. 18
Exhibit 1001, '174 Patent, Fig. 15(d)

Segawa ('174 Patent)

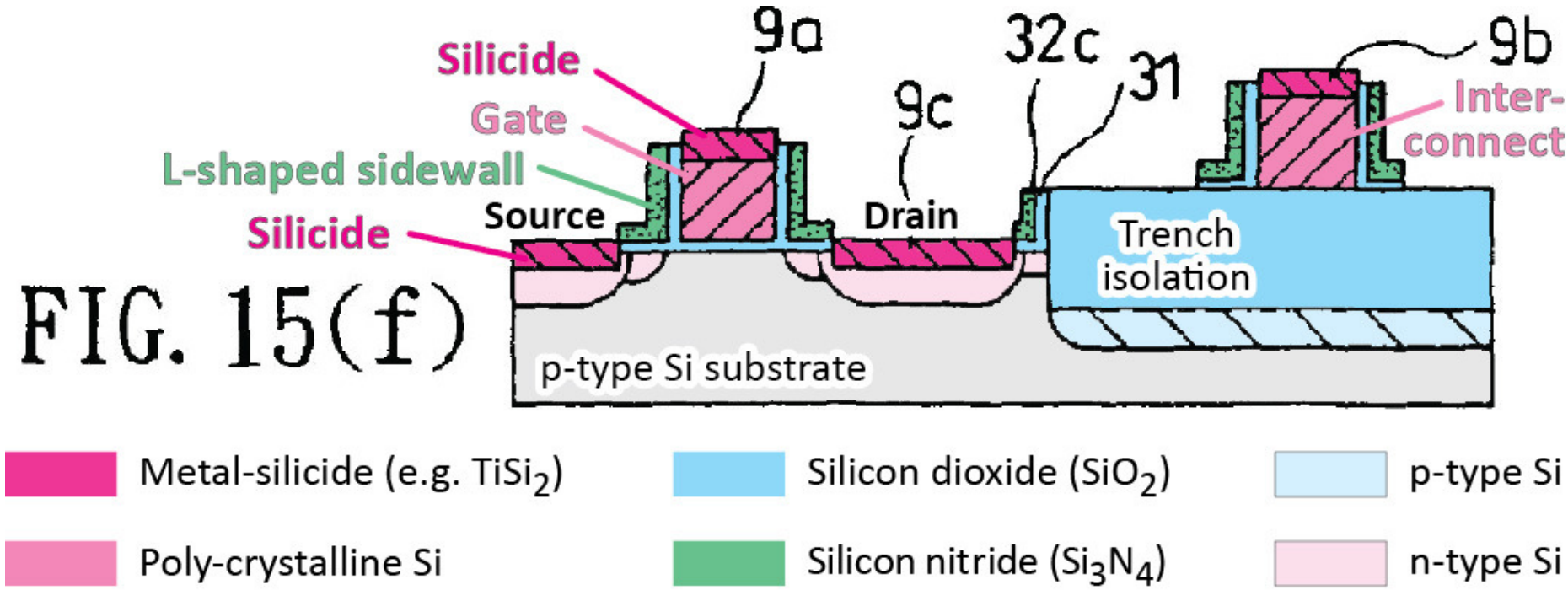
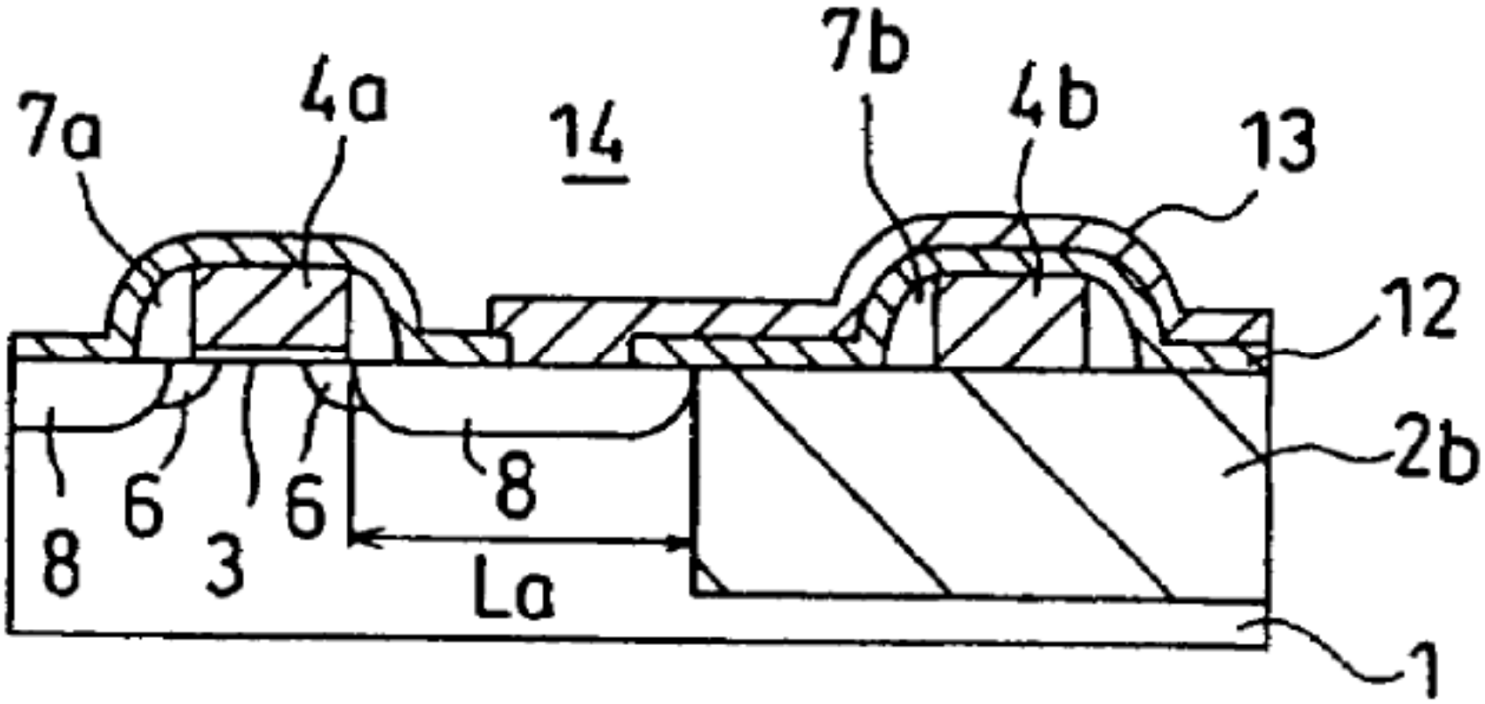


FIG. 15(f)

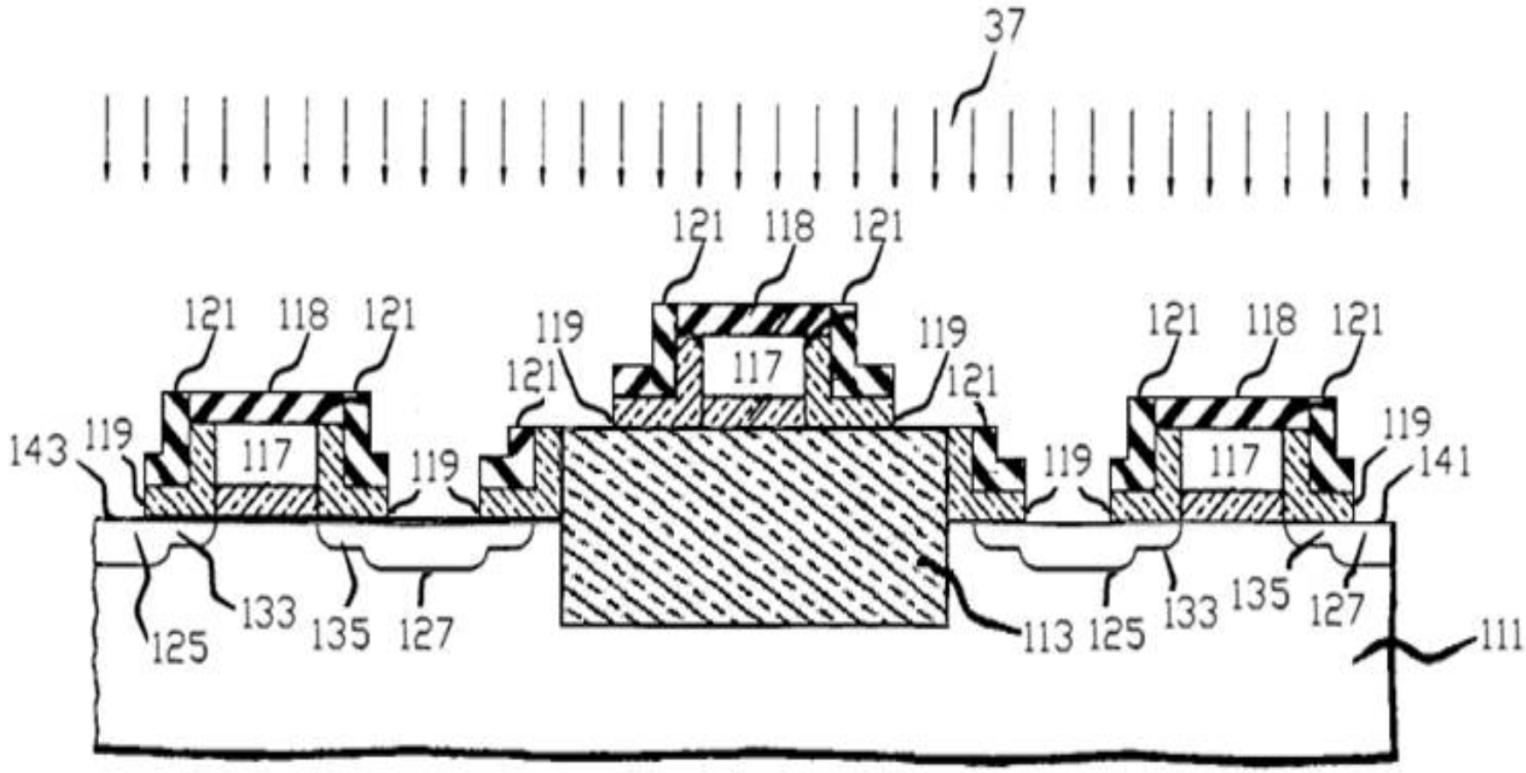
IPR2016-01246 Patent Owner's Preliminary Response, Paper 7, p. 17;
IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 19
Patent Owner's Response, Paper 14, p. 15
Exhibit 1001, '174 Patent, Fig. 15(f)

Segawa/‘174 Patent

FIG. 17
PRIOR ART



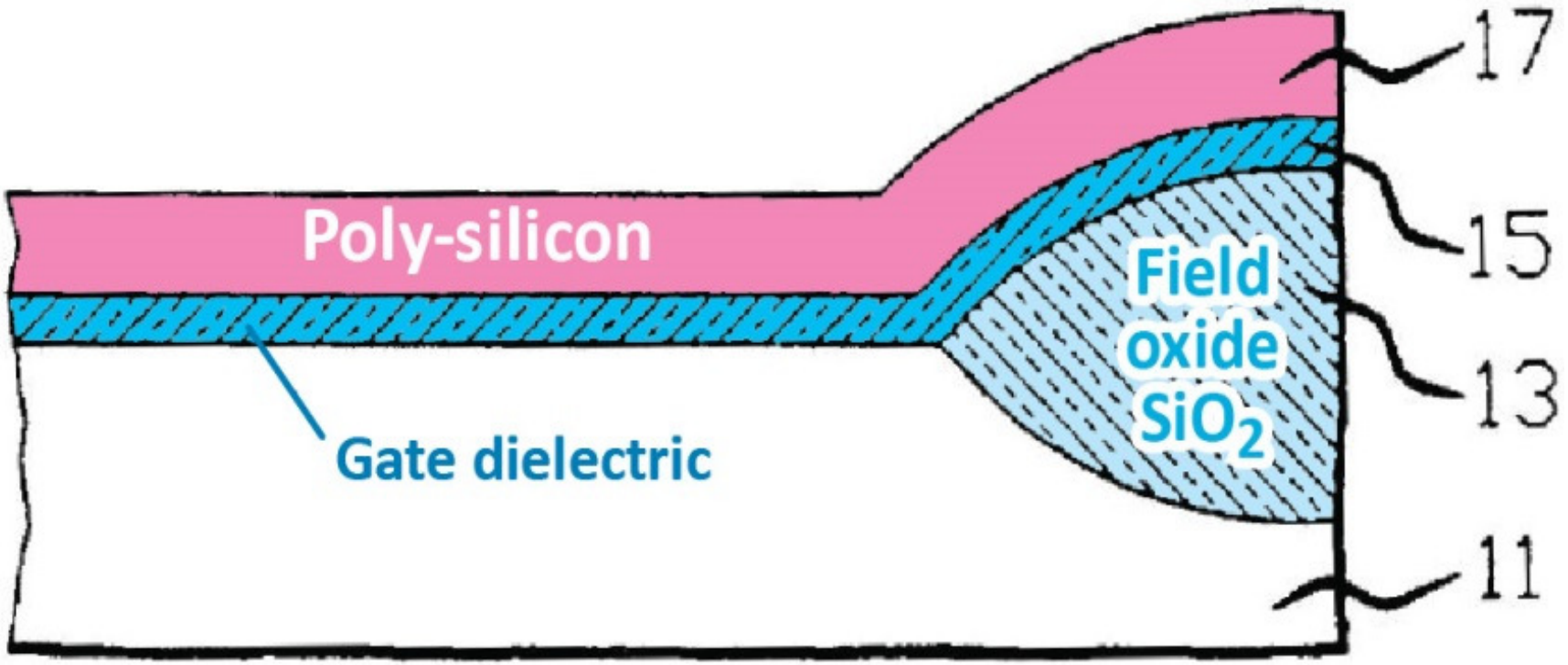
Patent Owner’s Response, Paper 14, p. 49
Exhibit 1001, ‘174 Patent, Fig. 17



Patent Owner's Sur-Reply, Paper 37, p. 21
Exhibit 1002, Lee, Fig. 6 (Modified)

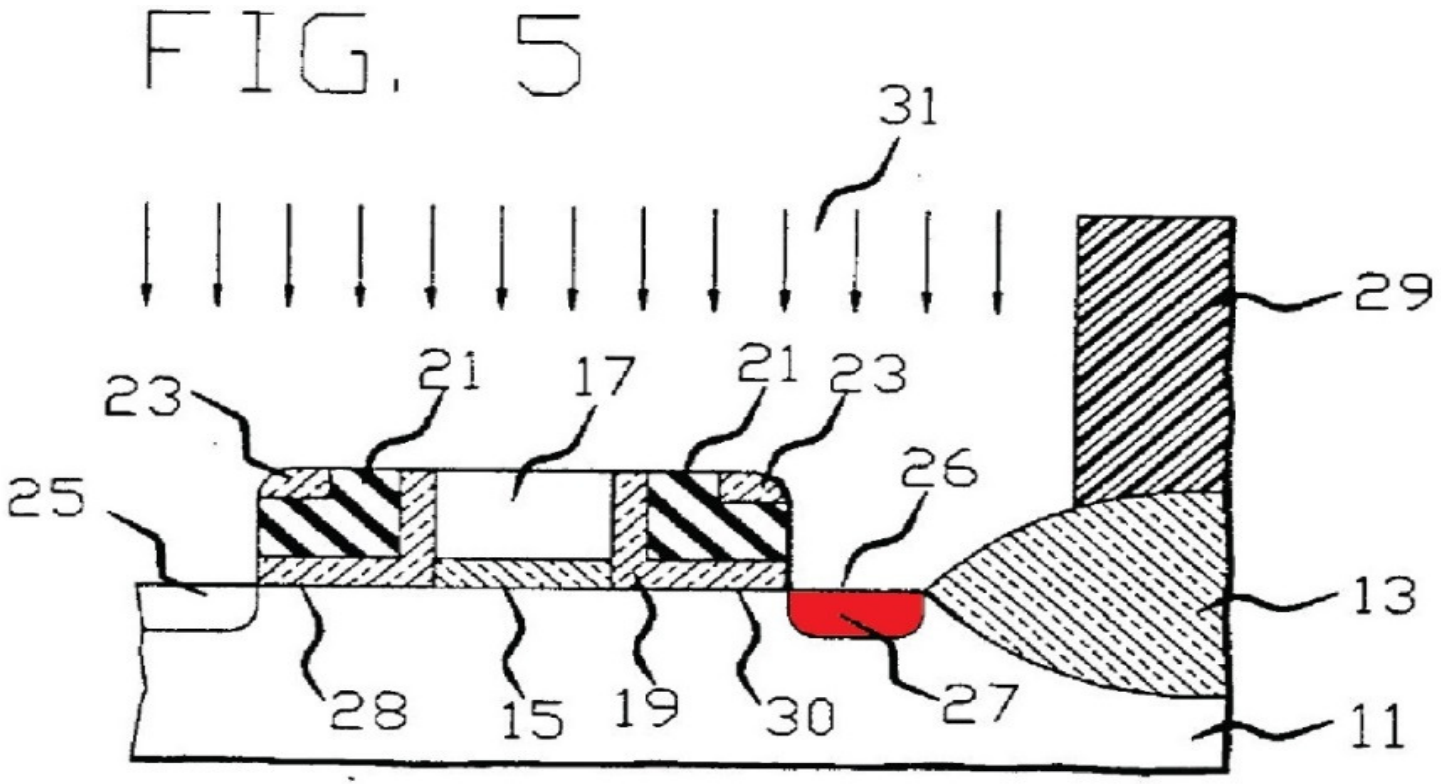
Lee

FIG. 1



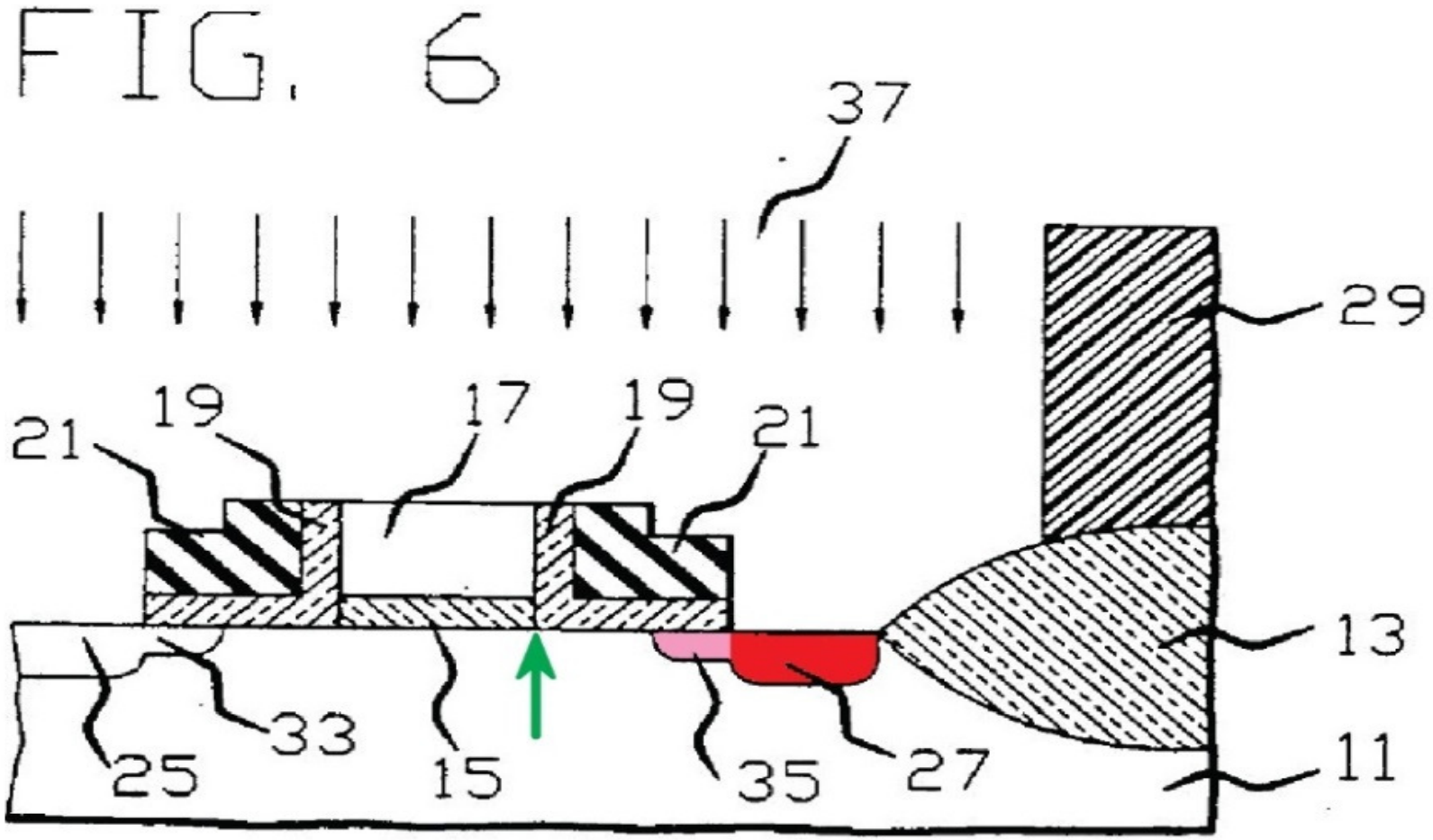
IPR2016-01246 Patent Owner's Preliminary Response, Paper 7, p. 21;
Patent Owner's Response, Paper 14, p. 21
Exhibit 1002, Lee, Fig. 1

Lee



Patent Owner's Sur-Reply, Paper 37, p. 12
Exhibit 1002, Lee, Fig. 5

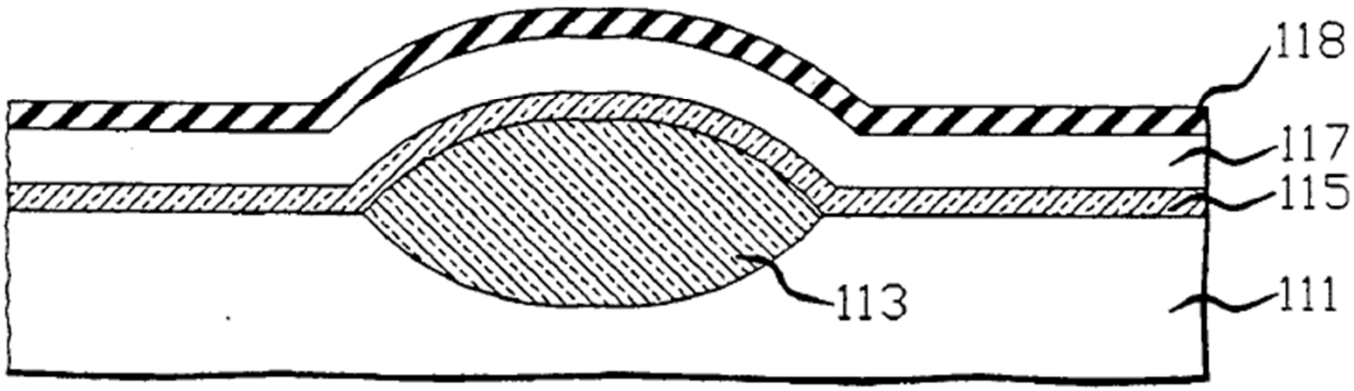
Lee



Patent Owner's Sur-Reply, Paper 37, p. 13
Exhibit 1002, Lee, Fig. 6

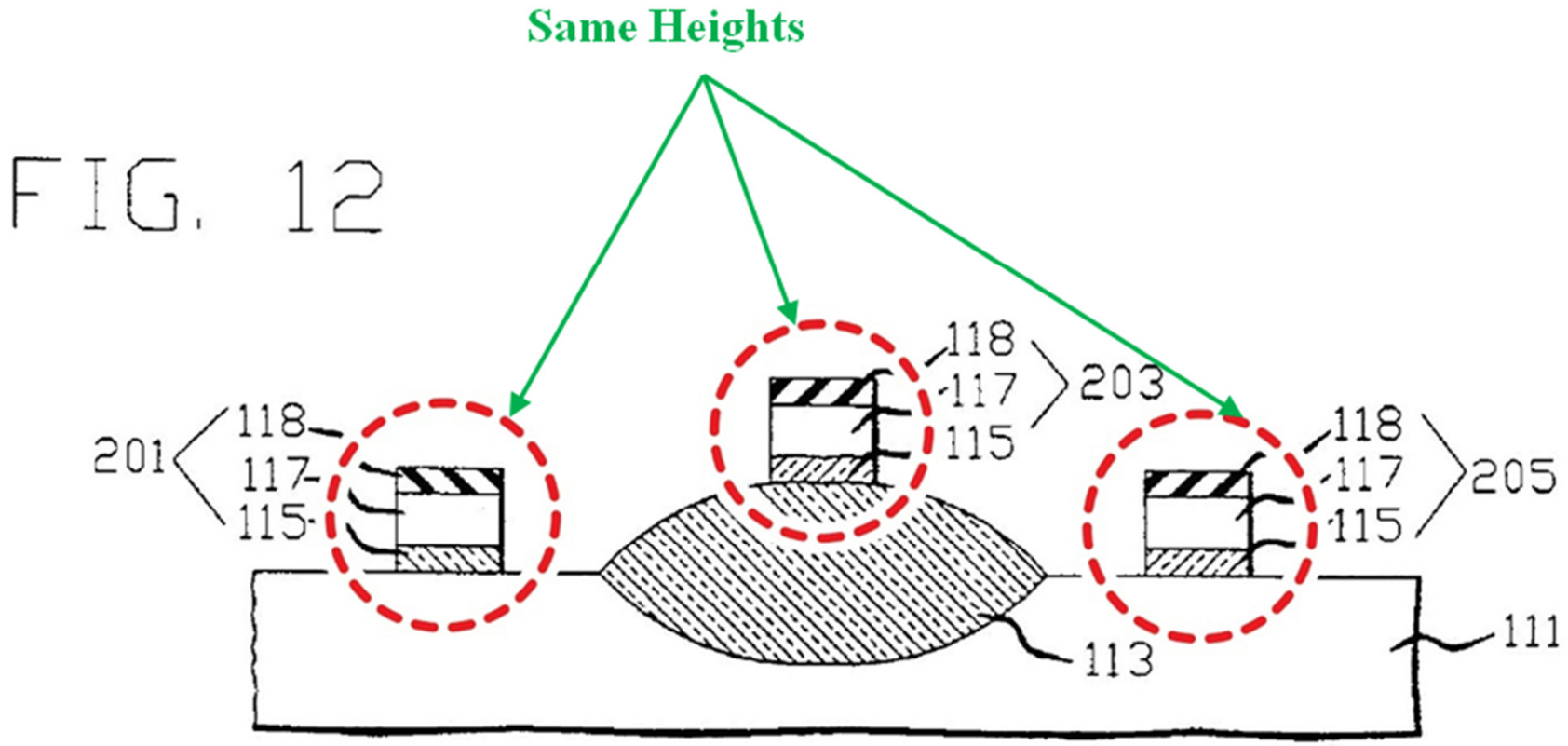
Lee

FIG. 11



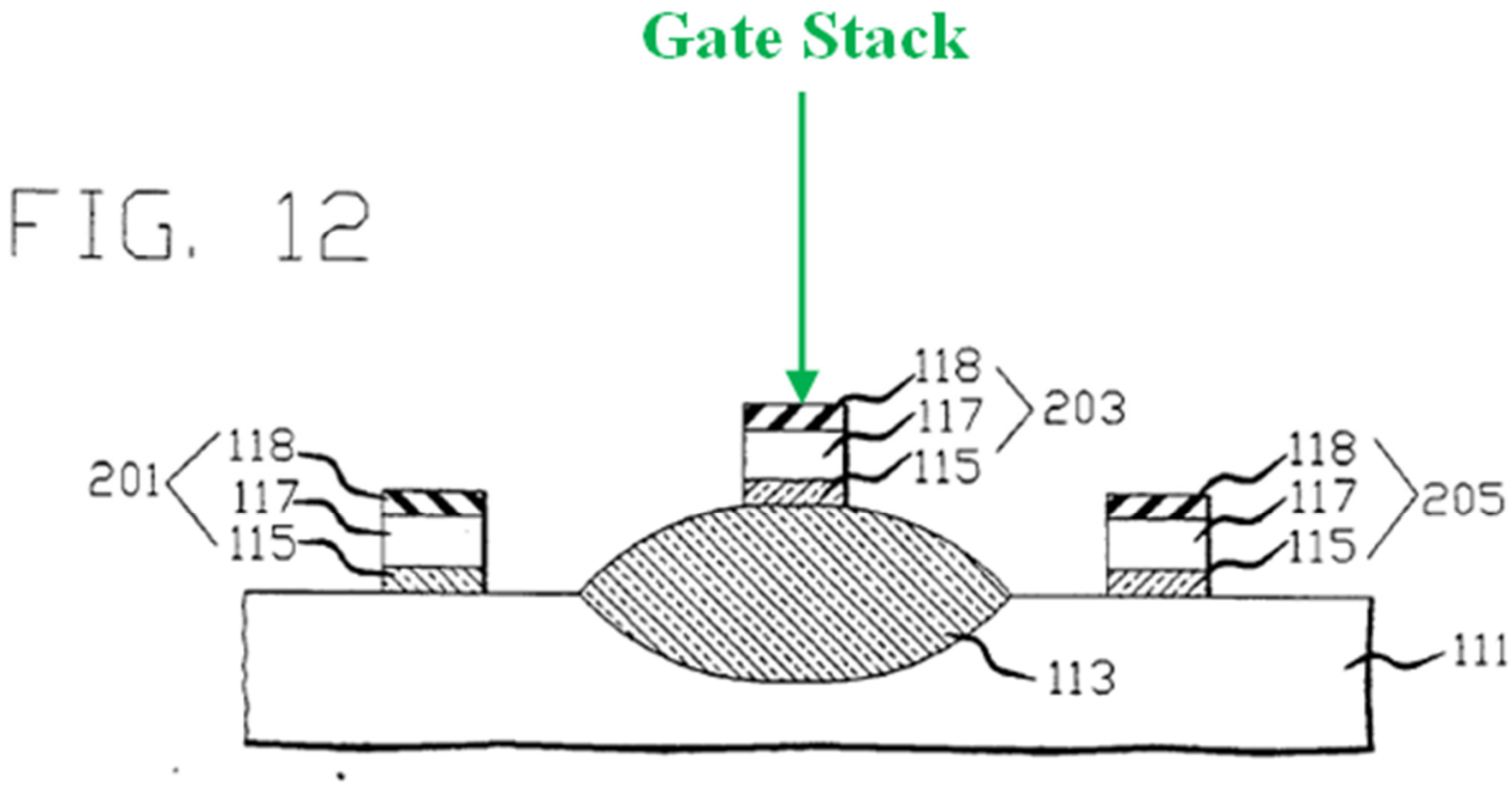
Patent Owner's Response, Paper 14, pp. 25, 45, 51
Exhibit 1002, Lee, Fig. 11

Lee



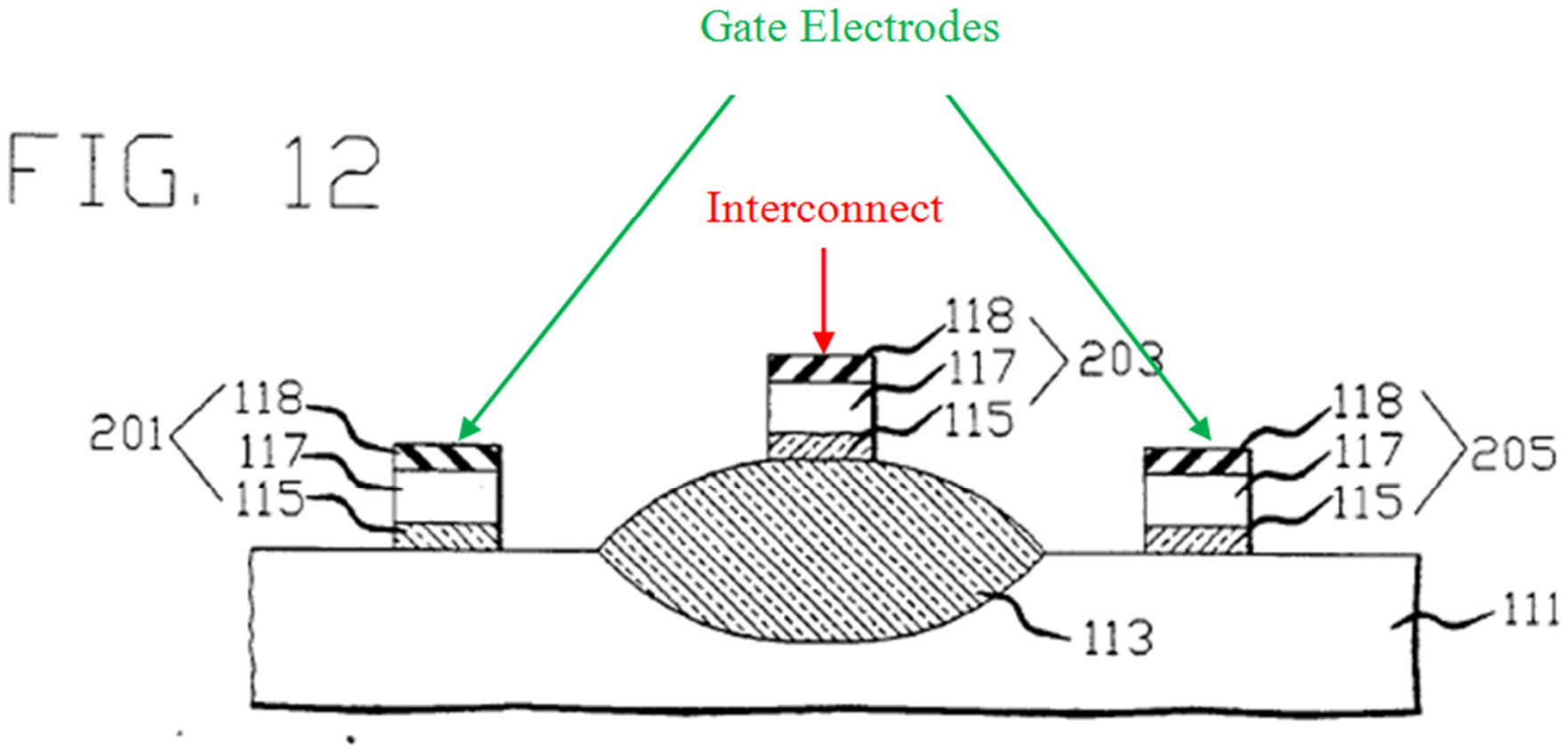
Patent Owner's Response, Paper 14, p. 67
Exhibit 1002, Lee, Fig. 12

Lee



Patent Owner's Response, Paper 14, p. 46
Exhibit 1002, Lee, Fig. 12

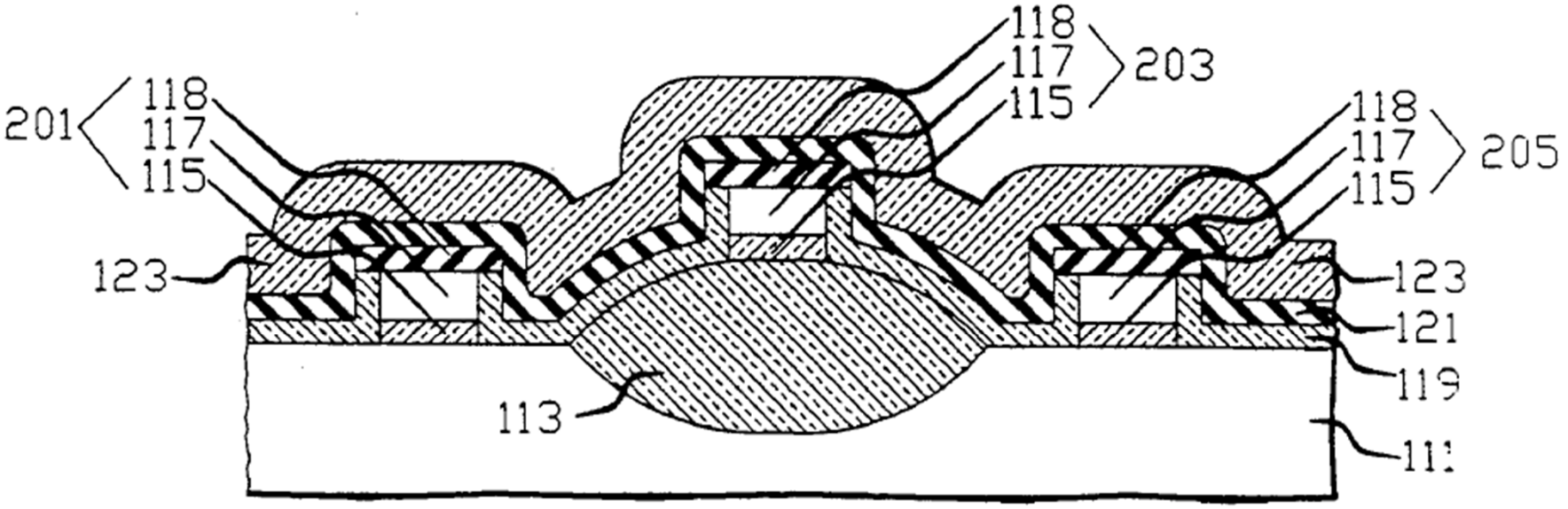
Lee



Patent Owner's Response, Paper 14, p. 53
Exhibit 1002, Lee, Fig. 12

Lee

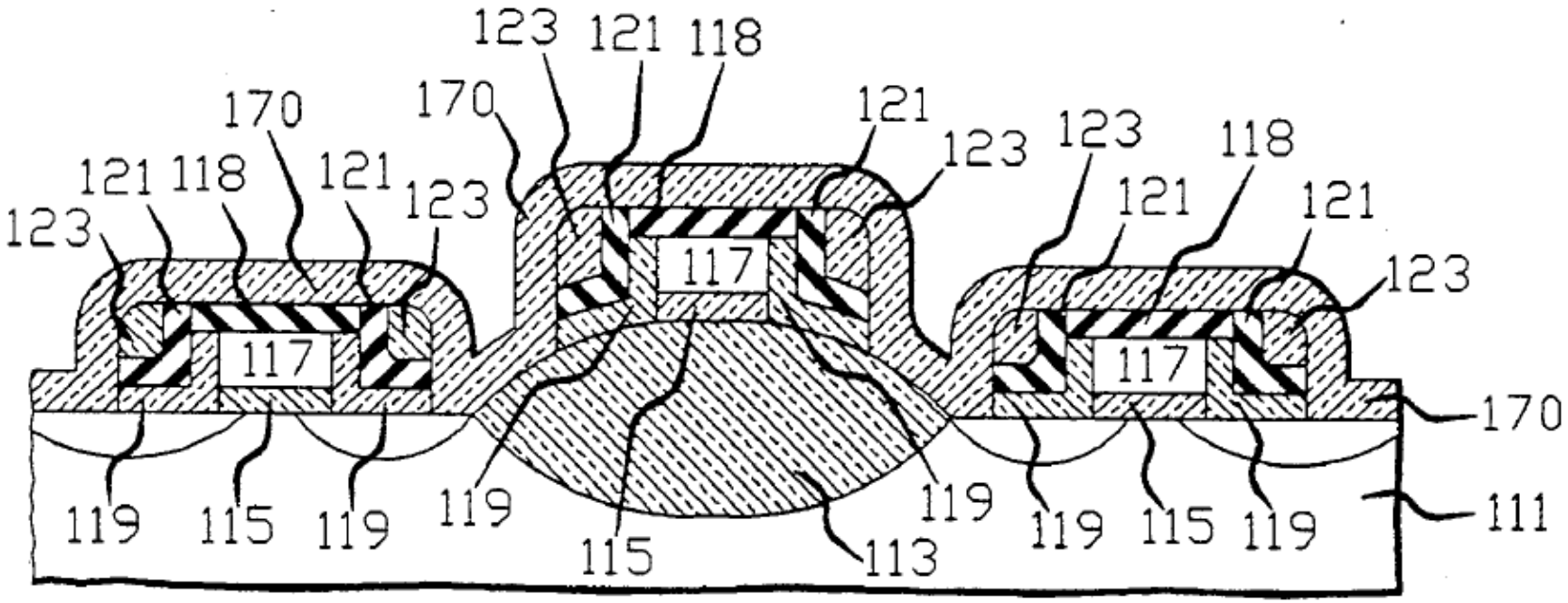
FIG. 13



Patent Owner's Response, Paper 14, p. 26
Exhibit 1002, Lee, Fig. 13

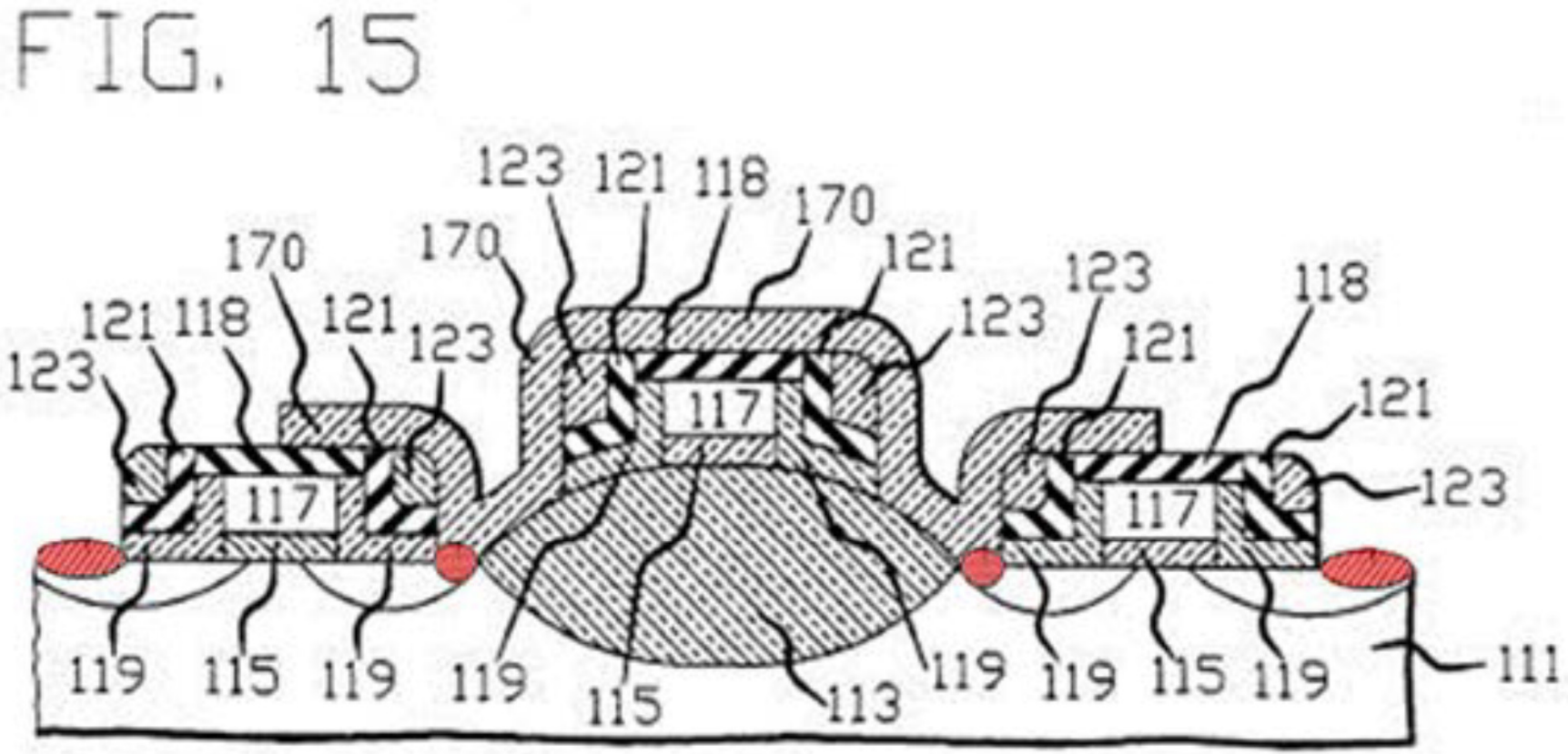
Lee

FIG. 14



Patent Owner's Response, Paper 14, p. 80
Exhibit 1002, Lee, Fig. 14

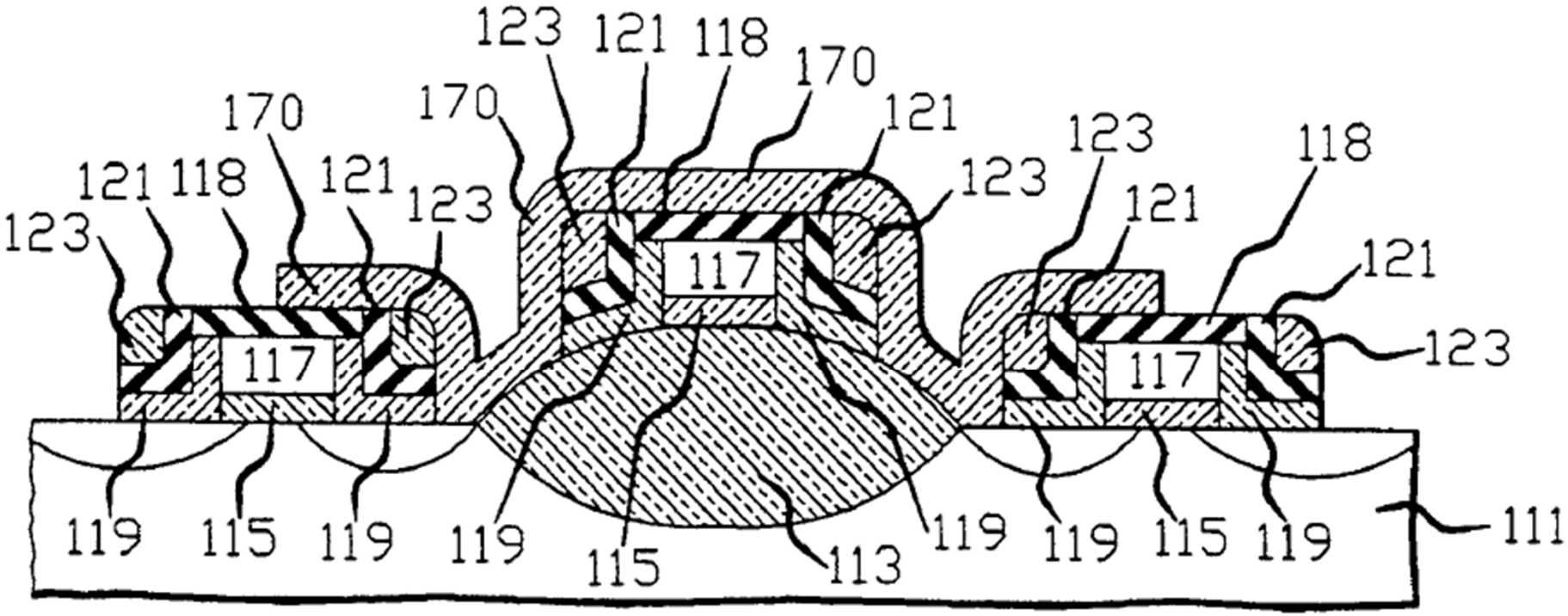
Lee



Patent Owner's Response, Paper 14, p. 82
Exhibit 1002, Lee, Fig. 15

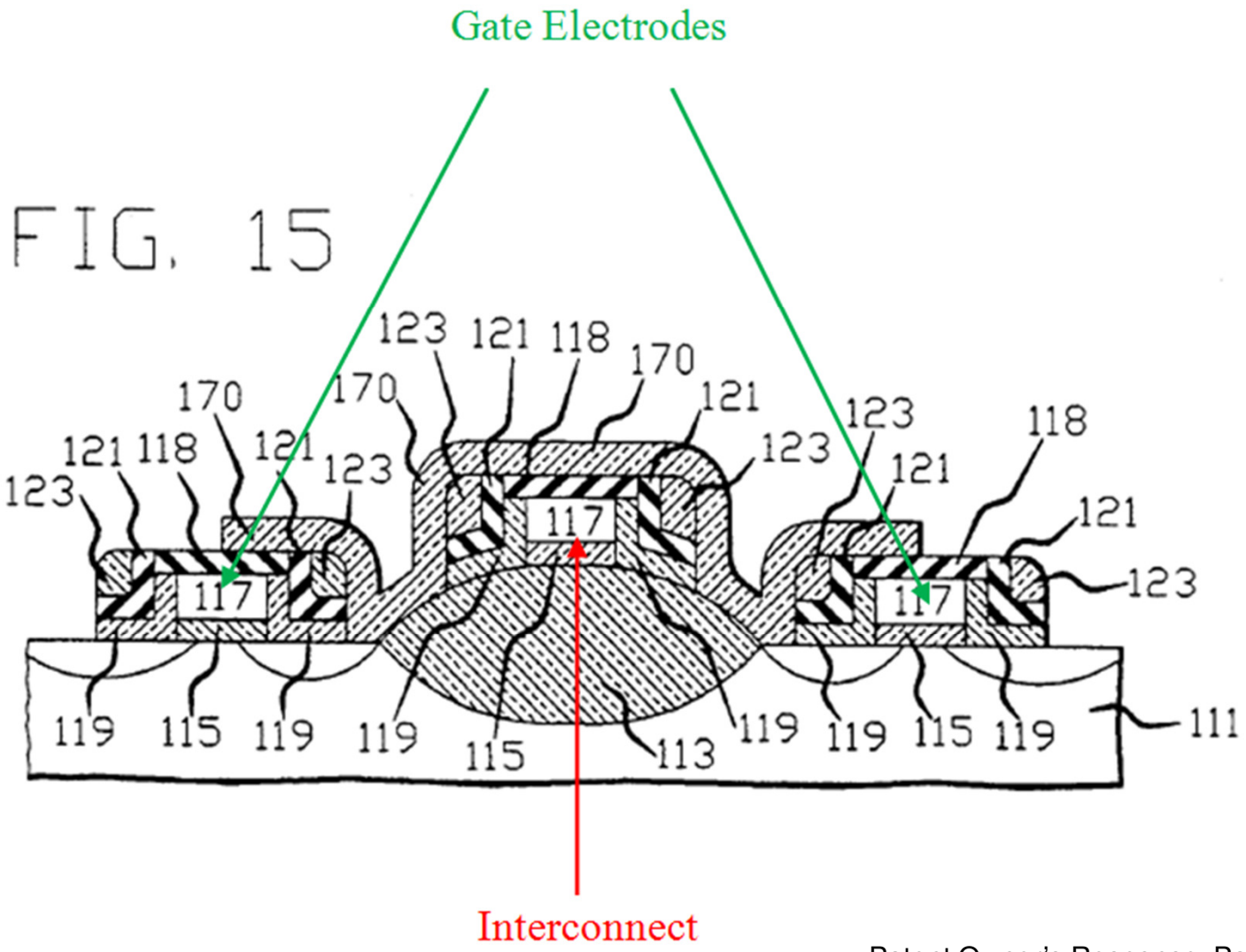
Lee

FIG. 15



Patent Owner's Response, Paper 14, p. 26
Exhibit 1002, Lee, Fig. 15

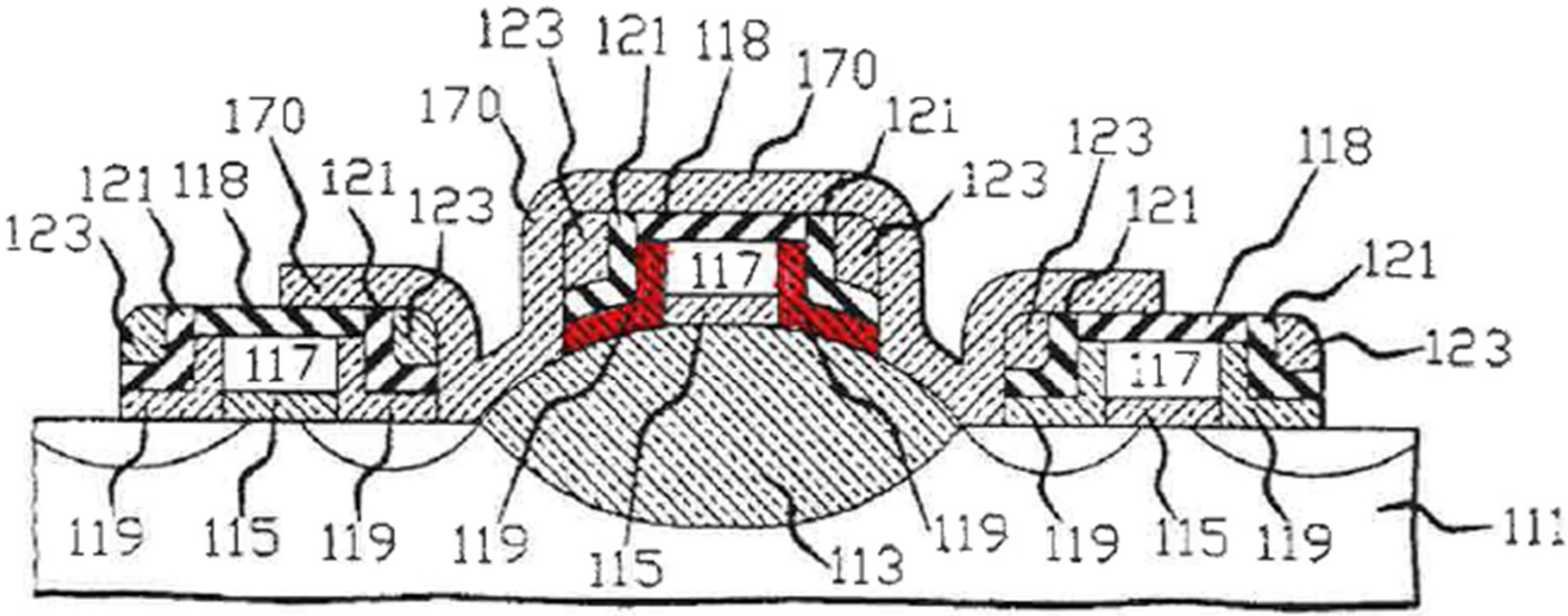
Lee



Patent Owner's Response, Paper 14, p. 52
Exhibit 1002, Lee, Fig. 15

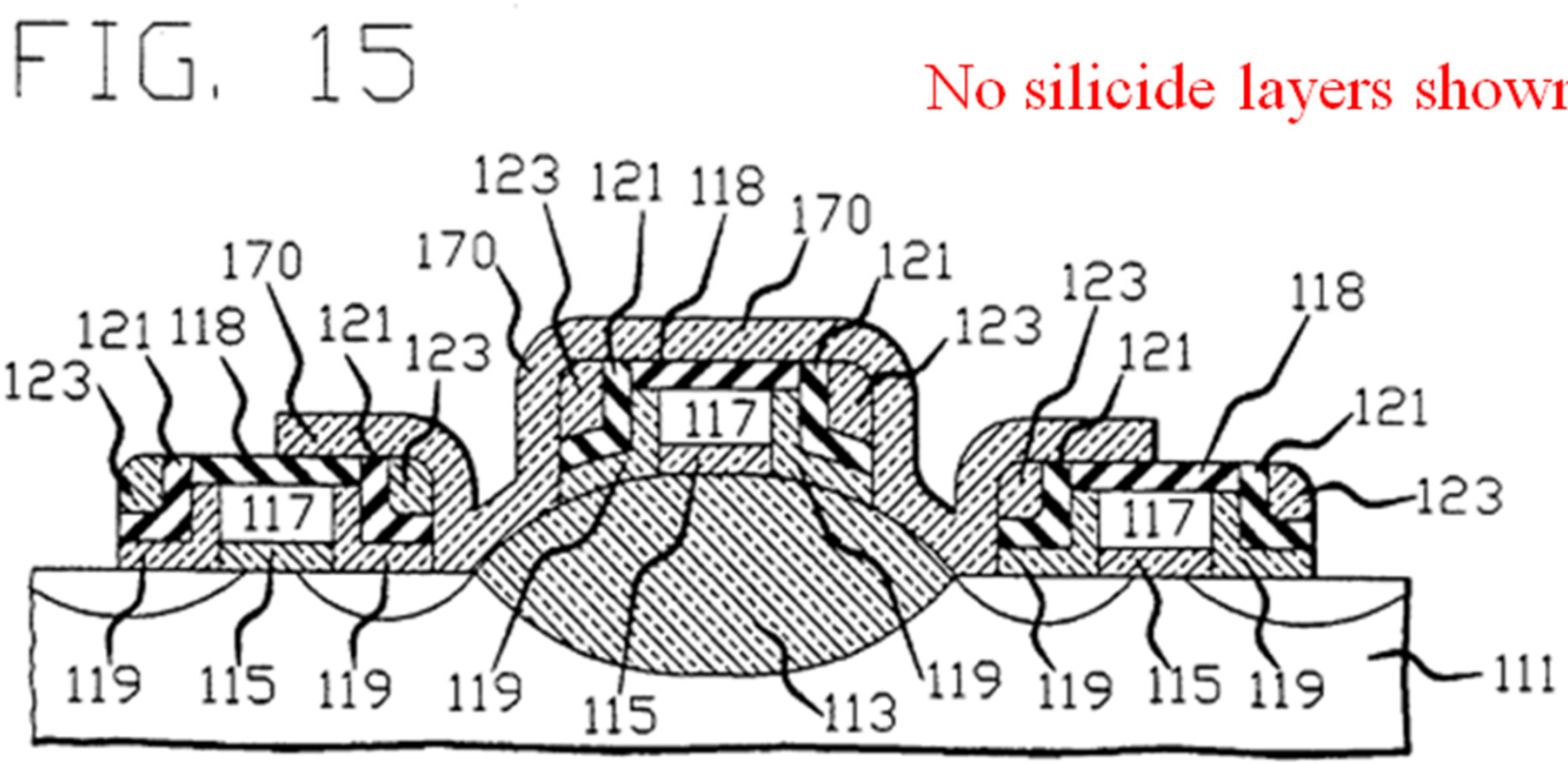
Lee

FIG. 15



Patent Owner's Response, Paper 14, p. 71
Exhibit 1002, Lee, Fig. 15

Lee



Patent Owner's Response, Paper 14, p. 79
Exhibit 1002, Lee, Fig. 15

Noble

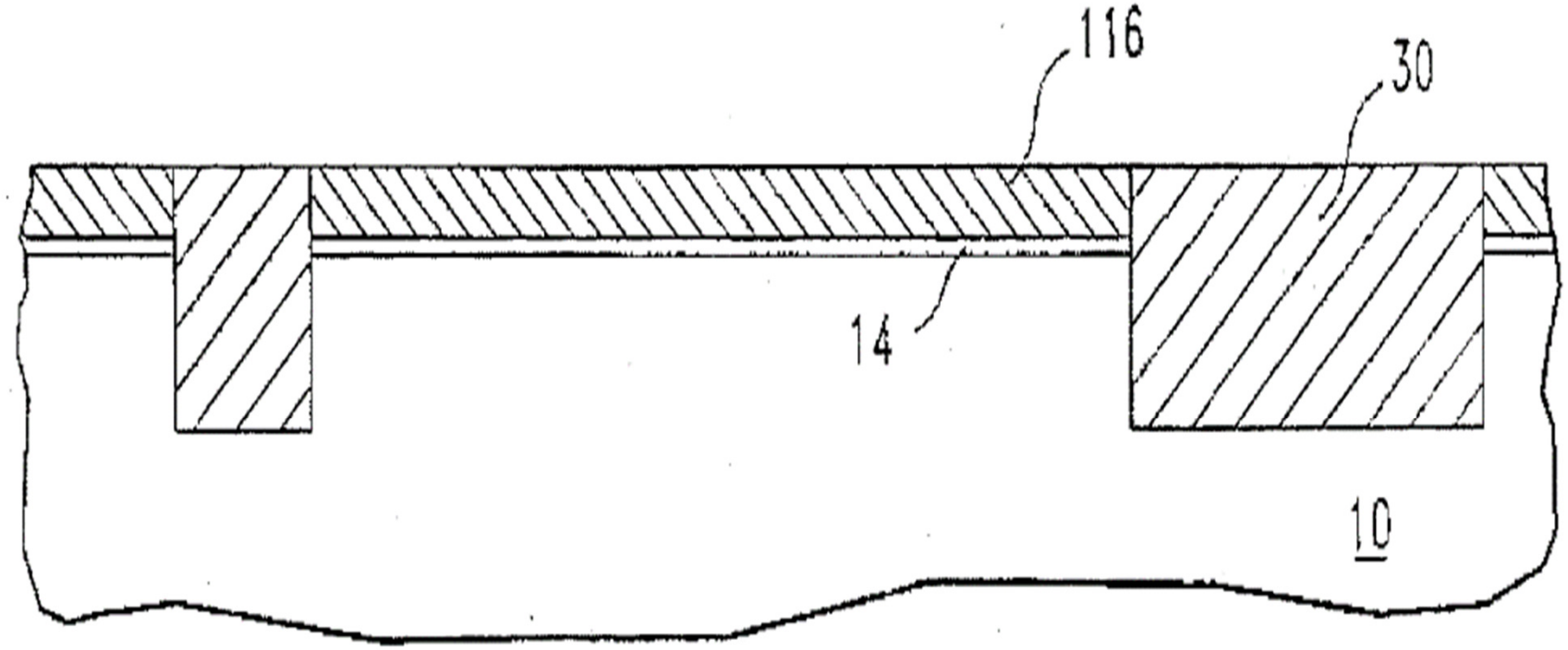


FIG. 9

IPR2016-01246 Patent Owner's Preliminary Response, Paper 7, p. 28
Patent Owner's Response, Paper 14, pp. 45, 55, 105
Exhibit 1015, Noble, Fig. 9

Noble

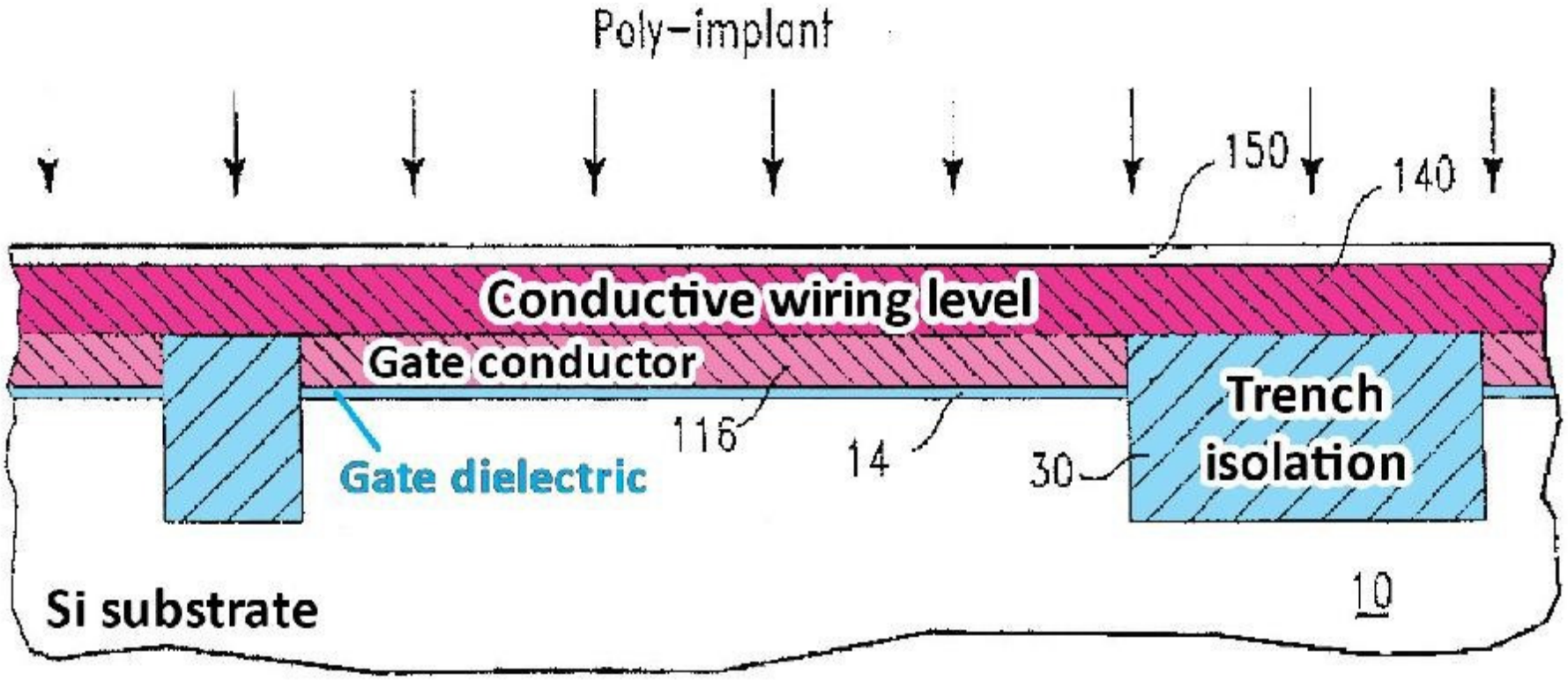


FIG. 10

Patent Owner's Response, Paper 14, p. 55
Exhibit 1015, Noble, Fig. 10

Noble

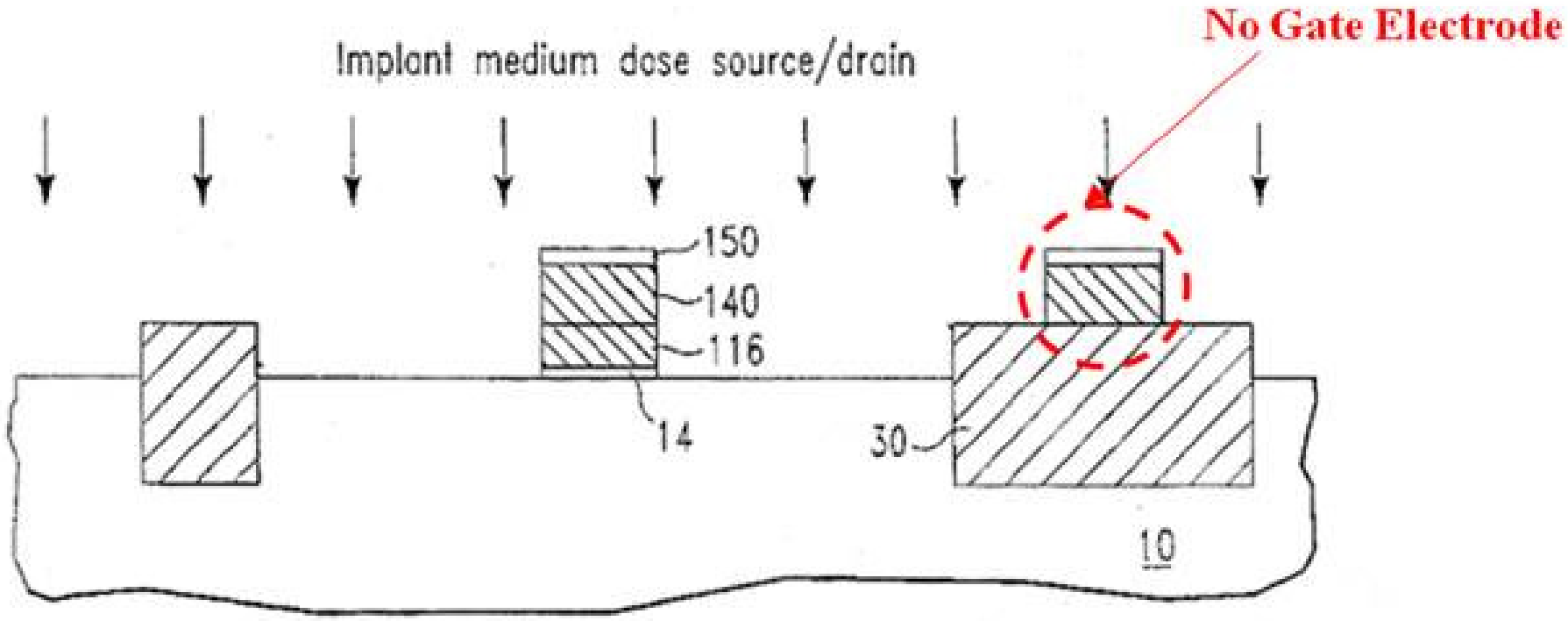


FIG. 11 - Noble (Annotated)

Patent Owner's Response, Paper 14, p. 56
Exhibit 1015, Noble, Fig. 11

Noble

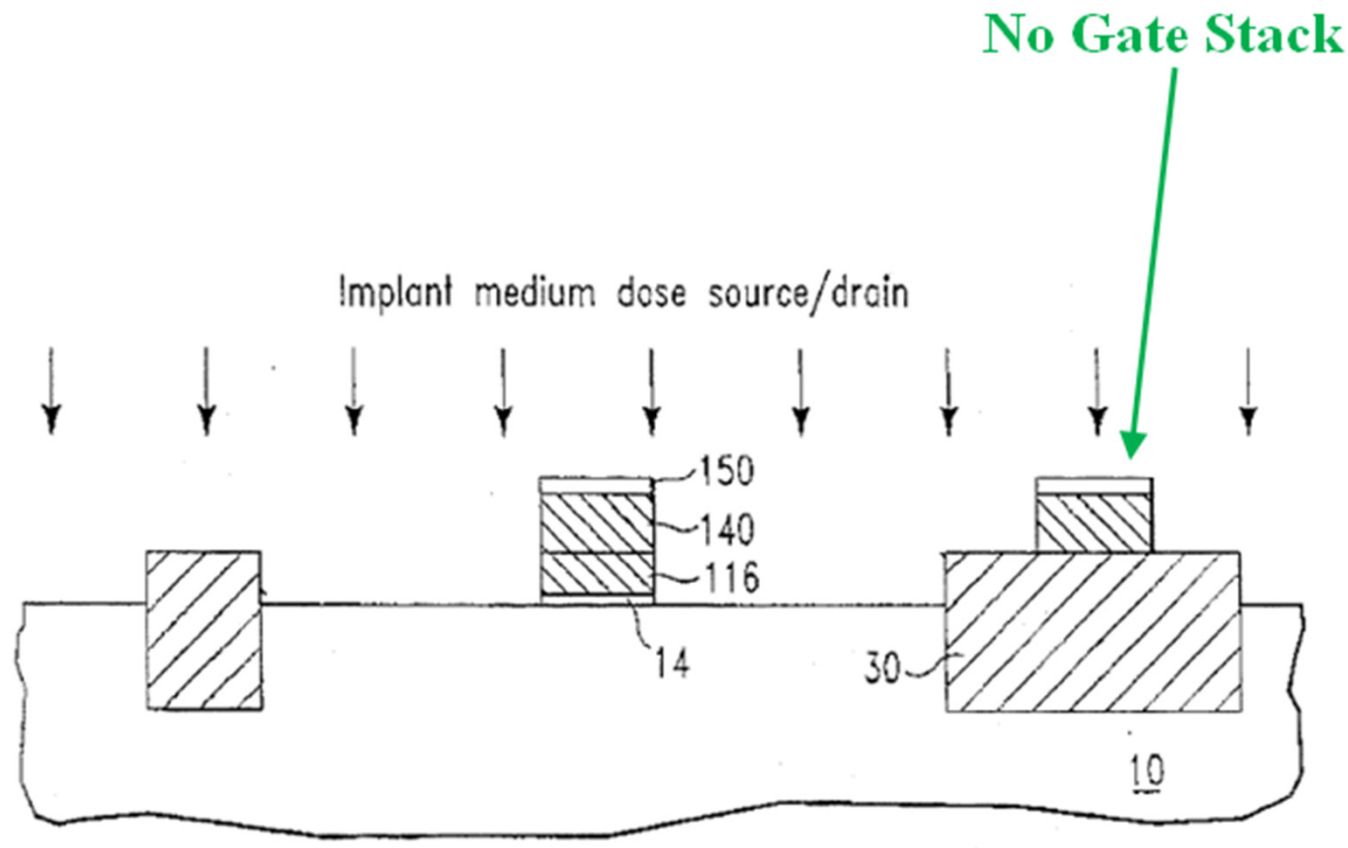


FIG. 11

Patent Owner's Response, Paper 14, p. 47
Exhibit 1015, Noble, Fig. 11

Noble

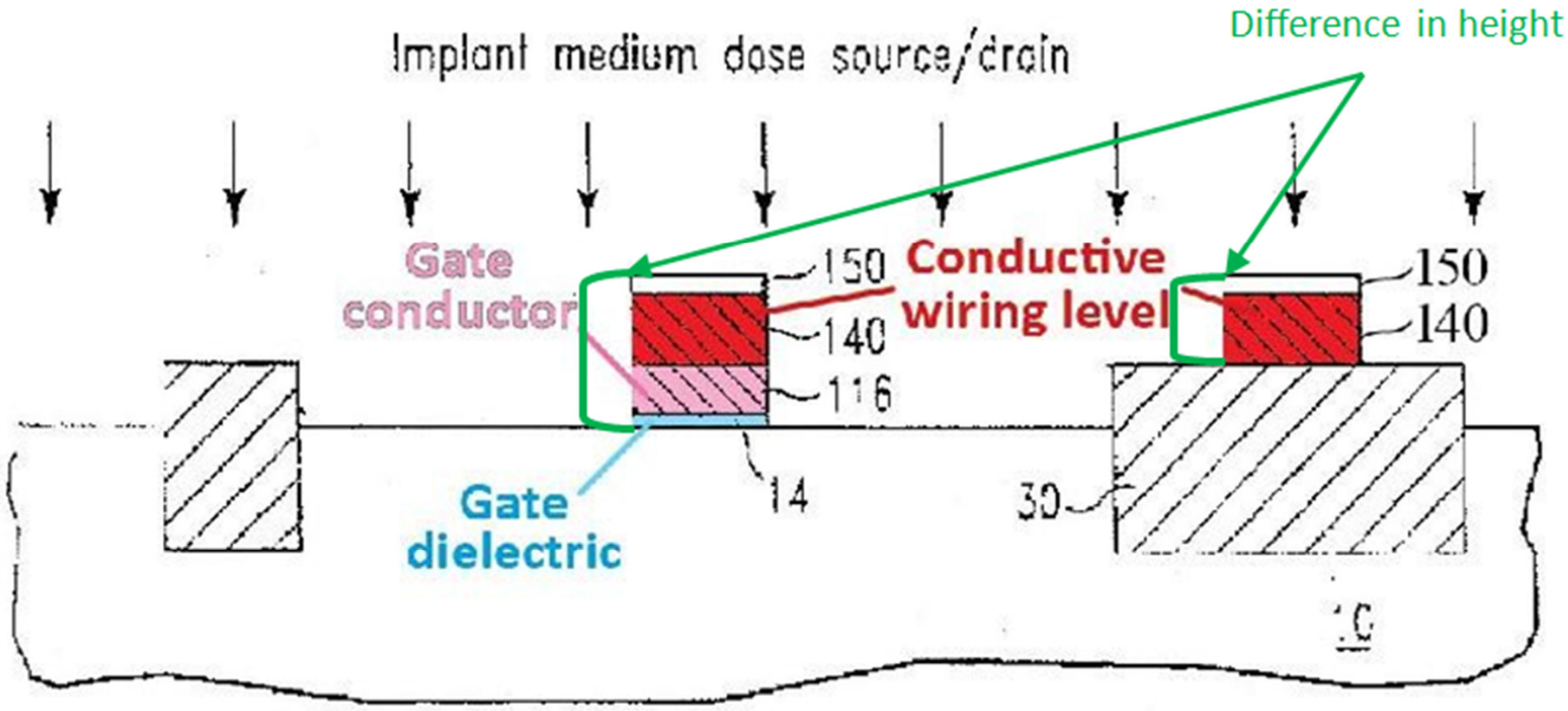


FIG. 11

Patent Owner's Response, Paper 14, pp. 37, 65
Exhibit 1015, Noble, Fig. 11

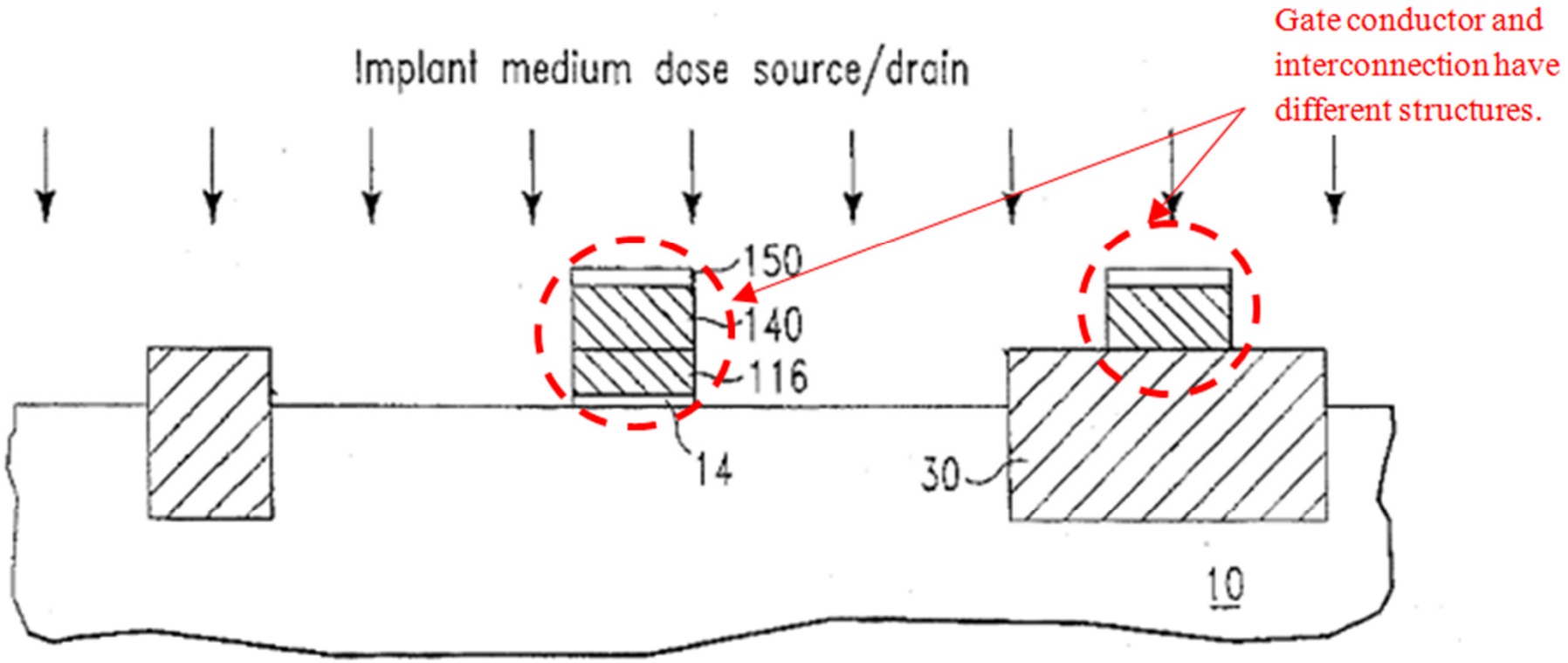


FIG. 11 - Noble (Annotated)

Patent Owner's Response, Paper 14, p. 114
Exhibit 1015, Noble, Fig. 11

Ogawa

Fig.4(a)

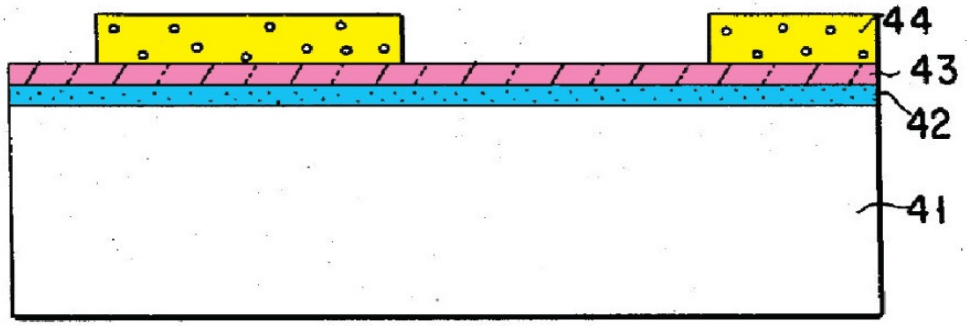
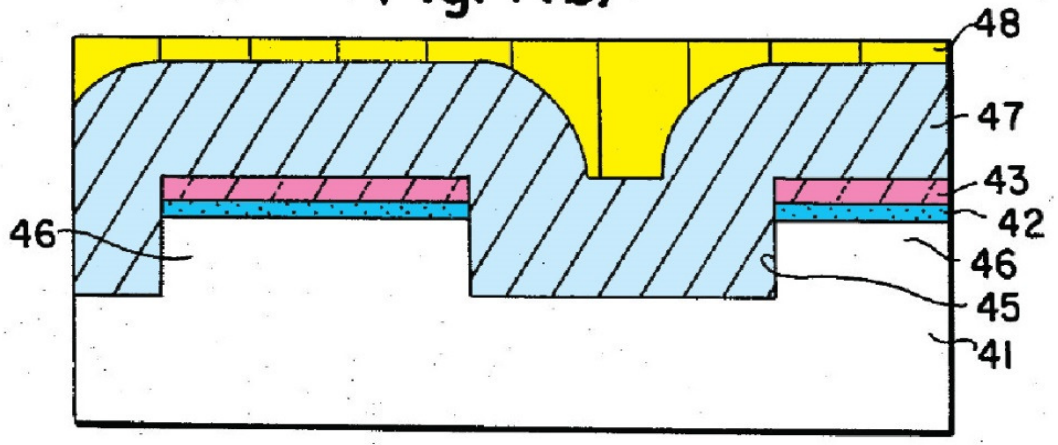


Fig.4(b)



Photoresist
(Organic polymer)

Gate conductor;
Poly-crystalline
silicon (Si)

Gate dielectric;
Silicon dioxide
(SiO_2)

Trench insulation;
Silicon dioxide
(SiO_2)

IPR2016-01246 Patent Owner's Preliminary Response, Paper 7, p. 43
IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 44
Exhibit 1010, Ogawa, Figs. 4(a) and 4(b)

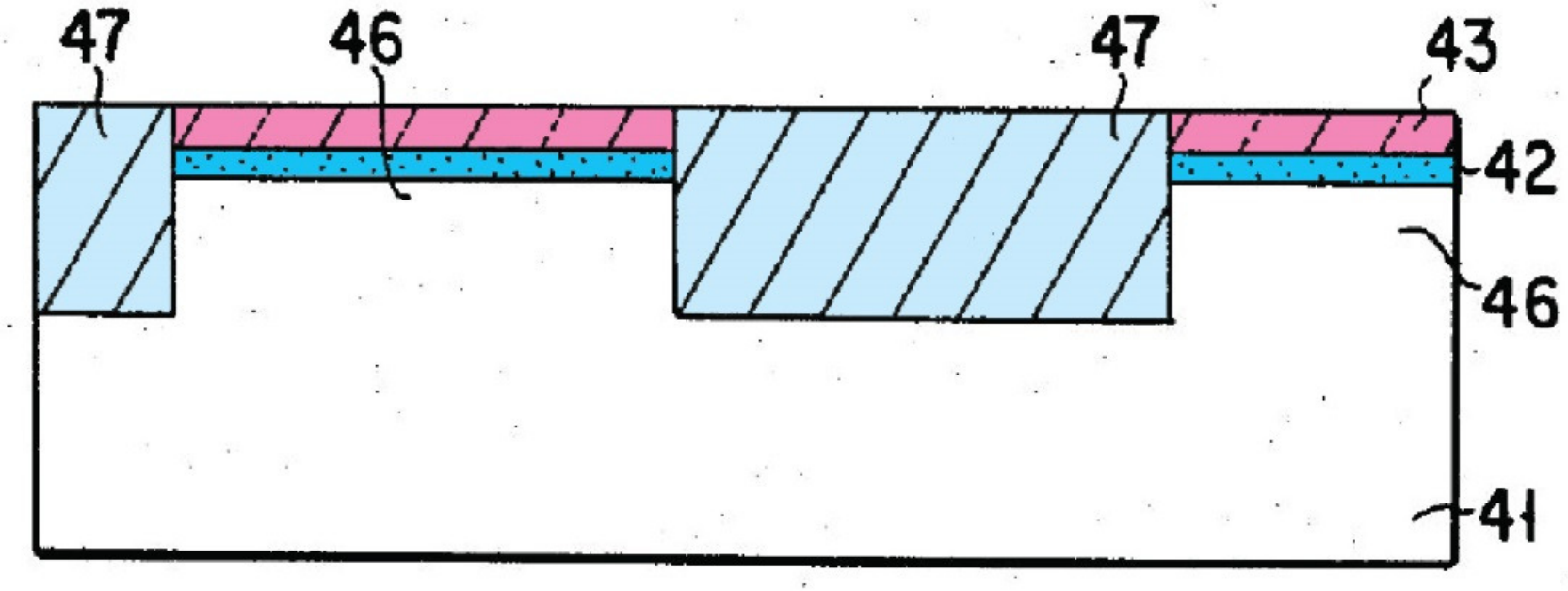
Ogawa

Gate conductor; Poly-crystalline silicon (Si)

Gate dielectric; Silicon dioxide (SiO_2)

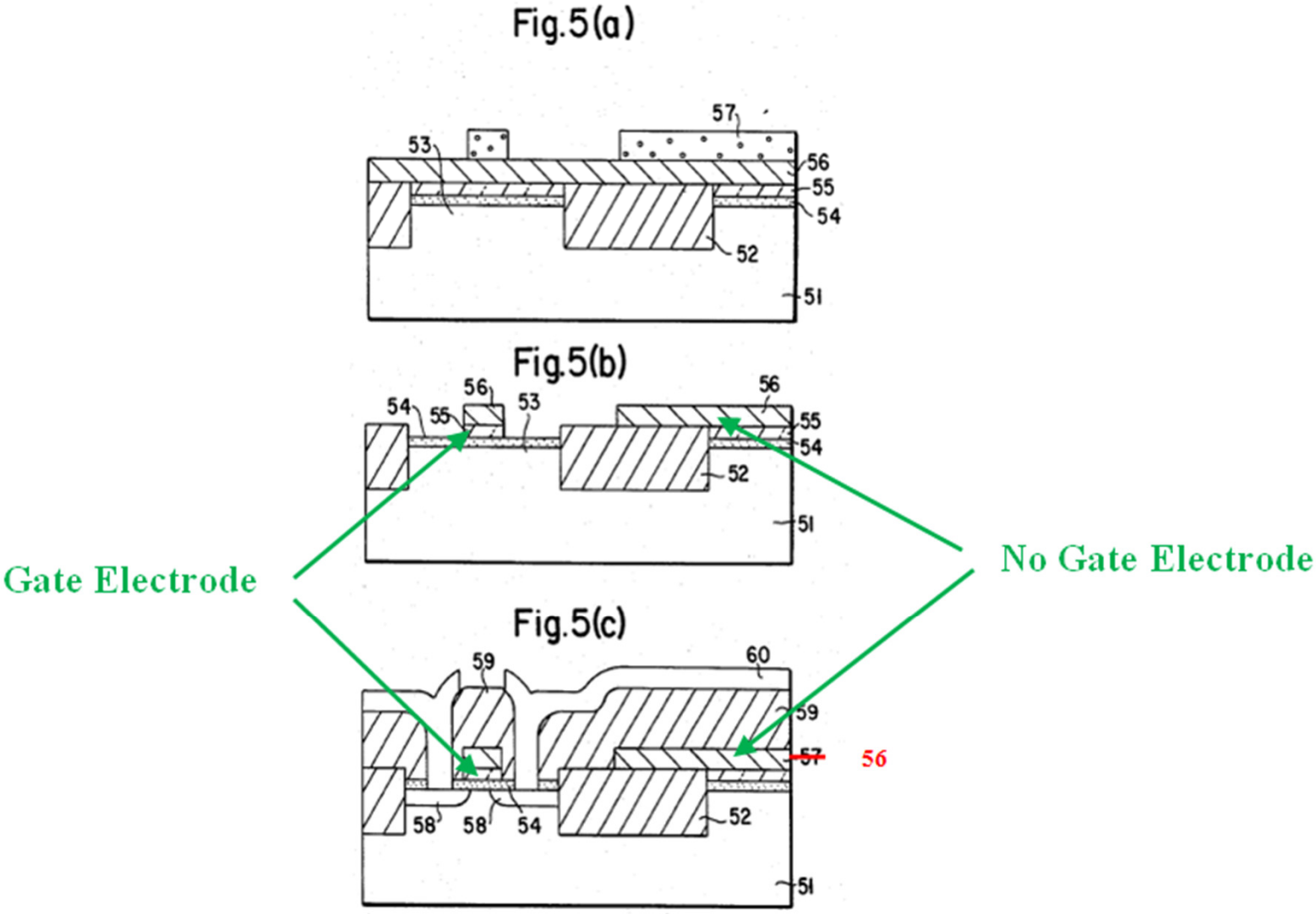
Trench insulation; Silicon dioxide (SiO_2)

Fig. 4(c)



IPR2016-01246 Patent Owner's Preliminary Response, Paper 7, p. 44
IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 45
Exhibit 1010, Ogawa, Fig. 4(c)

Ogawa



Patent Owner's Response, Paper 14, p. 62
Exhibit 1010, Ogawa, Figs. 5(a)-(c)

Ogawa

Fig.5(a)

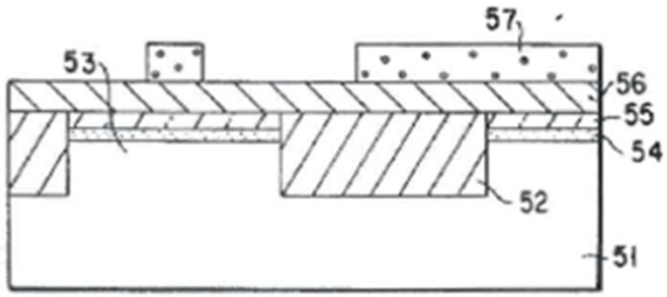


Fig.5(b)

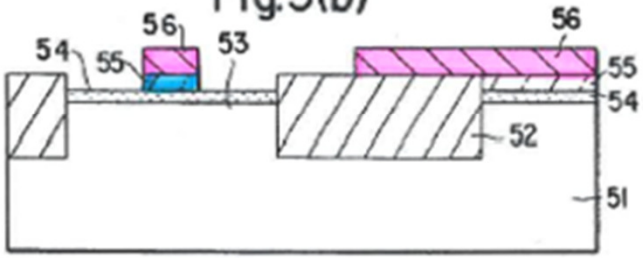
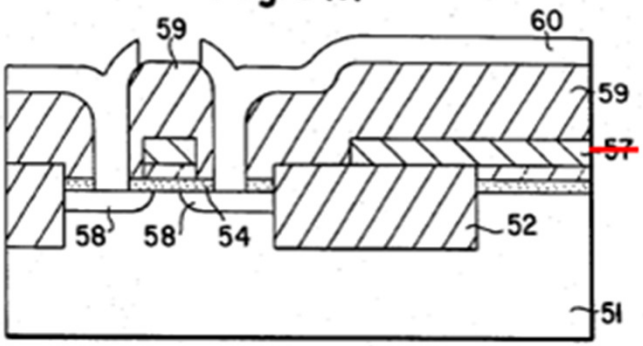
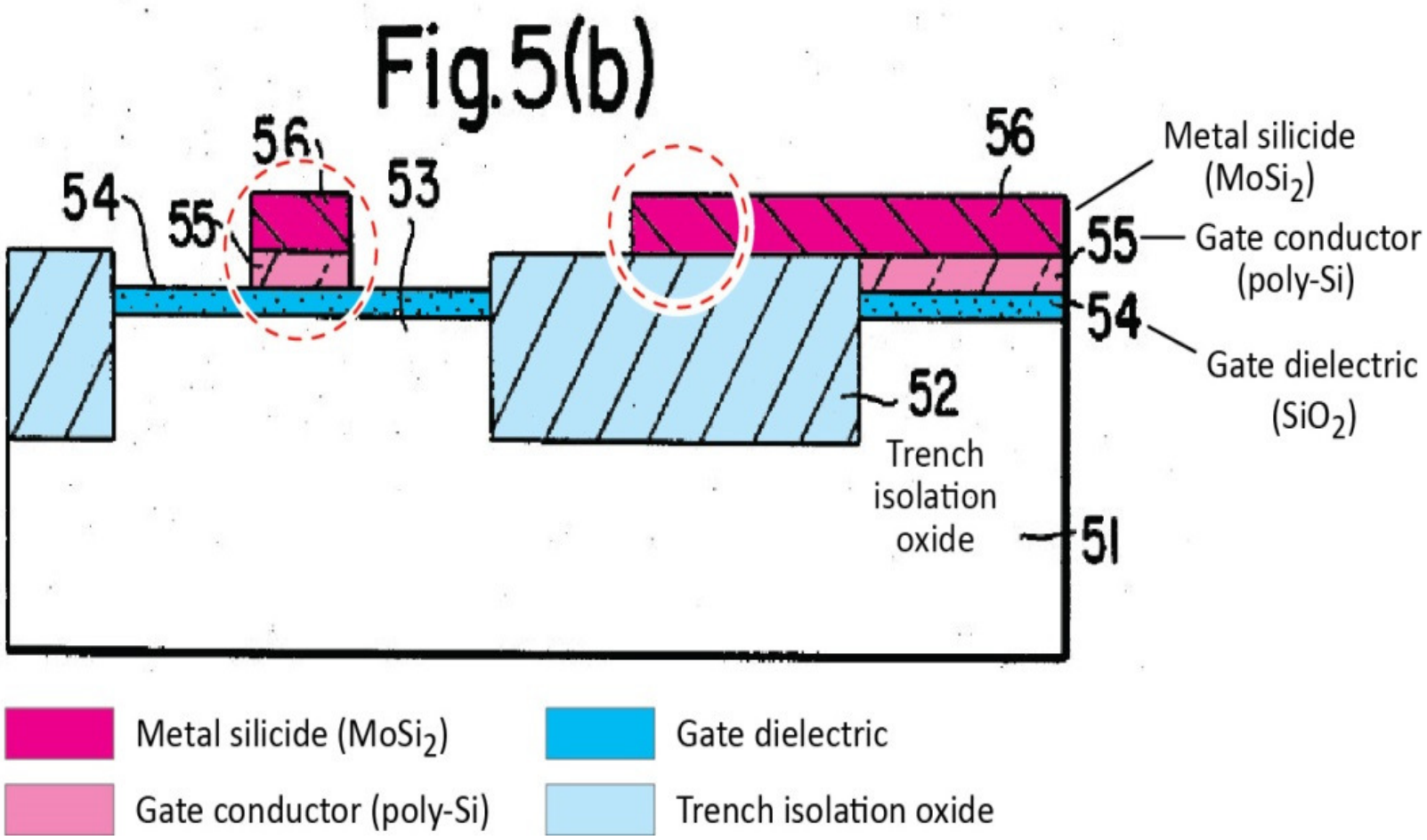


Fig.5(c)



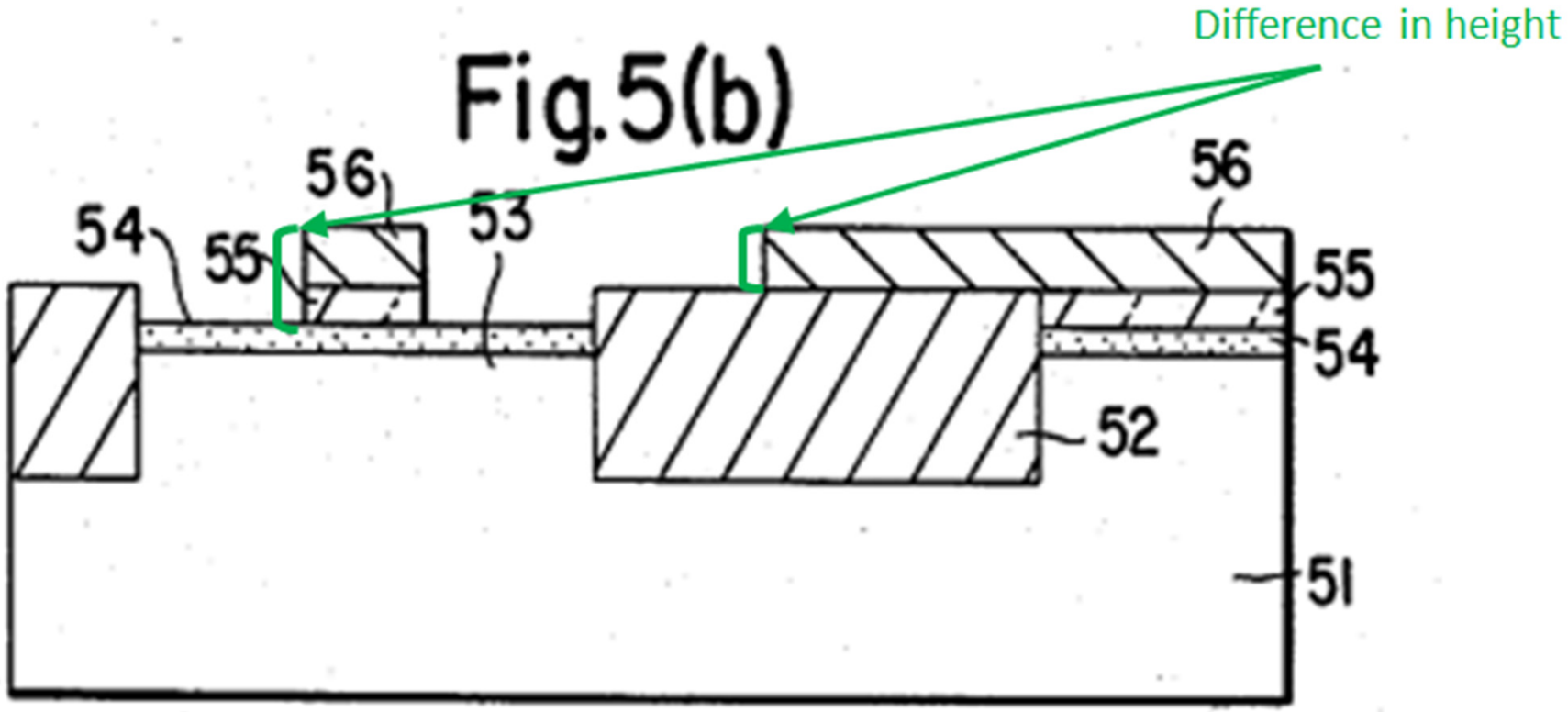
Patent Owner's Response, Paper 14, p. 109
Exhibit 1010, Ogawa, Figs. 5(a)-(c)

Ogawa



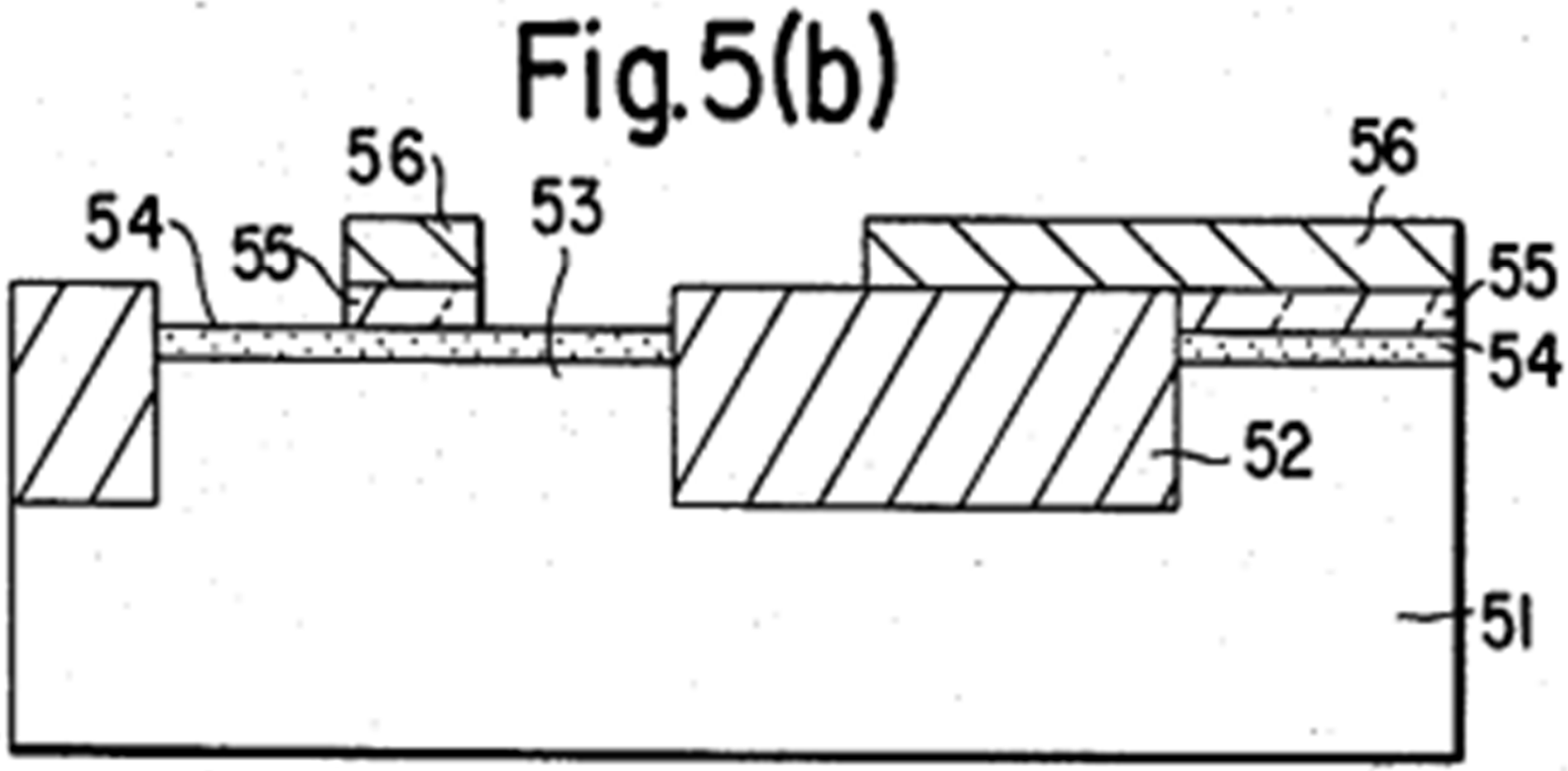
IPR2016-01246 Patent Owner's Preliminary Response, Paper 7, p. 49
Exhibit 1010, Ogawa, Fig. 5(b)

Ogawa



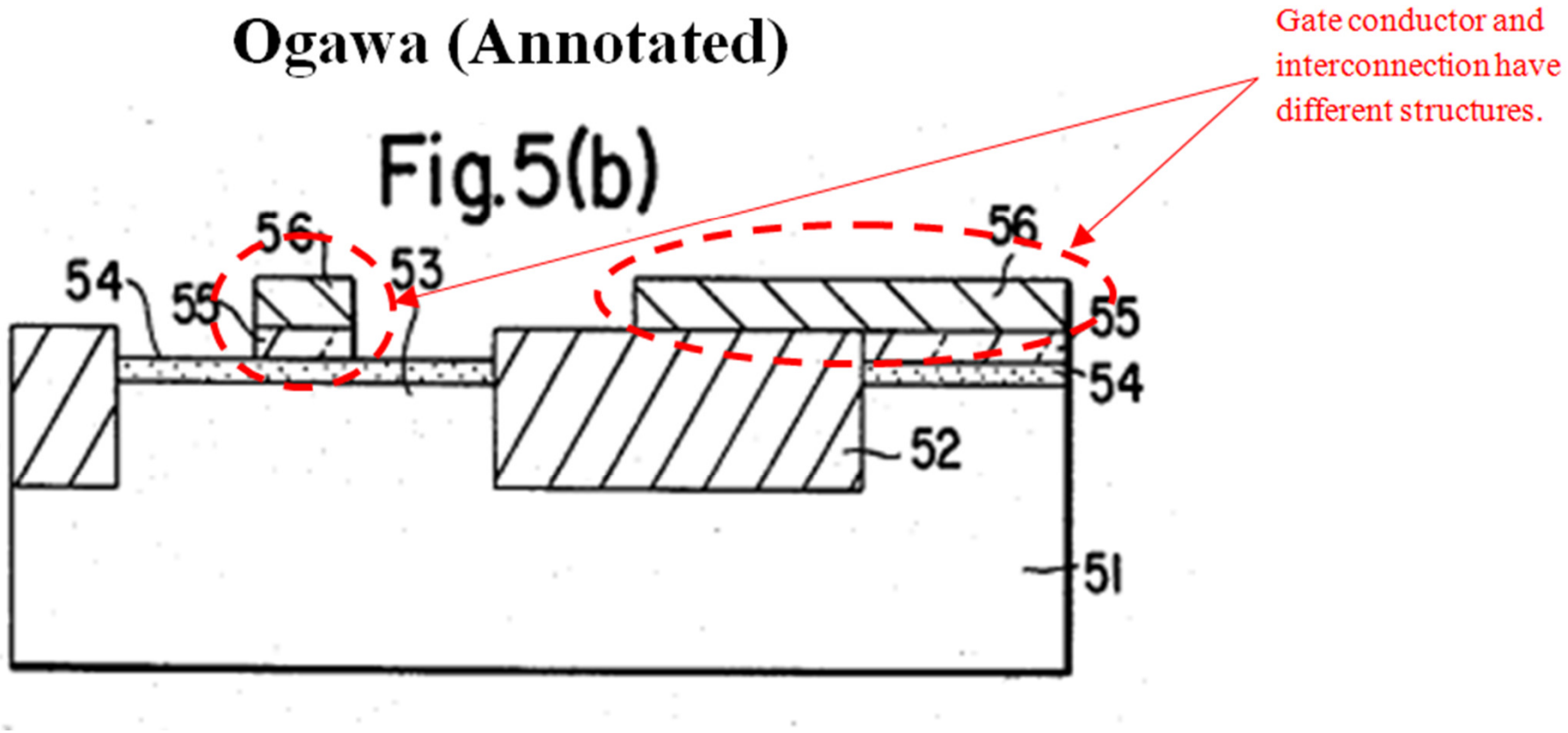
Patent Owner's Response, Paper 14, p. 66
Exhibit 1010, Ogawa, Fig. 5(b)

Ogawa



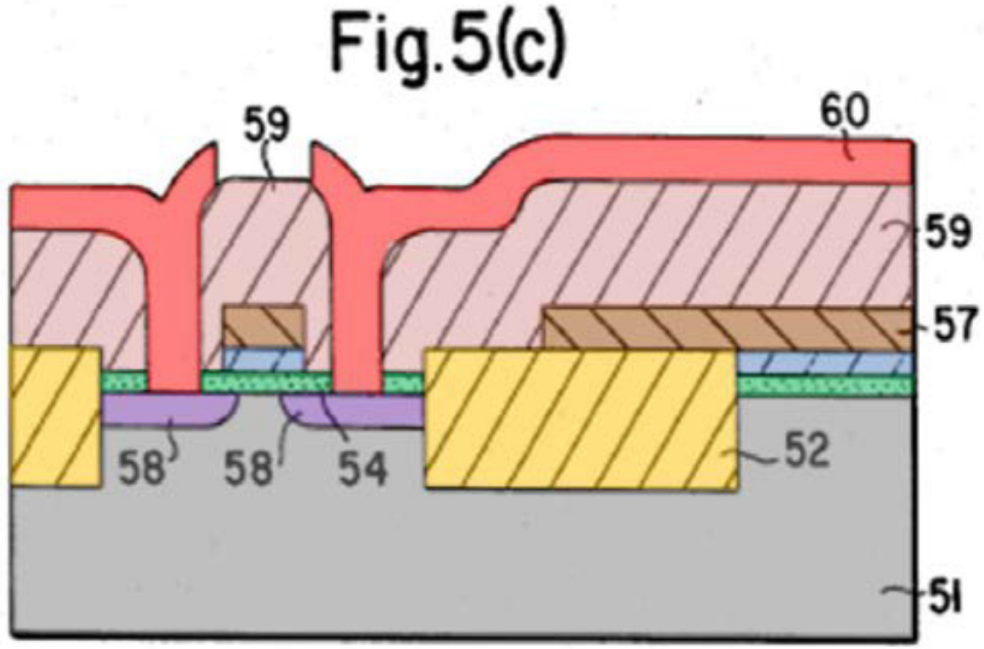
Patent Owner's Response, Paper 14, p. 76
Exhibit 1010, Ogawa, Fig. 5(b)

Ogawa (Annotated)



Patent Owner's Response, Paper 14, p. 113
Exhibit 1010, Ogawa, Fig. 5(b)

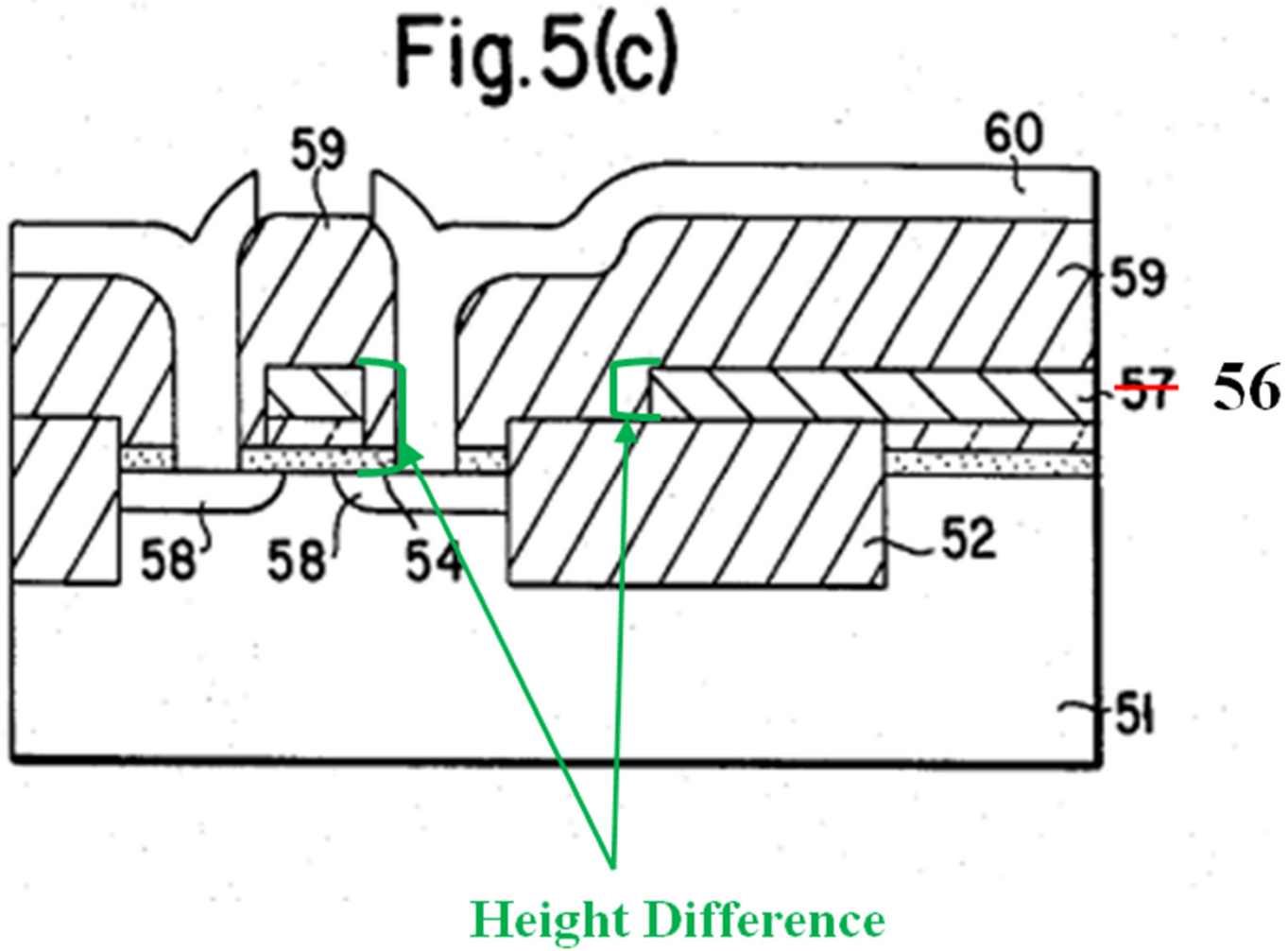
Ogawa



51—Substrate (Si)
54—Gate Oxide (SiO_2)
57[sic]—Gate Electrode/Interconnect (silicide)
59—Interior-Layer Insulating Layer
52—Buried Oxide (SiO_2)
55—Polysilicon Layer
58—Source/Drain
60—Upper Layer Wiring

Patent Owner's Response, Paper 14, pp. 60, 107
Exhibit 1010, Ogawa, Fig. 5(c)

Ogawa



Patent Owner's Response, Paper 14, p. 117
Exhibit 1010, Ogawa, Fig. 5(c)

Lowrey

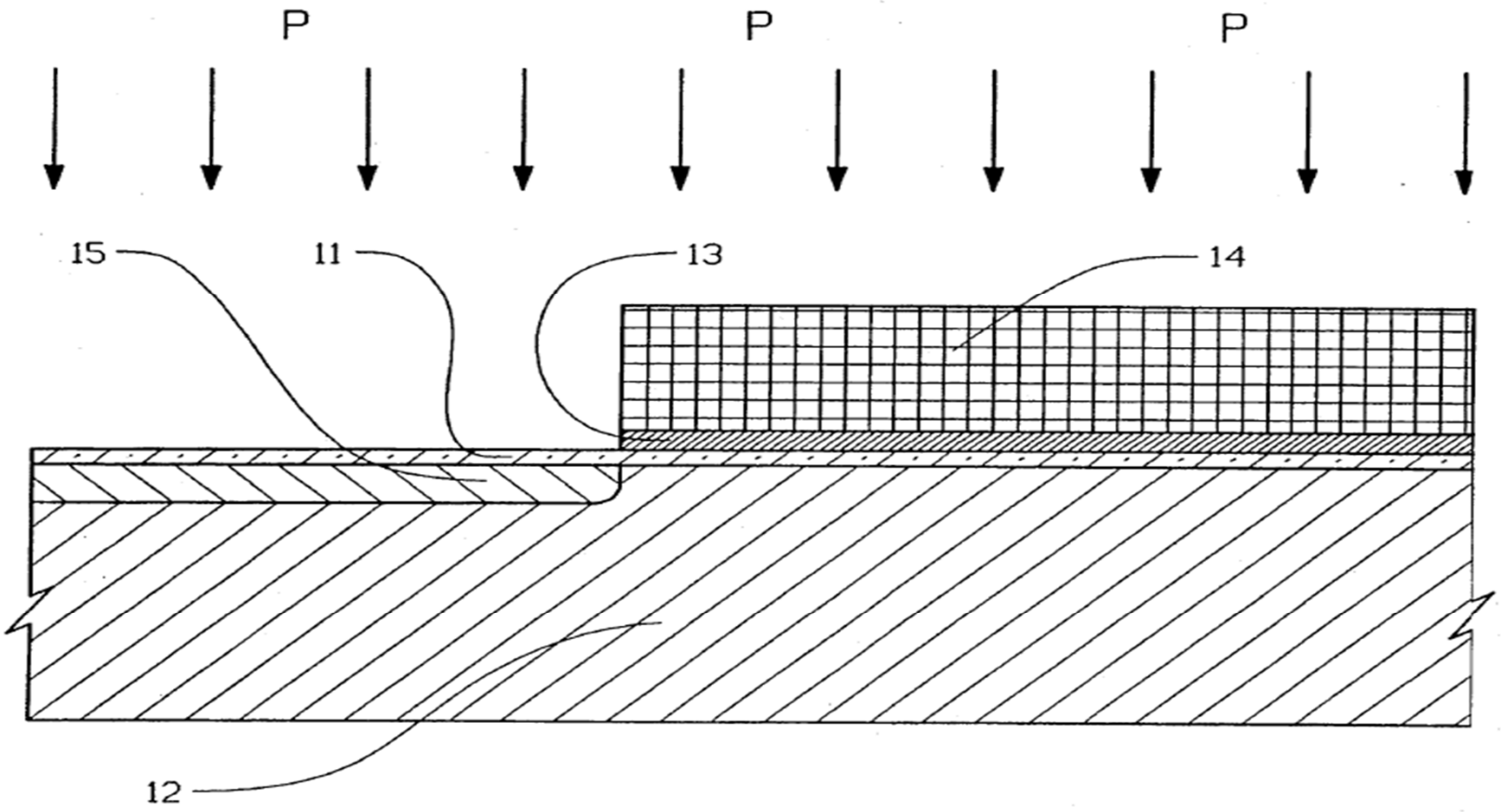


FIG. 1

IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 29
Patent Owner's Sur-Reply, Paper 37, pp. 25, 37
Exhibit 1017, Lowrey, Fig. 1

Lowrey

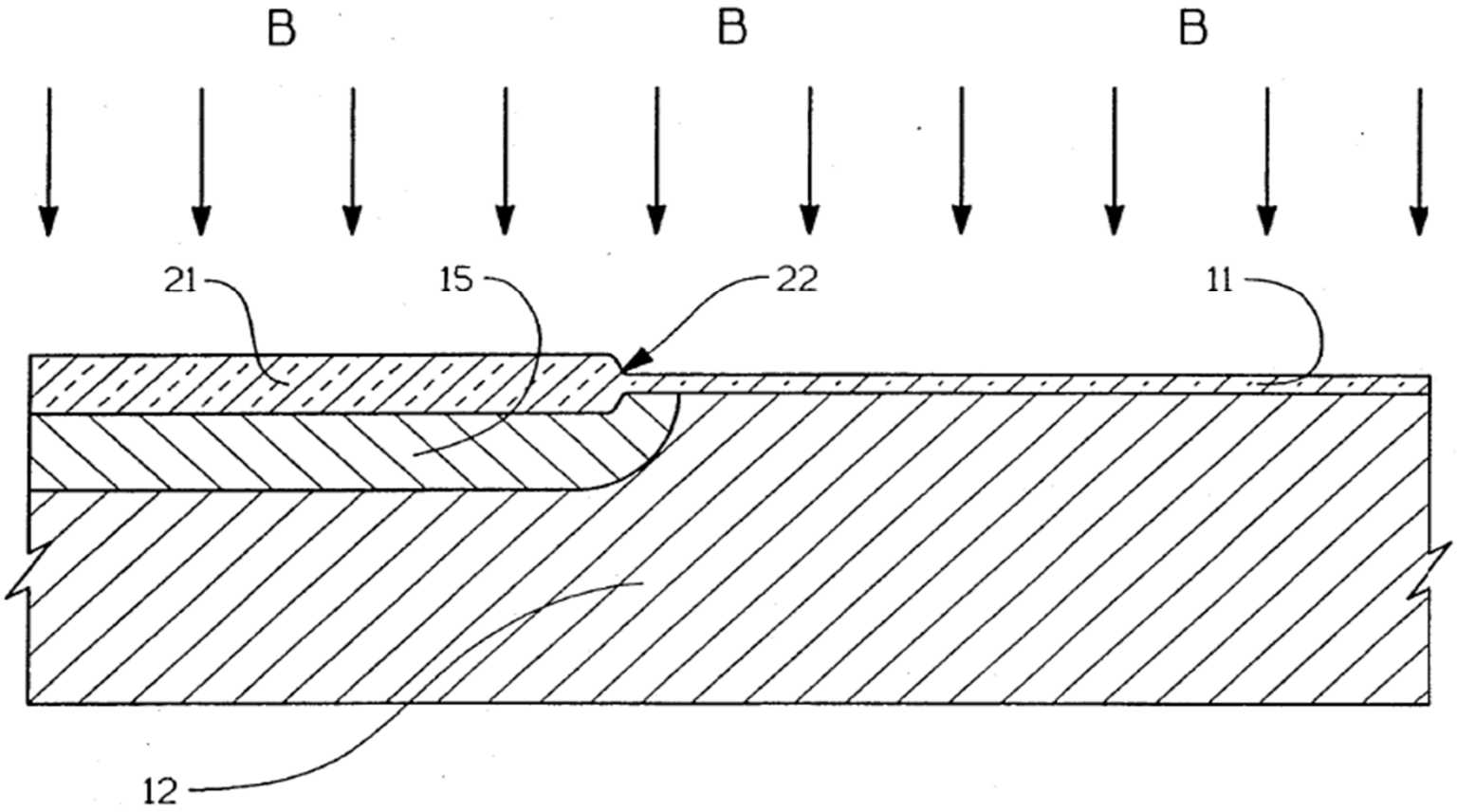


FIG. 2

IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 30
Patent Owner's Sur-Reply, Paper 37, p. 25
Exhibit 1017, Lowrey, Fig. 2

Lowrey

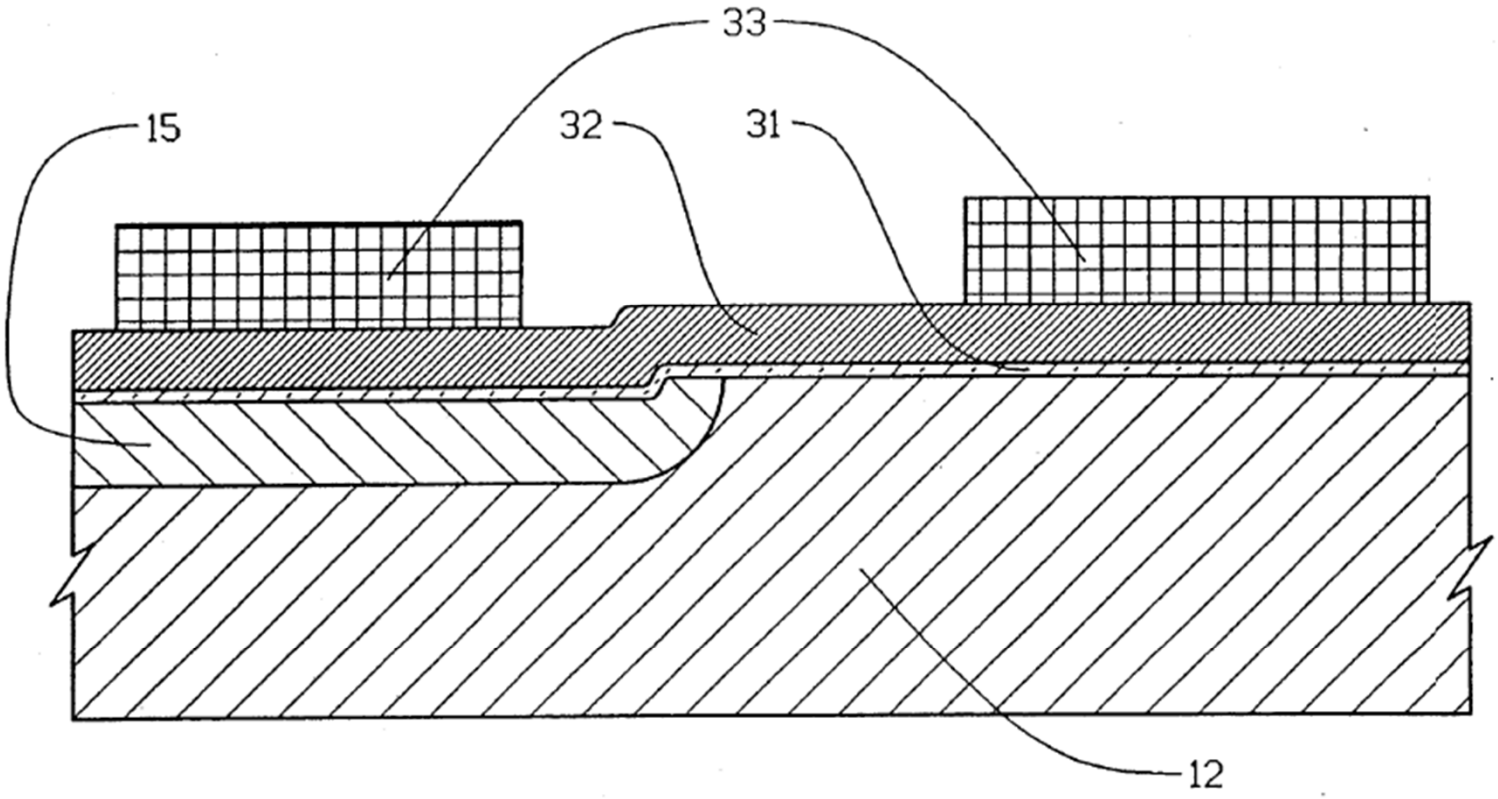


FIG. 3

IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 31
Patent Owner's Sur-Reply, Paper 37, p. 25
Exhibit 1017, Lowrey, Fig. 3

Lowrey

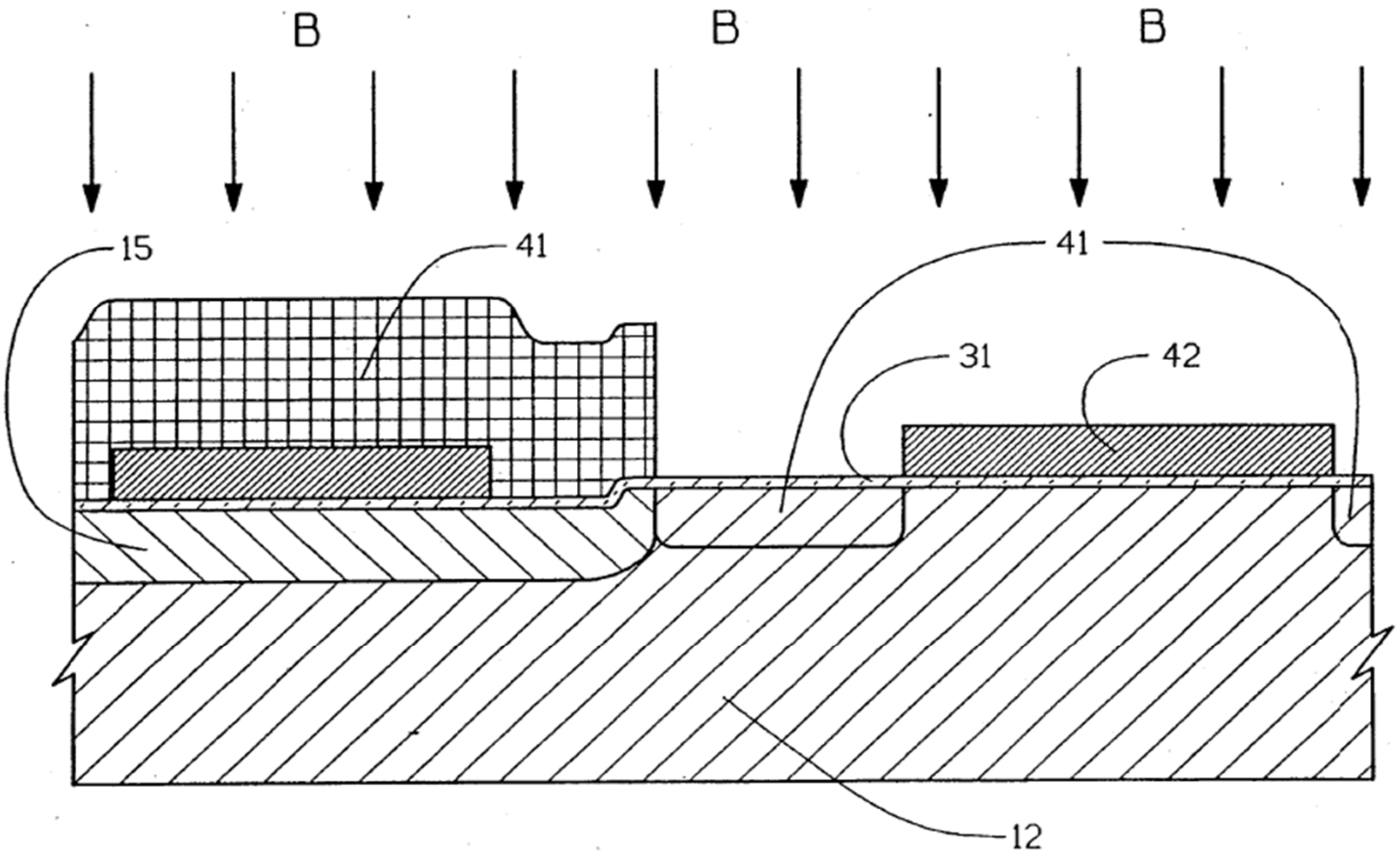


FIG. 4

IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, pp. 32, 35
Patent Owner's Sur-Reply, Paper 37, p. 25
Exhibit 1017, Lowrey, Fig. 4

Lowrey

Non-uniform surface

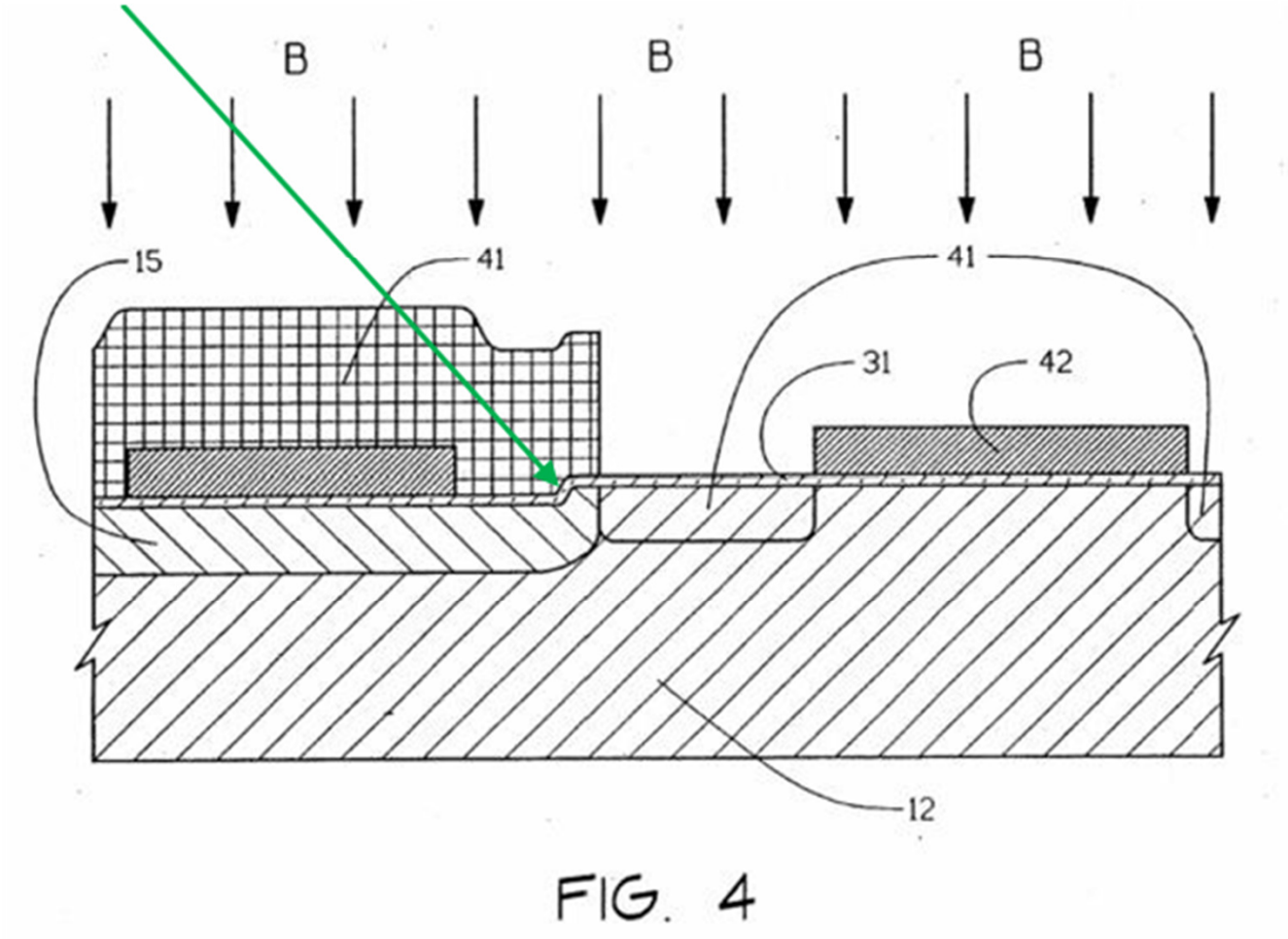


FIG. 4

Patent Owner's Response, Paper 14, p. 96
Exhibit 1017, Lowrey, Fig. 4

Lowrey

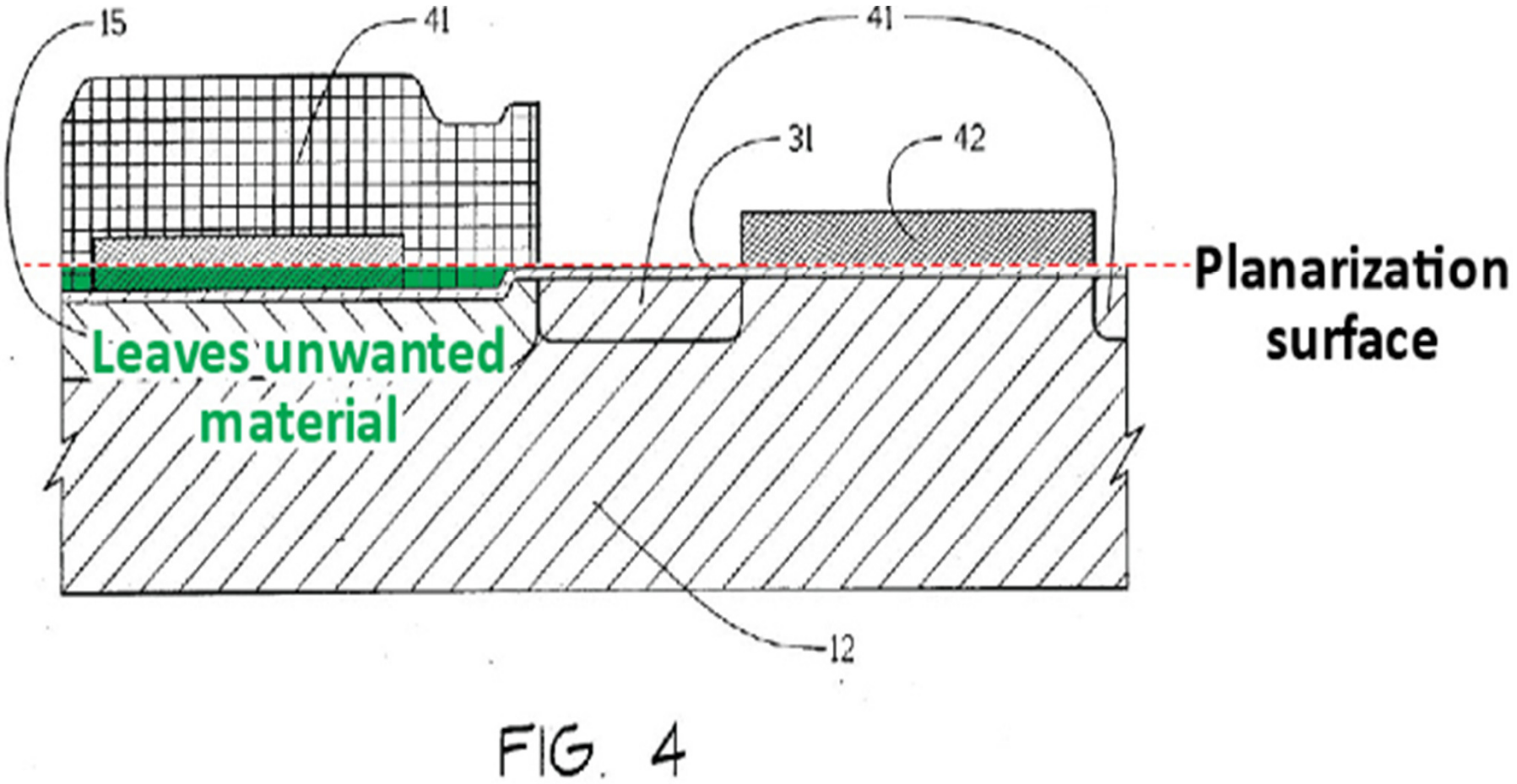


FIG. 4

IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 39
Patent Owner's Response, Paper 14, p. 101
Exhibit 1017, Lowrey, Fig. 4

Lowrey

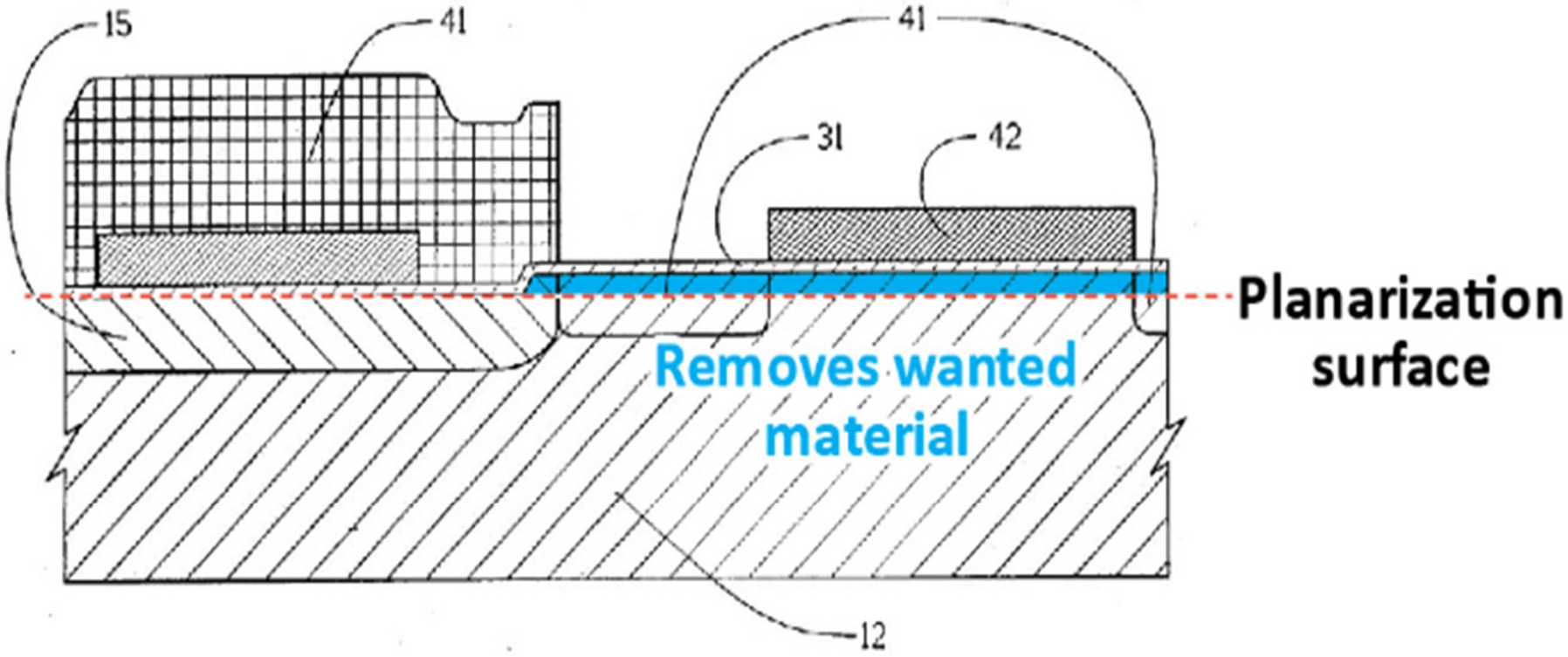


FIG. 4

IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 39
Patent Owner's Response, Paper 14, p. 101
Exhibit 1017, Lowrey, Fig. 4

Lowrey

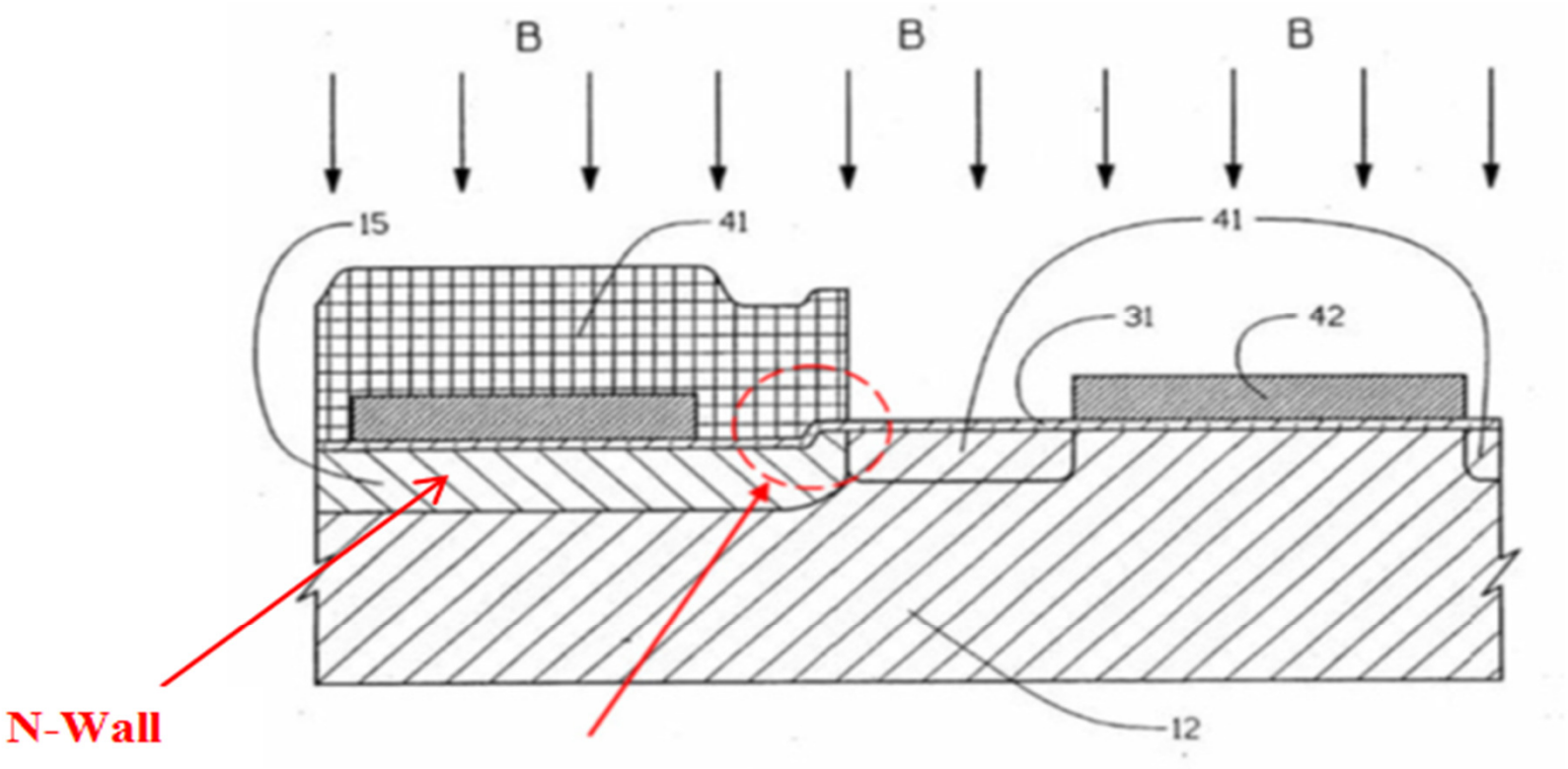


FIG. 4

Patent Owner's Sur-Reply, Paper 37, p. 27
Exhibit 1017, Lowrey, Fig. 4

Lowrey

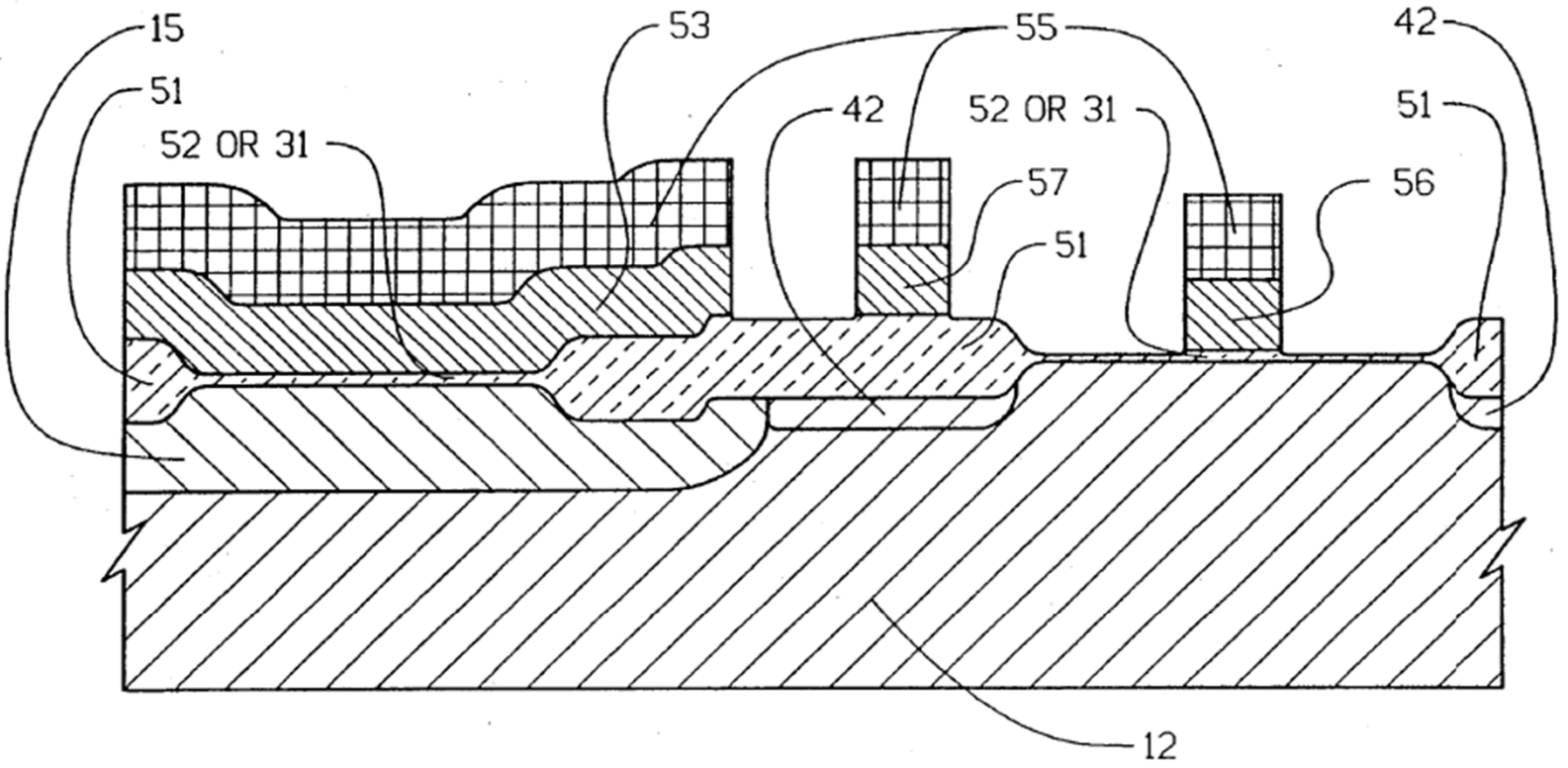


FIG. 5

IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, pp. 33, 36
Patent Owner's Response, Paper 14, pp. 28, 31
Exhibit 1017, Lowrey, Fig. 5

Lowrey

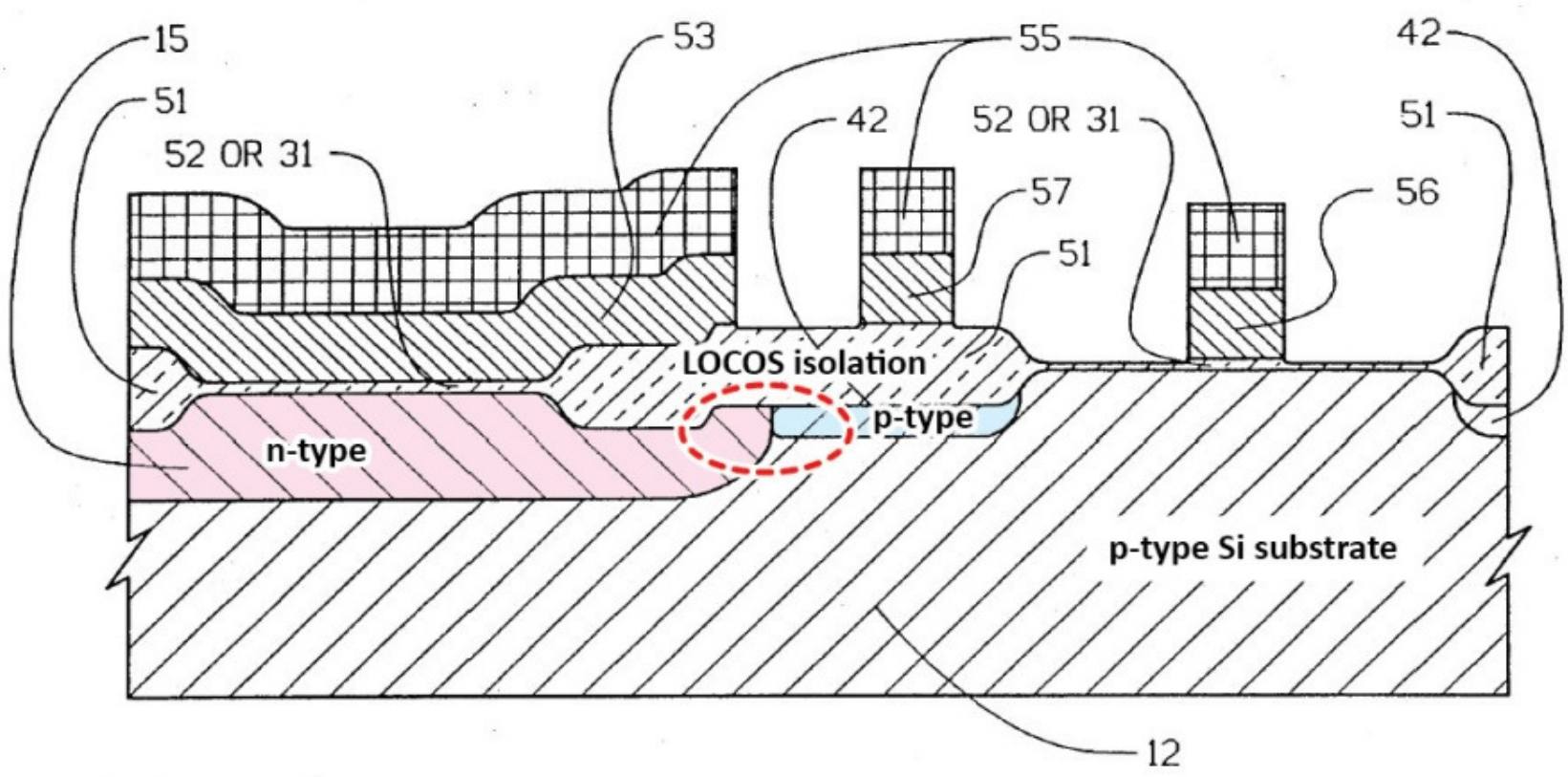


FIG. 5

IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 40
Exhibit 1017, Lowrey, Fig. 5

Lowrey

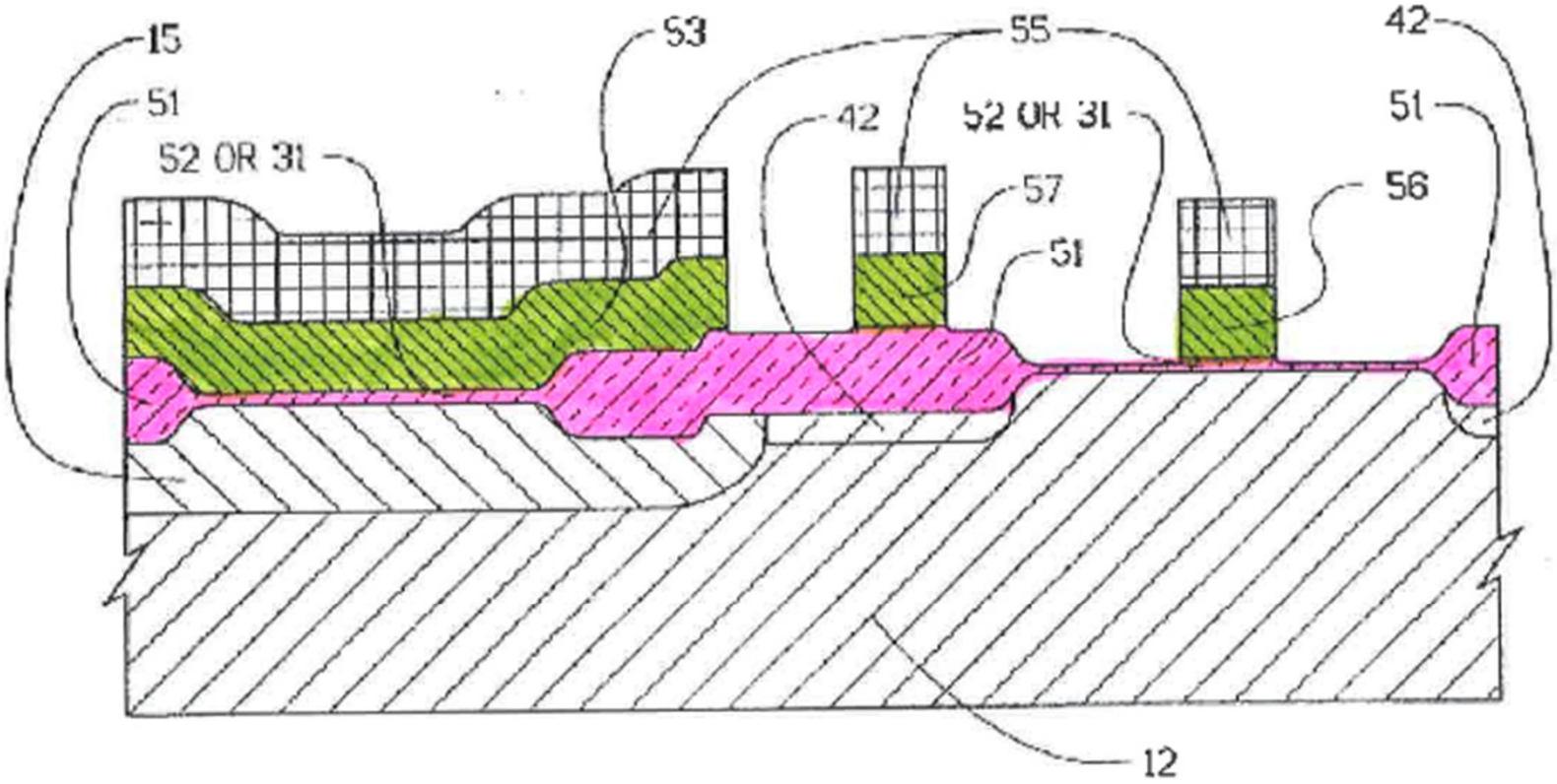


FIG. 5

Patent Owner's Response, Paper 14, p. 97
Exhibit 1017, Lowrey, Fig. 5

Lowrey

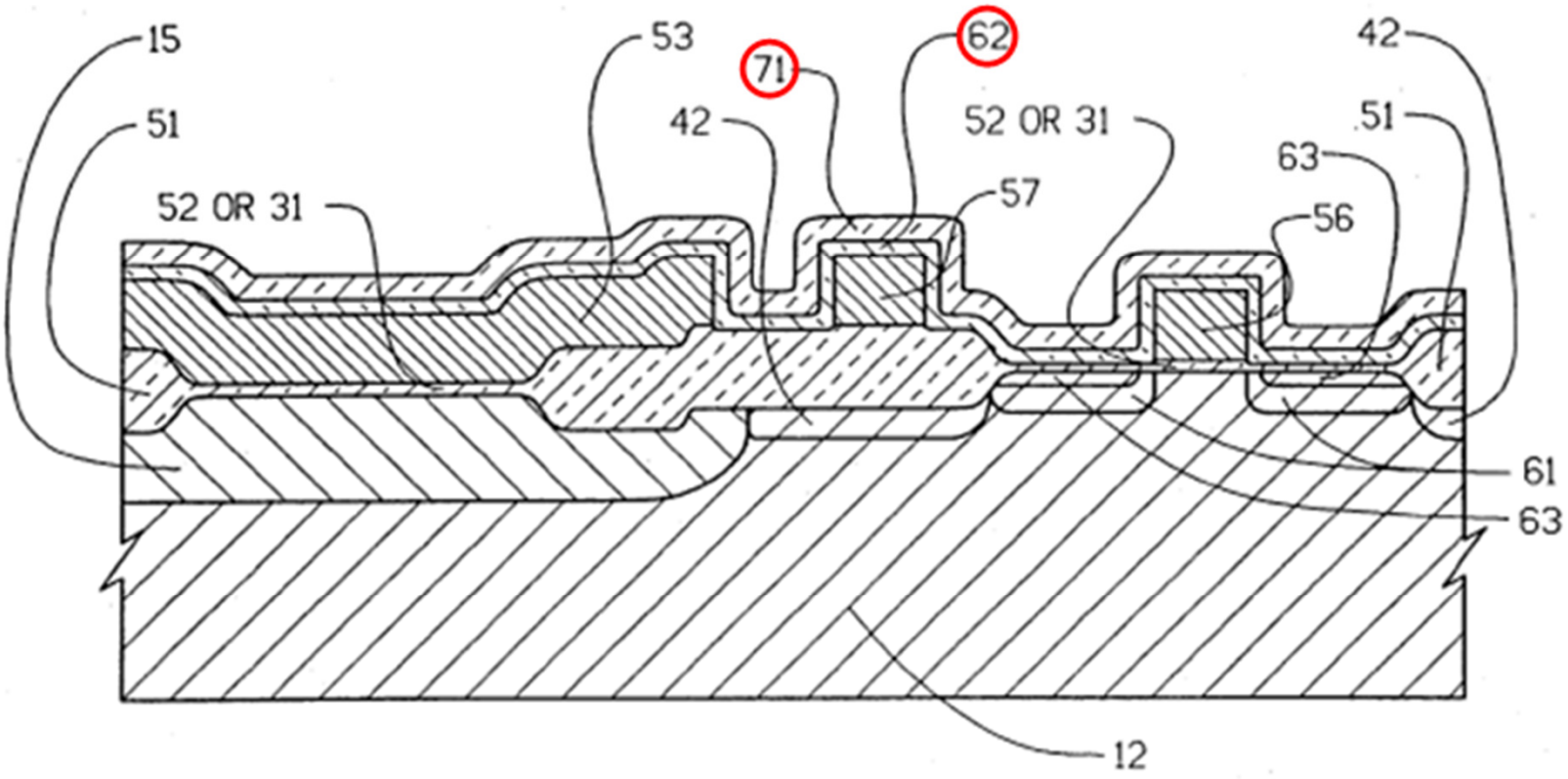


FIG. 7

Patent Owner's Response, Paper 14, p. 98
Exhibit 1017, Lowrey, Fig. 7

Lowrey

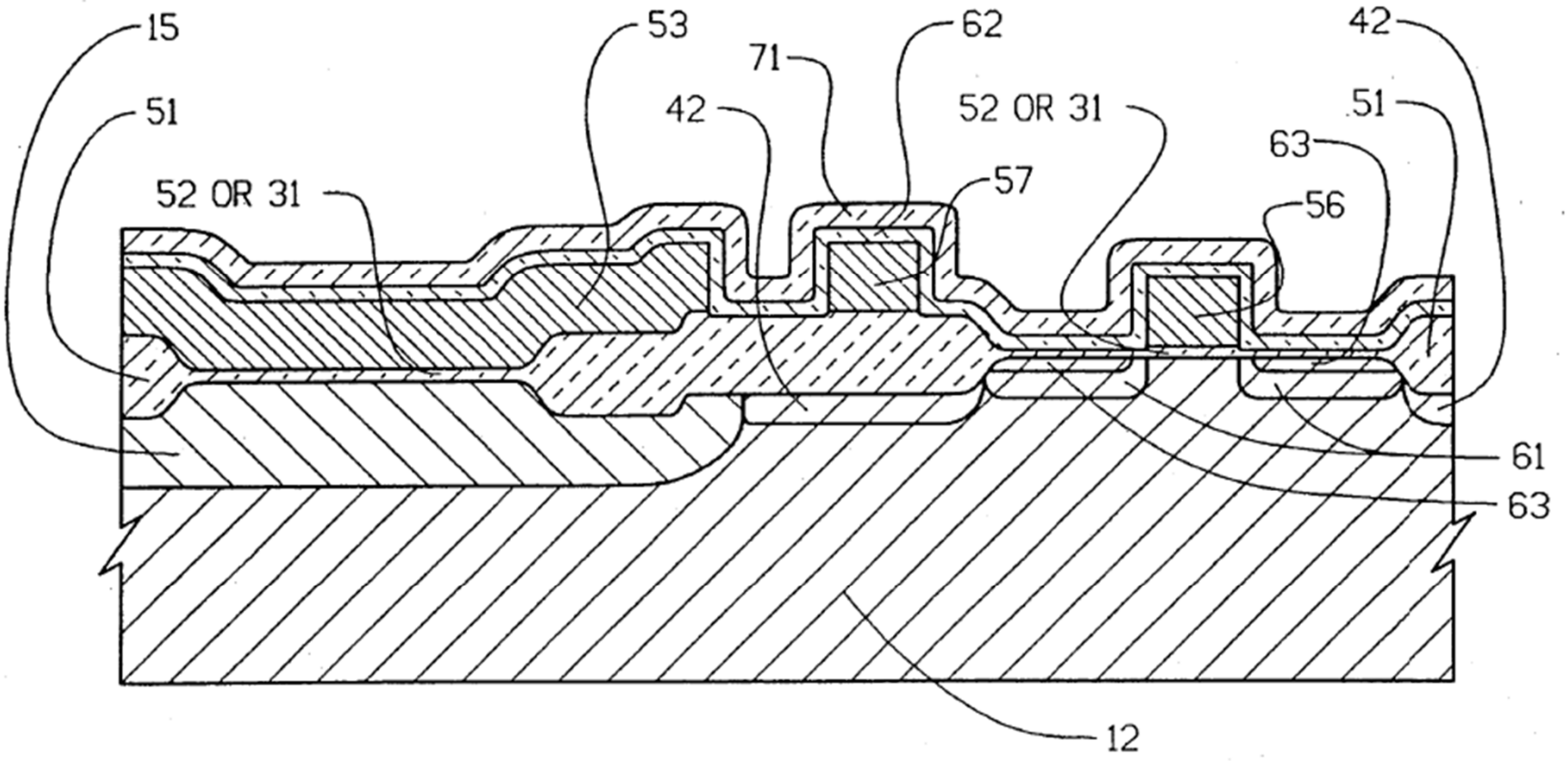


FIG. 7

Patent Owner's Response, Paper 14, p. 29
Exhibit 1017, Lowrey, Fig. 7

Lowrey

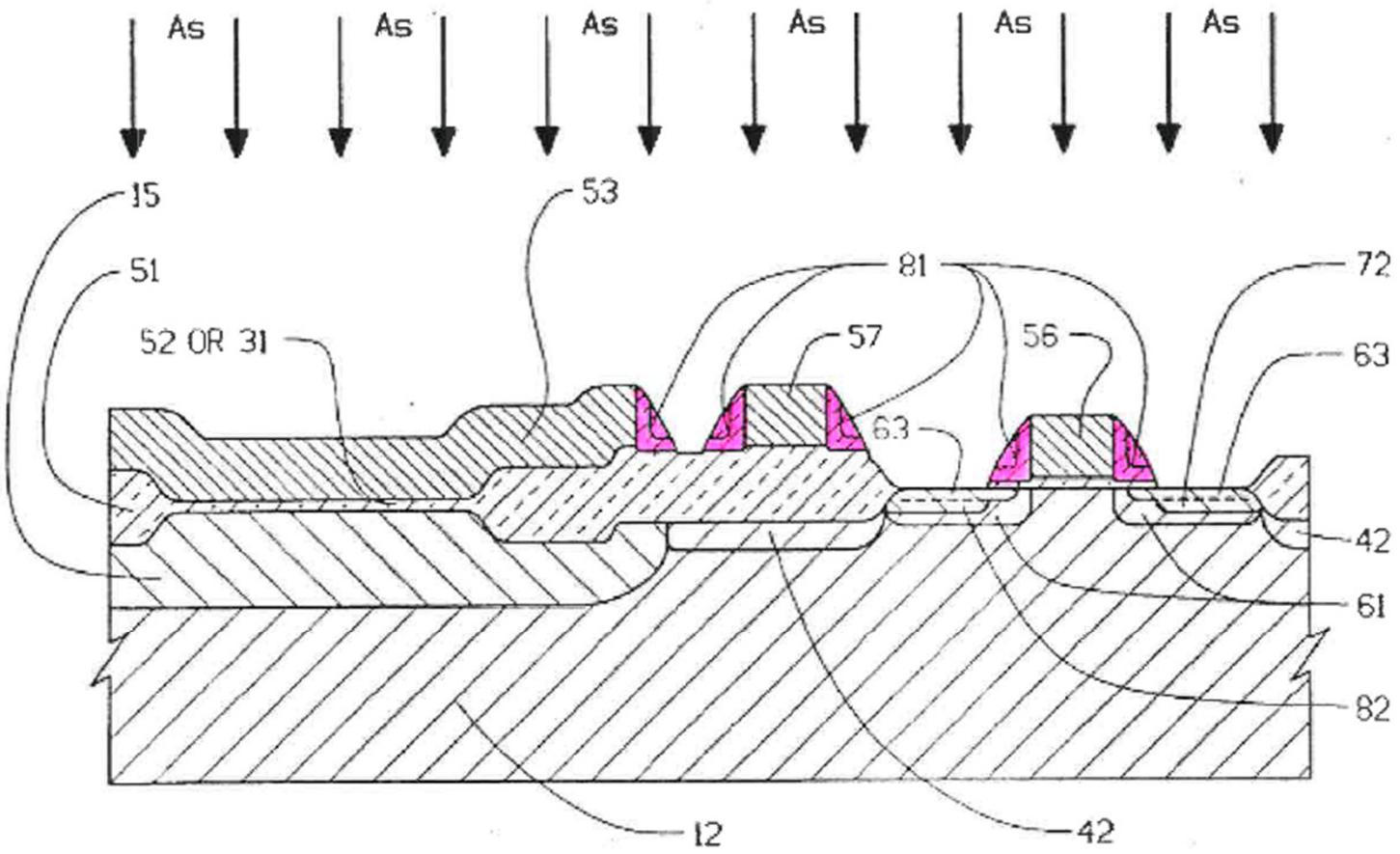


FIG. 8

Patent Owner's Response, Paper 14, p. 30
Exhibit 1017, Lowrey, Fig. 8

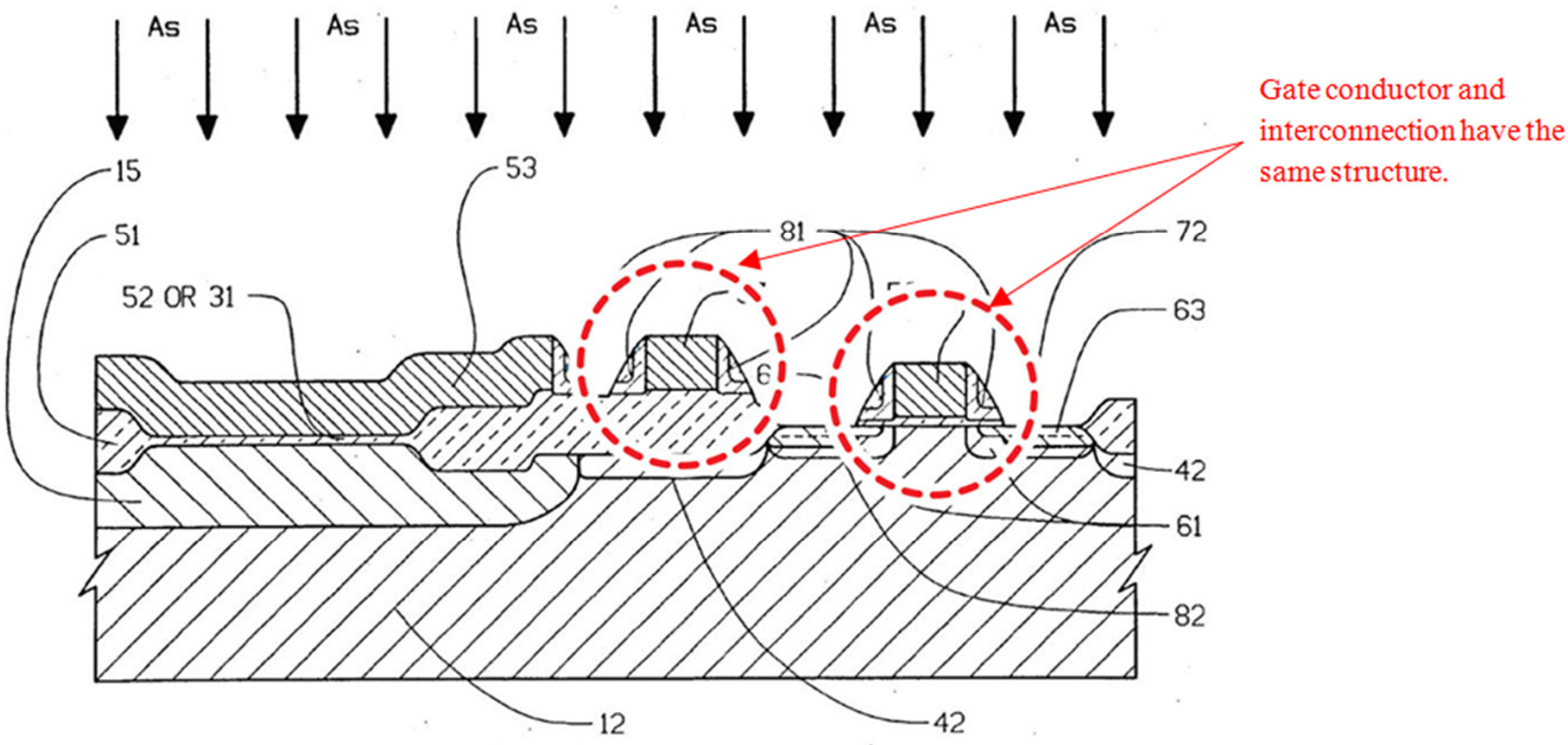


FIG. 8 - **Lowrey (Annotated)**

Patent Owner's Response, Paper 14, p. 113
Exhibit 1017, Lowrey, Fig. 8

Lowrey

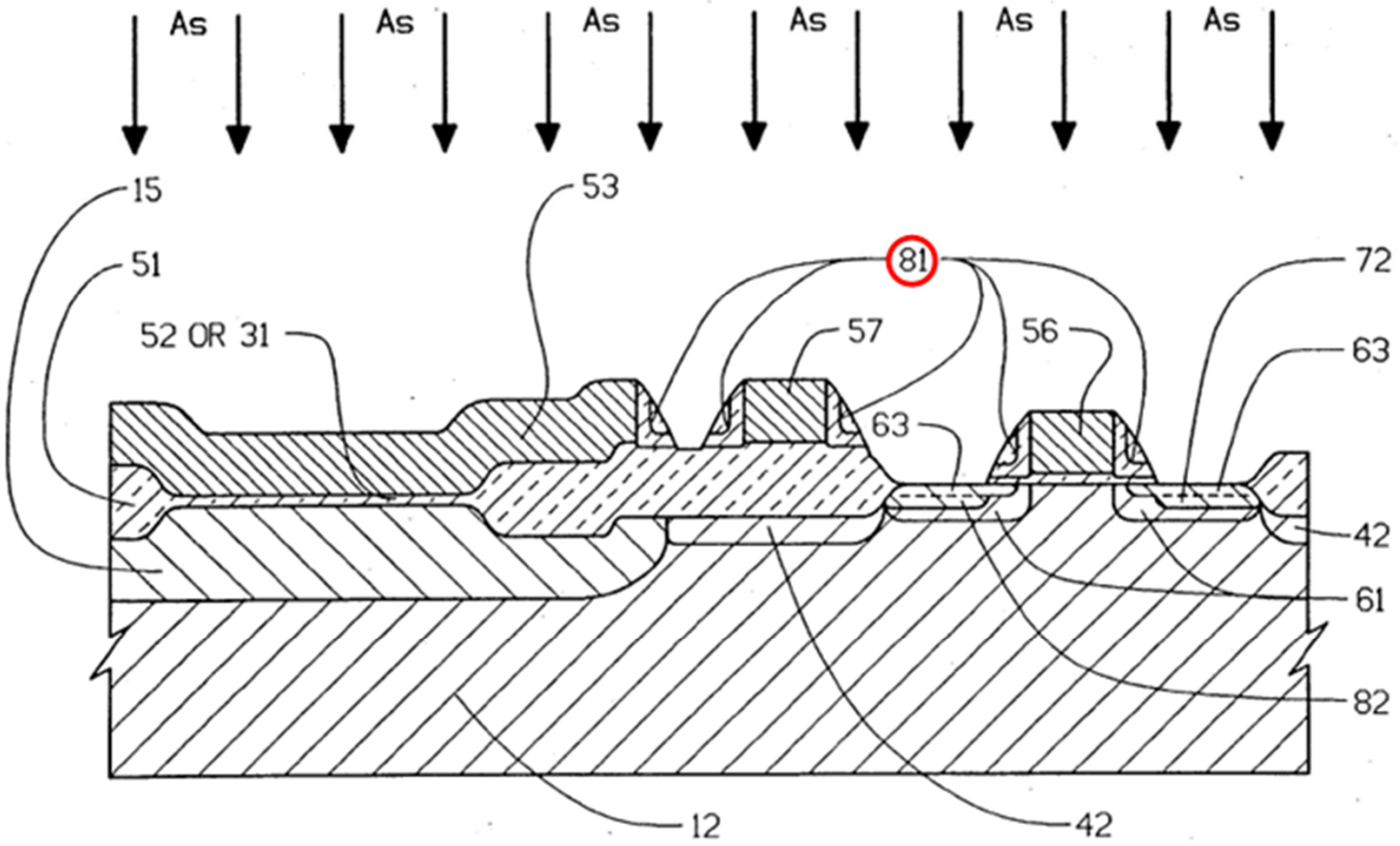
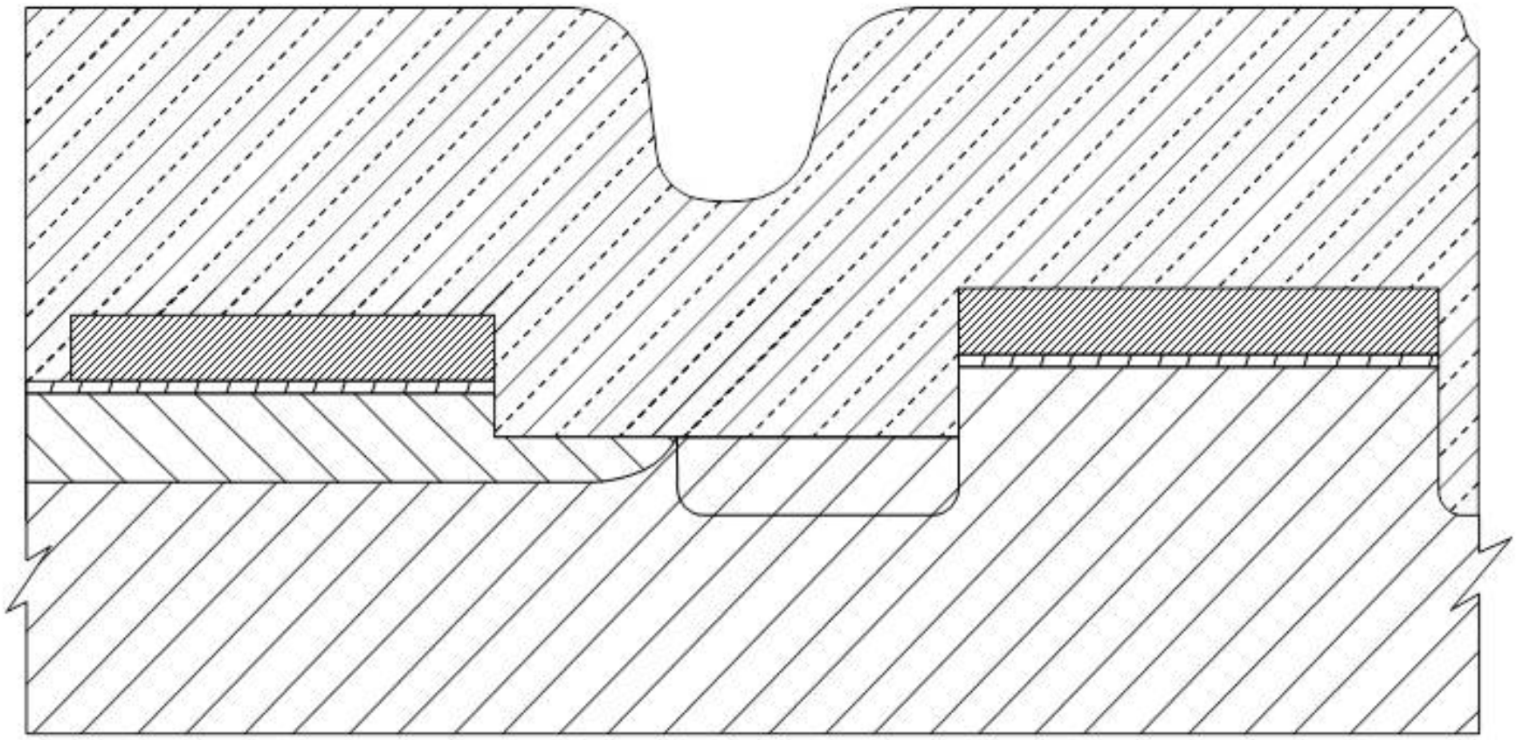
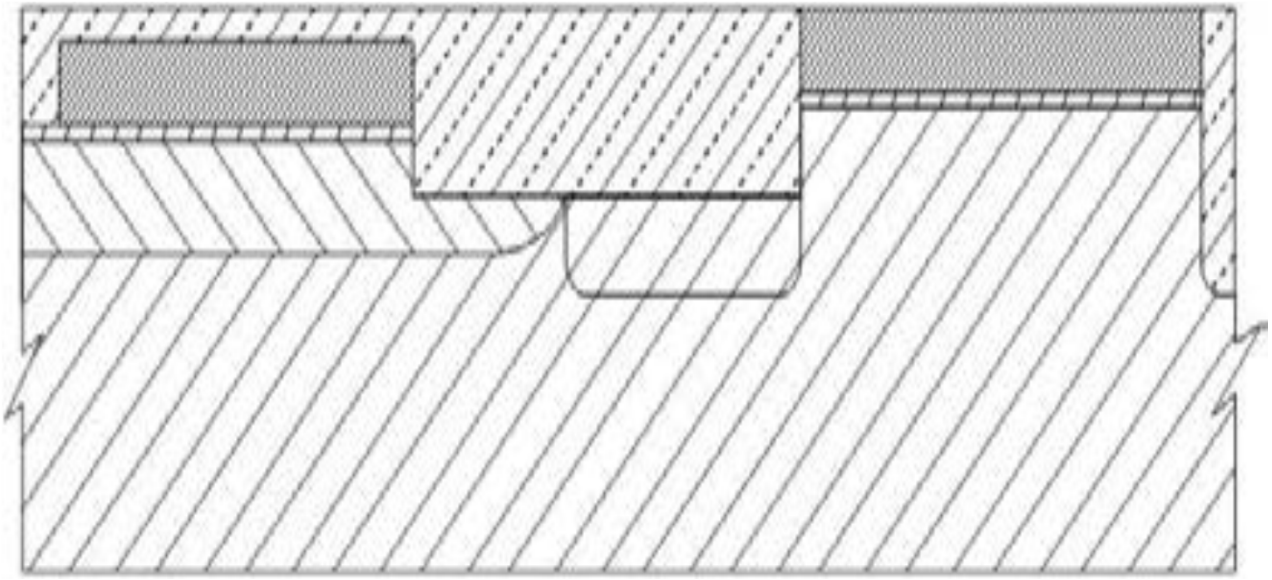


FIG. 8

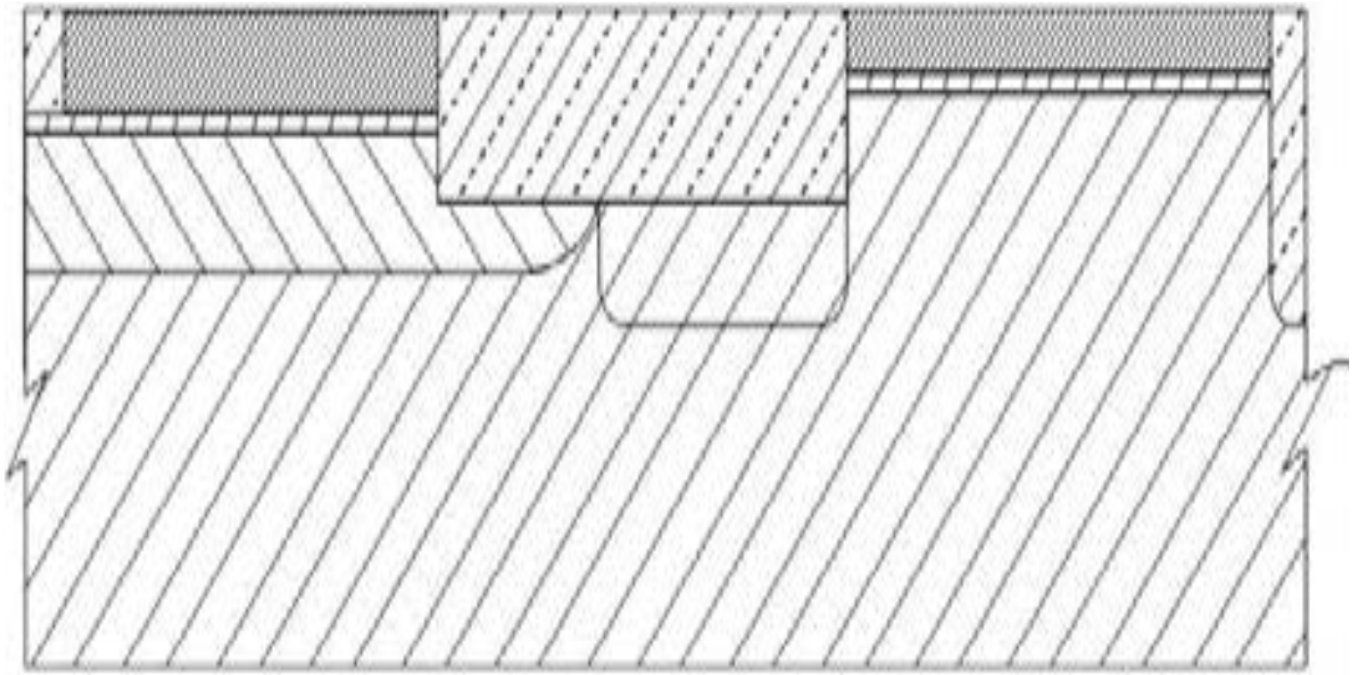
Patent Owner's Response, Paper 14, p. 99
Exhibit 1017, Lowrey, Fig. 8



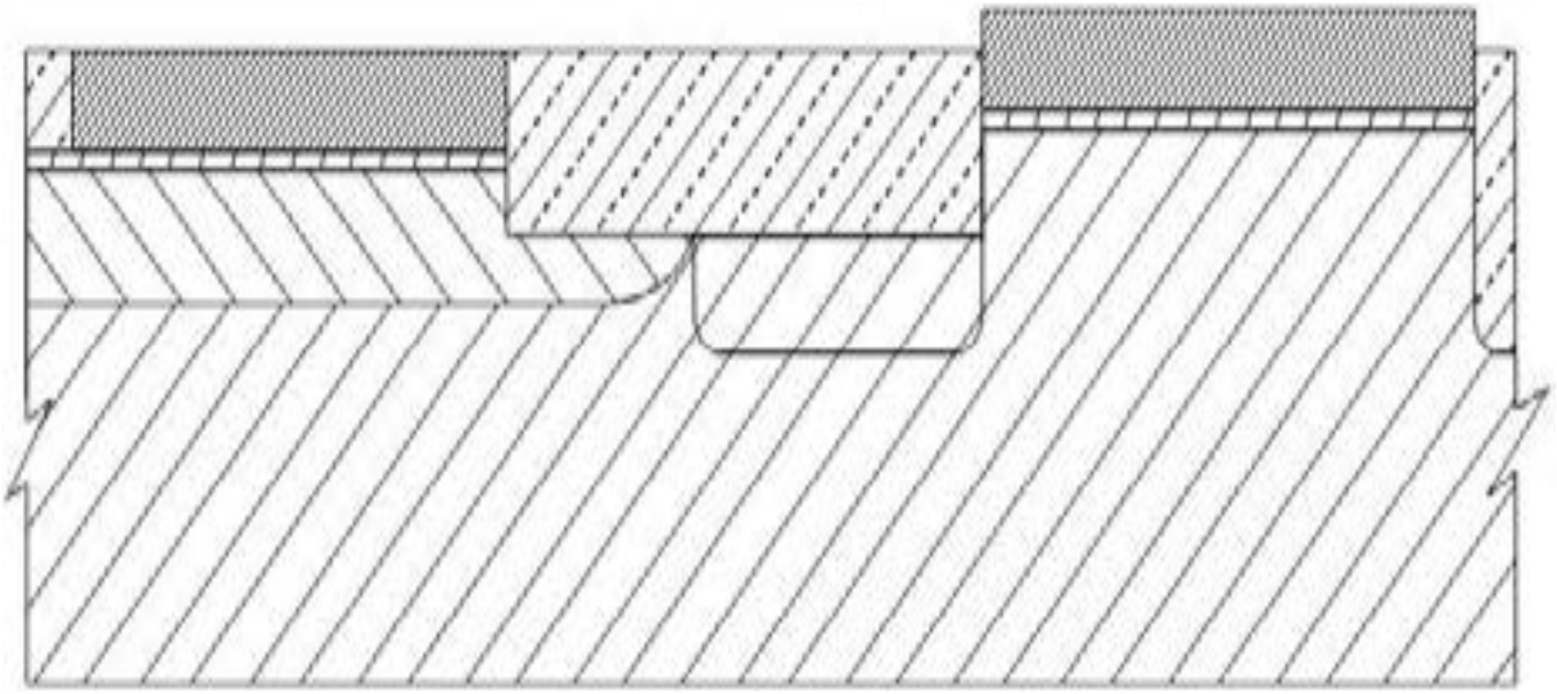
Petitioner's Reply, Paper 21, p. 21, 23
Patent Owner's Sur-Reply, Paper 37, p. 25



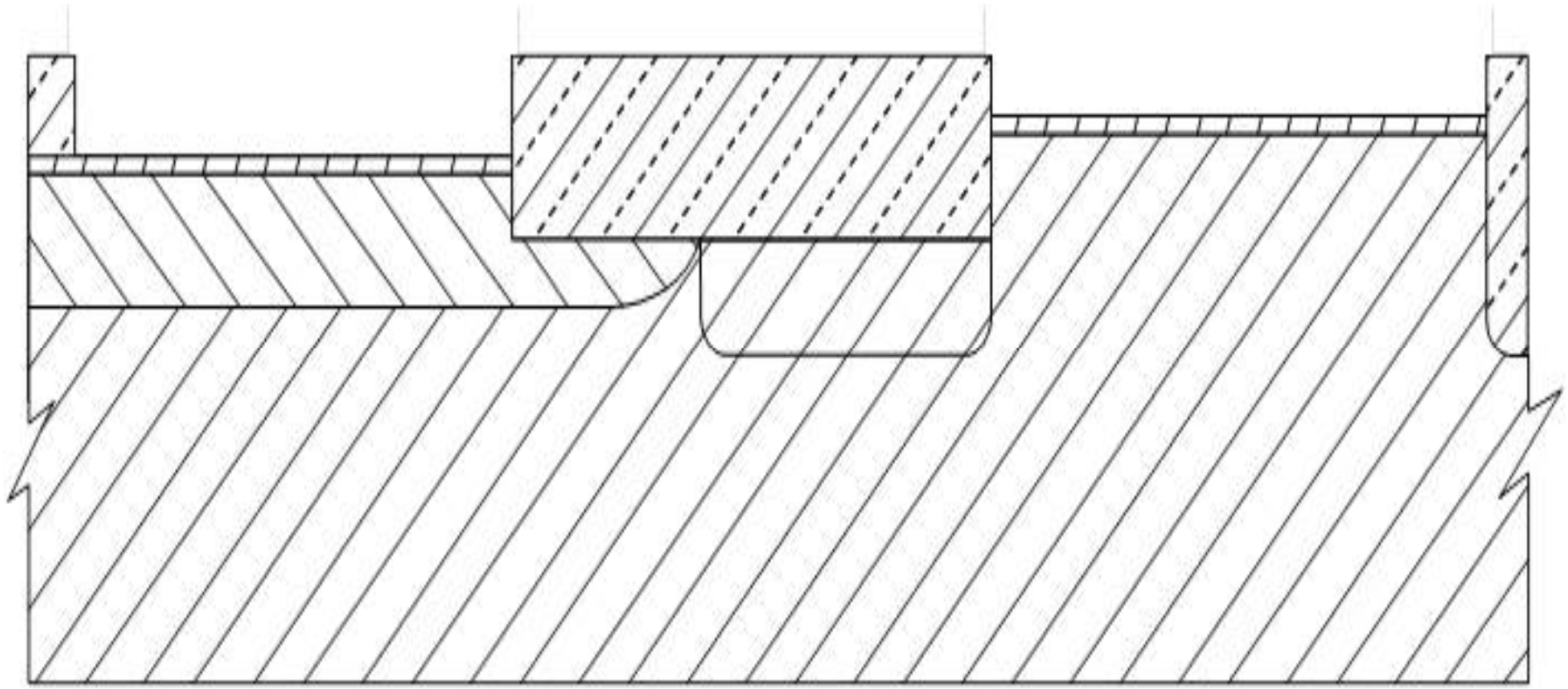
Petitioner's Reply, Paper 21, p. 21
Patent Owner's Sur-Reply, Paper 37, p. 25, 26



Petitioner's Reply, Paper 21, p. 21, 23
Patent Owner's Sur-Reply, Paper 37, p. 25

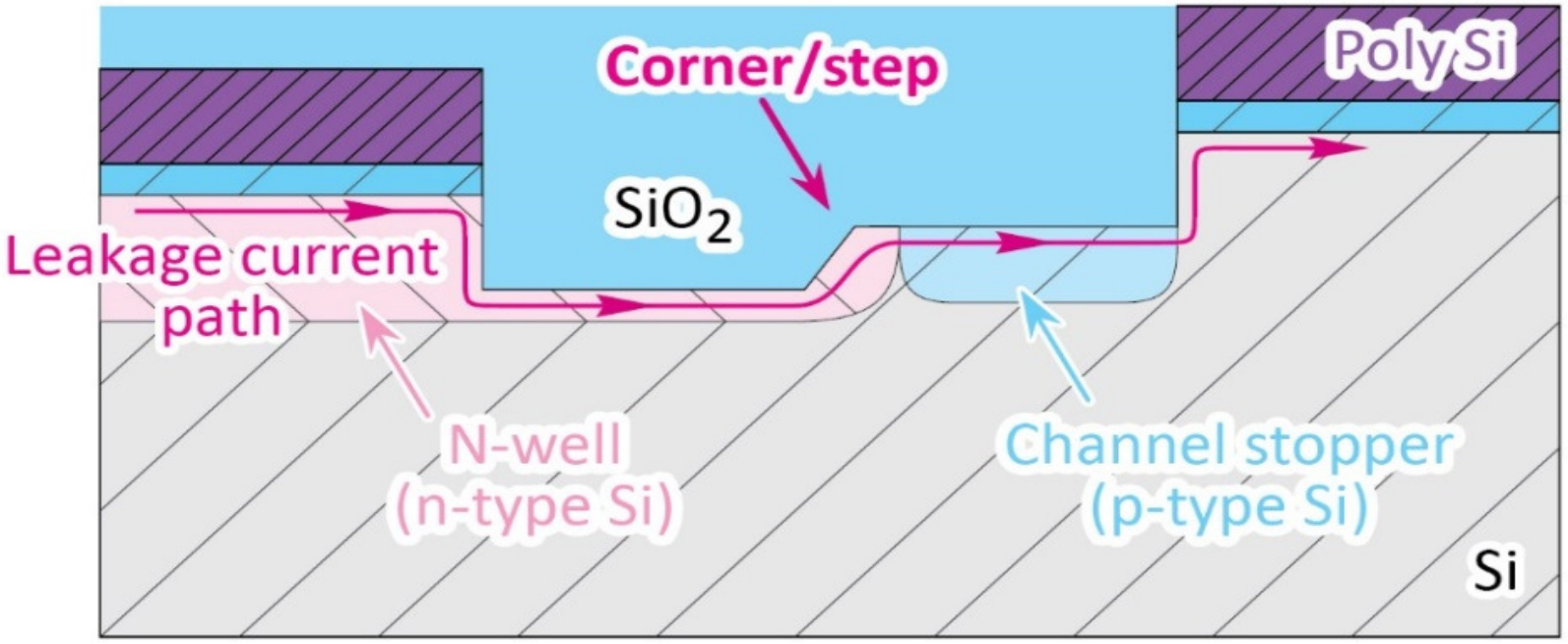


Patent Owner's Sur-Reply, Paper 37, p. 26



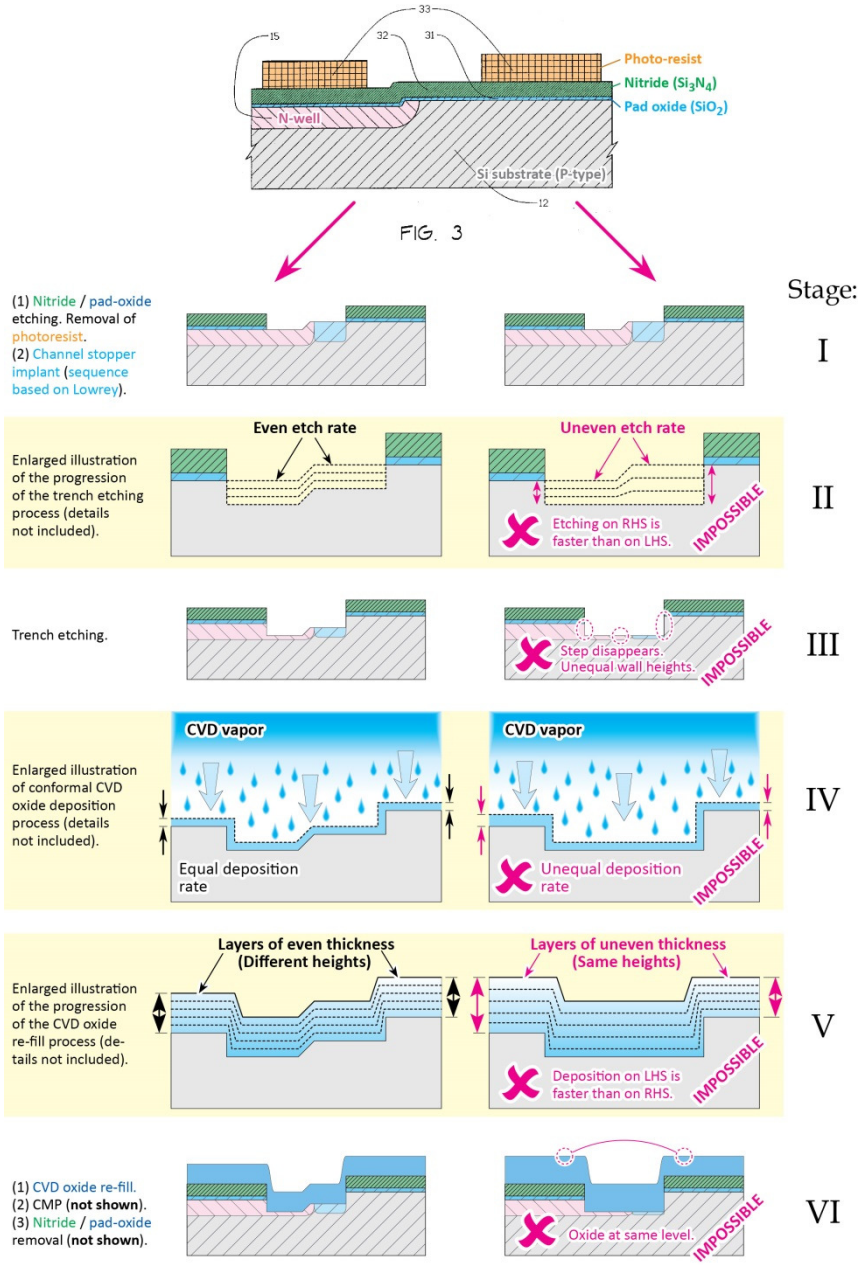
Petitioner's Reply, Paper 21, p. 24
Patent Owner's Sur-Reply, Paper 37, p. 26

Lowrey with Noble/Ogawa:



Corner/step → Non-uniformity → Higher electric fields → Greater leakage current

Patent Owner's Sur-Reply, Paper 37, p. 29



Patent Owner's Sur-Reply, Paper 37, p. 31 (modified)

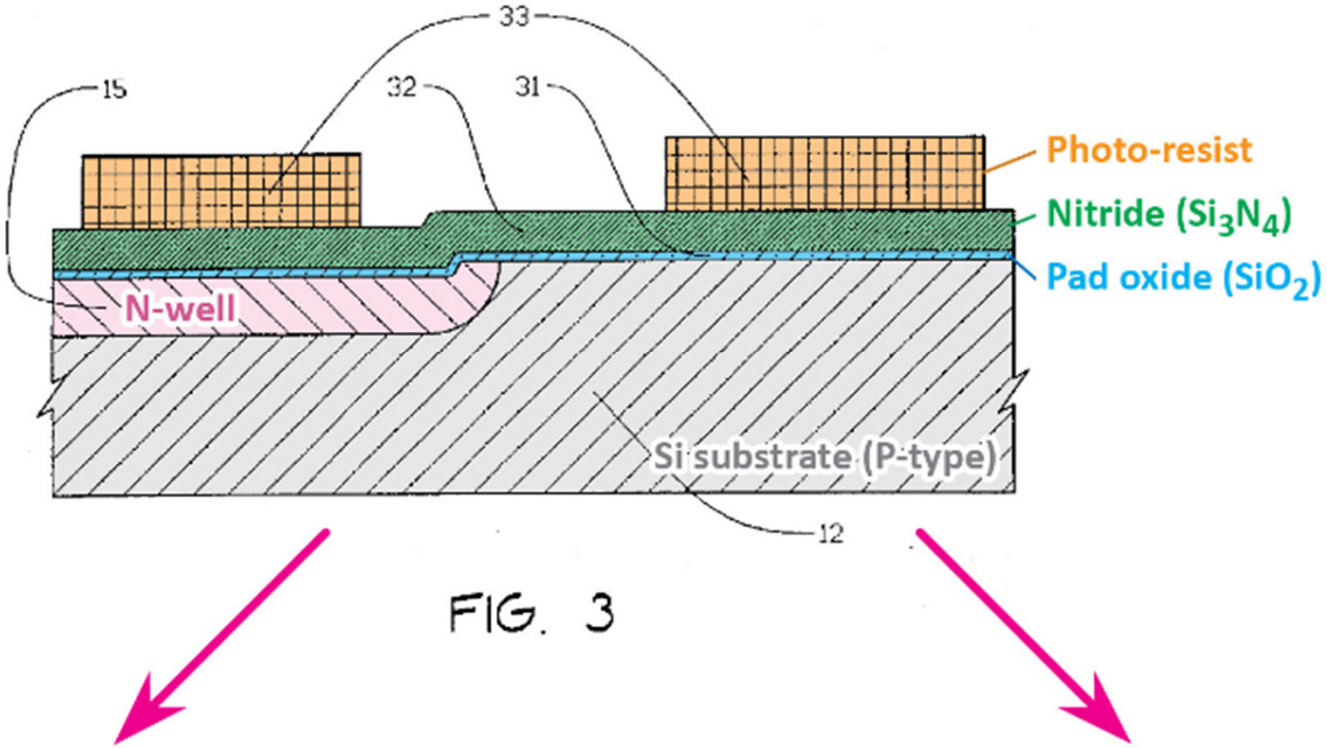
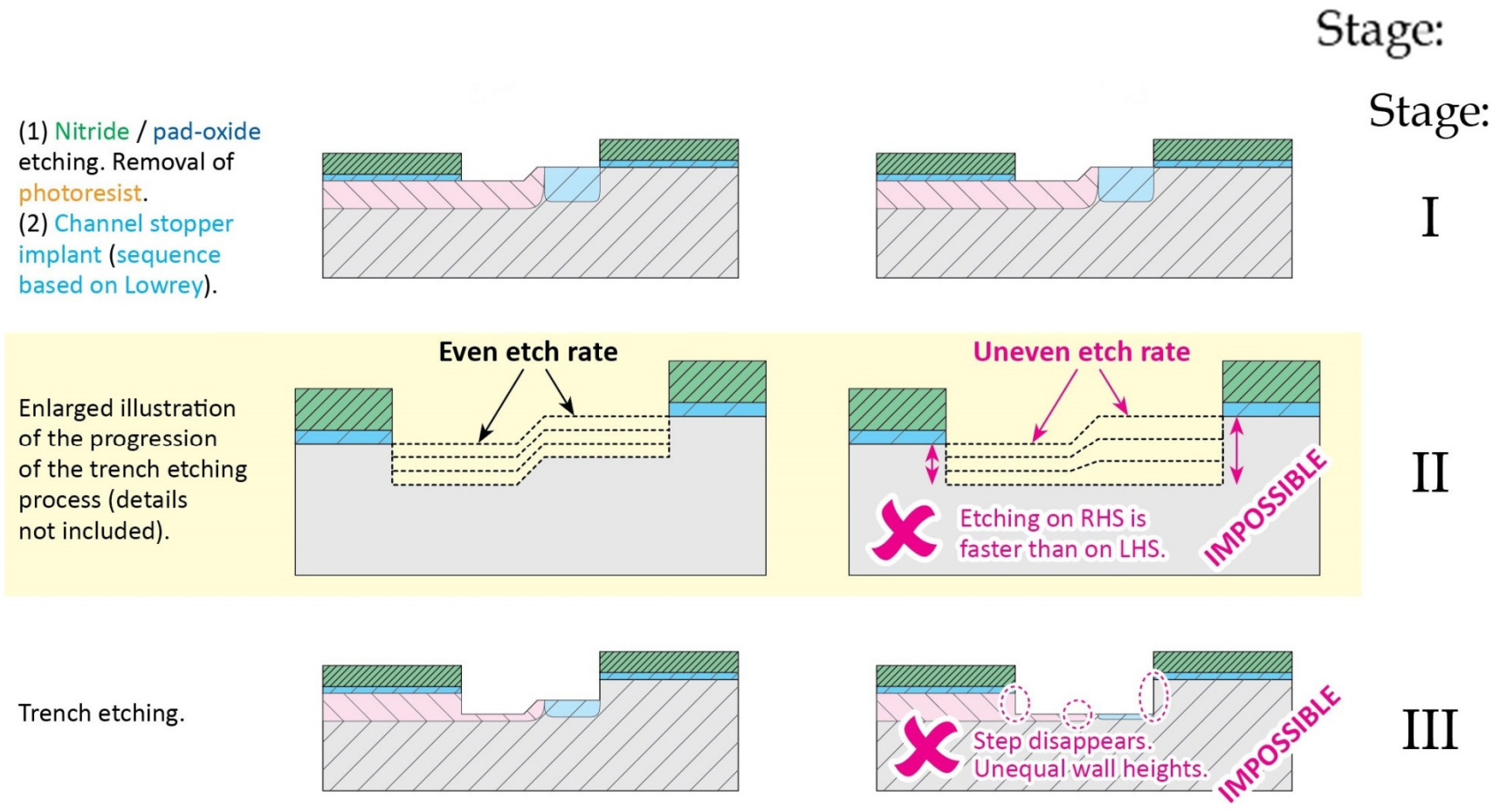


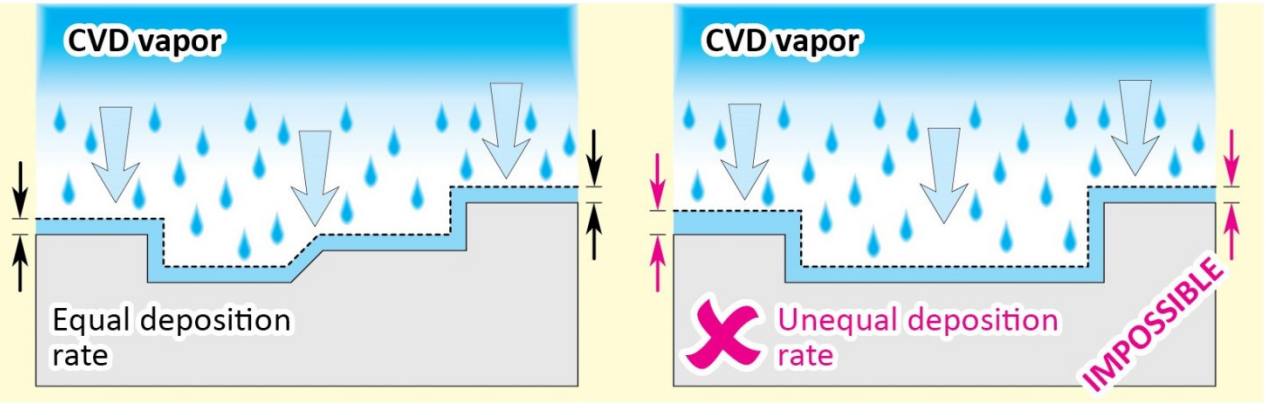
FIG. 3

Patent Owner's Sur-Reply, Paper 37, p. 31



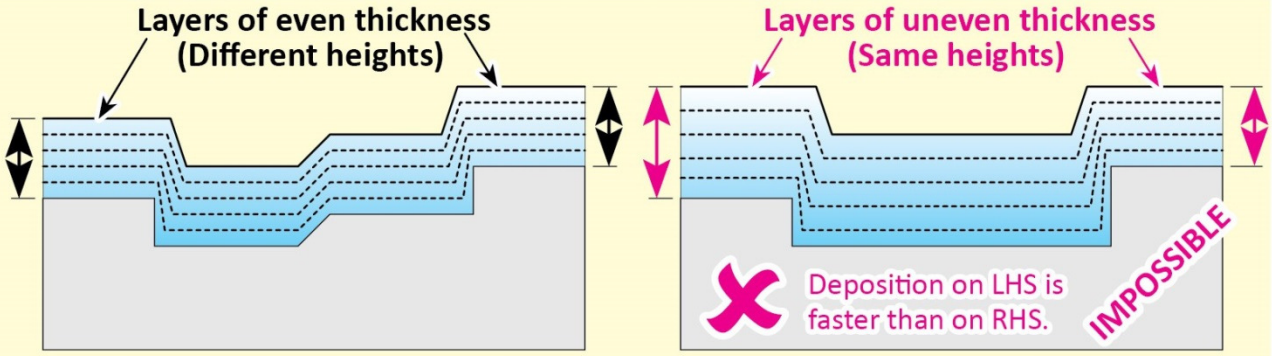
Patent Owner's Sur-Reply, Paper 37, p. 31 (modified)

Enlarged illustration of conformal CVD oxide deposition process (details not included).



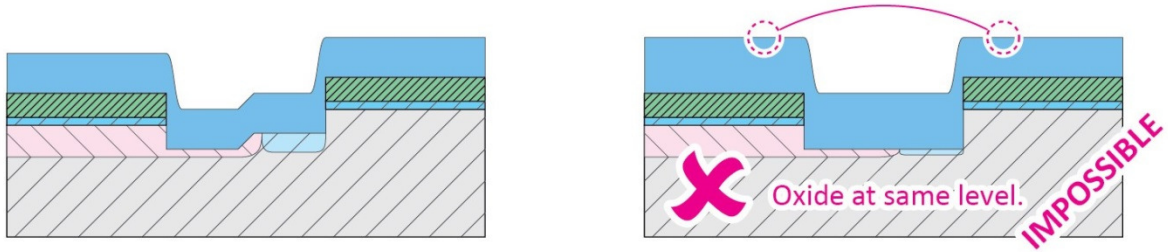
IV

Enlarged illustration of the progression of the CVD oxide re-fill process (details not included).



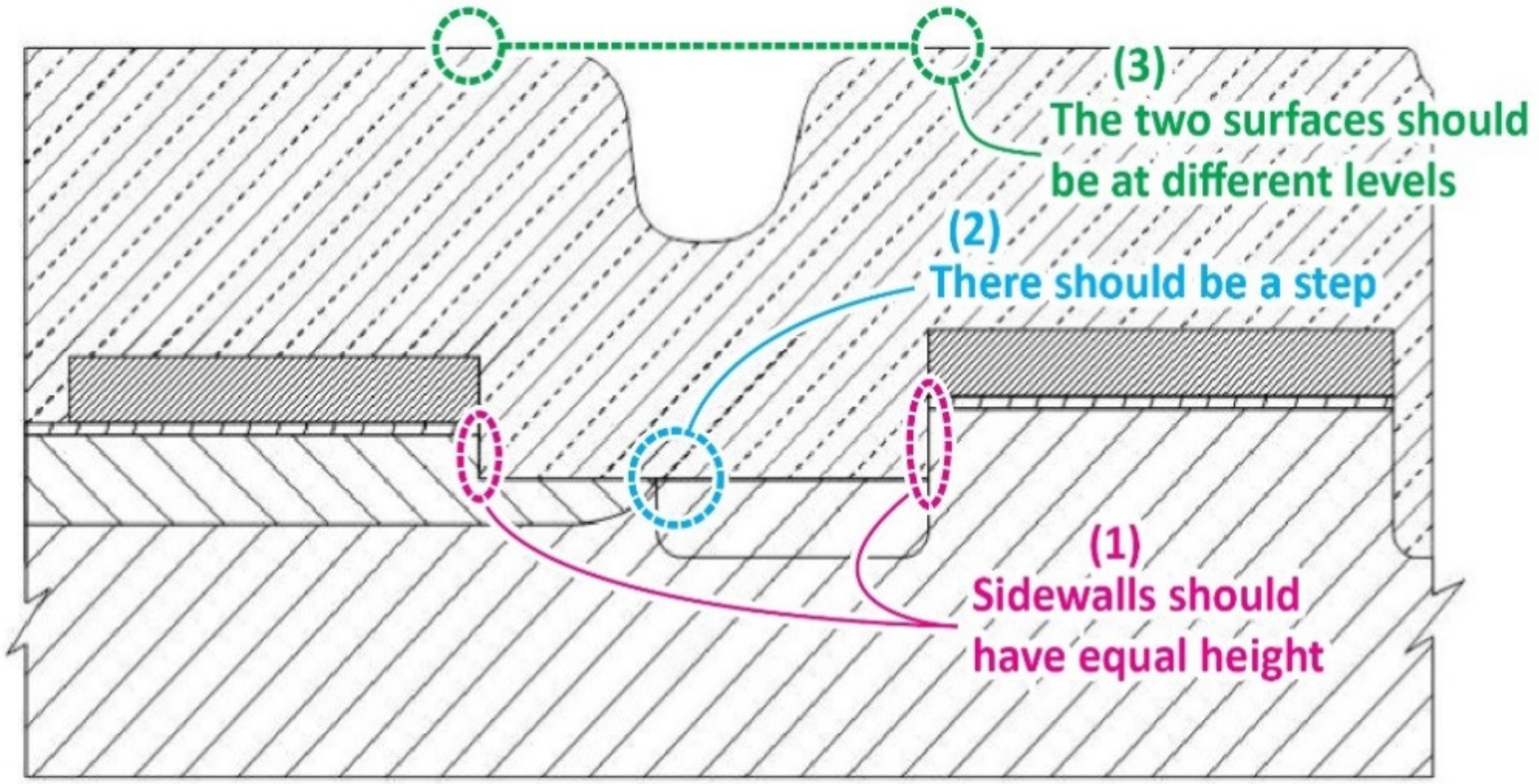
V

(1) CVD oxide re-fill.
(2) CMP (**not shown**).
(3) Nitride / pad-oxide removal (**not shown**).

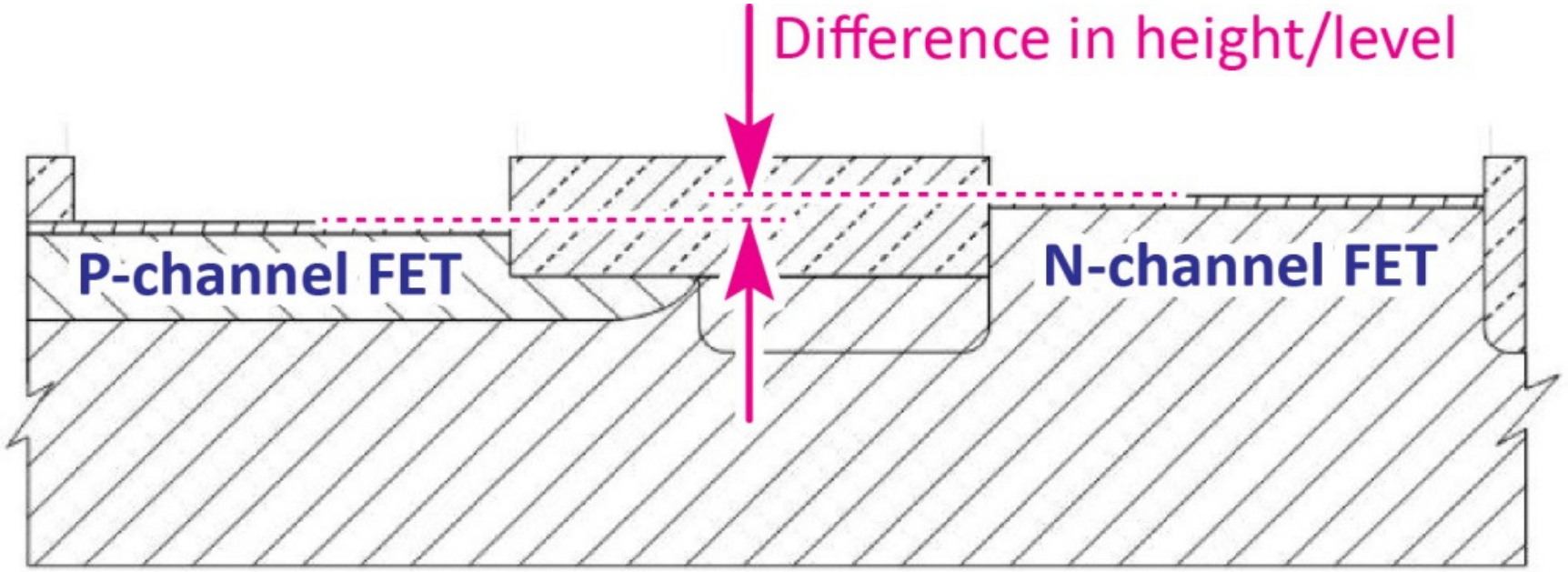


VI

Patent Owner's Sur-Reply, Paper 37, p. 31 (modified)



Patent Owner's Sur-Reply, Paper 37, p. 33



Nitride Removal

Patent Owner's Sur-Reply, Paper 37, p. 34

Silicon is the dominant material for microelectronic circuits, primarily because of the ease with which it oxidizes to form insulating barriers for the subsequent implanting of tiny amounts of dopants into selected regions to achieve the requisite electrical properties. The silicon dioxide insulator and other dielectric films that are commonly encountered such as silicon nitride films are patterned by a process known as photolithography. Photolithography is probably *the* key process in microelectronic fabrication technology, because it is repeated 5 — 12 times before the three-dimensional circuit geometries necessary for a completed metal oxide semiconductor (MOS) or bipolar device are achieved. Figure 4 is an outline of the manufacturing sequence of a large-scale integrated circuit and illustrates the importance of understanding the lithographic technology used to delineate the patterns of thin-film dielectrics and conductors. The structure of an integrated circuit is complex both in the topography of its surface and in its internal composition. Each element of such a device has an intricate three-dimensional architecture that must be reproduced exactly in every circuit. The structure is made up of many layers, each of which is a detailed pattern. Some of the layers lie within the silicon wafer and others are stacked on the top. The manufacturing process consists in forming this sequence of layers precisely in accordance with the plan of the circuit designer.

This photolithography process is repeated (to more than 10 times) before the three-dimensional circuit geometries necessary for a completed metal oxide semiconductor (MOS) or bipolar device are achieved. The structure of an integrated circuit is complex, both in the topography of its surface and in its internal composition. Each element of this device has an intricate three-dimensional structure that must be reproduced exactly in every circuit. The structure is made up of many layers, each of which is a detailed pattern. Some of the layers lie within the silicon wafer and others are stacked on the top. The process is described in detail in the book of L.F. THOMPSON, C.G. WILLSON and M.J. BOWDEN "Introduction to Microlithography", American Chemical Society Symposium Series 219, Amer.Chem.Soc., Washington D.C., 1983.

Since semiconductor devices are becoming more complex in structure and materials, and since the CMP planarization process is dependent on structure and materials, apparatus and techniques that permit the fabrication engineer to control and design the CMP process would be highly desirable.

Generally, a change in one phase of the integrated fabrication process usually impacts other phases. Since integrated circuit fabrication processes are highly complex and require sophisticated equipment, developments of entirely new processes and materials can be quite costly. Thus new apparatus and methods for control of the CMP process that can be incorporated into current fabrication technology would be highly desirable because expensive modification of equipment and processes can be avoided.

Patent Owner's Response, Paper 14, p. 13
Exhibit 2015, 2:52-61

aspect ratios; that is, they become deeper and narrower. Conventional deposition techniques, e.g. sputtering, have difficulty coating such deep, narrow recesses, because the atoms tend to contact one of the walls before reaching the bottom of the recess. Thus, with respect to diffusion barriers, the use of conventional production techniques, such as sputtering, leads to a decrease in the thickness of the diffusion barrier at the base of a contact as the aspect ratio increases. As the thickness of the diffusion barrier decreases, the ability of the diffusion barrier to withstand thermal energy introduced in subsequent processing decreases, and the reliability of the device degrades. Thus there has been an impetus in the industry toward new barrier technology that will deposit an adequate barrier in high aspect ratio contacts, which impetus has tended toward the development of equipment and materials not presently used in semiconductor device fabrication. Generally, a change in one phase of the fabrication process usually impacts other phases. Since semiconductor device fabrication processes are highly complex and require sophisticated equipment, developments or entirely new o processes and materials can be quite costly. Thus a diffusion barrier that is more effective and yet can be incorporated into current fabrication technology would be highly desirable because expensive modification of equipment and processes can be avoided.

Patent Owner's Response, Paper 14, p. 13
Exhibit 2016, 2:19-24

above) using diffusion or ion implantation techniques in order to generate p-n junctions which form active semiconductor devices such as diodes or transistors.

Finally, various types of processes (called "metallization") can be used to produce the interconnecting wiring pattern between the various circuit elements which form the integrated circuit. Wiring patterns can be formed on the wafer using flash evaporation, filament evaporation, electron-beam evaporation, planar and cylindrical sputtering, or induction evaporation methods.

3. Etching-Masking Processes

The etching-masking processes result in selective removal or addition of the deposited or grown layers of semiconductive or passivation materials in accordance with the patterned geometry which defines the integrated circuit elements. The etching-masking steps can be accomplished in a variety of ways, depending upon the particular type of material that is to be masked or etched. Materials commonly used in the etching-masking steps are silicon dioxide, doped silicon dioxide, polysilicon, silicon nitride, metals and polyimide.

The result of these highly complex imaging, deposition and growth, and etching-masking processes is the transformation of each substrate into a large number of integrated circuits which may contain literally tens or hundreds of thousands of individual circuit elements. Once these processes are completed, each wafer is scribed and diced so as to separate it into individual integrated circuits or chips, to which wire leads are then bonded prior to final encapsulation and packaging.

Patent Owner's Response, Paper 14, p. 13
Exhibit 2017, 6:23-31

INTEGRATED CIRCUIT MICRO-FABRICATION USING DRY LITHOGRAPHIC PROCESSES

The United States Government has rights in this invention pursuant to the Department of Air Force Contract No. F19628-85-C-0002.

This application is a continuation of application Ser. No. 07/514,394, filed Apr. 27, 1990, now abandoned which is a continuation of application Ser. No. 07/149,426, filed Jan. 29, 1988, now abandoned.

BACKGROUND OF THE INVENTION

This invention generally relates to micro-fabrication of integrated circuits and, particularly, to an improved process and apparatus for pattern formation on semiconductor wafers to form such circuits.

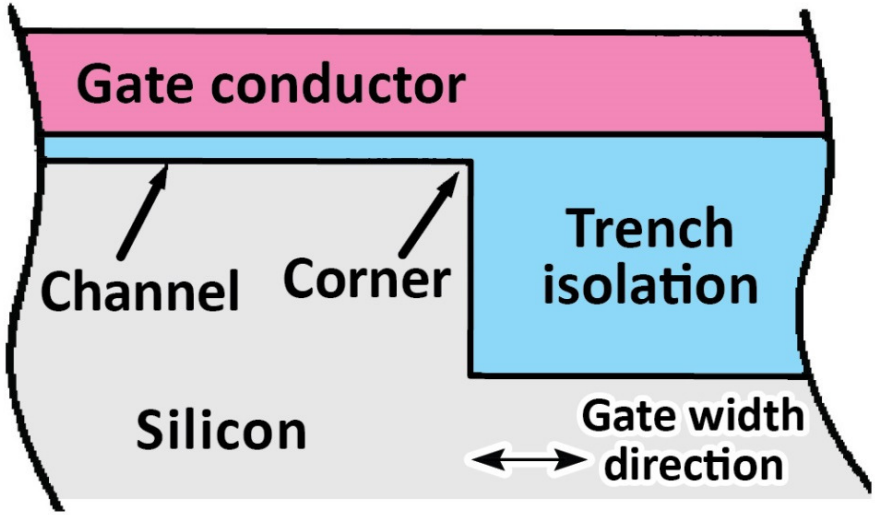
Within the semiconductor industry, production of electronic circuits by very large scale integration ("VLSI") techniques is constrained by a variety of factors which limit yield and inhibit process flexibility. These detrimental factors include, for example, the exposure of wafers to contaminants and/or oxidation during fabrication. Such processing constraints adversely affect mass production of integrated circuits. In addition, conventional processes are slow and inordinately expensive for the fabrication of low-volume products, thus posing an impediment to new device and circuit designs.

Patent Owner's Response, Paper 14, p. 13
Exhibit 2018, 1:18-29

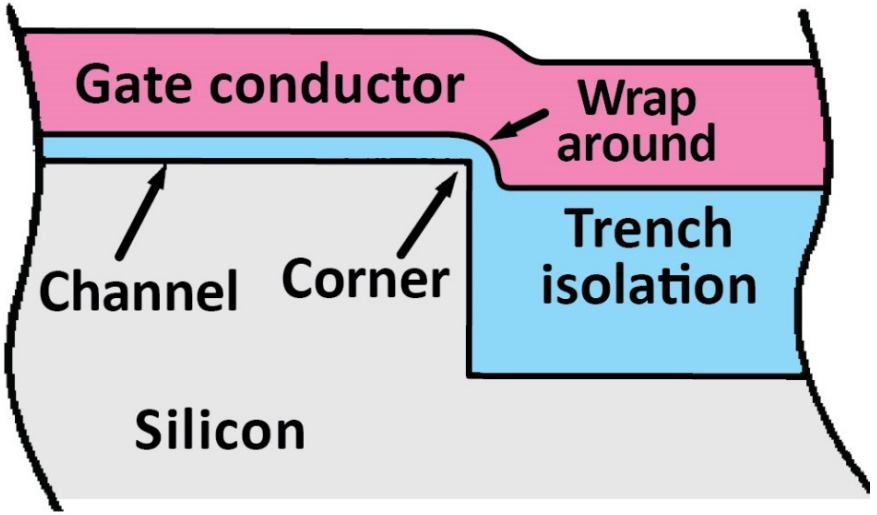
mask. A layer of metal or other suitable conductor is then deposited onto portions of the exposed areas of the semiconductor wafer to form the desired interconnections between components on the wafer. Though there are many fabrication technologies, fabrication techniques, and integrated circuit materials, fabricating the design for the integrated circuit through one or more masks is used consistently.

Depending on the fabrication technologies and techniques, and the materials used, different configuration constraints apply. These constraints are commonly referred to as "geometric design rules" or "design rules." Design rules include, for example, specifications for minimum spacing between transistors and minimum separation between conductors to prevent shorting, specifications for minimum metal width, and specifications for maximum metal heights and slopes of walls which form metal junctions.

Patent Owner's Response, Paper 14, p. 13
Exhibit 2019, 2:9-19



(a) after Bryant, 1993, Exhibit 2022, page 413



(b) Gate-wrap-around problem

Patent Owner's Response, Paper 14, p. 34
Adapted from Exhibit 2022, Bryant, p. 413

Patent Owner's Response, Paper 14, pp. 63, 77