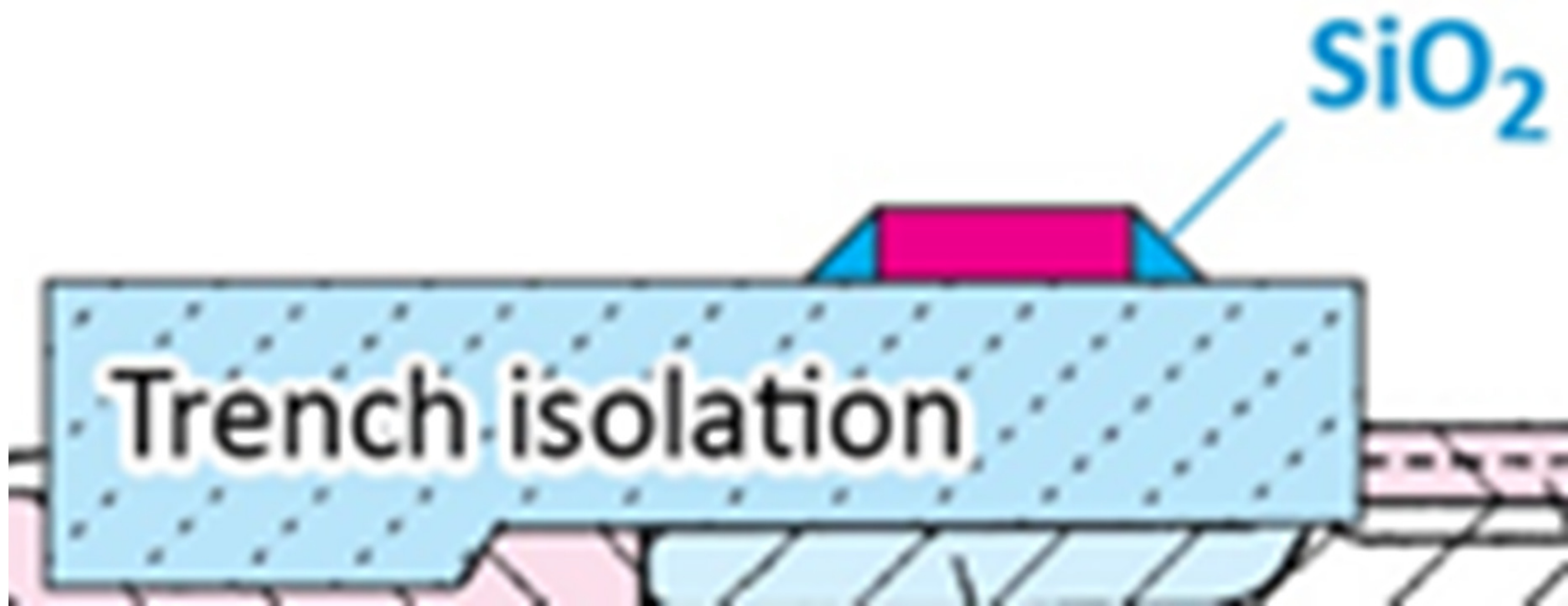
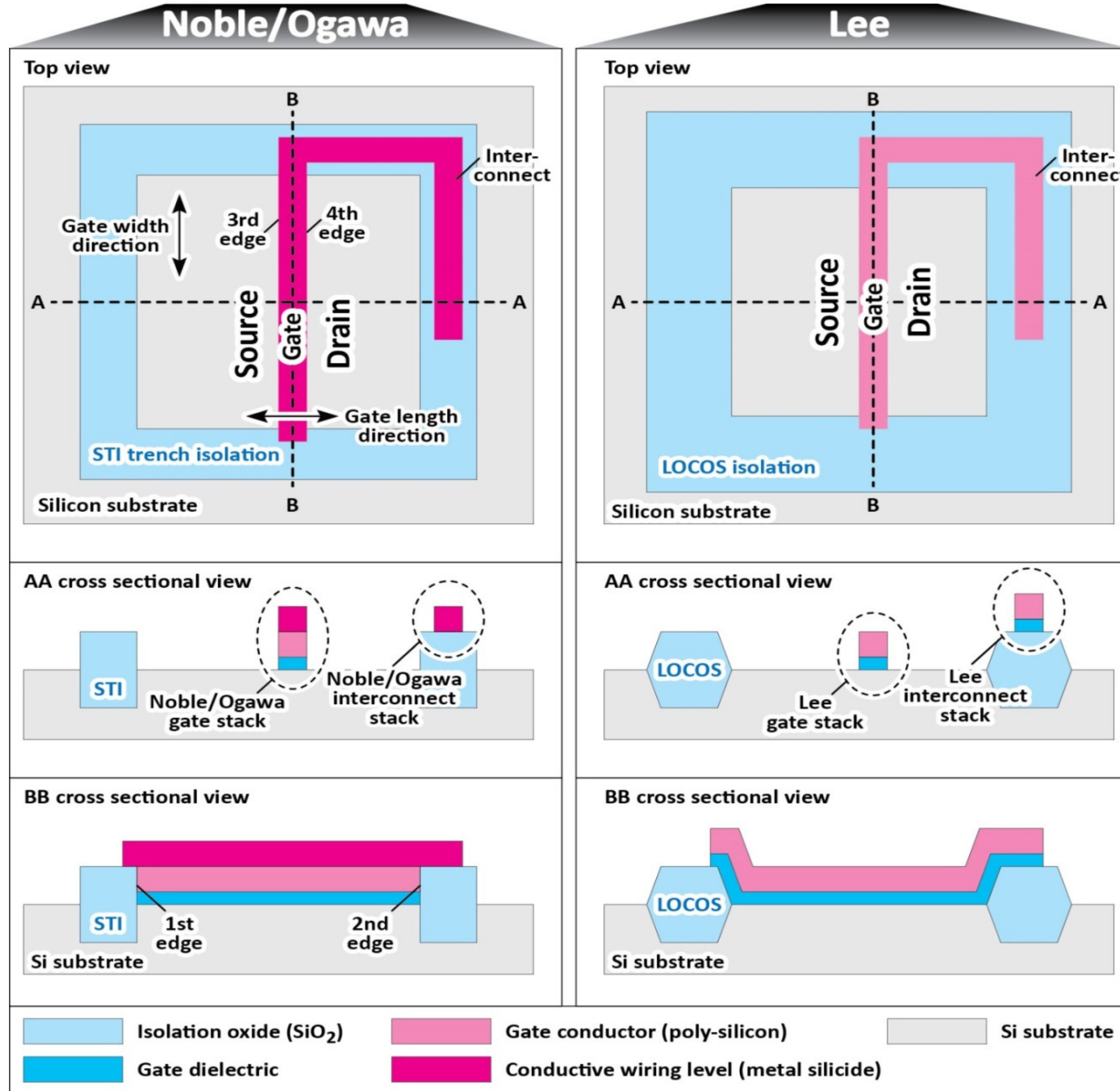
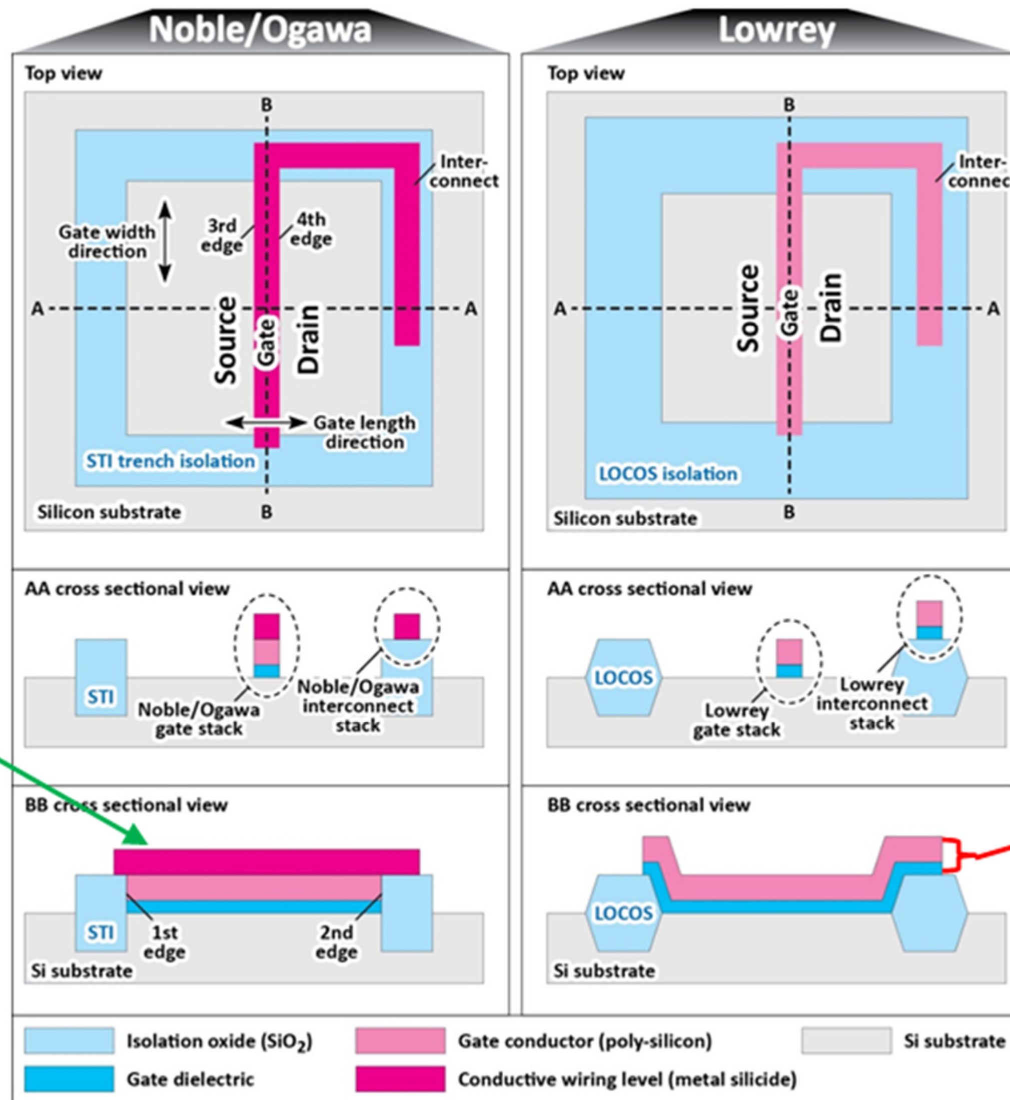


Patent Owner’s Response, Paper 14, p. 119



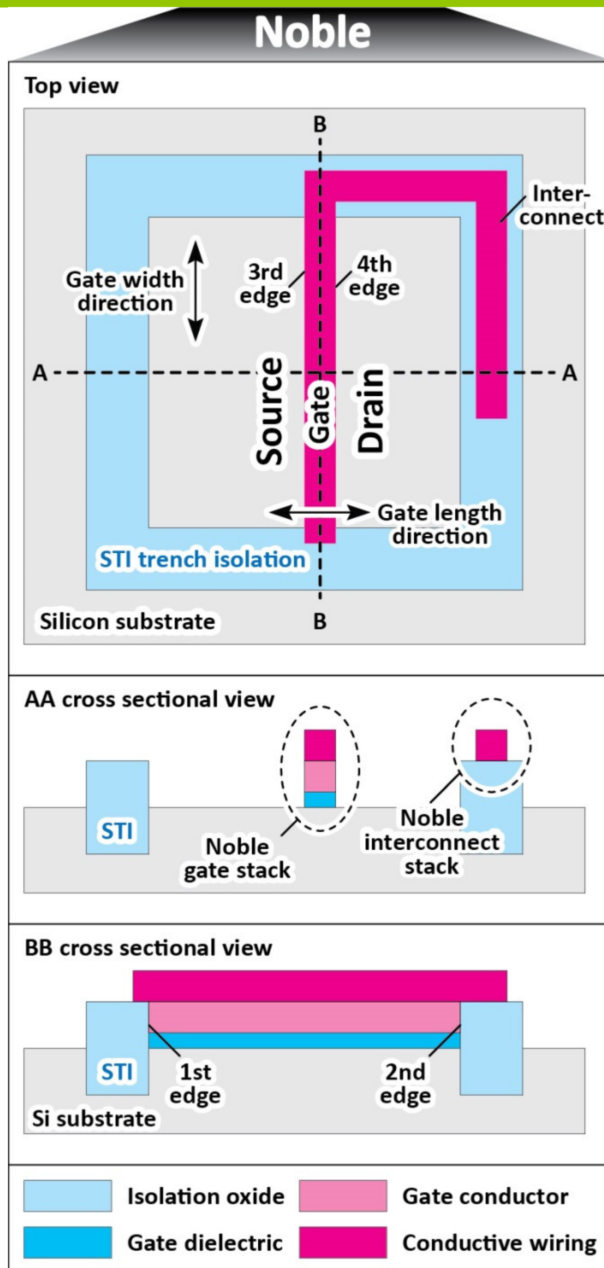
IPR2016-01246 Patent Owner’s Preliminary Response, Paper 7, p. 30

Only the wiring layer goes across

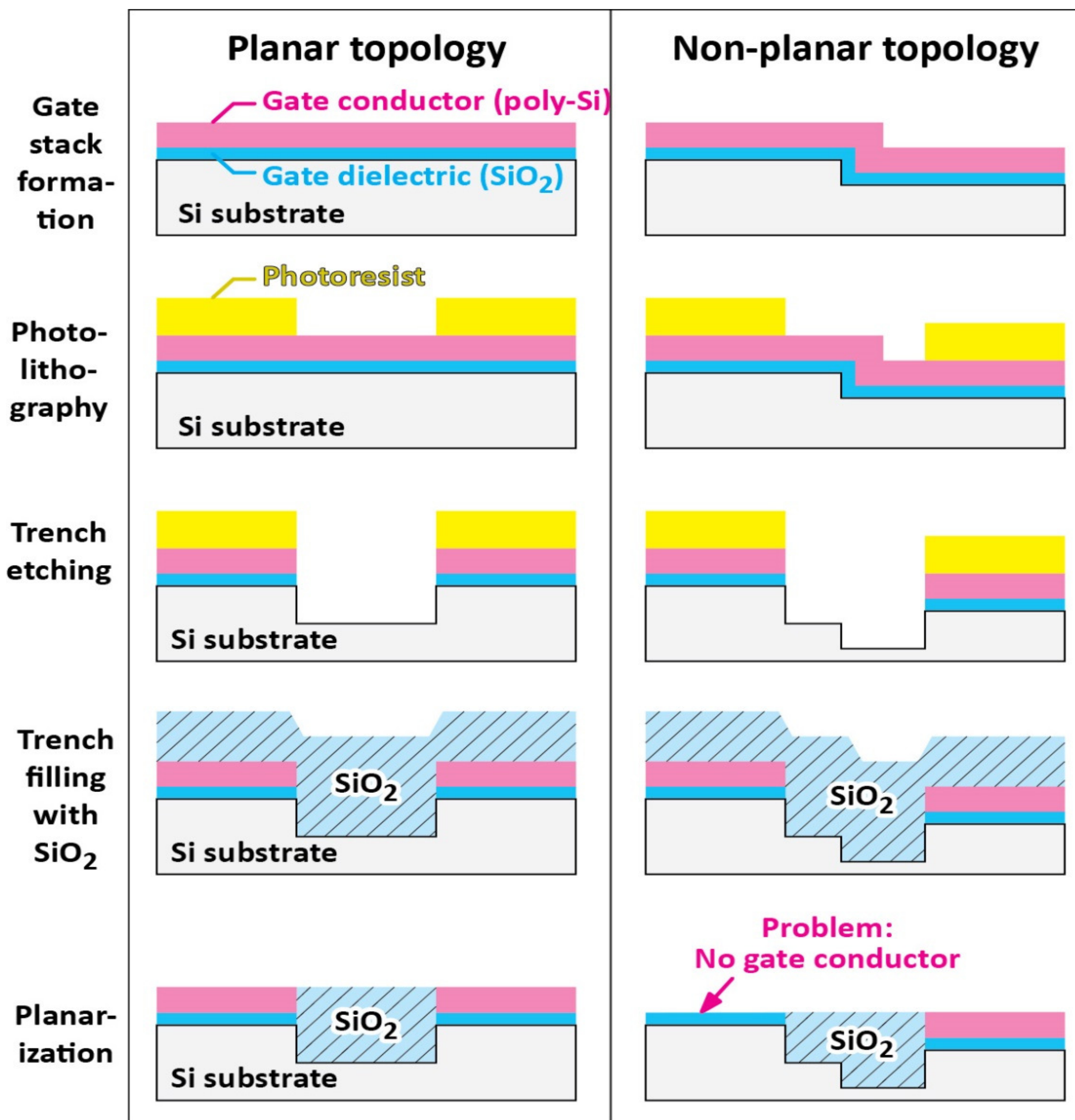


Gate electrode and gate dielectric extend across

Patent Owner's Response, Paper 14, p. 111



Patent Owner's Response, Paper 14, p. 54



IPR2016-01247 Patent Owner's Preliminary Response, Paper 7, p. 38

Process sequence forming the *Noble* gate stack and interconnect:

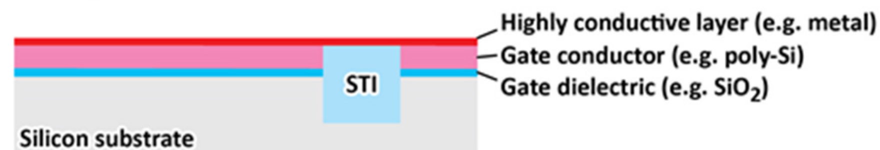
Gate stack deposition / growth:

Trench etching:

Oxide deposition (trench re-fill):

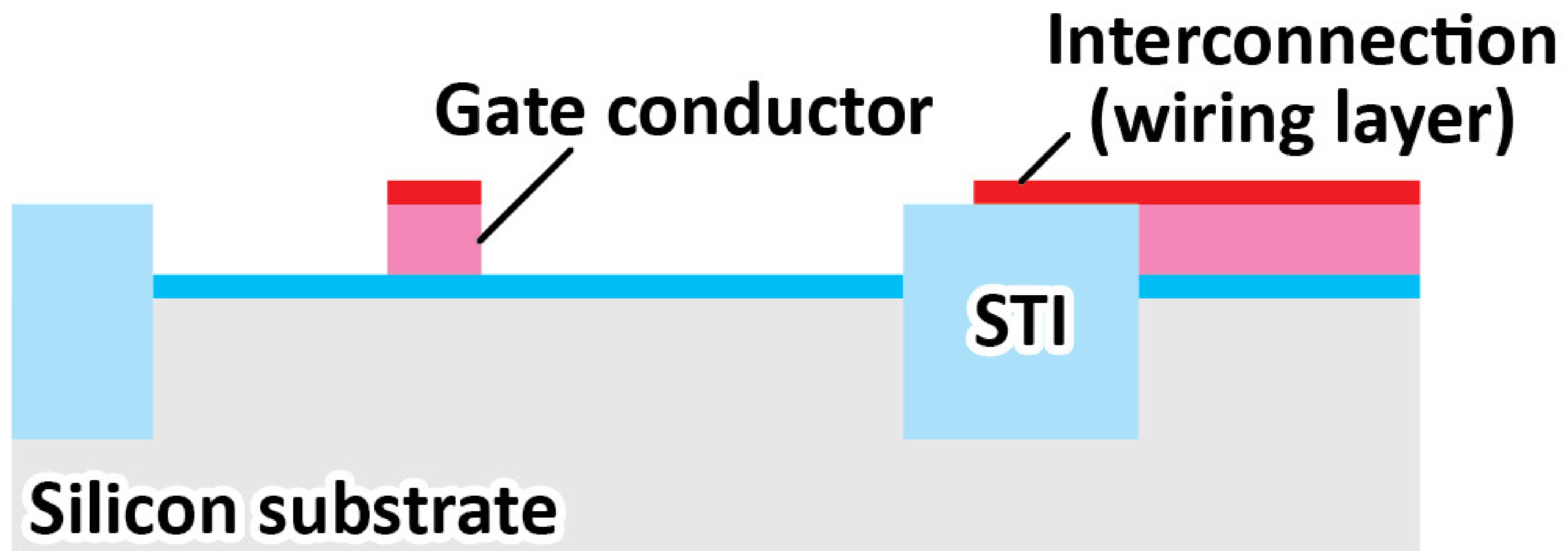
Planarization (e.g. by CMP):

Noble gate and interconnection:

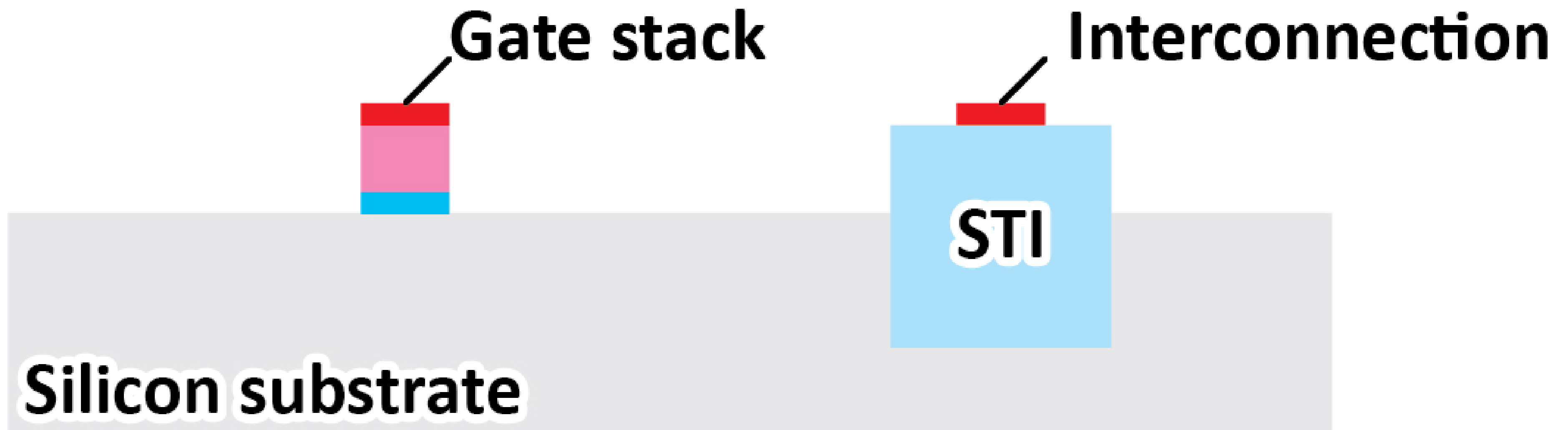


Patent Owner’s Response, Paper 14, p. 74

Cross section along gate length and width direction:

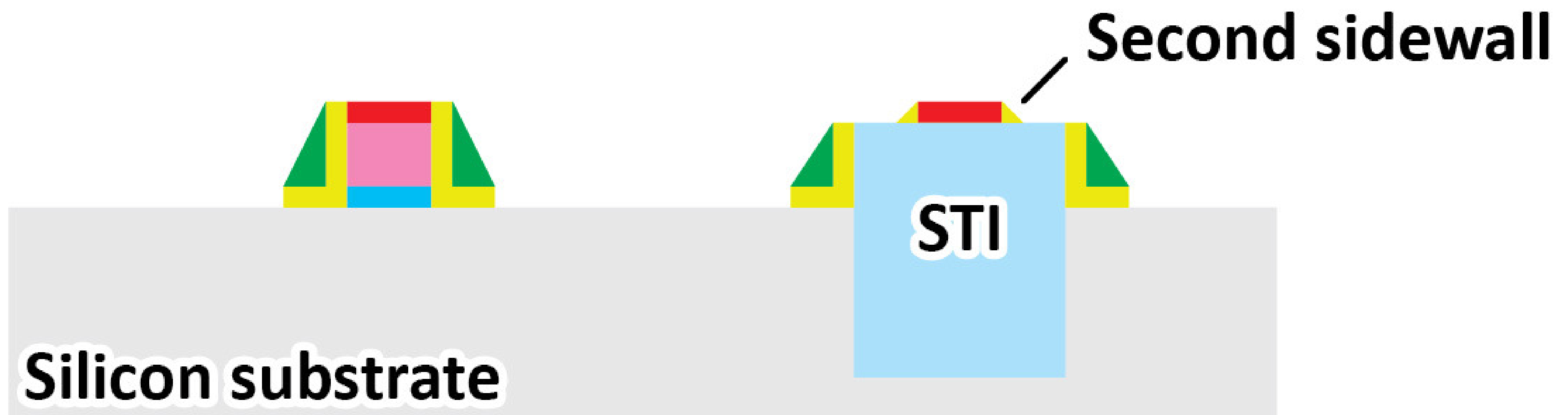


Patent Owner’s Response, Paper 14, pp. 58, 76

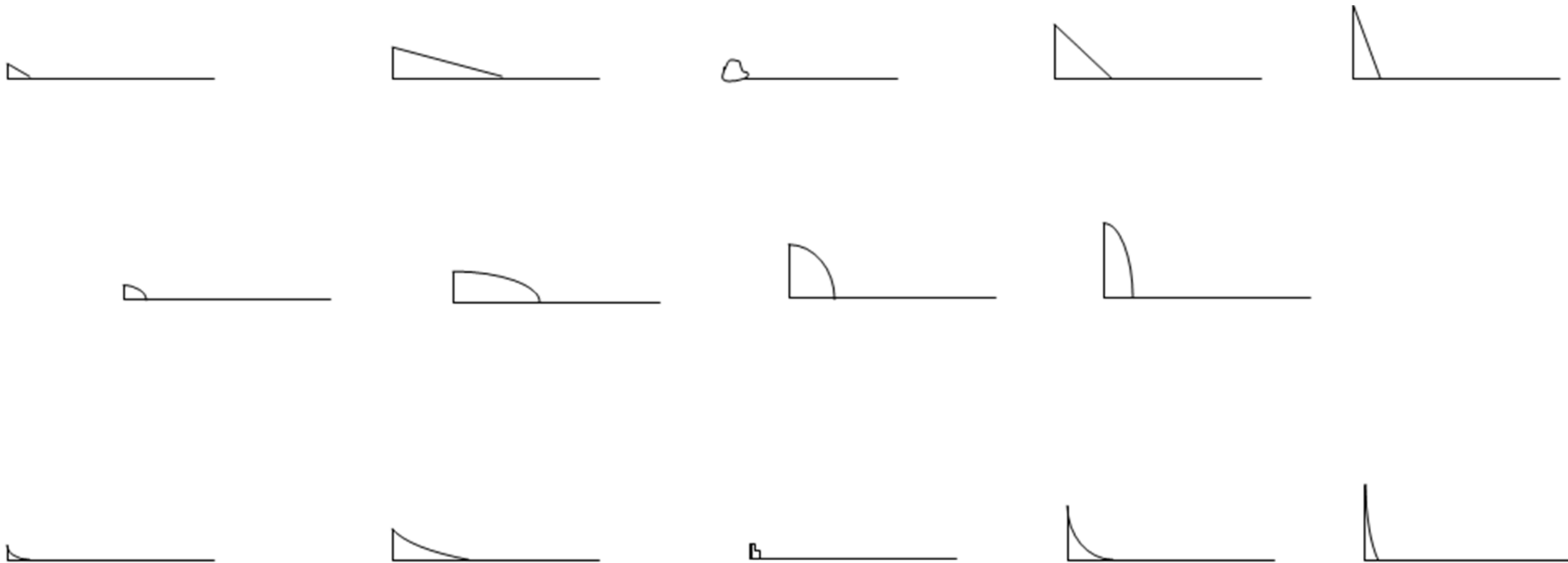


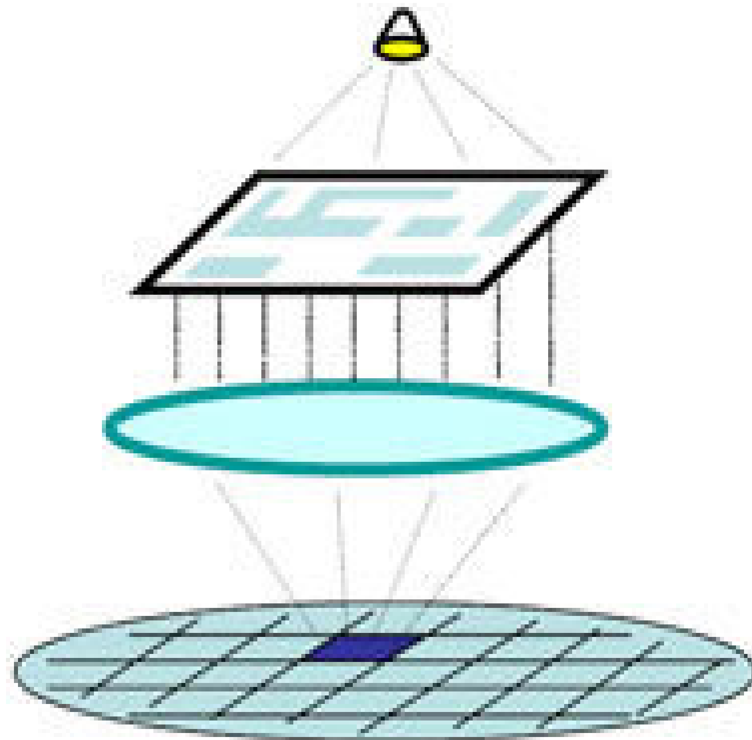
Patent Owner’s Response, Paper 14, p. 75

Anisotropic etching:



Patent Owner's Response, Paper 14, p. 77





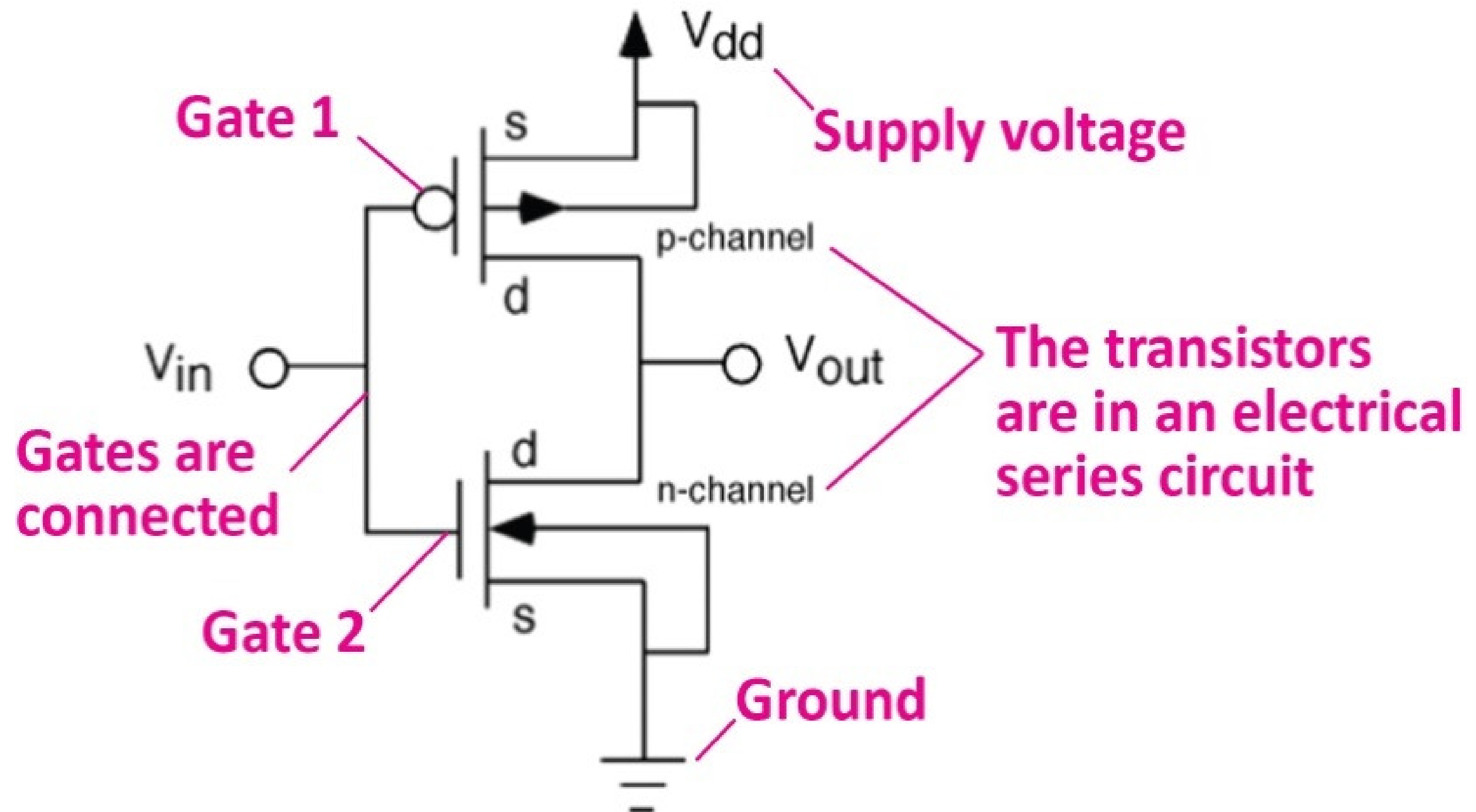
Light source

Mask

Lens to reduce image

Die being exposed on wafer

Patent Owner’s Sur-Reply, Paper 37, p. 35



Patent Owner's Sur-Reply, Paper 37, p. 38

Lee

Now that formation of a nested double or triple layer 45
spacer has been described, a variety of applications of
the inventive structure together with alternative embodiments
and their advantages will be described.

FIGS. 5-7 illustrate how the inventive concept may
now be utilized to form a lightly-doped drain structure. 50
Referring first to FIG. 5, an ion implantation step,
shown schematically by species denoted by reference
numeral **31** is performed to form deeply-doped junctions
25 and **27**. The appropriate ion species **31** is determined
by whether an NMOS or PMOS device is to be 55
formed. Of course, should a CMOS pair of devices be
desired, photoresist **29** is deposited upon that portion of
the structure which must be shielded from the implantation
species **31**. It will be noted, as illustrated in FIG. **5**,
that gate **18** flanked by spacers **19**, **21**, and **23** effectively 60
mask portions **28** and **30** of substrate **11** from implantation
species **31**. (If layer **19** has not been etched, it may
serve to protect surface **26** during the implantation step.
Spacers **21** and **23** will still serve as protective masks for
regions **28** and **30**.) 65

A variety of other techniques may be utilized to form
junctions **25** and **27**. In each case spacers **21**, **23** (and
spacer **19** if formed) will mask portions **28** and **30** of

Exhibit 1002, Lee, 3:49-4:33

substrate **11**. For example, a variety of gaseous and solid diffusion techniques known to those skilled in the art may be employed to form junctions **25** and **27**.

Next, as illustrated by FIG. **6**, spacers **23** are removed in anticipation of formation of the shallow portion of the device junctions. If spacers **23** are made from undensified TEOS or even densified TEOS or BPTEOS, they may be etched much more quickly than field oxide **13** or any protective oxide (such as layer **19** or another regrown oxide layer) which may cover deep junction **27**. For example, using a 15:1 HF etch, the etch rate for thermal oxide is approximately 200 Å per minute, while for undensified TEOS the etch rate is approximately 1400 Å per minute and for phosphorous doped TEOS, 20,000 Å per minute. If spacer **23** has been made from polysilicon, it may be removed by plasma etching. (However, if material **17** is also polysilicon, it will also be attacked by the plasma etching process. Consequently, it is desirable that there be a protective layer such as silicon nitride material **17** if spacer **23** is polysilicon. The use of various layers, such as silicon nitride over the gate stack is discussed in greater detail in subsequent paragraphs.)

After spacer **23** has been removed, a second implant using ion species **37** shown in FIG. **6** is performed. The second implantation species must penetrate the "foot" of spacers **21** and **19**. The foot serves to absorb some of the ionic species, thus creating shallow junction regions **33** and **35** in portions **28** and **30** of substrate **11**. Proper tailoring of the implant energy and dosage and the thickness of the feet of layers **21** and **19** permits the achievement of carefully controlled shallow junctions **33** and **35**.

Exhibit 1002, Lee, 3:49-4:33 (continued from previous page)

Lowrey

2

arsenic or phosphorus to create the N-wells. The N-well regions are then oxidized using a first conventional LOCOS (LOCal Oxidation of Silicon) step to create a silicon oxide layer to protect them from an optional boron implant which adjusts the concentration of the P-type substrate for the N-channel devices. During the LOCOS process, the pad oxide serves as a stress relief layer. Alternatively, an oxide deposition or oxide growth step could replace the first LOCOS step, eliminating the need for the first pad oxide layer and the first nitride layer. A subsequent high-temperature drive step is used to achieve the desired N-well junction depth. Following removal of the oxide layer, a second layer of pad oxide is grown over the entire wafer. A second silicon nitride layer is then deposited on top of the pad oxide layer.

Exhibit 1017, Lowrey, 2:1-6

Lowrey

8

22 at the edge of masking layer **21** during the oxide growth step. Following the stripping of first silicon nitride layer **13**, the wafer is exposed to an optional boron adjustment implant which optimizes the concen-
5 tration of P-type charge carriers in the substrate regions outside the N-well where N-channel devices will be created. Silicon dioxide masking layer **21** protects the N-well region from this boron adjustment implant. Next, the phosphorus atoms implanted in the N-well
10 regions **15** and the boron atoms outside the N-well from the optional adjustment implant are driven into the substrate during a high-temperature step.

Exhibit 1017, Lowrey, 8:2-12

Lowrey

9

mini-spacer oxide layer **62** on the edges of the N-channel transistor gates **56**.

Referring now to FIG. **7**, all circuitry is blanketed with a first spacer oxide layer **71** by one of various techniques (e.g., chemical vapor deposition).

Referring now to FIG. **8**, first spacer oxide layer **71** and mini-spacer oxide layer **62** are etched with a first anisotropic etch, then optionally etched once again with a first isotropic etch to form a first set of sidewall spacers **81** for N-channel transistor gates **56**, N-channel interconnects **57** and the portion of polysilicon layer **53** which blankets the P-channel regions. The anisotropic etch is used to remove most of the spacer oxide layers, but not to the point where the substrate is cleared. The task of clearing the substrate is left to the wet etch, which can be made far more selective to silicon dioxide than to the substrate, thus minimizing silicon crystal damage on the substrate surface. A high-dosage arsenic or phosphorus implant then creates self-aligned heavily doped n-type source/drain regions **82** for N-channel devices. The high-dosage implant is self-aligned to the edges of the N-channel transistor gates **56**.

Exhibit 1017, Lowrey, 9:6-12

Ogawa

duce a semiconductor device having a high quality. 30

The second embodiment, which is an extension of the previous embodiment, is a method for production of a semiconductor device in accordance with the first embodiment, wherein the polycrystalline silicon (Si) layer, which functions to absorb thermal strains, is further 35 employed for production of electrodes for gates and/or some of the metal wiring. This simplifies the production steps thereof. This embodiment will be described, referring to FIGS. 5(*a*), 5(*b*) and 5(*c*).

Exhibit 1010, Ogawa, 7:31-39

Noble

single masking step defines the edge between the trench and gate stack and provides perfect alignment therebetween. Thus, the gate is bounded by a raised trench on two opposite sides. However, since the gate dielectric and gate conductor were formed as blanket layers before the trench was etched, there is no corner sharpening, no gate dielectric thinning, and no gate wrap around.

Exhibit 1015, Noble, 4:22-26

Q. I think you said before that the substrate dopings vary from wafer to wafer.

MR. YOCHES: Objection.

BY MR. GREENBLUM:

Q. They can vary?

MR. YOCHES: Objection.

THE WITNESS: I don't remember if I said that, but, yeah, they can vary.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 59:9-16

131. *Lee*'s "L-shaped" spacers (Exhibit 1002, 3:8-21) are formed by etching away layers **119** and **121** shown in Fig. 13. Layers **115**, **117** and **118** are "typically formed during initial steps of semiconductor fabrication." Exhibit 1002, 6:53-56. The purpose of the "L-shaped" spacers is to allow for the specific method used by *Lee* to dope the source/drain regions.

Exhibit 2012, Schubert Declaration, ¶131

Lee's method includes the implantation into the Si partially through the sidewalls, rather than using the sidewalls as a mask for the implantation. *Lee* discloses: "Referring first to FIG. 5, an ion implantation step, shown schematically by species denoted by reference numeral **31** is performed to form deeply-doped junctions **25** and **27**." (Exhibit 1002, 3:51-54) (Emphasis added.) *Lee* then discloses: "After spacer **23** has been removed. a second implant using ion species **37** shown in FIG. 6 is performed. The second implantation species must penetrate the 'foot' of spacers **21** and **19**. The foot serves to absorb some of the ionic species. Thus, creating shallow junction regions **33** and **35** in portions **28** and **30** of substrate **11**." (Exhibit 1002, 4:24-29) (Emphasis added.).

Exhibit 2012, Schubert Declaration, ¶131 (continued from previous slide)

That is, *Lee*'s removal of spacer **23** enables the shallow implant contrary to the teachings of the '174 patent. In summary, the *Lee* sequence and the '174 sequence with respect to the deep/shallow S/D implant are opposite, the purposes of the sidewalls are different, and the function of the individual elements are different.

Exhibit 2012, Schubert Declaration, ¶131 (continued from previous slide)

152. Different from *Lee*, *Noble* uses a diffusion process to for ultrashallow S/D junctions after the spacers are formed.

In this regard, *Noble* states:

> Then, after spacers **152** are formed (FIG. 12), intrinsic polysilicon (or intrinsic amorphous silicon) is deposited or selective silicon is growth for raised source/drain **154** as shown in FIG. 13. Dopant for the raised source/drain is implanted at low energy so as to avoid damage to the single crystal silicon below. Then the dopant is diffused from the polysilicon to form [source/drain] ultrashallow junctions **156** without damage.

Exhibit 1015, 6:17-24 (emphasis added). Based on these differences, a POSITA implementing *Noble*'s transistor would not be motivated to implement the spacers **152** using the L-shaped sidewalls of *Lee*.

Exhibit 2012, Schubert Declaration, ¶152

158. This configuration is achieved because *Noble* begins the fabrication process by first laying down layers **14** and **116** and then boring (or etching) through these layers to form a trench that is then filled with oxide material. The opening formed through layers **14** and **116** is bordered by these two layers.

Exhibit 2012, Schubert Declaration, ¶158

Q. Okay. So did you take into account whether these references were 700 nanometers, 500 nanometers, or 350 nanometers in your analysis?

MR. YOCHES: Objection.

THE WITNESS: I didn't look at specific node sizes, and I don't believe that's relevant.

BY MR. GREENBLUM:

Q. Okay. But you didn't do it?

A. No.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 84:14-18

MR. YOCHES: Objection.

BY MR. GREENBLUM:

Q. Okay. Now, since we're on Lee, I -- I noticed that -- well, why don't we talk about -- why don't we talk about the sequence of forming the LDD in figure 6. Because that seems to be what you relied upon.

A. So as described in column 4, line 4, you will remove spacers 23.

Q. 23. Is it 23? Yes, you remove spacer 23.

A. 23. And then you do the lightly doped drain implant, lightly doped drain implant, LDD implant, which will be masked by the gate electrode 17 as well as in this case layer 20 -- the vertical portion of layer 21.

Then after that, you'll do the second heavier implant.

Q. Where is that shown?

A. In the figure that's this deeper part of the junction, which is labeled 27. The LDD is labeled as layer 35.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 84:19-85:18

Q. So I want to get the sequence here straight. First you form the shallow dose?

A. Yes.

Q. Then you form the deeper dose. Is that correct?

A. Yes.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 85:19-86:2

Q. Why is it done that way? Why is that sequence there? Why -- why not do it the reverse?

MR. YOCHES: Objection.

THE WITNESS: That's because the device requires it. You want to have the shallower lightly doped drain abutting the gate, gate electrode, because that helps with a variety of effects known as short channel effects.

But you need the deeper source, heavier doped source drain to help with your series resistance and contact resistance.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 86:3-13

Q. So you want the shallow done first. And then the deep done second.

A. That's the way -- that is the way it's done because it helps make the structure easily.

Q. Is it always done in this order?

A. To my knowledge, yes.

Q. It's always done in this order. I'm talking not only about Lee, but in general, is the shallow always done before the deep?

A. To the best of my knowledge, yes. Everything that I've seen, it has been in that sequence.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 87:14-88:3

Q. Now, is there any disadvantage if this is -- if it's done the other way? I mean, why can't you do it in the reverse order?

MR. YOCHES: Objection.

BY MR. GREENBLUM:

Q. Here in Lee?

A. I cannot think of a straightforward process flow where you do it in reverse order. These implants are done using what are called self-alignment techniques and very straightforward ways to do the sequence of LDD first, followed by the heavier, deeper source drain.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 88:4-15

Q. And am I to understand that a person of ordinary skill in the art would not perform Lee in the opposite direction, in the opposite sequence; that is, the deep first and the shallow second?

MR. YOCHES: Objection.

BY MR. GREENBLUM:

Q. Is that correct?

A. Based on the specifications, if you look at column 4, line 24 onwards, it says clearly after a spacer 23 has been removed, a second implant using species -- ion species 37 shown in figure 6 is performed. So it shows it here.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 89:2-13

Q. And can you think, as you sit -- as you prepared your declaration and as you sit here today, can you see a way to modify Lee so that it -- this doping sequence would be opposite to the one we've been talking about? In other words, deep first and shallow second?

MR. YOCHES: Objection.

THE WITNESS: I mean, everything that I am aware of, you do the LDD first and then the deeper implant second. Is it possible to do it the other way? I'd have to --

BY MR. GREENBLUM:

Q. You have given no opinion on that?

A. I have not given any opinion to that.

Q. And as -- and as you sit here now, you don't know of any?

A. No, not offhand.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 89:14-90:8

MR. YOCHES: Counsel, I asked for a break.

MR. GREENBLUM: I'm sorry, go ahead.

(A recess was taken at 11:45 a.m., after which the deposition resumed at 11:54 a.m.)

BY MR. GREENBLUM:

Q. I wanted to confirm something that you said before. When you ran through your explanation of Lee, did you -- did I understand you correctly that in your understanding of Lee, the lightly doped region is formed before the deeply doped region? Or the shallow region is formed before the deep region?

MR. YOCHES: I'm going to object to that question.

THE WITNESS: I misspoke earlier. In this Lee process, you actually do the deep junction first, layer 27, and then the shallow LDD region afterwards.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 124:12-125:7

BY MR. GREENBLUM:

Q. Didn't you say previously that you could not imagine doing it that way? And I'll read to you the section where you said that. I asked you: It is always done in this order? And at that time, you had the wrong order. And I'm talking not only about Lee but in general. Is the shallow always done before the deep? To the best of my knowledge, yes.

Is that wrong?

A. In the vast majority of cases that I'm aware of, you do the shallow first and then the deep, but clearly now I see in the case of Lee, they flipped the order.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 125:8-20

What I really meant was you could -- it's generally done in the order that I mentioned. You do the LDD first and then you put a spacer and use that to do the deeper, heavier implant. That's the usual mode, but in this case, they flipped the order. My apologies. I misspoke earlier. Yeah.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 126:11-17

Q. So -- but you did -- there is two problems here. One is that you misspoke about what Lee does. But you also said that the other way, you can't imagine that anybody would do it. And that turns out to be the way that Lee is doing it.

So how can you possibly imagine somebody doing that, Lee? You said you couldn't imagine it.

MR. YOCHES: Objection.

THE WITNESS: Yeah, I -- I misspoke earlier in the heat of the moment.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 126:18-127:5

BY MR. GREENBLUM:

Q. I asked you: As you sit here -- and can you think -- as you prepared your declaration and as you sit here today, can you see a way to modify Lee so that this doping sequence would be opposite to the one we've been talking about; in other words, deep first and shallow second?

And your answer: I mean, everything that I'm aware of, you do the LDD first and then the deeper implant second.

Now you're saying: No, well, it could be done, Lee could do it; is that correct?

A. Lee does it the other way. Lee does the heavier deeper implant first.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 128:2-15

Q. But you couldn't think of a way that that could be done before? A straightforward process, you said there would be no straightforward process for doing this. Now -- now look at Lee.

A. Yes, I misspoke earlier.

Q. Well, now, when you did your declaration did you analyze the sequence of doping in Lee?

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 128:16-22

A. Yes, I did.

Q. And was it correct?

MR. YOCHES: Objection.

THE WITNESS: I was focusing mostly on the claim elements in the '174 patent, and I was paying special attention to that. And, of course, I was looking at the overall flow also.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 129:1-7

BY MR. GREENBLUM:

Q. Well, am I to understand that the overall flow that you had in mind was wrong? In other words --

MR. YOCHES: Objection.

BY MR. GREENBLUM:

Q. -- the doping sequence was wrong?

A. I had the doping sequence flipped over here, but it doesn't change my opinion about the claim elements.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 129:8-17

Q. You could not imagine previously -- you could not imagine -- you said you couldn't imagine anybody doing it the way that Lee does it. Is that correct?

A. If that's what I said earlier, I misspoke.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 131:14-19

A. I mean the -- the sequence in which you do the heavy versus the lightly doped implant --

Q. Yeah.

A. -- doesn't ultimately impact the device functionality. What is important is the LDD region should abut the gate electrode and the heavy source drains should be farther away.

Q. Well, yeah, but what you said was -- but you couldn't -- you said there would be no straightforward process -- oh, okay.

You said: I cannot think of a straightforward process flow where you do it in reverse order.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 132:12-133:2

These implants are done using what are called cell alignment techniques and very straightforward ways to do the sequence of the LDD first, followed by the heavier, deeper source drain.

And I said -- I said to you: And can you think -- as you prepared your declaration and as you sit here today, can you see a way to modify Lee so that this doping sequence would be opposite to the -- to the way we have been talking about; in other words, deep first and shallow?

"The witness: I mean, everything that I'm aware of, everything that I am aware of, you do in the LDD first and then the deeper implant second."

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 133:2-15

That's what you said. Now, you know, you say here: "Everything that I am aware of." Was that -- am I to understand that everything that you were aware of, you didn't mean it?

A. I was thinking of the vast majority of cases that are -- I was thinking off the top of my head in terms of making these LDD structures. Once again, as I said, I misspoke as it pertains to Lee. But it does not change my opinions in terms of the claim elements.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 133:16-134:3

Q. Okay. Now, in your declaration --

MR. GREENBLUM: And let's give him those two declarations. He has the declarations. And they are Exhibits -- there are actually three of them, 1004, 1024, and 1057.

BY MR. GREENBLUM:

Q. Did you ever discuss the sequence of doping in Lee?

A. I don't see any discussion of the order of the lightly doped drain and the deep source drain.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 136:1-11

Q. But these are not? You notice it's different at the STI than it is at the gate relative to the L. That's an error, isn't it?

A. Once again, these are stylized drawings, yeah, I should have -- the draftsman drew those and I should have caught those, but to me that's sort of in the -- I hate to use the word "noise" -- the essential point is would a person of ordinary skill be able to take a raised STI structure and replace LOCOS with the raised STI structure, and it doesn't change that opinion.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 148:20-149:8

Q. Okay. And I am going to ask you again.
Do you know of any way how it could be as shown here
in real life? You can say no.

A. These are stylized drawings and I was
trying to make the point that it will place -- you
could insert the trench isolation process into
Lowrey. That was the essential point over here.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 200:21-201:5

Q. Look, the height is different on page 68 of 204 also, right?

A. Yes, I see that.

Q. That's also wrong, right?

A. That's because the draftsman took a basic template and added components on top of that.

Q. Did you review what he did?

A. Yes, I did.

Q. Did you sign your name at the end of it?

A. Yes.

Q. It is not true, is it, this is not true? It can't be.

A. These are stylistic errors that do not change my opinion at all.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 201:6-19

Q. You know, I am not so sure, because I think that anyone who could draw that difference in height, which would violate every rule of etching and physics, I think you didn't pay very close attention to this at all.

Am I correct?

A. No, it is not correct.

Q. So there were three errors in just this drawing here, and these errors go to the fabrication process, right, that's what you are showing here?

A. These are minor stylistic errors which have no bearing on my conclusion.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 201:20-202:9

Q. You are proposing here a process, right?
And the heights are wrong. The relative heights are
wrong. It can't be.

So how can you propose a process based
upon something that can't possibly be?

A. The height difference that you are
talking about is relatively minor.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 202:15-21

Q. So you are saying that there are errors in here but they don't change your final conclusion?

A. The minor stylistic errors, they do not change my final conclusion, yes.

Q. What do you mean by stylistic? What does stylistic mean to you? This violates basic rules of nature.

MR. YOCHES: Wait.

THE WITNESS: I consider it a serious error if it impacted the final conclusion. These are at the end of the day stylized drawings. Nothing is really to scale.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 203:14-204:3

I admit, I mean, I should have been perhaps more accurate in showing the step differences and height differences, but, once again, because the step difference that you are talking about for typical tank oxides is of the order of 100 nanometers, that's going to be small compared to the other dimensions, such that at the end of the day it does not change the final conclusion.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 204:4-11

BY MR. GREENBLUM:

Q. Now, are you aware of any prior art as you sit here that you cited that has this step at the bottom of the trench?

A. Not offhand. I can't remember.

Q. Have you ever seen a step on the bottom of a trench?

A. Sitting here I cannot recall.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 204:12-19

Q. It is a question. The fact that the spatial dimensions of the trench are smaller than the LOCOS of Lowrey, substantially smaller than the LOCOS, doesn't that suggest to you that there is a greater likelihood that this non-uniformity in the bottom of the trench could be problematic? You can say yes or no.

A. The answer is, the short answer is no. I can expound on that if you want me to.

Q. Go ahead, expound.

A. So the main advantage going from LOCOS to shallow trench isolation is you get rid of these bird's beak.

How wide you make this isolation region, be that LOCOS or STI, ultimately depends on the isolation capabilities between the adjacent transistors, okay, which would depend on the parasitic field transistor action underneath the isolation region, which in turn depends on mostly the thickness of that field oxide because at the end of the day you are looking at parasitic capacitive coupling between interconnects on top of the field oxide.

As long as that field oxide is thick enough and you optimize the process, I see no problems whatsoever.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 207:12-208:15

Q. And the way you showed it here, it has been optimized so that there would be no problem?

A. Presumably a person of ordinary skill would do things -- choose thicknesses of oxides, thickness --

Q. Okay, finish.

A. Thickness of the oxides, et cetera, so that you get adequate electrical isolation between adjacent devices, which in turn depends on many parameters.

It depends on the power supply voltage that are used, et cetera, et cetera, the leakage that you can afford. There is many parameters that a person of ordinary skill should know.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 208:16-209:7

Q. Are you telling me that because of these parasitic -- I'm sorry, because of these discontinuity at the bottom of the trench, that there would have to be some other precautions taken to eliminate any chance of anything negative happening?

A. You always want to design the isolation region such that you get negligible leakage current from one active region to the next.

And that in turn depends on many parameters, such as the width of the isolation region, the thickness of the field oxide, et cetera. And there is other parameters also.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 209:8-20

Q. Did you explain any of those -- well, are any of those parameters necessary in this case, that you have drawn here on page 69 out of 204, are any of those other parameters required to take -- to overcome the problem associated with the step in the trench?

MR. YOCHES: Objection.

THE WITNESS: These things should be part of the standard knowledge base of a person of -- a person of ordinary skill in the art. I mean, you don't spell out in gory detail every single aspect of every single process.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 209:21-210:10

And I'm asking you are electrical fields naturally higher at the bottom of the trench when there are stepped features?

A. It is an electrostatics problem, so in reality you have to solve what is known as a three-dimensional Poisson equation and couple that with electrical transport equations.

Q. Poisson?

A. Yes, Poisson. It's French. It's P-o-i-s-s-o-n.

So from that, depending on the structure including this step, you would get the contours and enhanced electrical field in some cases may increase the potential barrier. And, if it does, it will actually help with electrical isolation.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 212:14-213:6

Q. Now, did you have a claim definition in mind for L-shaped members when you wrote your -- or L-shaped sidewalls when you wrote your declaration?

MR. YOCHES: Objection.

THE WITNESS: I looked at the plain and ordinary meaning.

BY MR. GREENBLUM:

Q. And what was the plain and ordinary meaning to you?

A. Looks like the letter L, maybe a distorted L.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 272:11-21

BY MR. GREENBLUM:

Q. But did you discuss what would have to be scaled and what the node size would be of the modification, the modified Lee structure? Did you discuss that anywhere in your declaration?

MR. YOCHES: Objection.

THE WITNESS: Not in gory detail, no.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 227:2-7

Q. So you would see if something is L-shaped?

A. If the L-shaped region had, for instance, different chemical dopant, compared to the adjacent region, yes, you would see an L-shaped image.

Q. And is there a threshold below which you wouldn't see it?

MR. YOCHES: Objection.

BY MR. GREENBLUM:

Q. I assume there is some threshold value where you wouldn't see it?

A. There is always thresholds, yes.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 275:6-17

Q. And the L-shaped -- the -- what is the threshold values of these types of devices that you are talking about seeing it with?

MR. YOCHES: Objection.

THE WITNESS: I couldn't tell you offhand without looking at the instruments, the specifications of the instruments, et cetera, et cetera.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 275:18-276:3

BY MR. GREENBLUM:

Q. So if the doping in Lowrey is below the threshold, would you see it here in these machines?

A. Once again, the threshold depends on the specific machine you are using to do the imaging. And if it so happened that the instrument was not sensitive enough to distinguish the doping that was in the L-shaped region in Lowrey, yeah, in that case you would not see it, that's true.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 276:4-12

Q. Can you tell me specifically which machine would be able to see it?

A. My experience is in this business, the more money you are willing to pay, the more sensitive instrument you can get. So I couldn't tell you offhand in terms of exact numbers and thresholds for, you know, various classes of used machines.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 276:17-277:2

Q. And what would be the dosage that -- oh, you don't know as you sit here now --

A. Right.

Q. -- whether or not the dosage that would be present in Lowrey would be seeable in the machines that are used by Servanton and Pantel and Clement; is that correct?

A. Right, I don't have those threshold numbers.

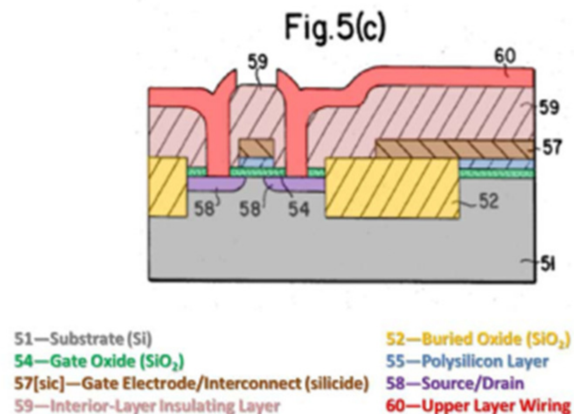
Q. Okay. Thank you.

Exhibit 2078, Deposition Transcript of Dr. Banerjee, 277:17-278:4

Unlike *Innogenetics*, TSMC devotes dozens of pages to explaining both how and why a POSITA would have modified the combined references. Paper 2, at 21, 70; Paper 2 (IPR2016-01247), at 21, 62. TSMC also explained why a POSITA would have made those modifications (i.e., to facilitate scaling of the *Lee* and *Lowrey* devices), and why a POSITA would have reasonably expected to succeed. Paper 2, at 5-7, 21-30, 70-76; Paper 2 (IPR2016-01247), at 5-7, 21-30, 62-68; EX1004, ¶82, 198; EX1024, ¶93, 173.

Petitioner's Reply, Paper 21, pp. 27-28

and **sources and drains** (58) (*id.*, 8:3–7, Fig. 5(c)). (Ex. 1004, ¶80.) *Ogawa*'s Figure 5(c), a representative illustration, appears below with color and annotations.



B. The *Lee-Noble* combination renders claims 1–3, 5–7, 9–12, and 14–18 obvious

Lee teaches every limitation of the challenged claims except trench isolation. A POSITA would have understood that *Noble*'s STI was a known substitute for *Lee*'s LOCOS isolation. (Ex. 1004, ¶82; *see also* Ex. 1009, 1:31–2:24; Ex. 1011, 4:8–16; Ex. 1012, 3:3–10; Ex. 1013, 5:56–67; Ex. 1014, 22:49–52; Ex. 1015, Title, 1:7–10, 2:53–57, 4:14–23, Figs. 12, 13.) The combined teachings discussed in this section refer to the teachings of *Lee*, with its LOCOS isolation replaced by *Noble*'s STI.

C. The *Lee-Ogawa* combination renders claims 1–3, 5–7, 9–12, and 14–18 obvious

As demonstrated above in Section V.B., *Lee* teaches every limitation of the challenged claims except trench isolation. A POSITA would have understood that *Ogawa*'s trench isolation was a known substitute for *Lee*'s LOCOS isolation. (Ex. 1004, ¶198; *see also* Ex. 1009, 1:31–2:24; Ex. 1011, 4:8–16; Ex. 1012, 3:3–10; Ex. 1013, 5:56–67; Ex. 1014, 22:49–52; Ex. 1015, Title, 1:7–10, 2:53–57, 4:14–23, Figs. 12, 13.) The combined teachings discussed in this section refer to the teachings of *Lee*, with its LOCOS isolation replaced by *Ogawa*'s trench isolation.

1. A POSITA would have combined the teachings of *Lee* and *Ogawa*

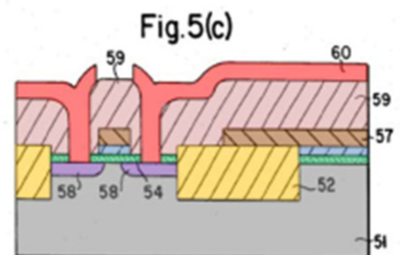
The same reasons that would have compelled a POSITA to replace *Lee*'s LOCOS with *Noble*'s STI also would have compelled a POSITA to replace *Lee*'s LOCOS with *Ogawa*'s trench isolation. (Ex. 1004, ¶199; *see also* §§II.B, V.A.3, V.B.1.)

a. Admitted prior art teaches replacing LOCOS with known trench isolation

The '174 patent shows trench isolation, including trench isolation with a top surface higher than the surface of the semiconductor substrate, as prior art. (*See supra* §V.B.1.a.)

Unlike *Innogenetics*, TSMC devotes dozens of pages to explaining both how and why a POSITA would have modified the combined references. Paper 2, at 21, 70; Paper 2 (IPR2016-01247), at 21, 62. TSMC also explained why a POSITA would have made those modifications (i.e., to facilitate scaling of the *Lee* and *Lowrey* devices), and why a POSITA would have reasonably expected to succeed. Paper 2, at 5-7, 21-30, 70-76; Paper 2 (IPR2016-01247), at 5-7, 21-30, 62-68; EX1004, ¶82, 198; EX1024, ¶93, 173.

Petitioner's Reply, Paper 21, pp. 27-28



51—Substrate (Si)
54—Gate Oxide (SiO_2)
57[sic]—Gate Electrode/Wiring ($MoSi_2$)
60—Upper Layer Wiring
52—Buried Oxide (SiO_2)
55—Polysilicon Layer
58—Source/Drain

B. The *Lowrey-Noble* combination renders claims 1, 4, 5, 8–12, 14, and 16 obvious

Lowrey teaches every limitation of the challenged claims except trench isolation. A POSITA would have understood that *Noble*'s trench isolation was a known substitute for *Lowrey*'s LOCOS isolation. (Ex. 1004, ¶80; *see also* Ex. 1009, 1:31–2:24; Ex. 1011, 4:8–16; Ex. 1012, 3:3–10; Ex. 1013, 5:56–67; Ex. 1014, 22:49–52; Ex. 1015, Title, 1:7–10, 2:53–57, 4:14–23, Figs. 12, 13.) The combined teachings discussed in this section refer to the teachings of *Lowrey*, with its LOCOS isolation replaced by *Noble*'s STI.

1. A POSITA would have found it obvious and even desirable to have combined the teachings of *Lowrey* and *Noble*

Many reasons would have compelled a POSITA to replace *Lowrey*'s LOCOS with *Noble*'s STI. (Ex. 1004, ¶¶80–94.) LOCOS was cheaper and simpler at the time of *Lowrey* (February 1990), and the bird's beak was not a major

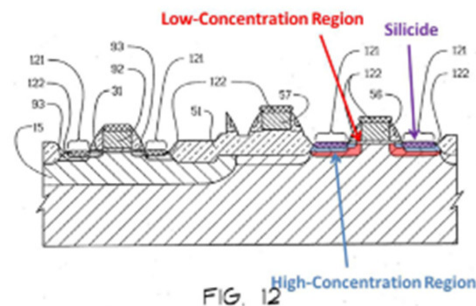
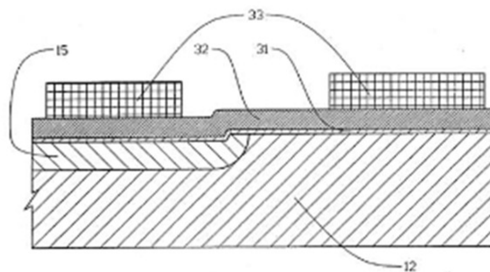


FIG. 12

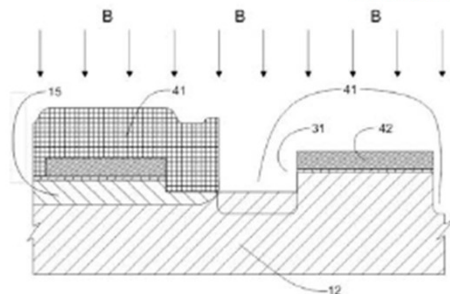
A POSITA would have understood that the *Lowrey-Noble* combination teaches "the source/drain regions include low-concentration source/drain regions and high-concentration source/drain region, and the first silicide layers are formed on the high-concentration source/drain regions." (Ex. 1004, ¶¶157–62; *see also supra* §V.B.1.)

C. The *Lowrey-Ogawa* combination renders claims 1, 4, 5, 8–12, 14, and 16 obvious

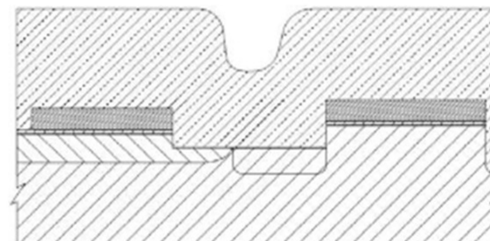
As explained in Section V.B, *Lowrey* teaches every limitation of the challenged claims except trench isolation. A POSITA would have understood that *Ogawa*'s trench isolation was a known substitute for *Lowrey*'s LOCOS isolation.. (Ex. 1004, ¶163; *see also* Ex. 1009, 1:31–2:24; Ex. 1011, 4:8–16; Ex. 1012, 3:3–10; Ex. 1013, 5:56–67; Ex. 1014, 22:49–52; Ex. 1015, Title, 1:7–10, 2:53–57, 4:14–23, Figs. 12, 13.) The combined teachings discussed in this section refer to the teachings of *Lowrey*, with its LOCOS isolation replaced by *Ogawa*'s trench isolation.



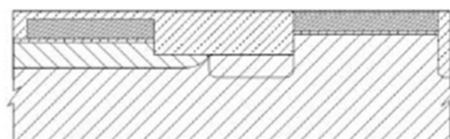
EX1017 (*Lowrey*), FIG. 3

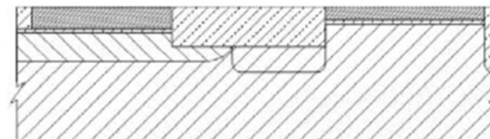


Trench Etch & Channel-Stop Implant



Resist Removal & Trench Filling





Planarization[10]

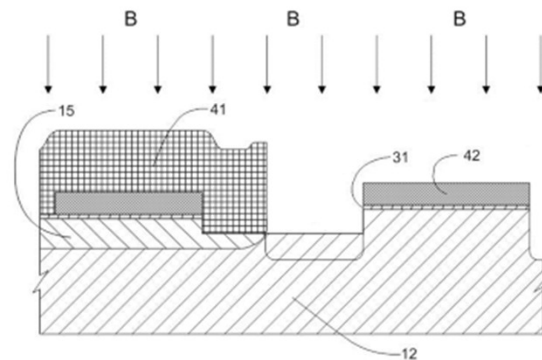
Nitride Removal

Petitioner's Reply, Paper 21, pp. 21-22

107. At this point of *Lowrey*'s illustrated embodiment, the isolation regions start to form. The first step is to prepare a channel stop region 41 after removing the exposed portions of the second nitride layer 32. (*Lowrey* at 8:21–30, FIG. 4.) That is followed by forming the LOCOS isolation. (*Lowrey* at 8:31–35, FIG. 5.) To integrate STI, a person of ordinary skill in the art would have immediately recognized STI formation can be done here in the alternative. I note, for example, that in FIG. 3 of *Lowrey* a pad oxide and nitride layer are already present. The well-known STI processes I described in Section VII.A begin the same way. For example, *Noble*'s FIG. 9 and *Ogawa*'s Fig. 4(c) are formed the same way, although

Exhibit 1057, Declaration of Dr. Banerjee, ¶107

they use a polysilicon polish/etch stop layer instead of a nitride polish/etch stop layer. As I explained in Section VII.A, both polysilicon and silicon nitride were well-known options available to a person of ordinary skill in the art, and either could be used (as could any number of other materials). In other words, a person of ordinary skill in the art would have immediately recognized that FIG. 3 of *Lowrey* is suitable for a trench etch. A person of ordinary skill in the art would have also recognized that the channel stop implant should be performed after the trench is defined.[11] This modification to the *Lowrey* process is illustrated below.



[11] I do not agree with Dr. Schubert that non-uniformity at the bottom of the trench would enhance leakage currents. *Lowrey* itself discloses a non-planar LOCOS isolation with non-uniformity at the bottom of the isolation region. Using STI with non-uniformity at the bottom of the trench would be no different and would not have deterred a person of ordinary skill in the art from this solution.

Exhibit 1057, Declaration of Dr. Banerjee, ¶107

384. Layer **62** is made of "oxide" (e.g. thermal oxidation) and layer **71** is also made of "oxide" (e.g. chemical vapor deposition), where "oxide" refers to silicon dioxide or SiO_2. That is, both layers, **62** and **71**, are made of the same material, "oxide". Subsequently, the two layers are subjected to an anisotropic etch to form a single sidewall spacer **81**:

> Referring now to FIG. 8, first spacer oxide layer **71** and mini-spacer oxide layer **62** are etched with a first anisotropic etch, then optionally etched once again with a first isotropic etch to form a first set of sidewall spacers **81** for N-channel transistor gates **56**, N-channel interconnects **57** and the portion of polysilicon layer **53** which blankets the P-channel regions."

Exhibit 1017, 9:6-12.

Exhibit 2012, Declaration of Dr. Schubert, ¶384

IPR2016-01246, IPR2016-01247
Patent 7,126,174 B2

Patent Owner cites it. Exhibit 2026 is further irrelevant because it bears a date of January 2008 and significantly post-dates the invention, providing only "impermissible . . . later knowledge about later art-related facts." *Hogan*, 559 F.2d at 605. The Sample Report provides analysis of a "45 nm process," which did not exist at the time of alleged invention. *See, e.g.*, EX1054 at 25 (showing the state-of-the-art was 350 to 250 nm).

IPR2016-01246, IPR2016-01247
Patent 7,126,174 B2

proposition, "The complexity of integrated circuit fabrication is appreciated by the technical community and widely supported by the technical literature." Ex. 2001 & 2011 at ¶ 53. The complexity of IC fabrication and the technical community's recognition of that premise are not at issue in these proceedings, making these references irrelevant.

The citations to Exhibits 2013–2019 are cited merely to support the idea that semiconductor fabrication is complex or, as Dr. Schubert puts it, that "the complexity of integrated circuit fabrication was appreciated by the technical community and widely supported by the technical literature." Ex. 2012 at ¶ 61. The complexity of IC fabrication and the technical community's recognition of that premise are not at issue in these proceedings, making these references irrelevant.