

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,  
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,  
Patent Owner.

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Case IPR2016-01246<sup>1</sup>  
Patent 7,126,174 B2

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**PETITIONER'S MOTION TO EXCLUDE EVIDENCE  
UNDER 37 C.F.R. § 42.64(c)**

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<sup>1</sup> Case IPR2016-01247 has been consolidated with this proceeding.

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## I. Introduction

For the reasons discussed below, Petitioner TSMC hereby moves to exclude the following evidence under 37 C.F.R. § 42.64(c):

Exhibit	Description
2001	Declaration of Dr. E. Fred Schubert, Ph.D. in support of Patent Owner's Preliminary Response filed in IPR2016-01246 on October 5, 2016
2002	Schematic illustration of the Chemical Mechanical Polishing process from Steigerwald, Murarka, and Gutmann, <i>Chemical Mechanical Planarization of Microelectronic Materials</i> (1997).
2003	Schematic illustration of the Chemical Mechanical Polishing process from the Motorola Company. SCSolutions.com. Accessed September 30, 2016. <a href="http://www.scsolutions.com/chemical-mechanicalplanarization-cmp-controllers-0">http://www.scsolutions.com/chemical-mechanicalplanarization-cmp-controllers-0</a>
2004	Photograph of a Chemical Mechanical Polishing Tool from the Applied Materials Company. BusinessWire.com. Accessed October 5, 2016. <a href="http://www.businesswire.com/news/home/20040711005007/en/Applied-Materials-Revolutionizes-Planarization-Technology-Breakthrough-Reflexion">http://www.businesswire.com/news/home/20040711005007/en/Applied-Materials-Revolutionizes-Planarization-Technology-Breakthrough-Reflexion</a>
2005	Troxel, Boning, McIlrath "Semiconductor Process Representation." <i>Wiley Encyclopedia of Electrical and Electronics</i> , pp. 139 –147 (1999).
2006	U.S. Patent No. 6,052,319 to Jacobs
2007	U.S. Patent No. 6,952,656 to Cordova et al.
2008	Hunt, "Low Budget Undergraduate Microelectronics Laboratory." <i>University Government Industry Microelectronics Symposium</i> , pp. 81-87 (2006).
2009	U.S. Patent No. 7,074,709 to Young
2010	Burckel, "3D-ICs created using oblique processing." <i>Advances in Patterning Materials and Processes XXXIII</i> , pp. 1–12 (2016).
2011	Declaration of Dr. E. Fred Schubert, Ph.D. in support of Patent Owner's Preliminary Response filed in IPR2016-01247 on October 7, 2016
2012	Declaration of Dr. E. Fred Schubert, Ph.D. in support of Patent Owner's Response filed in IPR2016-01246 on March 24, 2017.
2013	Thompson, L. F. "An Introduction to Lithography." <i>Introduction to Microlithography</i> , ACS Symposium Ser., American Chemical Society, pp. 1–13 (1983).
2014	CA1275846 C to Roland et al.

<b>Exhibit</b>	<b>Description</b>
2015	U.S. Patent No. 5,314,843 to Yu et al.
2016	U.S. Patent No. 5,231,306 to Meikle et al.
2017	U.S. Patent No. 4,529,621 to Ballard.
2018	U.S. Patent No. 5,310,624 to Ehrlich.
2019	U.S. Patent No. 5,097,422 to Corbin, II et al.
2021	U.S. Patent No. 4,952,524 to Lee et al.
2026	“Structural Analysis Sample Report” downloaded from <a href="https://www.chipworks.com/TOC/Structural_Analysis_Sample_Report.pdf">https://www.chipworks.com/TOC/Structural_Analysis_Sample_Report.pdf</a> (2008).
2027	U.S. Patent No. 4,776,922 to Bhattacharyya et al.
2028	Subbanna, S.; Ganin, E.; Crabbé, E.; Comfort, J.; Wu, S.; Agnello, P.; Martin, B.; McCord, M.; Newman, H. Ng. T.; McFarland, P.; Sun, J.; Snare, J.; Acovic, A.; Ray, A.; Gehres, R.; Schulz, R.; Greco, S.; Beyer, K.; Liebmann, L.; DellaGuardia, R.; Lamberti, A. “200 mm Process Integration for a 0.15 $\mu\text{m}$ Channel-Length CMOS Technology Using Mixed X-Ray / Optical Lithography.” <i>Proceedings of 1994 IEEE International Electron Devices Meeting</i> , pp. 695–698 (1994).
2029	Chung, J.; Jeng, M.-C.; Moon, J.E.; Wu, A.T.; Chan, T.Y.; Ko, P.K.; Hu, Chenming. “Deep-Submicrometer MOS Device Fabrication Using a Photoresist-Ashing Technique.” <i>IEEE Electron Device Letters</i> , Vol. 9, No. 4, pp. 186–188 (1988).
2030	Tanaka, Tetsu; Suzuki, Kunihiro; Horie, Hiroshi; Sugii, Toshihiro. “Ultrafast Low-Power Operation of p <sup>+</sup> -n <sup>+</sup> Double-Gate SOI MOSFETS.” 1994 Symposium on VLSI Technology Digest of Technical Papers, pp. 11–12 (1994).
2032	Kaufman, F. B.; Thompson, D. B.; Broadie, R. E.; Jaso, M. A.; Guthrie, W. L.; Pearson, D. J.; and Small, M. B. “Chemical-Mechanical Polishing for Fabricating Patterned W Metal Features as Chip Interconnects.” <i>Journal of The Electrochemical Society</i> , Vol. 138, No. 11, pp. 3460–3465 (1991).
2033	Landis, H.; Burke, P.; Cote, W.; Hill, W.; Hoffman, C.; Kaanta, C.; Koburger, C.; Lange, W.; Leach, M.; and Luce, S. “Integration of chemical-mechanical polishing into CMOS integrated circuit manufacturing.” <i>Thin Solid Films</i> , Vol. 220, No. 1–2, pp. 1–7 (1992).

**II. The Board should exclude paragraphs 33–159 of Patent Owner’s Exhibit 2001, paragraphs 33–149 of Patent Owner’s Exhibit 2011, and paragraphs 4–10 and 35–458 of Patent Owner’s Exhibit 2012 as unreliable expert testimony.**

The Board should exclude paragraphs 33–159 of Patent Owner’s Exhibit 2001, paragraphs 33–149 of Patent Owner’s Exhibit 2011, and paragraphs 4–10 and 35–458 of Exhibit 2012 because they contain unreliable testimony under Fed. R. Evid. 702 and *Daubert v. Merrell Dow Pharm., Inc.*, 509 U.S. 579 (1993). Petitioner objected to Exhibits 2001 and 2011 in objections dated January 19, 2017. Paper 13, at 2–3. Petitioner objected to Exhibit 2012 in objections dated March 31, 2017. Paper 16, at 3–4. Patent Owner relies extensively on Exhibits 2001 and 2011 throughout its Preliminary Response (Paper 7), and relies extensively on Exhibit 2012 throughout its Response (Paper 14).

Under Rule 702, an expert must be qualified in the area about which he testifies. “[T]he expert’s scientific, technical, or other specialized knowledge [must] help the trier of fact to understand the evidence or to determine a fact in issue.” Fed. R. Evid. 702(a). Because Dr. Schubert is not qualified to opine on shallow trench isolation in silicon MOSFET devices, the Board should not consider the opinions he expressed in paragraphs 33–159 of Patent Owner’s Exhibit 2001, paragraphs 33–149 of Patent Owner’s Exhibit 2011, or paragraphs 4–10 and 35–458 of Exhibit 2012.

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