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Segawa et al.

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(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

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(65) **Prior Publication Data**

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Related U.S. Application Data

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.⁷** **H01L 29/40**

(52) **U.S. Cl.** **257/774**

(58) **Field of Search** 257/304, 510,
257/774, 311

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,578,128 A 3/1986 Mundt et al.
4,966,870 A 10/1990 Barber et al.
5,177,028 A 1/1993 Manning
5,196,910 A 3/1993 Moriuchi et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP 0234988 A1 4/1987
EP 0 243 988 11/1987

(Continued)

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(57) **ABSTRACT**

An isolation which is higher in a stepwise manner than an active area of a silicon substrate is formed. On the active area, an FET including a gate oxide film, a gate electrode, a gate protection film, sidewalls and the like is formed. An insulating film is deposited on the entire top surface of the substrate, and a resist film for exposing an area stretching over the active area, a part of the isolation and the gate protection film is formed on the insulating film. There is no need to provide an alignment margin for avoiding interference with the isolation and the like to a region where a connection hole is formed. Since the isolation is higher in a stepwise manner than the active area, the isolation is prevented from being removed by over-etch in the formation of a connection hole to come in contact with a portion where an impurity concentration is low in the active area. In this manner, the integration of a semiconductor device can be improved and an area occupied by the semiconductor device can be decreased without causing degradation of junction voltage resistance and increase of a junction leakage current in the semiconductor device.

81 Claims, 21 Drawing Sheets

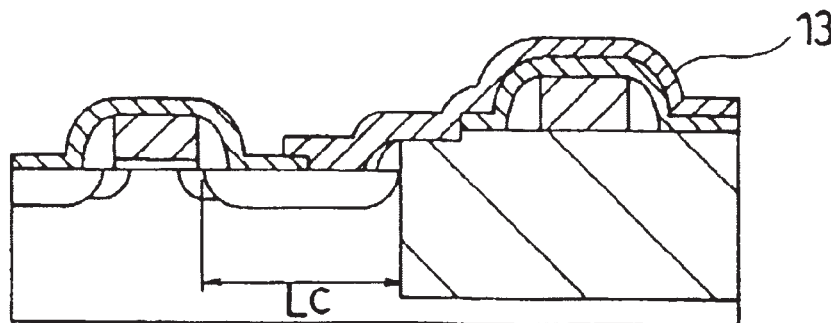


Exhibit 2076

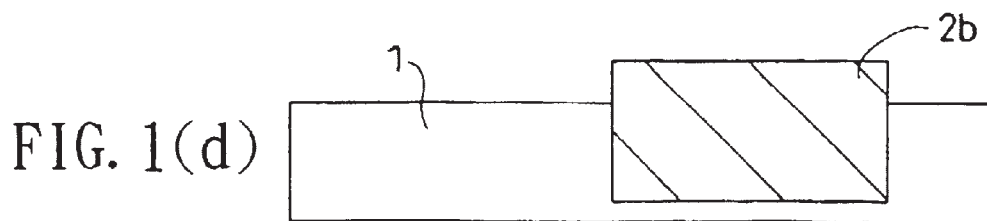
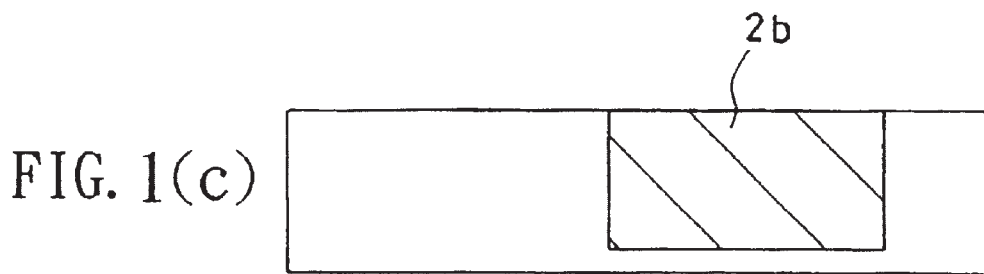
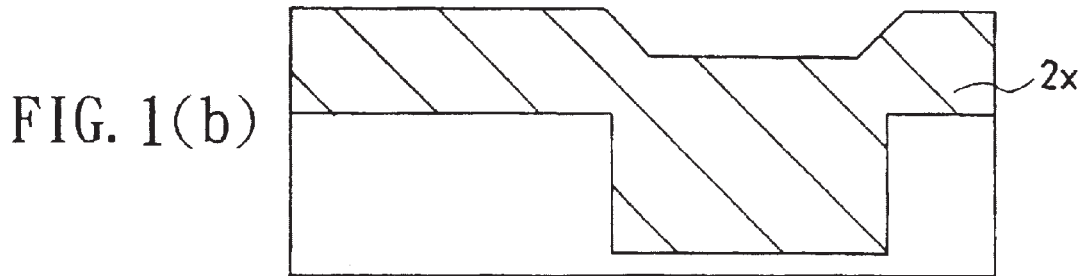
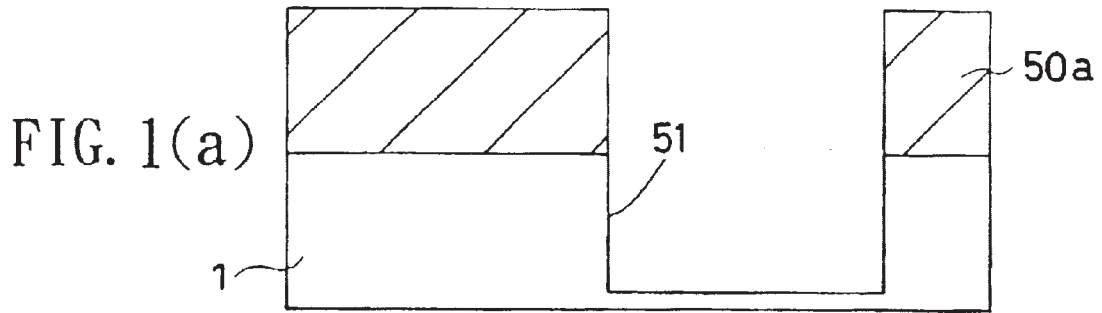
U.S. PATENT DOCUMENTS

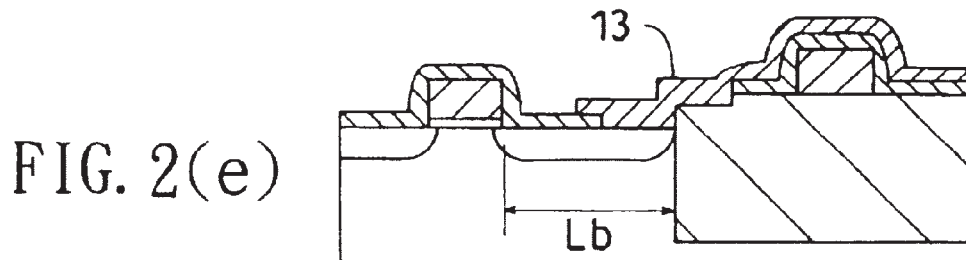
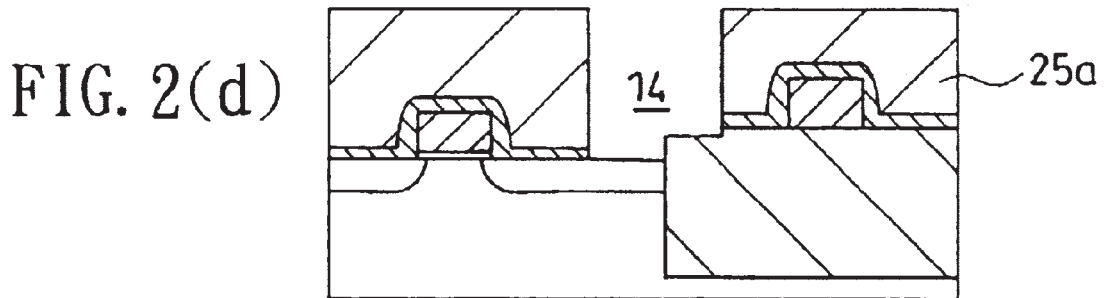
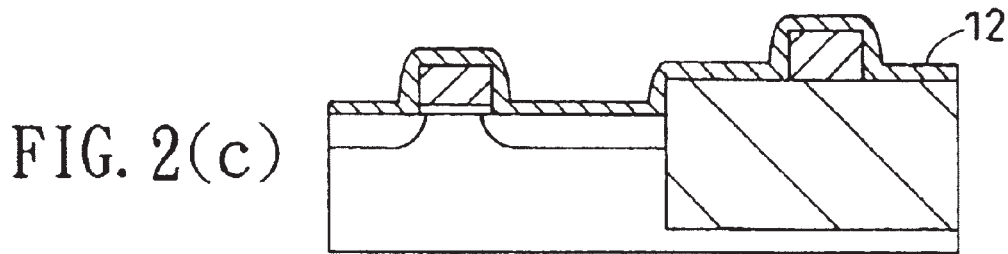
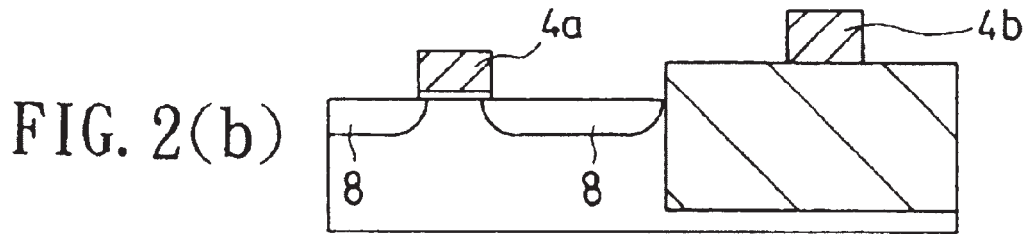
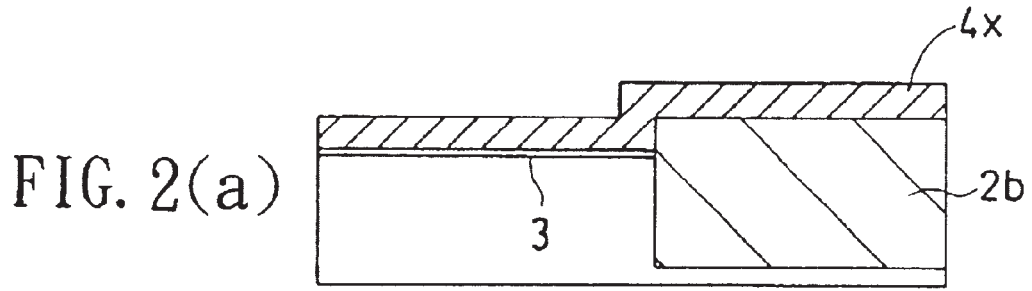
5,286,674 A 2/1994 Roth et al.
5,319,235 A 6/1994 Kihara et al.
5,384,281 A 1/1995 Kenney et al.
5,393,708 A 2/1995 Hsia et al.
5,397,910 A 3/1995 Ishimaru
5,401,673 A 3/1995 Urayama
5,413,961 A 5/1995 Kim
5,433,794 A 7/1995 Fazan et al.
5,497,016 A 3/1996 Koh
5,521,422 A 5/1996 Mandelman et al.
5,561,311 A 10/1996 Hamamoto et al.
5,777,370 A 7/1998 Omid-Zohoor et al.
5,804,862 A * 9/1998 Matumoto 257/396
6,022,781 A 2/2000 Noble, Jr.
6,281,562 B1 8/2001 Segawa et al.

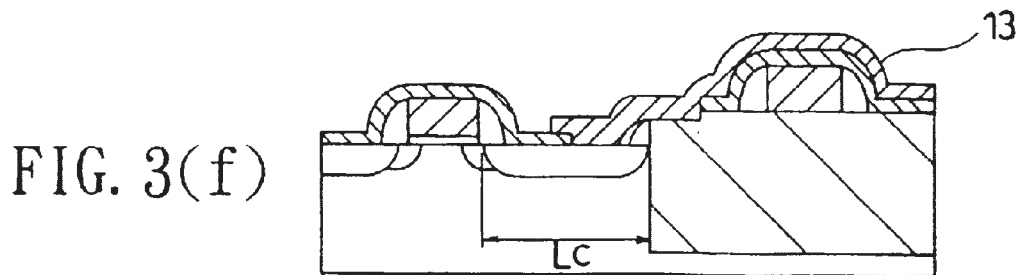
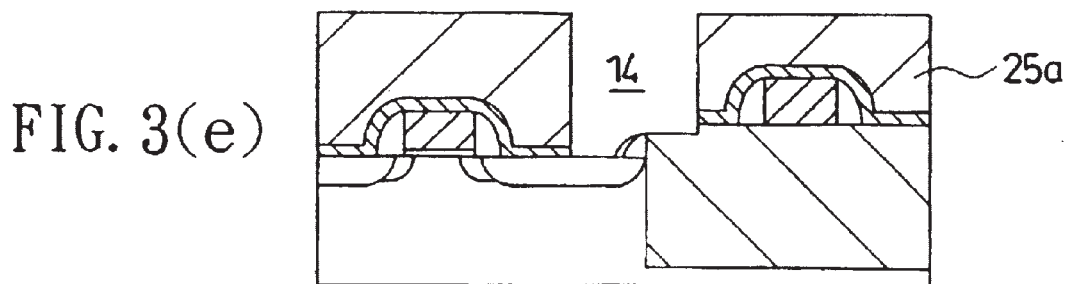
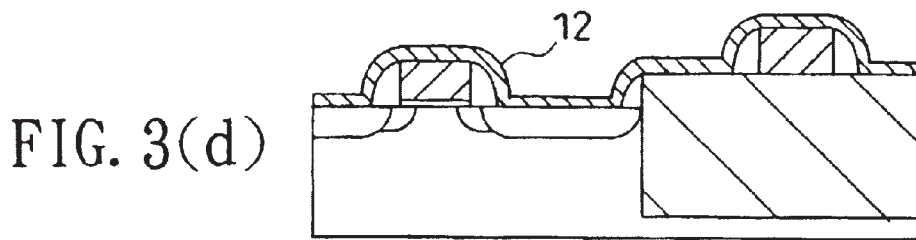
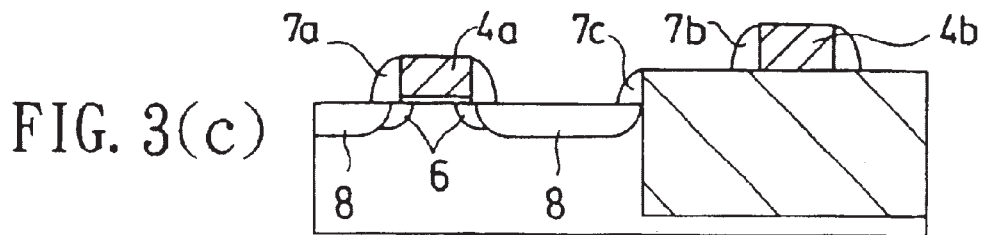
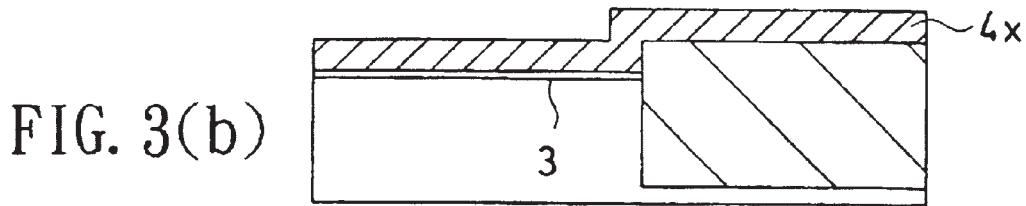
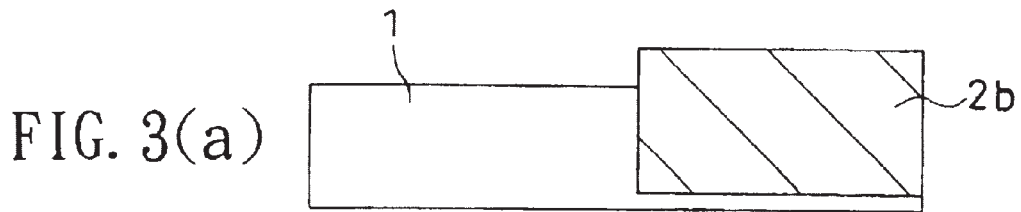
FOREIGN PATENT DOCUMENTS

EP 0 513 639 11/1992
EP 0 706 206 A2 4/1996
JP 59181062 A 10/1984
JP 62-85461 4/1987
JP 03079033 A 4/1991
JP 4-48647 2/1992
JP 4-68564 3/1992
JP 4-305922 10/1992
JP 6-45432 2/1994
JP 6-163843 6/1994
JP 7-273330 10/1995
JP 09162392 A 6/1997

* cited by examiner







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