A NEW PLANARIZATION TECHNIQUE, USING A COMBINATION OF RIE AND CHEMICAL MECHANICAL POLISH (CMP)

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ABSTRACT

In this paper a new planarization technique for vari able size and pattern factors is presented. It is demonstrated that by the combination of RIE and Chemical Mechanical Polish (CMP), the process window is improved to an extent that the planarization becomes a reality. This technique is applied in the Shallow Trench Isolation (STI, (1)) process which is used in 16 Mb DRAM technology (2). to achieve 0.5 μm isolation/device dimensions. By a proper combination of RIE and CMP processes, the fundamental problem of tolerance accumulation from deposi tion and etch back of large film thicknesses is avoided. Excellent planarization is achieved in different areas of DRAM chip with varying isolation sizes and pattern factors, including the deep trench integration. High gate oxide breakdown yield (comparable to LOCOS isolation), which is indicative of the planarization low defect density is dem onstrated.

INTRODUCTION

Planarization is rapidly becoming one of the key components in the realization of scaled, high density / high performance VLSI circuits. With lithography advancements into the 0.5 μm regime and beyond, planarization is needed to achieve lithography limited dimensions in key areas such as isolation (1) and metallization.

Planarization of the variable size and pattern factor trench isolation, represents one of the most demanding process control requirements. The reason is that in the traditional resist planarization and RIE etch back process (3) , the deposition and etch back tolerances associated with large film thicknesses are cumulative. Also, since the etch rate ratio of the trench fill material and the photoresist should be close to one, any non-planarity of the resist is replicated into the final planarized surface and thus adds directly to the process tolerance.

In this work a new planarization technique, using a combination of RIE and chemical mechanical polish (4) is presented which alleviates the above problems. The RIE + CMP is employed in such a manner that inevitable process non-uniformities in intermediate steps do not operate cumulatively, as well as reducing the sensitivity to the process tolerances. Two distinct features of the CMP, which are: 1) the averaging effect of the removal rate (polish rate is an average over all the exposed regions), and 2) the fast removal rate of the small elevated features (spikes) are demonstrated and utilized.

RIE + CMP PLANARIZATION PROCESS AND RESULTS

Schematic cross sections of variable size shallow trench isolation before and after planarization are shown in Fig.1. After isolation photo resist definition, the nitride/pad oxide and silicon (trench) are etched, followed by CVD oxide deposition (Fig.1a). Subsequently, a block resist is patterned over large isolation area (down regions) to bring up the surface to about the same level as the active area. The block resist is then hardened, followed by planarizing resist spin and cure (Fig.1b). The planarization that follows must satisfy the following requirements for all isolation pattern factors and sizes (Fig.1c): 1) All oxide being cleared from the nitride surface, 2) Greater than zero nitride remaining on all active area, and 3) Field oxide surface being above the silicon surface after planarization (prior to nitride/pad oxide etch). For "RIE only" planarization, a one-to-one etch (oxide/resist) is used and the stack height to be etched back is typically over 1.5 μm. Therefore it is very difficult to achieve better than se veral 100 nm control of the final oxide thickness, even with small process tolerances. Non-idealities of the planarizing resist (Fig.1b) due to the resist viscous flow and shrinkage after cure, and due to variable pattern factors (global effect (5),(6)) also add directly to the process tolerances. These problems can be reduced significantly by using CMP in conjunction with the RIE etch-back.

In the RIE+CMP planarization, the RIE etch back is followed by CMP. In this process, the RIE is stopped be fore removing all the oxide from the nitride surface, in contrast to the "RIE only" planarization. The remaining oxide is then removed by the CMP. This ability widens the planarization window, by allowing some non-planarity after the RIE, which is eliminated by the subsequent polish step. One distinguishing feature of the CMP is that the removal rate is an average of the rates for the different ex posed materials. Therefore as the polishing removes the

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oxide over the nitride, once it reaches the nitride surface, the oxide removal rate becomes almost the same as the nitride removal rate, if the nitride is polished slower than the oxide. Therefore a selective CMP step, polishes the oxide over the nitride, with minimal oxide removal from the field. The contribution of the CMP step to the total process tolerance is therefore negligible. A polish rate ratio of about 5/1 (oxide/nitride) is used in this work.

Secondly, by the application of CMP, the RIE can be a multi-step process, ending with a step which etches the oxide faster than the photo-resist. This selectivity reduces

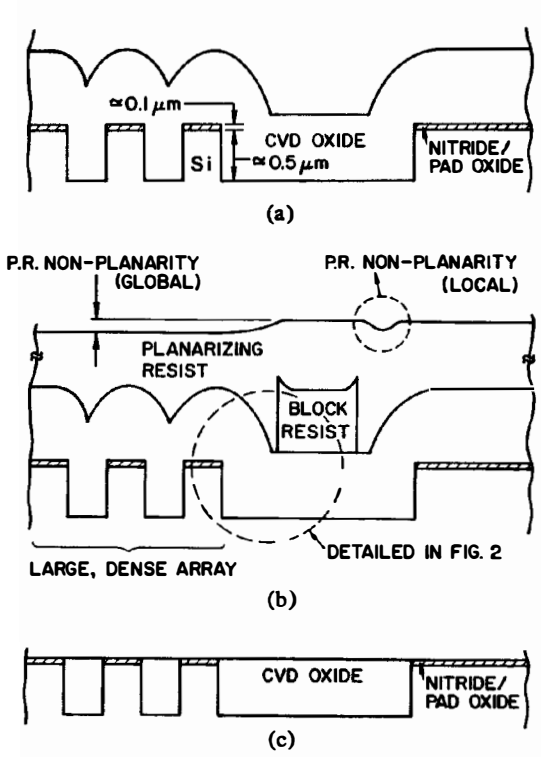


FIG.1 Variable size Shallow Trench Isolation (STI) schematic cross sections
(a) After CVD oxide conformal fill
(b) After block + planarizing resist
(c) After Planarization

the RIE sensitivity to the resist thickness/non planarity, and therefore improves the process window significantly as described below. Process simulated schematic cross sections before and after the RIE step with selective etch (from the circled area of Fig.1b) are shown in Fig.2a,b. In this simulation, a 3/1 RIE selectivity (oxide/resist) is used. The SEM cross section of a similar region with the same RIE selectivity is shown in Fig.2c (after the photo resist strip). It is shown that there is a spike present after the RIE. This spike is caused by the higher etch rate of the oxide relative to the resist (resist masking). By increasing the oxide/resist etch rate ratio, the spike height (dimension A in Fig.2b) increases while the dip in the oxide (dimension B in Fig.2b), which is caused by the resist non planarity, diminishes. For a "RIE only" planarization, dimension A

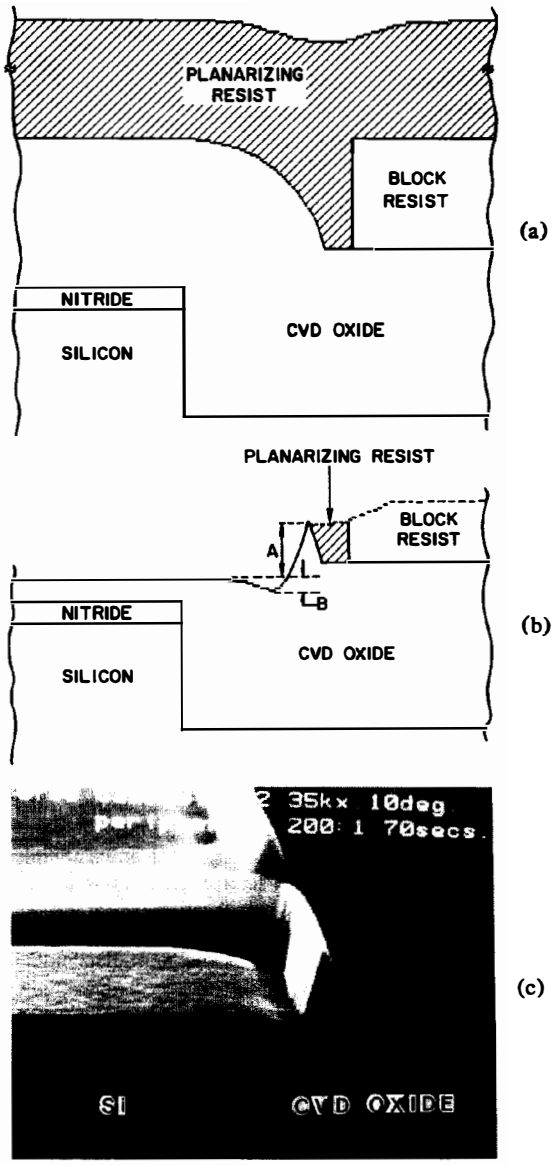


FIG.2 Cross sections before and after selective RIE step (oxide/resist etch rate ratio=3/1)
(a) Simulated cross section Before RIE
(b) Simulated cross section After RIE
(c): SEM cross section after selective RIE and resist strip

has to be almost zero and therefore the oxide dip (dimension B) can be large enough to consume a significant portion of the process window. Possible variations of the multi step RIE process include a first step which removes the resist very fast (for high throughput), and/or followed by a one to one oxide/resist etch to insure resist clearance from the oxide surface prior to the selective etch.

In the RIE+CMP planarization, the oxide spike (Fig.2c) is also removed by the CMP. This is due to another key feature of the CMP, which is the increased polish rate for small elevated features (spikes). This effect is experimentally demonstrated in Fig.3. A large area oxide step (width >100μm) with a height of about 100 nm is superimposed by a small area (width ≃4μm) spike with a height of about 300 nm. After 30 sec polish, the height of the narrow feature is reduced to about 40 nm (260 nm removal), while only 20 nm is removed from the large step. Therefore the polishing rate of the small feature in this case is more than 10 times faster than in the large area.

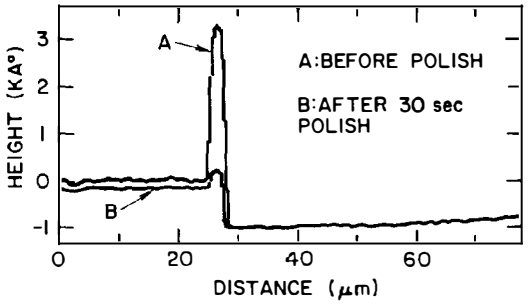
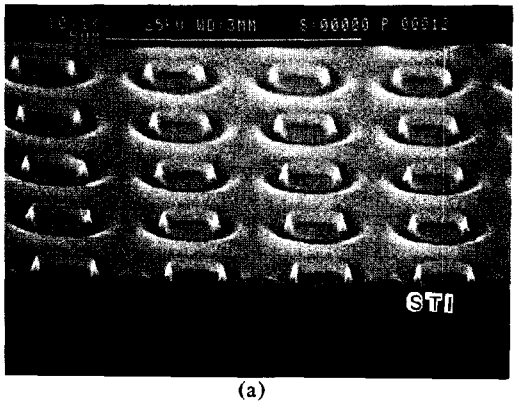


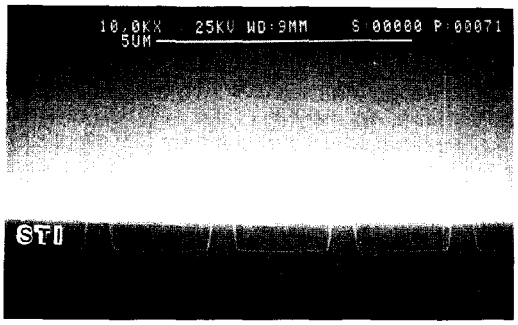
FIG.3 Measured oxide step heights before and after Chemical Mechanical Polish (CMP), demonstrating the fast removal rate of the small elevated features (spikes) by CMP

The CMP effectiveness in removing the spikes which are left by the selective RIE process, in a dense array region, is shown in Fig.4. It should be noted that the CMP alone (no RIE etch back step) is not a viable planarization alternative. The reason is the residual oxide which will be left in the middle of the large active area or arrays after polishing, as shown in Fig.5. The oxide which is removed by RIE in the RIE+CMP planarization, solves this problem (Fig.5).

The final planarization of different regions of a chip, with varying pattern factors and sizes, using RIE+CMP, is shown in Fig.6. Excellent planarization is achieved in all regions, including the DRAM array area, demonstrating the STI and deep trench integration. Gate oxide breakdown field histograms of 4 Mb arrays with STI and LOCOS isolation are shown in Fig.7a,b respectively (each data point represents one complete array) Each array contains large STI bounded gate oxide area (0.172854 cm^2) and perimeter (17.25125 m). The high breakdown yield of the STI



(a)



(b)

FIG.4 SEM cross sections of STI arrays
(a) After selective RIE, Before CMP
(b) After CMP

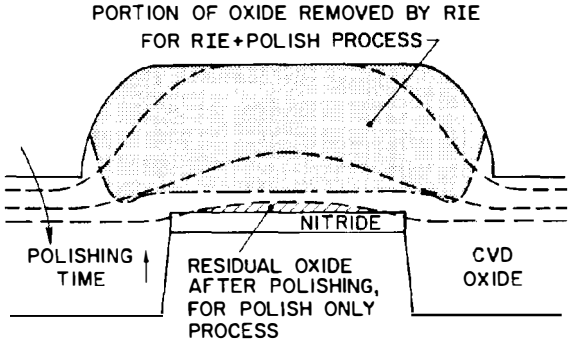


FIG.5 Schematic cross section, demonstrating the fundamental problem of the "CMP only" planarization. At the end of polishing (field oxide at the same level as the nitride surface), residual oxide is left in the middle of the active area. The oxide etch in the RIE+CMP planarization eliminates the formation of the residual oxide.

with RIE+CMP planarization (comparable to LOCOS isolation) demonstrates very low defect density from this process.

CONCLUSION

In summary, a planarization technique, using a combination of RIE and CMP, is presented for the first time. In this technique, the fundamental problems of independ ent RIE and CMP processes are largely avoided, resulting in excellent planarization with improved window for varying pattern factors and trench sizes. This planarization process is successfully applied to 16 Mb DRAM technology (1),(2).

ACKNOWLEDGEMENT

The authors wish to thank T.H. Ning, M.R. Polcari, P.E. Bakeman, A.S. Bergendahl, D.L. Critchlow and M.C. Hakey for many helpful discussions and D.V. Horak, H.Y. Ng for processing assistance. They also wish to acknowl edge IBM Yorktown Heights silicon facility and IBM Essex Junction TDL personnel for the hardware fabrication.

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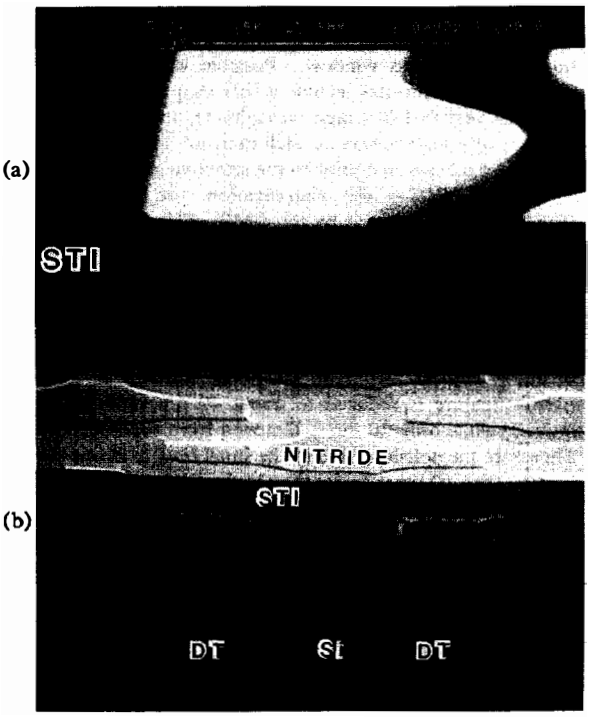

FIG.6 SEM cross sections of two regions of a DRAM chip with different isolation pattern factors and sizes, after RIE+CMP planarization
(a) Support circuit area
(b) Array area, including the deep trench (DT)

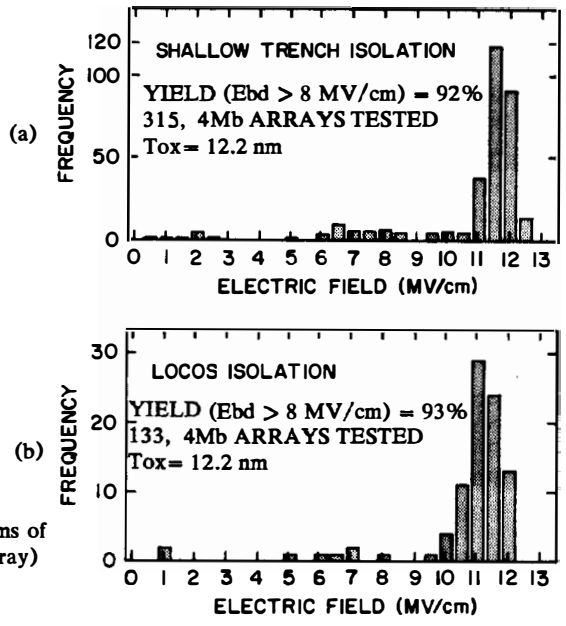

FIG.7 The gate oxide breakdown field histograms of 4Mb arrays (each measurement represents one array)
(a) STI, using RIE+CMP planarization
(b) LOCOS isolation