Highly Manufacturable Process Technology for Reliable 256 Mbit and 1 Gbit DRAMs

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Abstract

Ta_2O_5 dielectric on poly-Si cylinder capacitors, Chemical-Mechanical Polishing (CMP) planarization, pure W bit-line, and Al reflow were integrated into a highly manufacturable DRAM process technology. This technology provided larger process margin, higher reliability, and better design flexibility. In addition, the critical steps of the new process has been reduced by 25% of those of the conventional process. The manufacturability of the technology has been proven by applying it to 16Mbit density DRAMs with 256 Mbit design rule (0.28 μm).

Introduction

As the DRAM generation goes 256 Mbit and beyond, the DRAM fabrication process has become more and more complicated. This will cause the production cost of the high density DRAMs unacceptably high and will significantly degrade the device reliability. Thus, it is essential to develop a process technology that is simple and yet ensures high performance and high reliability.

We have developed a highly manufacturable process technology for 256 Mbit DRAMs and beyond. Process was simplified by employing a simple cell structure and metallizations with less complexity. Photolithography margin was significantly improved by realizing a better level of planarization. The main features of this process are Ta_2O_5 dielectric on poly-Si cylinder capacitors, CMP planarization, pure W bit-line, and Al reflow. This technology provided larger process margin, higher reliability, and better design flexibility.

Cell Architecture

Fig. 1 shows a schematic diagram of the DRAM cell we have implemented. Modified LOCOS isolation, W-polycide (WSi_2/poly-Si) word-line, and W bit-line were used. Fig. 2 shows the cross-sectional SEM micrograph of the memory cell. The KrF eximer laser lithography was used for patterning critical layers. The cell size is about 0.98 μm^2 with 0.28 μm design rule.

Unit Processes and Their Applications

A. Ta_2O_5 Capacitor

A CVD Ta_2O_5 dielectric film of 8.5 nm thickness was deposited on a poly-Si cylinder and followed by O_3-plasma treatment and dry-O_2 annealing. Thermally robust Ta_2O_5 capacitor was realized by forming the TiN/Poly-Si bilayer plate electrode [1]. Fig. 3 shows the capacitance and leakage characteristic as a function of the applied voltage. The oxide equivalent thickness (Toxeq) of 3.5 nm and the capacitance of 30 fF/cell was obtained. Low leakage current level was maintained even after high temperature thermal cycles of the full DRAM process.

B. Low Temperature ILD

O_3-TEOS USG/low temperature planarization replaced BPSG/reflow ILD (Inter-Layer Dielectric) to reduce the thermal budget, which improves device isolation and short channel properties of transistors. CMP achieved a perfect planarization of ILD between word-lines and bit-lines. It helped patterning bit-lines without using multilayer photoresist, resulting low defect density. Fig. 4 shows W lines patterned on the polished ILD. Carbon from the organic precursor of USG and mobile ions from the CMP chemistry could be potential contaminants. Threshold voltage of transistors, however, was not changed by replacing the BPSG/reflow ILD process with organic USG/CMP. Gate oxide integrity measured by TDDB did not also make much difference between the two groups (Fig. 5).

C. W Bit-Line

After opening bit-line contacts, about 30 nm thick Ti was deposited and rapid thermal annealed to form $TiSi_2$ on the

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exposed Si surface. The remained Ti, which was not reacted with Si, was stripped by wet-etch. Then TiN was deposited to a thickness of 30 nm by reactive sputtering. The TiN functions as a barrier metal, that prevents W from reacting with underlayer, and as a glue layer between W and oxide as well. Finally, about 80 nm of W was deposited by CVD and patterned by RIE.

The W bit-line widely extended the design flexibility in the core and periphery areas compared to the conventional W-polycide bit-line. This is because the W bit-line has a low sheet resistance and a feasibility of forming contacts to both N+ and P+ diffusion. As shown in Fig. 6(a), a thinner W bit-line has about one-quarter of sheet resistance of the thicker W-polycide. By the $TiSi_2$ salicidation on the active area and on the poly-Si landing pads before W bit-line deposition, all the bit-line contacts became low resistance metal-to-metal contacts. As a result, bit-line contacts have much lower resistance than that of W-polycide (Fig. 6 (b)-(d)).

D. Reflowed Al

Fig. 7 shows the first level interconnection with contact holes filled by Al reflow. Ti/TiN was used as the barrier metal. Overhang-free, conformal deposition profile at the contacts enhanced electromigration and stressmigration resistance [2] compared to the conventional Al deposition. Fig. 8 compares the surface roughness of non-reflowed and reflowed Al after forming gas anneal. High density of hillocks are observed on the non-reflowed surface, while almost none on the reflowed surface. It eliminated short-circuit failures between the first and the second metal lines.

CMOS Transistor Performance

LDD structure was used for both N- and P-channel MOS transistors. Transistors show satisfactory characteristics as summarized in Fig. 9. Thanks to the low thermal budget (65 minutes at 850°C equivalent) achieved by employing a low temperature ILD, the threshold voltage P-channel transistors vary less than 0.1 volt in the range of 0.3-3.0 μm gate length (Fig. 10).

DRAM Performance

Fully working 16 Mbit DRAM with 256 Mbit density was obtained by applying this technology. Fig. 11 shows the measured output wave forms of the fabricated 16 Mbit DRAM. The typical RAS access time is 48 ns.

Discussion

Table 1 compares the new process proposed in this paper with a conventional process. It is well known that deposition and dry-etch processes are the major sources of process induced particles and thus determine the device yield. As shown in Fig. 12, the number of deposition and dry-etch steps of the new process is 75% of those of the conventional process.

This technology can be scaled to the 1 Gbit DRAM generation with minor modifications, such as replacing LOCOS with trench isolation and adding hemispherical-grained poly-Si on cylinder capacitors.

References

[1] K.W. Kwon et al., Tech. Dig. of IEDM, 1993, p.53.

[2] C.S. Park et al., Proc. of VMIC, 1991, p.326.

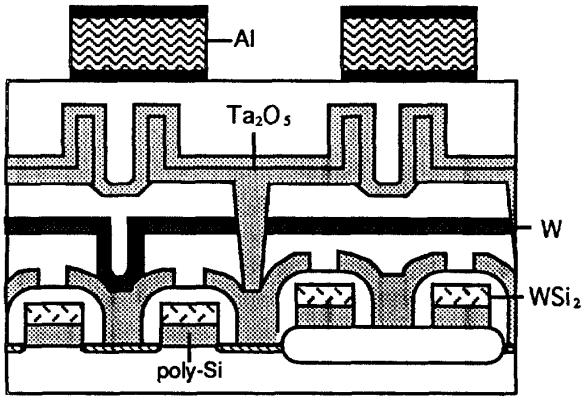

Fig. 1 Schematic cross-section of the DRAM cell.

Fig. 2 Cross-sectional SEM micrograph of the DRAM cell.

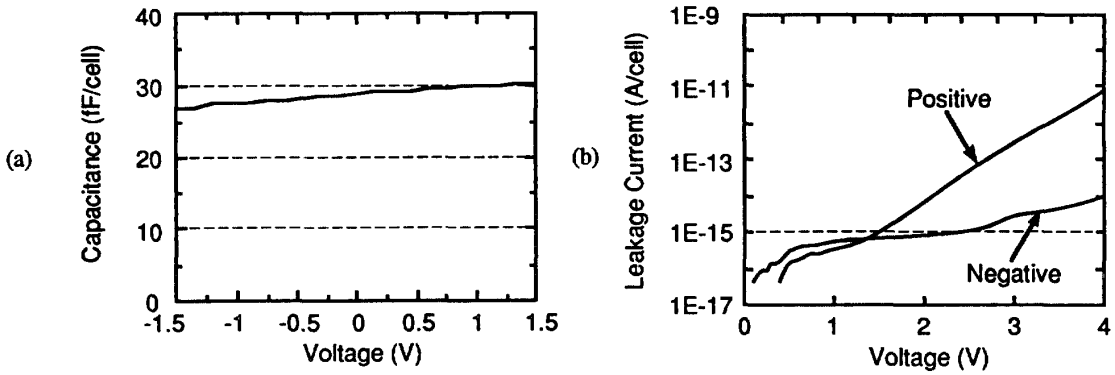

Fig. 3 (a) Capacitance and (b) leakage characteristics of Ta_2O_5 single cylinder capacitor as a function of applied voltage. Net capacitor area is about 3.2 μm^2/cell.

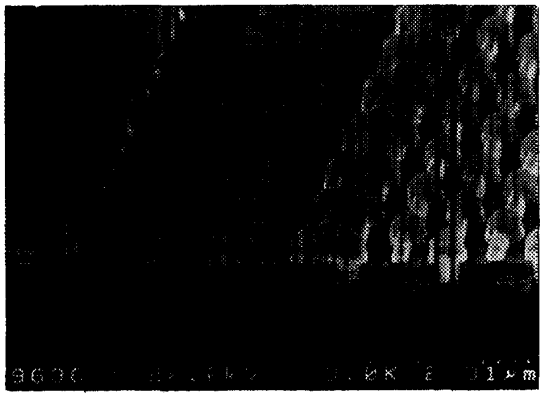

Fig. 4 Tungsten bit-line patterned on a polished USG surface. Bit-lines were RIE etched with a single layer photoresist mask.

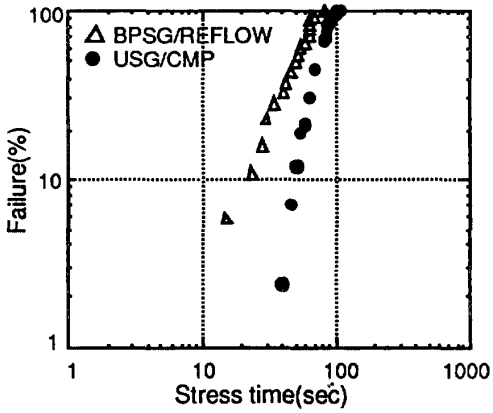

Fig. 5 Comparison of the gate oxide TDDB characteristics of (a) BPSG-flowed and (b) USG polished samples. Gate oxide thickness is 8 nm. Stress current density is about 50 mA/cm^2.

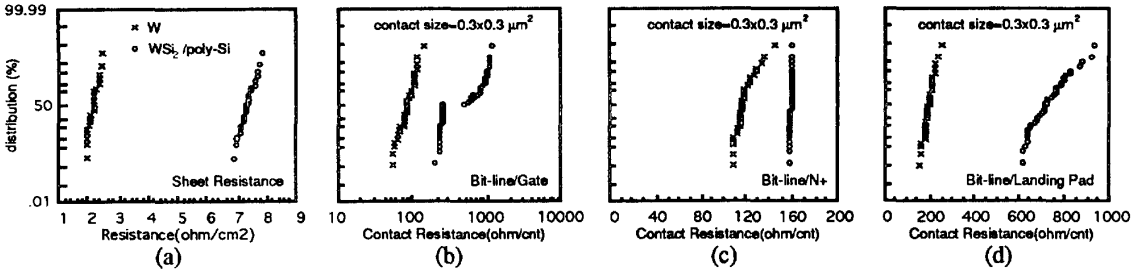

Fig. 6 Comparisons of W and W-polycide: (a) bit-line sheet resistance, (b) bit-line/tungsten policide gate, (c) bit-line/N+ substrate, and (d) bit-line/landing pad contact resistace. Thickness of tungsten is 80nm while tungsten silicide/poly Si is 150/50nm.

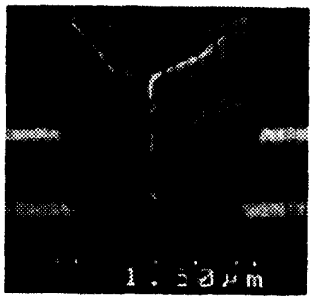

Fig. 7 Cross-sectional SEM of an Al alloy line formed by the reflow process.

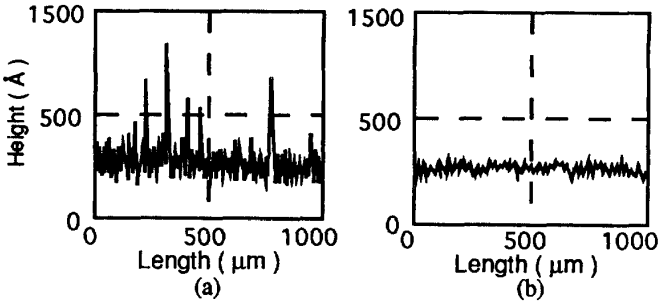

Fig. 8 Comparison of the hillock density on (a) non-reflowed and (b) reflowed Al alloy surfaces. Surface roughness was measured by surface profiler after forming gas anneal at 450°C for 30 min.

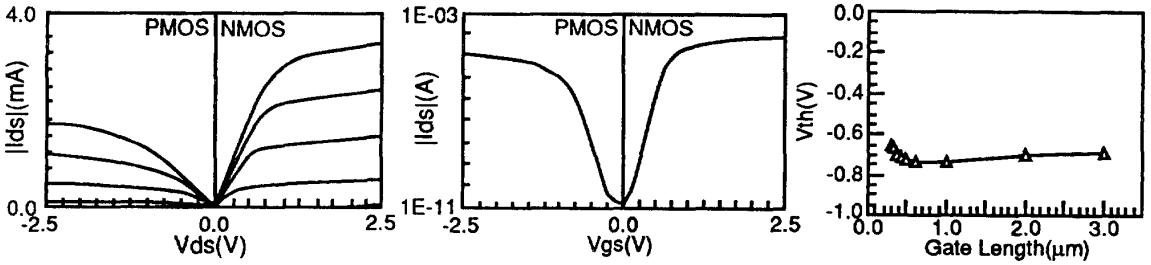

Fig. 9 (a) Ids-Vds and (b) Ids-Vgs characteristics of N-channel (W=10μm, L=0.4μm) and P-channel (W=10μm, L=0.4μm) MOS transistors. Vgs was varied from 0 to 2.5V for Ids-Vds curve. Vds =0.1V for Ids-Vgs curve.

Fig. 10 Variation of the threshold voltage of P-channel MOS transistors as a function of gate length.

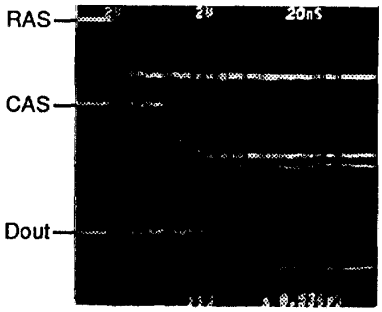

Fig. 11 Measured output wave forms of the 16M DRAM.

Table 1. Comparison of process steps between a conventional process and the new process.

	Conventional Process	New Process
1st ILD	BPSG/Reflow	USG/CMP
Bit-line	W-Polycide	W
Capacitor	5 fin/ONO	Single Cylinder/Ta_2O_5
2nd ILD	BPSG/Reflow	USG/Etch-Back
1st Metal	W-Plug/Al	Al-Reflow

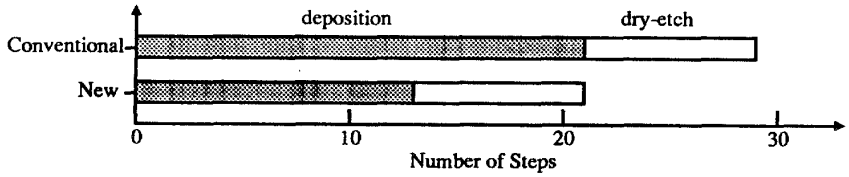

Fig. 12 Number of deposition and dry-etch steps of a conventional process and the new process.