A NEW BIRD'S-BEAK FREE FIELD ISOLATION TECHNOLOGY FOR VLSI DEVICES

Kei KUROSAWA, Tadashi SHIBATA and Hisakazu IIZUKA

Toshiba Research and Development Center,
Toshiba Corporation, Kawasaki, Japan

ABSTRUCT

A new field isolation technology ideal for VLSI devices has been developed incorporating a unique two step oxide-burying process. This technology is completely free from bird's beak formation which is particularly important for increasing the packing density. A near-perfect planar surface structure is also obtained. MOS devices fabricated by the new technology showed no thershold voltage increase due to the narrow channel effect for channel widths down to submicron region.

INTRODUCTION

The field isolation of device on silicon substrate is one of the most important process steps in the fabrication of integrated circuits. The widely-known LOCOS process[1] which uses silicon nitride as masks for selective oxidation has revealed several disadvantages as a process for future VLSI fabrication. The lateral oxidation under the nitride masks, for instance, creates so-called brid's beak,[2] resulting in a considerable reduction of packing density. Process-induced crystalline defects[3] and gate oxide failures due to "white ribbon",[4] both of which are associated with the LOCOS process, represent a difficult barrier for the development of VLSI devices.

The purpose of this paper is to present the newly developed field isolation technology which overcomes these difficulties. Since isolation is achieved by burying oxide into etched grooves formed in silicon substrates, the technology is called "BOX".[5]

In the BOX process, the grooves in the field region is completely filled up with SiO_2 using a two step oxide buring process. Since silicon substrates are not oxidized to form field oxide, the bird's beak length is exactly zero. This is particularly important for the density improvements of VLSI. The BOX structure is further characterized by its near-perfect planar surface which is also essential for fine patterning and high-reliability metallization. In this paper, the BOX process is described in detail and the electrical characteristics of test devices fabricated by BOX are discussed.

BOX TECHNOLOGY

The fabrication process of BOX is schematically outlined in Fig. 2. The active device areas on silicon wafer (P-type, 50 Ωcm) were covered with aluminum patterns, followed by the etching of silicon substrates in the field region. Reactive ion etching (RIE) employing CF_4 gas (21 cc/min) was used for the silicon etching. Borons were implanted using the aluminum patterns as masks.

These grooves were completely filled up with SiO_2 using the following two step oxide-burying technique. In the first oxide burying step, plasma-deposited SiO_2 was roughly filled into the engraved field region by the lift-off technique, leaving V-shaped grooves in the periphery. In the lift-off technique, we used the preferential etching characteristics of plasma deposited SiO_2 to buffered HF solution occuring at steep side walls. The SEM picture in Fig. 2 demonstrates the preferential etching of plasma deposited SiO_2 which occured at edges of the active region. As is clearly seen in the picture, the SiO_2 is completely removed from the steep side walls. Then the SiO_2 on top of aluminum mask was lifted-off by etching the aluminum mask. The boiling in H_2O_2 + H_2SO_4 (1:3) solution was employed for the etching of aluminum.

The remaining V shaped grooves were buried with SiO_2 in the second step. For burying SiO_2 into the V-grooves, surface levelling technique using spin-coated resist was utilized after the deposition of CVD SiO_2. The resist and CVD SiO_2 layers were simultaneously etched by RIE with equal etching rates for resist and SiO_2. After smoothing the oxide surfaces, the remaining oxide on the active device region was removed by solution etching.

After oxide-burying processes were completed, test devices were fabricated using a conventional n-channel MOS technology. For comparision, test devices were also fabricated by conventional LOCOS process using the same set of masks.

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RESULTS AND DISCUSSION

Figure 3 shows the current-voltage characteristics of test transistors fabricated by LOCOS and BOX. Cross sectional views of the transistors along the channel width direction are also shown by SEM pictures. As is clearly seen in the figure, a submicron transistor with a channel width exactly equal to the mask dimension (0.9 μm) is realized by BOX technology. While the transistors fabricated by LOCOS have collapsed due to the bird's beak when the channel width are smaller than 1 μm on the mask. In the optimized LOCOS the bird's beak length is minimized to about 0.5 μm.[6]

Figure 4 shows the threshold voltage as a function of the channel width defined by mask. The threshold voltage of LOCOS samples increases significantly when the channel width is reduced below 2 μm. This threshold increase is a result of the narrow channel effect which is further enhanced by the bird's beak and the lateral diffusion of field borons. On the other-hand, in the case of BOX sample, the threshold voltage is almost constant for channel widths down to submicorn region.

Figure 5 shows reverse current-voltage characteristics of p-n junction diode. It is clearly seen in the figure that the reverse current level of the BOX sample is as low as that of the LOCOS sample. In LOCOS sample, the degradation in reverse characteristics is often observed caused by the crystalline defects induced in the periphery of field oxide.

Figure 6 shows the field boron dose dependence of the field inversion voltage. It indicates that about one order of magnitude larger dose is required for LOCOS since the implanted borons are lost into field oxide during field oxidation.

One of the difficulties associated with the BOX structure is a parasitic channel formation occuring at the side walls of silicon. This results in a channel leakage current of the order of $\sim 10^{-6}$A. One example of the degraded subthreshold characteristics is demonstrated in Fig. 7. The leakage current appears as a hump superimposed on the subthreshold characteristics of the transistor. As is clearly seen in the figure, this effect has been successfully eliminated by the side wall boron implantation. The boron implantation to the side walls near perpendicular to the wafer surface has been carried out in the following way. Borons of $\sim 10^{13}$ cm^{-2} implanted to the field region prior to the formation of grooves in silicon substrates. The lateral penetration of implanted borons due to the ion straggle introduced enough amount of impurities in the substrate under the aluminum mask which prevented the paracitic channel formation at the side walls.

SUMMARY

The new field isolation technology, BOX has been described. This process is completely free from bird's beak formation, which is essential for high device density. According to the simple estimation of dynamic memory cell density,[7] BOX achieves an 80% density improvement as compared to the LOCOS under 1.0 μm layout rules. Near-planar topography is also obtained. This is very important for fine patterning and high reliability of metallization. Furthermore, transistors fabricated by BOX show no threshold voltage increase for channel widths even below 1 μm.

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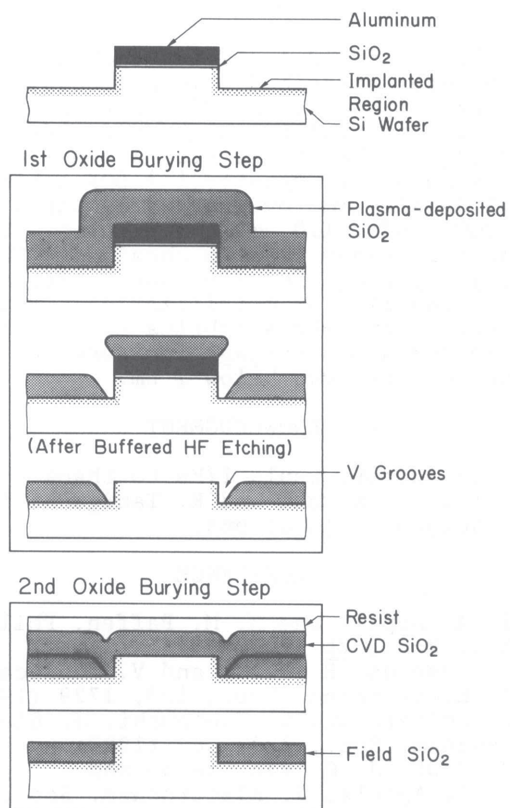


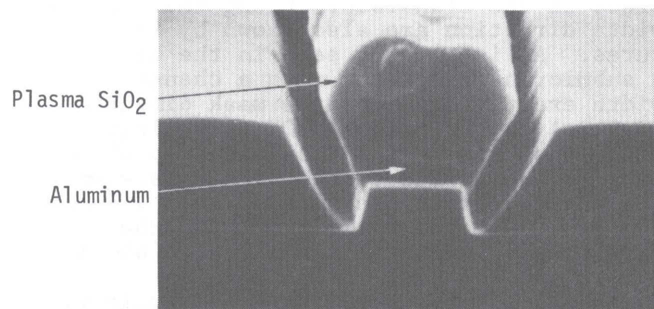
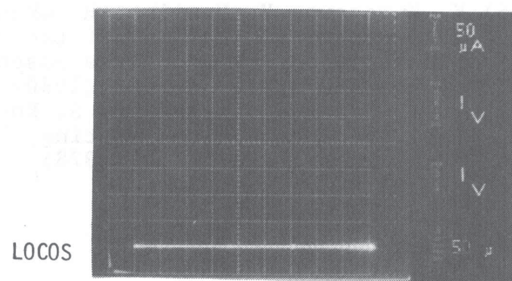
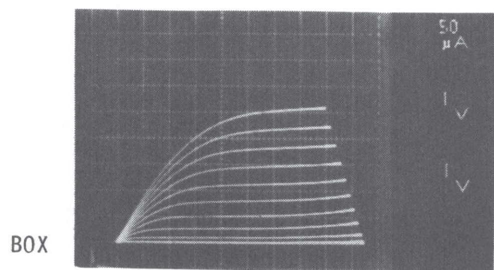


Fig. 2. The SEM picture which explains the 1st oxide-burying step. The plasma-deposited SiO_2 on steep side walls is preferentially etched by buffered HF solution.

Fig. 1. Fabrication process steps of BOX.





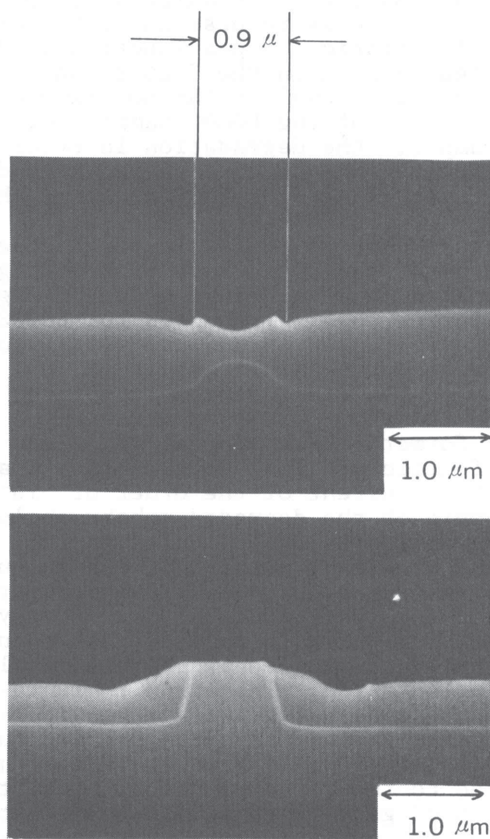


Fig. 3. Current-voltage characteristics of transistors fabricated by LOCOS and BOX. In the case of LOCOS, the active device area has disappeared due to the bird's beak, while BOX realizes a transistor with identical dimensions to the mask.

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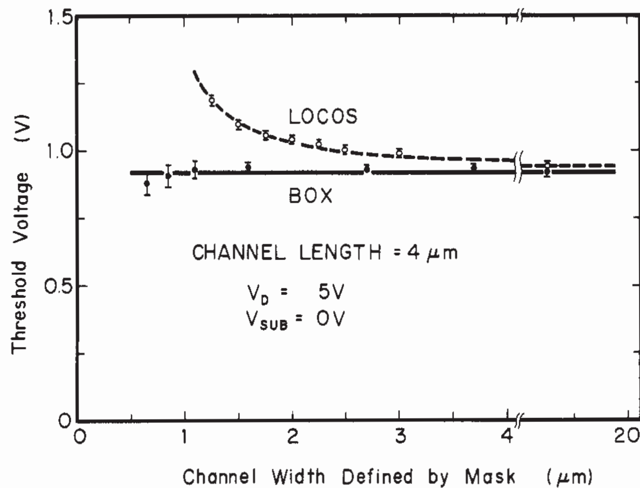

Fig. 4. Threshold voltage as a function of channel width defined by the mask. Negligible narrow channel effects are seen in BOX samples.

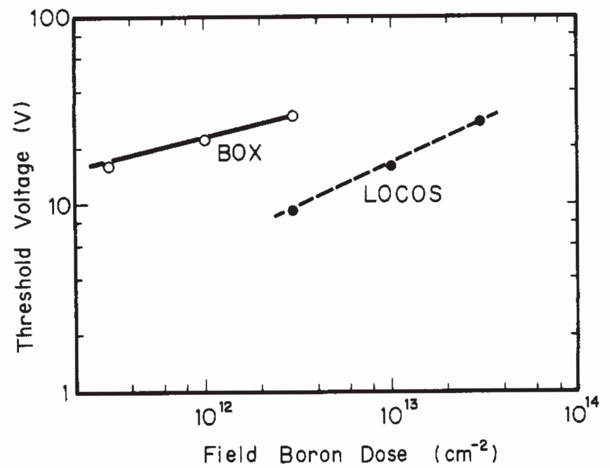

Fig. 6. Field inversion voltage as a function of field boron dose. Channel length of the field transistors is 20 μm.

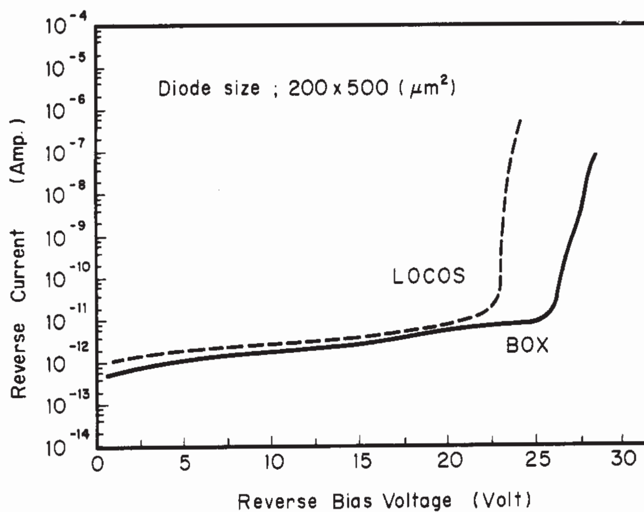

Fig. 5. Reverse current-voltage characteristics of p-n junction diode.

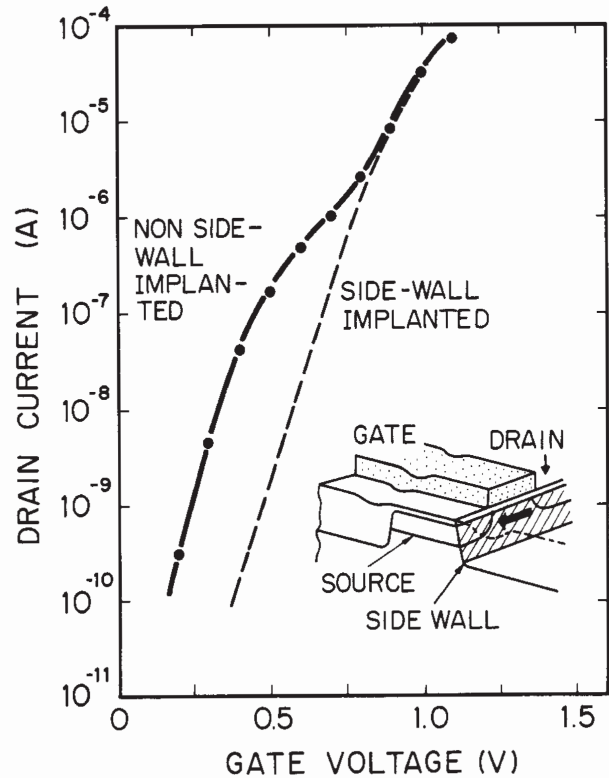

Fig. 7. Subthreshold characteristics of a transistor with W/L=20 μm/3 μm. (V_{sub}=0V, V_D=5 V.) Parasitic channel formation occuring at the side-walls of silicon results in a increased leakage current of the order of 10^{-6}A. The side-wall boron implantation successfully eliminated the leakage current.

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