OXIDE-FILLED TRENCH ISOLATION PLANARIZED USING CHEMICAL/MECHANICAL POLISHING

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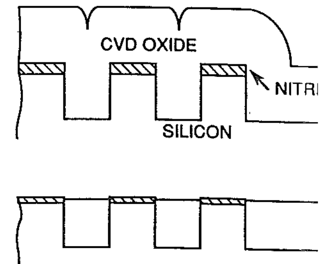
An oxide-filled shallow trench isolation process is described, which includes a chemical/mechanical polishing (CMP) step to planarize the CVD oxide used to fill the trenches. The stringent leveling requirements for this application are discussed, and a newly developed CMP process is demonstrated with a leveling length of several mm. The isolation process has been applied to both CMOS and bipolar devices with good results.

INTRODUCTION

Shallow trench isolation (STI) filled with CVD oxide is attractive for scaled ULSI, because the encroachment and stress problems associated with field oxide growth are largely avoided. Figure 1 shows a simplified STI process flow, a key requirement of which is planarization of the CVD oxide to expose the nitride mask while controlling the relative heights of the active areas and field areas. The final height of the field oxide must be higher than that of the active silicon under the nitride mask, but not high enough to produce a substantial step. A reasonable range for the step is 0-100 nm, which poses a severe challenge for the planarization process. Previous STI processes [1,2] have used planarizing resist over the CVD oxide and RIE etchback of the composite stack. Field areas wider than a few micrometers must be protected by a blocking resist layer patterned using an extra photomasking step, because planarizing resists lose leveling ability beyond this range. Chemical/mechanical polishing (CMP) has also been used in conjunction with resist etchback to improve process margins [2]. These processes are obviously complex and expensive, and accumulation of tolerances associated with the many steps makes it difficult to achieve the final tolerances required.

In this work, an improved CMP process has been used alone to planarize STI, without resist etchback and without the use of an extra masking step. We have named this simplified process ISO-P. The improved CMP process which makes the ISO-P process feasible levels over much longer distances than those leveled by spin-on processes. In addition, exposure of the masking nitride results in a reduction of the polishing rate of oxide in nearby field areas to match that of the nitride. Thus the nitride mask tends to act as a polishing stop layer.



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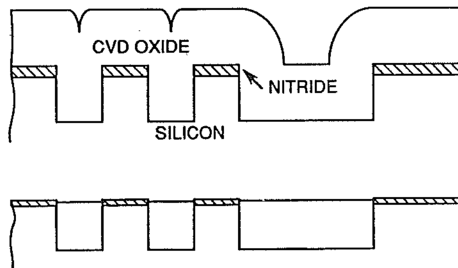

Fig. 1. ISO-P process cross-sections before and after CMP planarization.

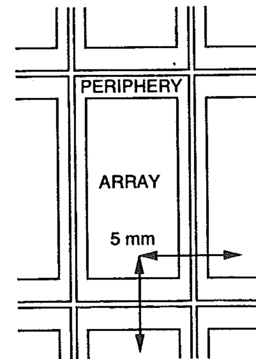

Fig. 2. Typical wafer layout showing need for long distance leveling.

Nevertheless, STI planarization using CMP alone requires an extremely long planarizing range or leveling length to avoid over polishing in low density regions of the circuit where elevated areas naturally polish faster. The key requirement is to remove all oxide from the masking nitride in dense areas without breaking through the nitride in low density areas. Since the oxide/nitride polishing rate ratio is only about 3/1, the stopping power of a 150 nm nitride layer is quite limited. Therefore most of the burden falls on the leveling ability of the CMP process. Figure 2 shows a typical memory wafer layout where the density varies from high to low to high over 5 mm, indicating the range of leveling required. One can conclude that a CMP process used for ISO-P isolation must have a leveling length approaching the size of a chip. A significantly greater leveling length is not desirable, however, because it results in nonuniform oxide removal rates across a wafer due to variations in wafer thickness. The leveling length of a CMP process for ISO-P isolation must therefore be optimized.

PROCESS DETAILS

The process used for this work followed the scheme shown in Fig. 1. A 20 nm layer of thermal SiO_2 was grown on the silicon substrate, followed by deposition of 150 nm of CVD Si_3N_4. After masking and etching the active area pattern in the oxide/nitride stack, the silicon substrate was anisotropically etched using RIE to a depth 0 - 100 nm less than the desired final isolation oxide thickness. Trench depths in the range 0.5 - 1.0 um were used in this study. After removing the photoresist and cleaning the wafers chemically, 20 - 40 nm of thermal SiO_2 was grown to seal the sidewalls of the trenches. At this point, channel stop implants were

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made in some cases. Next, the trench fill oxide was deposited using CVD to a thickness approximately 50% greater than the trench depth.

CMP planarization was carried out using a glass-impregnated polyurethane polishing pad with fumed colloidal silica slurry. Polishing was terminated when the nitride over the active silicon areas was completely exposed. The pad, slurry and polishing parameters were optimized to produce the leveling results discussed below. After planarization, the nitride/oxide stack was stripped, and the devices were completed using normal process steps.

RESULTS

Figure 3 shows the leveling characteristics of the CMP process used in this work. Previously reported results [3] are also shown for comparison. The parameter used in Fig. 3 to characterize leveling is the planarization rate, p, a useful quantitative measure of the planarizing ability of CMP processes on wide patterns [3]. For pattern widths of approximately 1 mm or more, CMP processes quickly smooth the sharp steps at pattern edges and begin eroding oxide from low areas as well as high ones. Nevertheless, planarization continues because high areas are eroded faster than low ones. In this regime, the remaining step height A is decreases exponentially with the mean amount, d, of oxide removed, and p is defined to be the slope of the ln(A) vs. d line. As Fig. 3 indicates, p is high for narrow patterns and declines for wider ones. The current process shows useful planarization out to 5 mm widths, which is in the range needed for ULSI isolation. For example, $p = 2\ um^{-1}$ at w = 5 mm implies that the residual step height of a 5 mm wide pattern can be reduced by a factor of $e^2 = 7.4$ by polishing away 1 um of oxide.

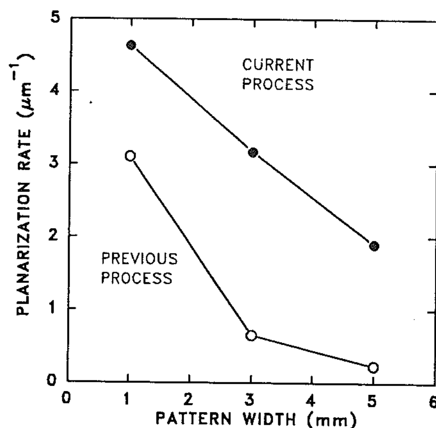

Fig. 3. Leveling characteristics of improved CMP process compared with process reported previously [3].

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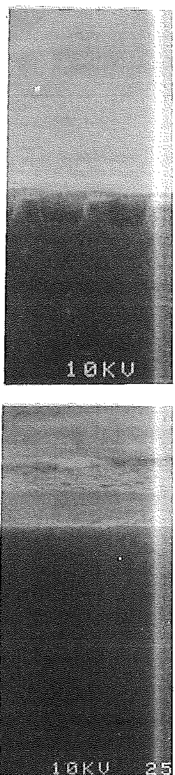

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Figure 4 shows SEM views of an ISO-P wafer after CMP planarization and before stripping the exposed nitride mask. A poly-Si layer has been added to improve contrast and delineate surface topography. High quality local planarization is evident. Long distance planarization is shown in Figs. 5-6. Figure 5 shows surface profilometer scans of a memory wafer before and after planarization. The 3 mm scans run from one array to the next across a low density region more than 1 mm wide. The initial step height was 1.2 um. As the expanded scale trace in Fig. 5C shows, the total remaining amplitude over a 3 mm span is less than 40 nm. At this scale, the bow in the wafer is significant, making it necessary to measure actual film thicknesses to evaluate leveling. Figure 6 shows the remaining nitride and field oxide thicknesses at a series of adjacent points along a 12 mm path crossing the low density

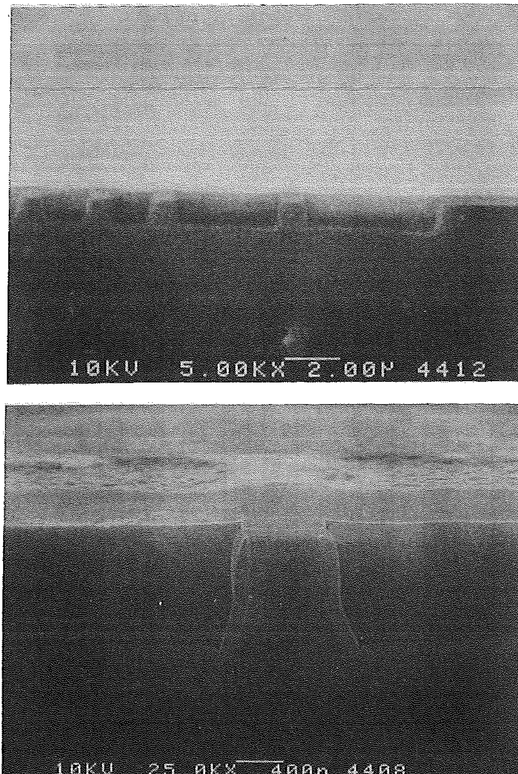

Fig. 4. SEM cross-sections of ISO-P structures after CMP planarization. A poly-Si layer was added to improve contrast.

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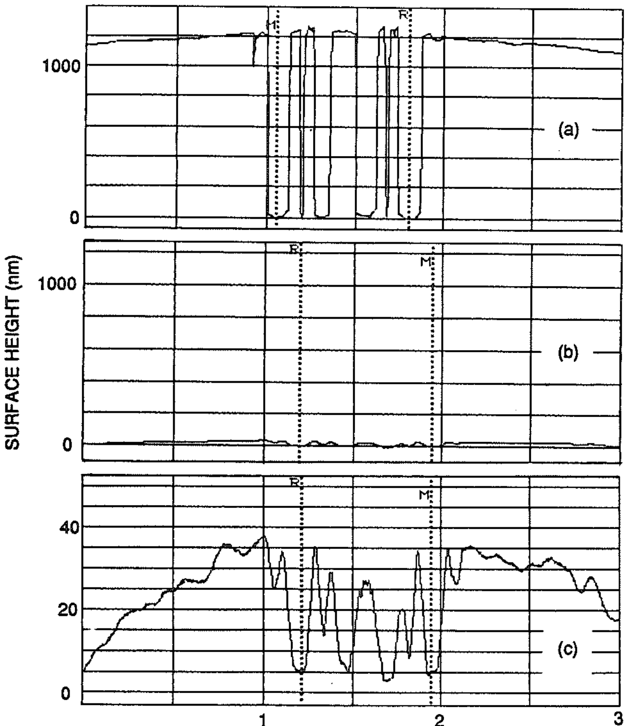

Fig. 5. Surface profiles of ISO-P wafers over 3 mm span. a. Before CMP. b. After. c. Expanded.

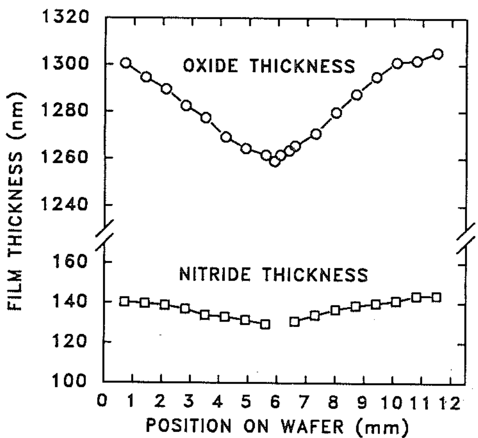

Fig. 6. Remaining nitride and field oxide thickness at adjacent points over 12 mm span. Figs. 5 and 6 are centered on the same low density region.

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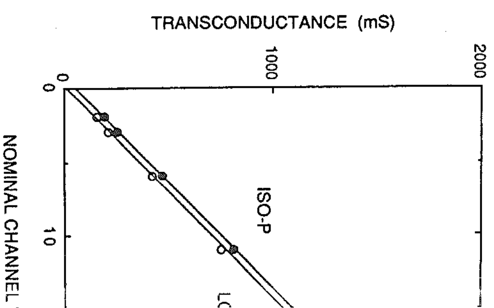

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