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EXTENDED ABSTRACTS

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Abstract No. 171

Optimization of a shallow trench isolation refill process for high density non volatile memories using 100% chemical-mechanical polishing. The BOx-ON process.

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A simple shallow trench fabrication process is given for high density Non Volatile memories. This process uses 70° sloped trenches to improve refill by CVD oxide, isolation area local stress, and finally the sidewall leakage. For the first time, the defects generated by chemical and mechanical polishing are related to electrical behaviour and high resolution TEM analysis. A solution to limit the defect generation is given.

1. INTRODUCTION

Shallow trench isolation for memory devices has received some interest in the past ten years[1], [2], [3], [4]. Non volatile devices[3] could be the best candidates because high voltage sustaining is needed. Nevertheless, process complexity is an issue when dealing with planarization. Mixed resist etch-back and chemical-mechanical polishing has been proposed to solve the long distance and short distance planarization [2] and implement the same isolation in the DRAM memory array and peripheries. The process complexity is still a problem. In this paper, we demonstrate the feasability of a simple process comprising sloped trench etching, void-free and charge free insulator, 100% chemical-mechanical polishing[5] that can match a damage free isolation in the memory array and the peripheries of high density 64 Mbit non-volatile devices.

2. PROCESS FLOW

The process flow of this process is given in figure 1. After a masking step using a silicon nitride/silicon dioxide stack (180nm/17.5nm), mask and trench etching are performed in a P5000 equipment, using an HBr,Cl2 chemistry in order to get 70° sloped grooves. After resist removal eliminating also the polymer residues, a sidewall oxidation is performed to control the silicon surface quality and screening of a possible sidewall implantation. The refill material is then deposited in a LPCVD reactor at 900°C using an SiH2Cl2,N2O based mixture. Chlorine is out-diffused using low temperature steam densification to avoid "pancakes shapes"[6] after gate oxidation. The planarization step is achieved by using a 100% chemical-mechanical polishing (CMP) process on a PRESI equipment. Silicon nitride is used as an etch-stopper with an oxide to niride selectivity of 4. Scrubbing is performed after this step to remove the generated particles. The influence of the subsequent HF dip is examined in the following. The active mask stack is removed by using standard a BOE, H3PO4, HF dip sequence before an implant sacrificial oxide growth and strip. The BOx-ON process is thus completed. The following process steps are derived from standard CMOS.

3. TRENCH REFILL AND SHAPE RELATED STRESS

Figures 2 and 3 show SEM cross sections of 1 µm pitch arrays respectively for 70° and 90° sloped grooves after refill. These two extreme cases show that: 1) no void is obtained in the 0.45 µm opening of the 70° sloped samples; 2) no stress figure is observed in same example using a BOE revelation; 3) in the 90° sloped trench (figure 2) voiding and stress figures can appear despite the densification . This confirms that the trench slope is an important parameter to achieve void free and a stress relaxed isolation oxide. Despite that, still voiding could be observed with conformal types refilling oxides in corner diffusions [7]. A sloped trench near to a Nabla shape [4] is also important to control the sidewall inversion of narrow active devices.

4. 100% CHEMICAL-MECHANICAL POLISHING PLANARIZATION

Figure 4 shows the SEM cross sections of short range and long range planarization respectively obtained after the chemical-mechanical polishing process step. The process is a good compromise to obtain a good planarization in a small and large patterns in which chemical-mechanical polishing can lack of homogeneity. The electrical impact of chemical-mechanical polishing use on silicon dioxide is expressed in figure 5 by achieving C(V) measurments on n+ poly gated MOS capacitors. The evolution of the insulator to silicon interface flat band voltage induced at the different steps of process is given on the graph starting from sidewall oxidation to the gate oxidation step. We can evidence the strong impact of the chemical mechanical polishing step on the induced charges. The charge density is a lot dependent on the densification state of the material. Finally, the charge density can be nearly returned to its initial stage (charge density lower or equal to 2×10^{10} cm^{-2}) by removing the mask and achieving high temperature gate oxidation. The differences between densified and undensified materials are correlated to High Resolution Transmission Electron Microscopy observations (figures 6 and 7). In these 5×10^{6} times magnified observations the poly gate to refill silicon dioxide interface is observed at the step of chemical-mechanical polishing for densified (figure 6) and undensified (figure 7) materials. We clearly point out the difference of interface roughness . The surface is short range perturbed on 7 to 8 atomic planes in the oxide bulk in the undensified case. Middle range induced damage is also obtained in the undensified case whilst the densified samples surface aspect is close to the as-deposited samples surface. We evidence, as Trogolo et al.[8], that chemical-mechanical polishing can damage the oxide surface but still this damage can be minimized by using proper densification of the material. For the first time, this is correlated to electrical results and the great impact of the densification process is reported. The saturation of possible dangling bonds by densification can explain why the surface dissolution and hydration by the CMP induces less damage on the densified material. The damaged areas can be a source of contamination (mobile and metallic ions) that can reach the oxide/silicon interface later in process. The removal of the damaged layer is necessary to achieve a contamination free process.

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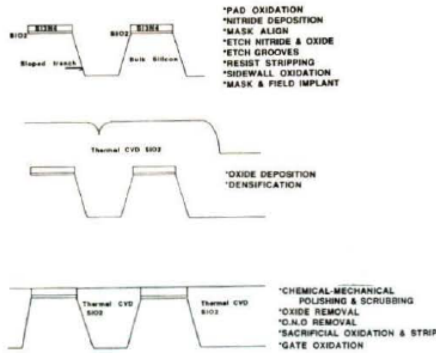

Figure 1 Box-ON process flow

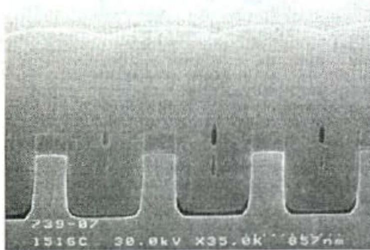

Figure 3 90° sloped trenches after 1000 nm deposition of high temperature CVD SiO2 and densification. Stress figures and voiding can be revealed in 1µm pitch /0.65µm space features.

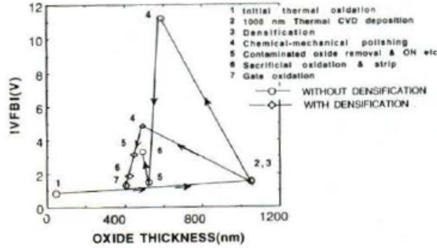

Figure 5. Flat-band voltage versus oxide thickness after different process steps of the Box-ON process. The evolution for densified and undensified material is given.

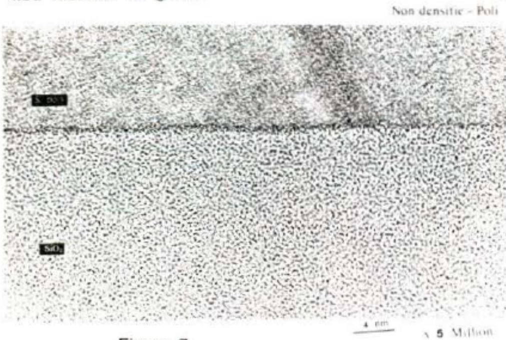

Figure 7

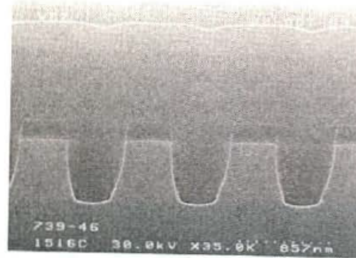

Figure 2 70° sloped trenches after 1000 nm deposition of high temperature CVD SiO2. Chemical revelation does not evidence any local stress or voiding in 1µm pitch /0.45µm space features.

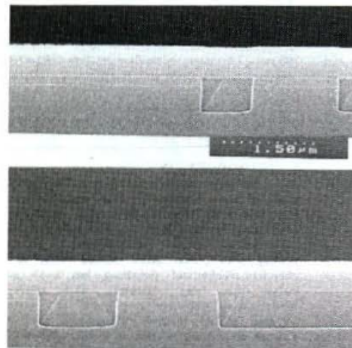

Figure 4 Short /Long range planarization topography after 100% chemical-mechanical polishing.on 90° sloped grooves.

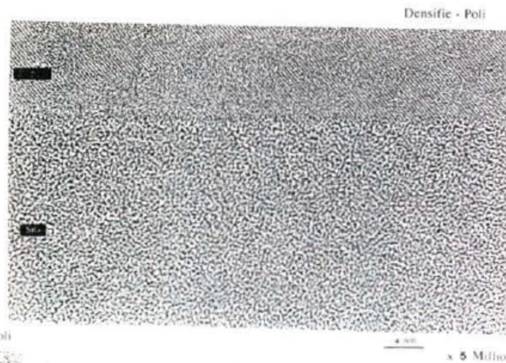

Figure 6

HRTEM observation of poly gate /CVD oxide interface on MOS capacitors for: densified-polished SiO2(figure 6); undensified-polished SiO2(figure 7).

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