United States Patent [19]

Hiroki et al.

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[54] **MOS TYPE SEMICONDUCTOR DEVICE HAVING A LOW CONCENTRATION IMPURITY DIFFUSION REGION**

[75] Inventors: **Akira Hiroki**, Osaka; **Kazumi Kurimoto**, Kobe; **Shinji Odanaka**, Hirakata, all of Japan

[73] Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka, Japan

[21] Appl. No.: **147,866**

[22] Filed: **Nov. 4, 1993**

[30] **Foreign Application Priority Data**

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Nov. 4, 1992 [JP] Japan 4-294820

[51] **Int. Cl.^{6}** **H01L 29/76**; H01L 29/94; H01L 31/062; H01L 31/113

[52] **U.S. Cl.** **257/369**; 257/336; 257/344; 257/408

[58] **Field of Search** 257/408, 336, 257/344, 369

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Primary Examiner—Steven H. Loke
Attorney, Agent, or Firm—Ratner & Prestia

[57] **ABSTRACT**

An MOS type semiconductor device comprises a semiconductor substrate including a p-type region doped with p-type impurities and having a surface and an MOS transistor formed in the p-type region, the MOS transistor including: an n-type source region formed in the p-type region; an n-type drain region formed in the p-type region and separated from the n-type source region by a predetermined distance; a channel region formed in the p-type region and located between the n-type source and drain regions; a pair of n-type impurity diffusion regions formed on both sides of the channel region and having an impurity concentration lower than that of the n-type source region; a gate insulating film formed on the surface of the semiconductor substrate, the gate insulating film directly covering the channel region and the pair of n-type impurity diffusion regions; a gate electrode formed on the gate insulating film; and side walls formed on the sides of the gate electrode, wherein each of the side walls has a bottom portion extending along the surface of the semiconductor substrate from each side of the gate electrode, and each of the n-type source and drain regions has a first portion covered with the bottom portion of the side wall and a second portion not covered with the bottom portion, a thickness of the first portion being smaller than that of the second portion. A method for fabricating such an MOS type semiconductor device is also provided.
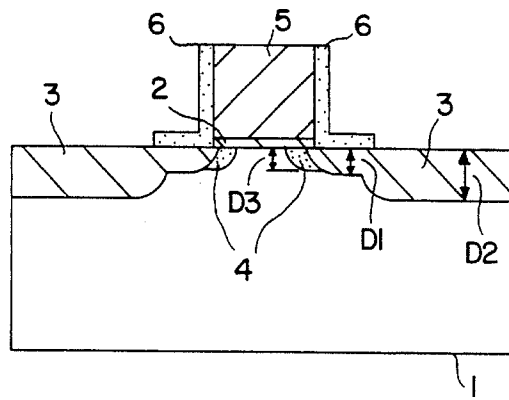
5 Claims, 9 Drawing Sheets
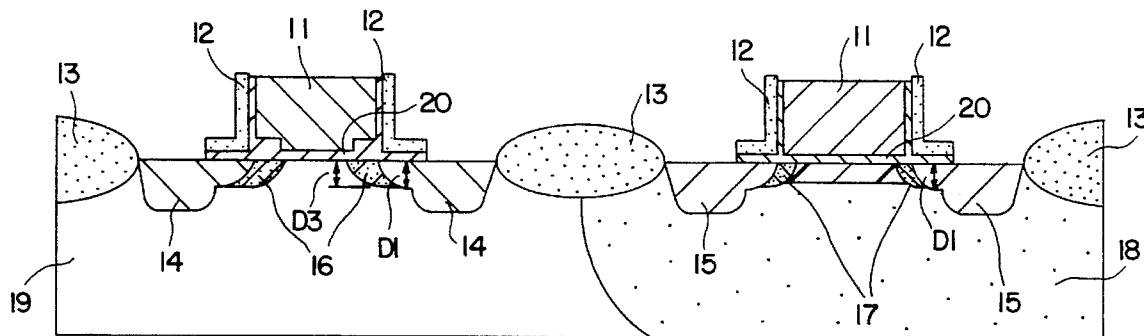
FIG. 1
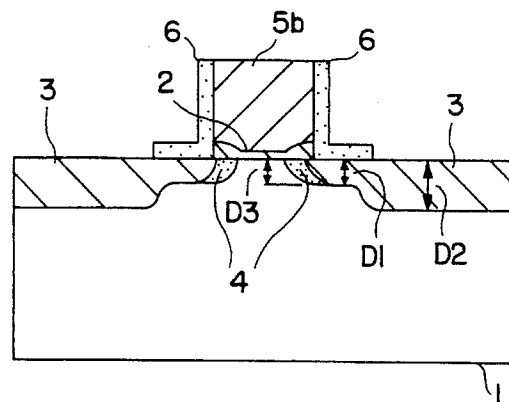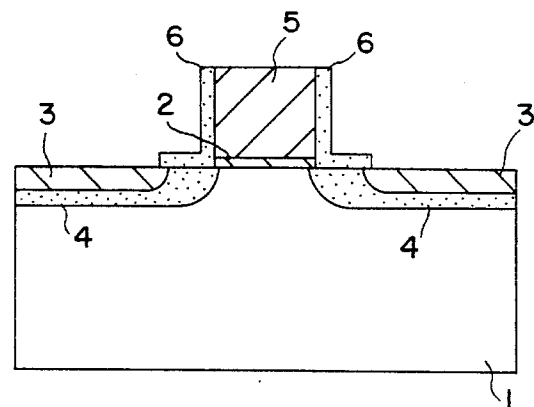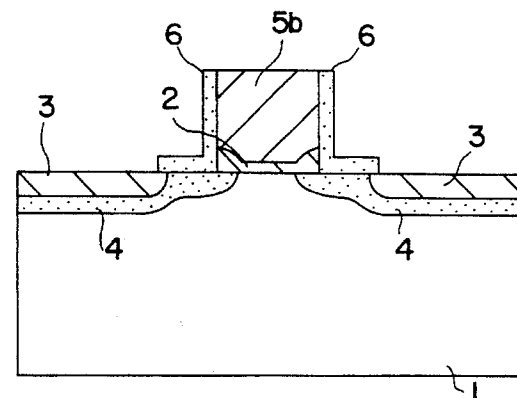

FIG. 2

FIG. 3

FIG. 4
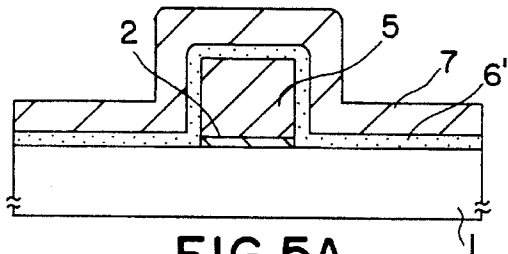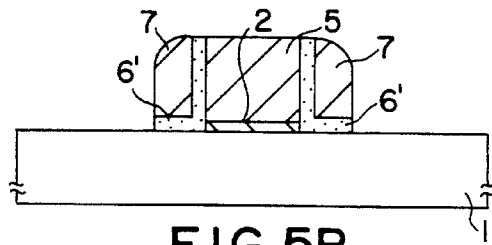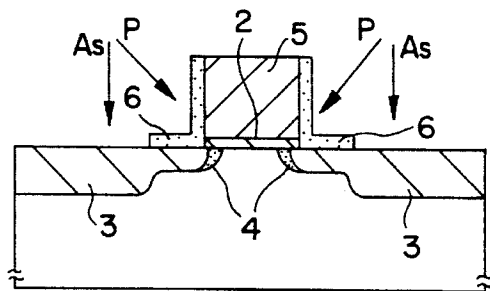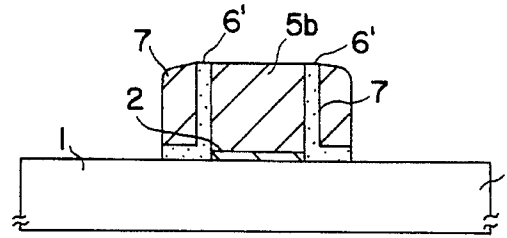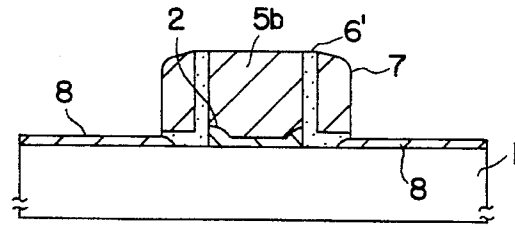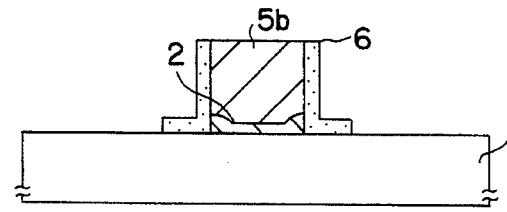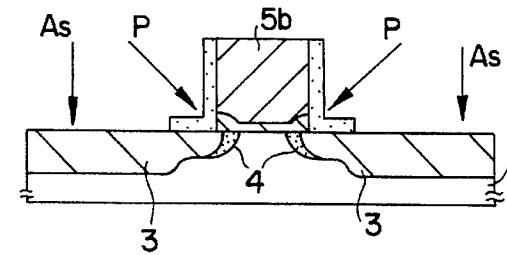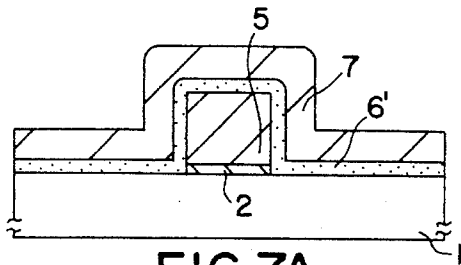
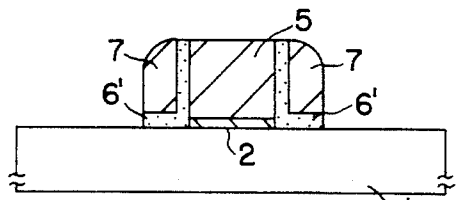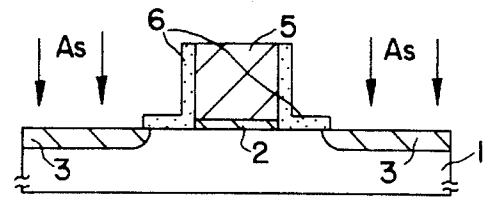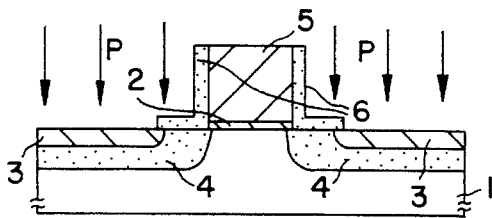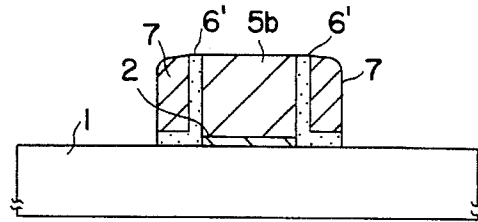FIG.5A

FIG.5B

FIG.5C

FIG.6A

FIG.6B

FIG.6C

FIG.6D

FIG. 7A

FIG. 8A

FIG. 7B

FIG. 8B

FIG. 7C

FIG. 8C

FIG. 7D

FIG. 8D
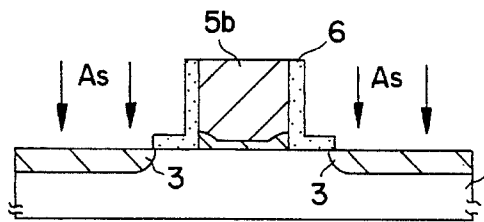
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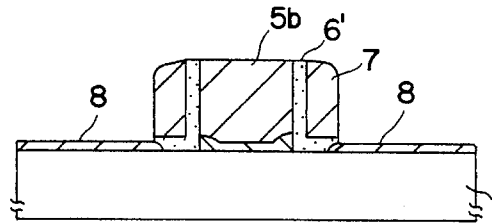
FIG. 9

DOCKET ALARM
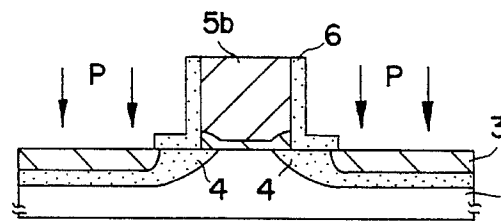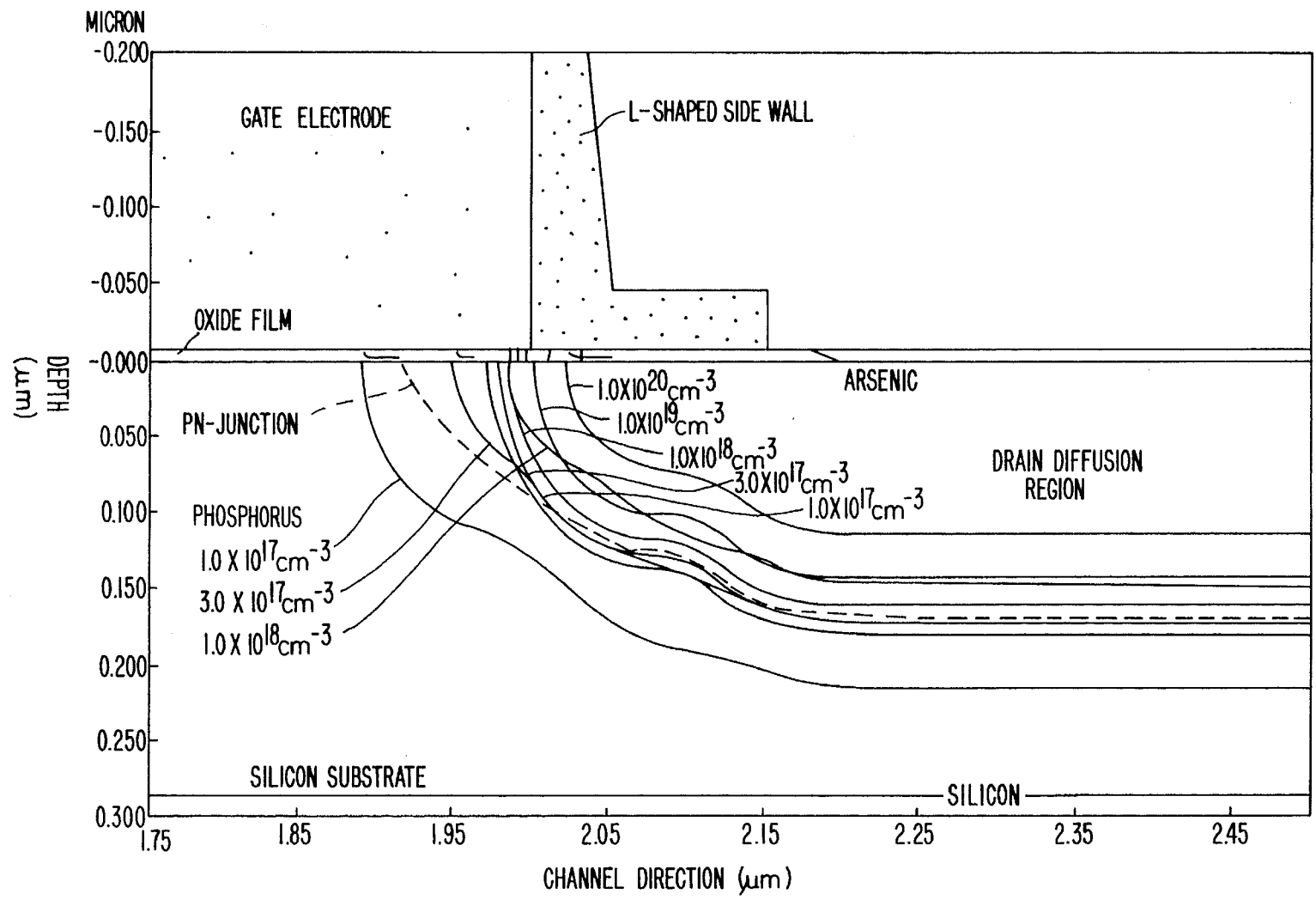
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