

United States Patent [19]

Manukonda et al.

[56]

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[54]	STAIRCASE SIDEWALL SPACER FOR IMPROVED SOURCE/DRAIN ARCHITECTURE		4,837,180	6/1989	Chao 437/44
			4,843,023	6/1989	Chiu et al 437/44
			4,855,247	8/1989	Ma et al 437/44
			4,873,557	10/1989	Kito 357/23
[75]	Inventors:	V. Reddy Manukonda; Thomas E.	4,998,150	3/1991	Rodder et al 437/44
	Seidel, both of Austin, Tex.		FOREIGN PATENT DOCUMENTS		
[73]	Assignee:	Sematech, Inc., Austin, Tex.	0173953	3/1986	European Pat. Off
[21]	Appl. No.:	679,160			European Pat. Off
	• •		0057024	12/1981	Japan .
[22]	Filed:	Mar. 26, 1991	0241267	11/1985	Japan 156/643
			0160976	7/1986	Japan .
Related U.S. Application Data			0118578	5/1987	Japan .
	••			7/1987	Japan .
[63]	Continuation of Ser. No. 499,783, Mar. 27, 1990, abandoned.		0046763	2/1988	Japan 437/34
			0132164	5/1989	Japan 437/34
[51]	Int. Cl. ⁵ H01L 21/336; H01L 27/092		2214349	8/1989	United Kingdom .
[52]				OTHER	PURI ICATIONS

Pfiester, "LDD MOSFET's Using Disposable Sidewall

357/23.3

437/30; 437/34; 437/41; 437/56; 437/67;

437/34, 40, 41, 44, 56, 57, 238, 241, 235; 357/23.3; 156/643, 650, 651, 652, 653, 646

Tasch, Jr. et al. 357/23

Momose 437/34

Shirato 437/44

Maeda 437/34

Parrillo et al. 437/44

Norström et al. 437/44

Hu et al. 156/643

Parrillo et al. 437/37

Parrillo et al. 437/57

Mueller 437/57

Chang et al. 437/34

Matsui 437/44

Haskell 437/34

Chao

[58] Field of Search 437/27, 28, 29, 30,

References Cited U.S. PATENT DOCUMENTS

Kerwin et al. .

Fu et al. .

3,472,712 10/1969 Bower .

2/1988

4/1988

5/1988

5/1988

6/1988

7/1988

8/1988 4,808,544 2/1989

4/1989

3,475,234 10/1969

3,615,934 10/1971

4,356,040 10/1982

4,384,301 5/1983

4,488,351 12/1984

4,530,150 7/1985

4,642,878 2/1987

4,728,617 3/1988

4,735,916 4/1988 4,740,484

4,818,714 4/1989

4,826,782 5/1989

4,722,909

4,744,859

4,745,086

4,753,898

4,760,033

4,764,477

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Attorney, Agent, or Firm-William W. Kidd

a conformal oxide layer and a subsequent etching of the oxide layer provide for a staircase shaped sidewall spacer which is used to align source and drain regions during implantation. Extent of the implanted n-/n+and/or p-/p+ regions within the substrate can be tightly controlled due to the tight dimensional tolerances obtained by the footprint of the spacer. Further the source/drain profiles can be utilized with elevated polysilicon and elevated polysilicon having subsequent

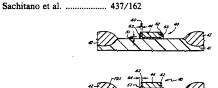
OTHER PUBLICATIONS

Spacer Technology", IEEE Electron Device Letters, vol. 9, No. 4, Apr. 1988, pp. 189–192.

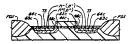
(List continued on next page.)

ABSTRACT Selective etching of a conformal nitride layer overlying salicidation.

14 Claims, 7 Drawing Sheets









OTHER PUBLICATIONS

IBM Technical Disclosure Bulletin, vol. 32, No. 5A, Oct. 1989, "Method for Making Lightly Doped Drain Shallow Junctions", pp. 110-111.

IBM Technical Disclosure Bulletin, vol. 28, No. 1, Jun. 1985, "New Scheme to Form Shallow N+ and P+ Junctions for MOS Devices", pp. 366-367.

2244 Research Disclosure (1989) Jul., No. 303, New York, U.S., "Method for Making Devices having Reduced Field Gradients at Junction Edges", p. 496. 1988 Symposium on VLSI Technology, Oh et al., Simultaneous Formation of Shallow-Deep Stepped Sour-

multaneous Formation of Shallow-Deep Stepped Source/Drain for Sub-Micron CMOS, May 10-13, 1988, pp. 73-74.

IEEE, Nov. 1989, Lu et al., Submicrometer Salicide

CMOS Devices with Self-Aligned Shallow-Deep Junctions, pp. 487-489.

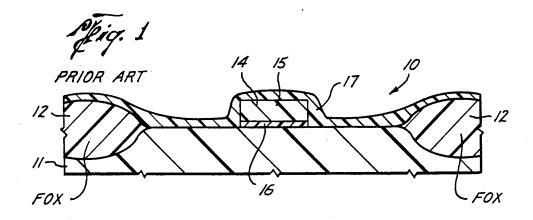
IEEE, Feb. 1985, Matsumoto et al., An Optimized and Reliable LDD Structure for 1-μm NMOSFET Based on Substrate Current Analysis, pp. 429-433.

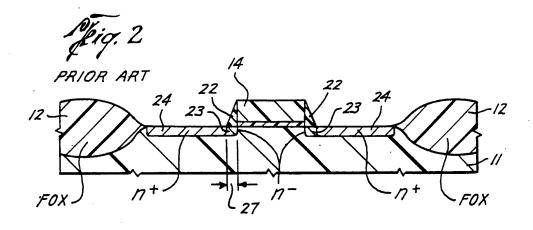
IEEE, Feb. 1986, Huang et al., A Novel Submicron LDD Transistor with Inverse-T Gate Structure IEDM 86, pp. 742-745.

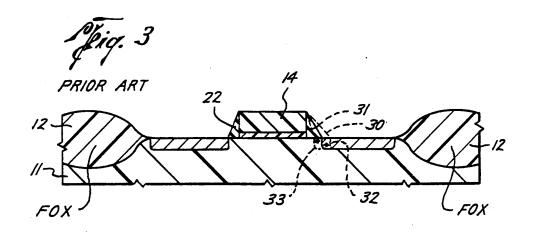
86, pp. 742-745. IEEE, Oct. 1984, Oh and Kim, A New MOSFET Structure with Self-Aligned Polysilicon Source and Drain Electrodes, pp. 400-402.

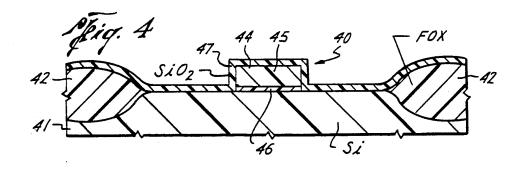
IEEE, Jul. 1989, Yamada et al., Spread Source/Drain (SSD) MOSFET Using Selective Silicon Growth for 64Mbit Drams pp. 2.4.1-2.4.4.

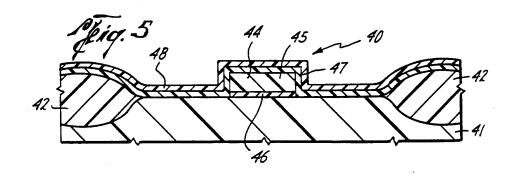


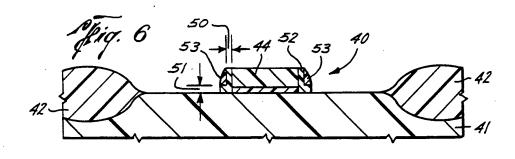


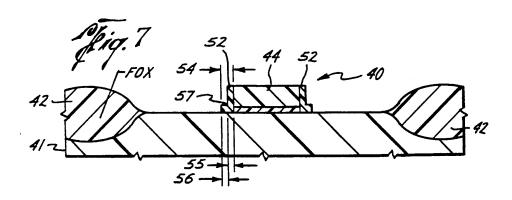


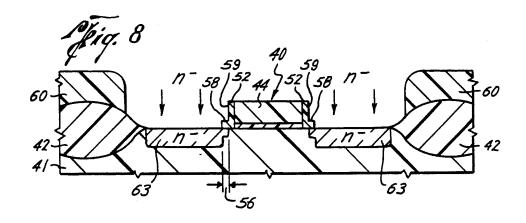


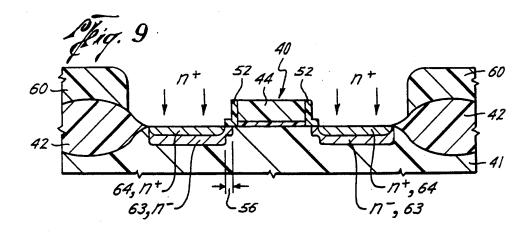


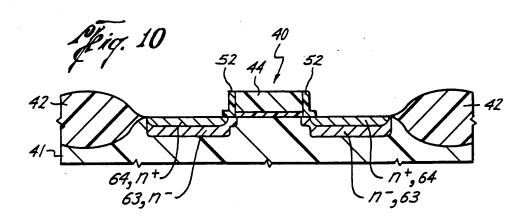












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