United States Patent [19]

Gasner

[11] **Patent Number: 4,599,789**

[45] **Date of Patent: Jul. 15, 1986**

[54] **PROCESS OF MAKING TWIN WELL VLSI CMOS**

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[73] Assignee: **Harris Corporation,** Melbourne, Fla.

[21] Appl. No.: **620,835**

[22] Filed: **Jun. 15, 1984**

[51] **Int. Cl.**⁴ **H01L 21/265;** B01J 17/00

[52] **U.S. Cl.** .... **29/571;** 29/576 B; 148/1.5; 148/187; 156/643; 357/42; 357/91

[58] **Field of Search** .... 148/1.5, 187; 29/571, 29/576 B; 156/643; 357/91, 42

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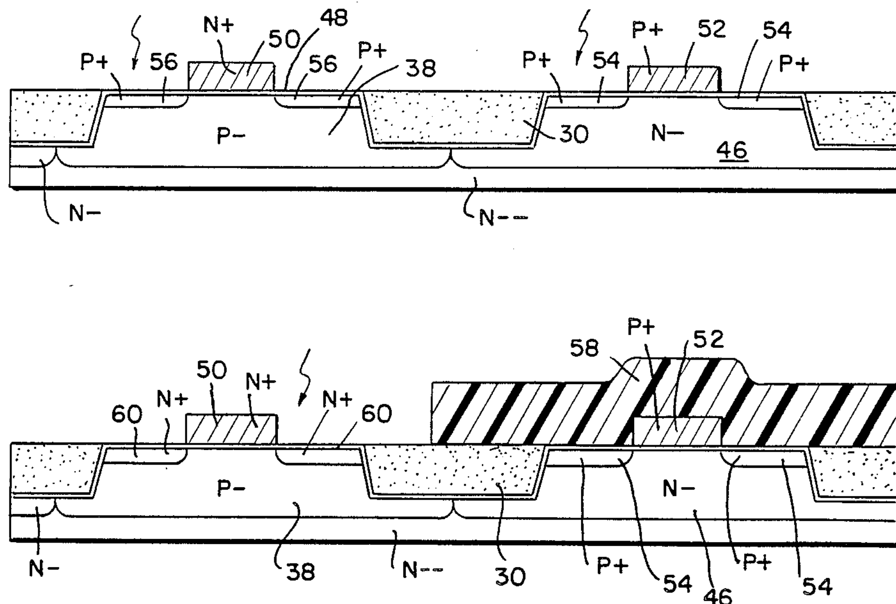
[57] **ABSTRACT**

CMOS devices are formed in self-aligned wells in a substrate produced by a two mask, one photolithographic step process wherein the first mask is used as a template to form the second inverse mask of substantially equal thickness. The gates are used as alignment mask for shallow source and drain regions and subsequently formed lateral gate spacers are used as alignment mask for deep source and drain regions. Exposed source and drain regions and silicon gates have silicide formed thereon by a non-selective process.

14 Claims, 20 Drawing Figures



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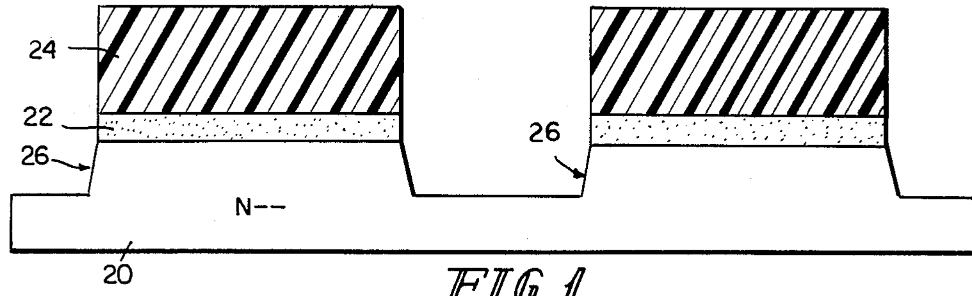

FIG. 1

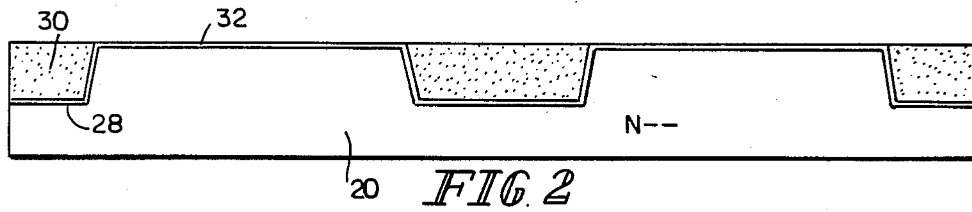

FIG. 2

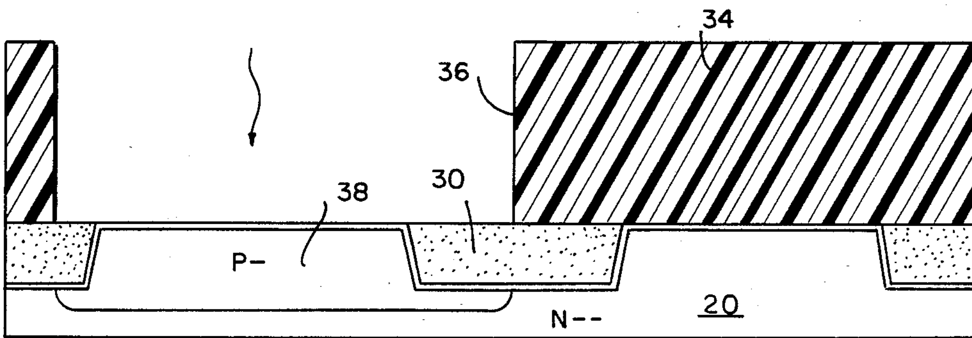

FIG. 3

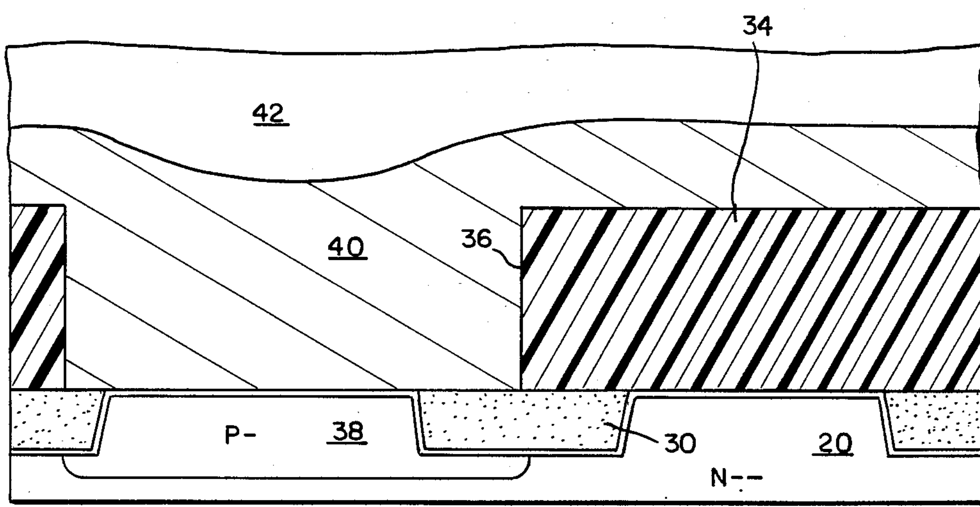

FIG. 4

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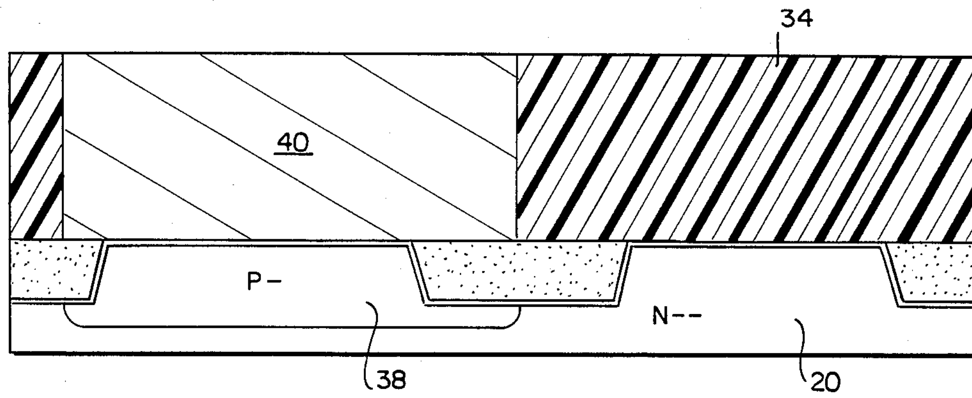

FIG. 5

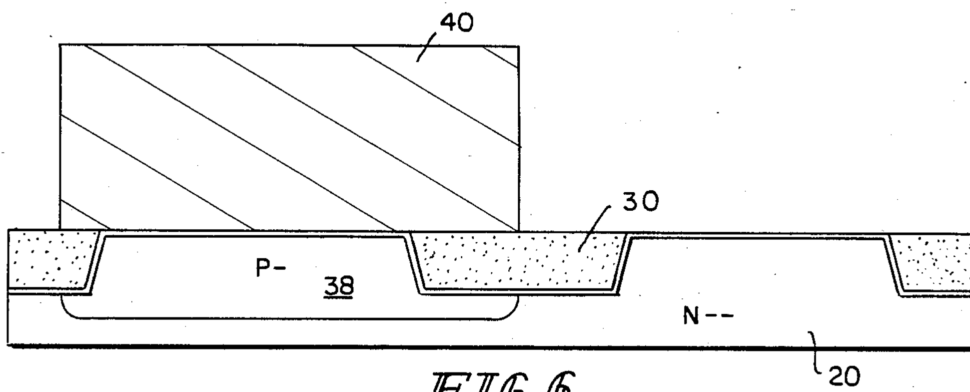

FIG. 6

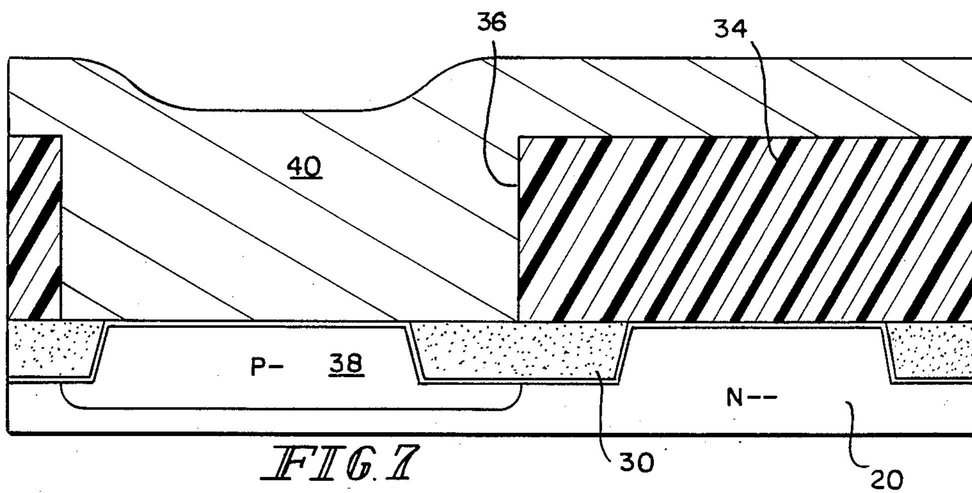

FIG. 7

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FIG. 8

FIG. 9

FIG. 10

FIG. 11

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FIG. 12

FIG. 13

FIG. 14

FIG. 15

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